



Low Power 14-Bit, 15 Bit & 16-Bit Sampling Analog-to-Digital Converters

DAS1157/DAS1158/DAS1159

FEATURES

Complete with High Accuracy Sample/Hold and A/D Converter

Low Power Consumption: 850mW max, $V_S = \pm 15V$

Rated Performance: $-25^{\circ}C$ to $+85^{\circ}C$

Low Nonlinearity (DAS1158 and DAS1159)

Differential: $\pm 0.0015\%$ FSR max

Integral: $\pm 0.003\%$ FSR max

Differential T.C.: $\pm 1\text{ppm}/^{\circ}C$ max

High Throughput Rate: 18kHz min

Byte-Selectable Tri-State Buffered Outputs

Internal Gain & Offset Potentiometers

Improved Second Source to A/D/A/M-834 and

A/D/A/M-835 Modules

APPLICATIONS

Seismic Data Acquisition

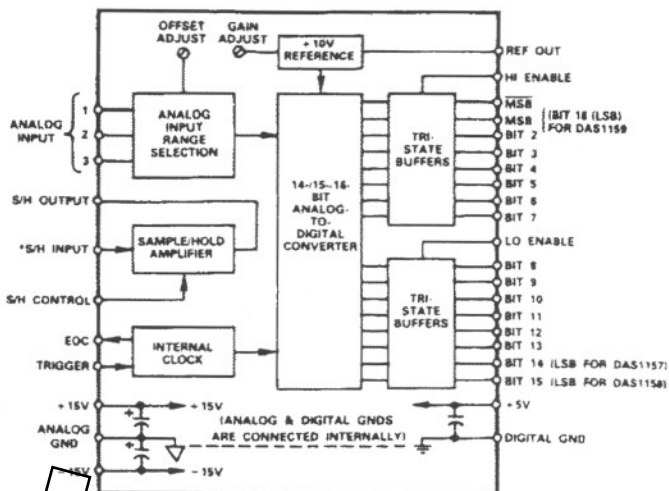
Portable Field Instrumentation

Automated Test Equipment

Process Control Data Acquisition

Medical Instrumentation

FUNCTIONAL BLOCK DIAGRAM



*S/H INPUT IS THE ANALOG SIGNAL INPUT IF THE INTERNAL SAMPLE/HOLD AMPLIFIER IS USED

GENERAL DESCRIPTION

The DAS1157/DAS1158/DAS1159 are 14-/15-/16-bit sampling analog-to-digital converters. They are ideally suited for use in portable and remote data acquisition equipment where low power consumption (650mW maximum) and wide temperature range ($-25^{\circ}C$ to $+85^{\circ}C$ rated performance) are required.

DAS1157/DAS1158/DAS1159 provide guaranteed high accuracy and high stability system performance essential to medical, analytical and process control equipment: differential nonlinearity of $\pm 0.0015\%$ max and integral nonlinearity of $\pm 0.003\%$ max (DAS1158 and DAS1159); no missing codes guaranteed; gain T.C. of $\pm 8\text{ppm}/^{\circ}C$ max, zero T.C. of $\pm 80\mu\text{V}/^{\circ}C$ max and differential nonlinearity T.C. of $\pm 1\text{ppm}/^{\circ}C$ max.

The wide dynamic range will enhance the performance of critical measurements in gas and liquid chromatography, blood analyzers, distributed data acquisition in factory automation and power generating equipment, and in automatic test equipment.

The DAS1157/DAS1158/DAS1159 make use of Analog Devices' proprietary CMOS technology to achieve low power operation, while utilizing the latest integrated circuit and thin-film components to achieve the highest level of performance and reliability.

As shown in Figure 1, each device contains a precision sample/hold amplifier, high accuracy 14-/15-/16-bit analog-to-digital converter, precision reference, CMOS tri-state output buffers (for direct 8-bit or 16-bit bus interface), user accessible gain and offset adjust potentiometers, and power supply bypass capacitors, all in a compact low profile $2'' \times 4'' \times 0.375''$ metal case package. No additional components are required for operation.

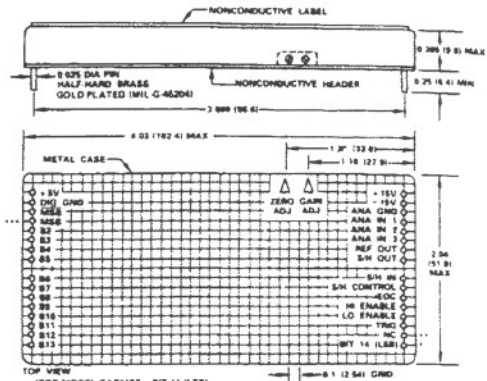
DAS1157/DAS1158/DAS1159 — SPECIFICATIONS

(typical @ +25°C, V_S = ±15V, V_D = +5V unless otherwise specified)

| MODEL | DAS1157 | DAS1158 | DAS1159 |
|--|--|-------------------------------|------------|
| RESOLUTION | 14 Bits | 15 Bits | 16 Bits |
| DYNAMIC PERFORMANCE | | | |
| Throughput Rate | 18k Hz min | * | * |
| Conversion Time | 50µs max | * | * |
| S/H Acquisition Time | 5µs max | * | * |
| S/H Aperture Delay | 250ns | * | * |
| S/H Aperture Uncertainty | 1ns | * | * |
| Feedthrough Rejection ¹ | -90dB min | * | * |
| Droop Rate | 0.05µV/µs, 0.1µV/µs max | * | * |
| Dielectric Absorption Error | ±0.005% of Input Voltage Change | * | * |
| ACCURACY | | | |
| Integral Nonlinearity ² | ±0.005% FSR ³ max | ±0.003% FSR ³ max | ** |
| Differential Nonlinearity ⁴ | ±0.003% FSR ³ max | ±0.0015% FSR ³ max | ** |
| No Missing Codes | Guaranteed | * | * |
| ±3σ Noise (S/H plus A/D) | 0.0022% p-p (75µV rms) | * | * |
| ±3σ Noise (A/D) | 0.0015% p-p (50µV rms) | * | * |
| STABILITY | | | |
| Differential Nonlinearity T.C. | ±2ppm/°C max | ±1ppm/°C max | ** |
| Gain T.C. | ±8ppm/°C max | * | * |
| Zero T.C. | ±30µV/°C typ, ±80µV/°C max | * | * |
| Conversion Time T.C. | ±0.05%/°C | * | * |
| Power Supply Sensitivity | ±0.001% FSR ³ /% V _S | * | * |
| Warm-Up Time | Less than 1 Minute | * | * |
| ANALOG INPUT | | | |
| Voltage Range | ±5V, ±10V | * | * |
| Bipolar | 0 to +5V, 0 to +10V | * | * |
| Unipolar ⁴ | | * | * |
| ADC Input Impedance | 0 to +5V, ±5V: 2.5kΩ 0 to +10V, ±5V: 5kΩ | * | * |
| S/H Input Impedance | ±10V: 10kΩ ±5V: 100kΩ/5pF | * | * |
| DIGITAL INPUTS | | | |
| A/D Trigger ⁵ | Positive Pulse, Neg. Edge Triggered | * | * |
| Logic Levels | 5V CMOS Compatible | * | * |
| S/H Control | SAMPLE = Logic 1, TTL Compatible | * | * |
| Low Enable, High Enable ⁶ | ENABLE = Logic 0, CMOS/TTL Compatible | * | * |
| DIGITAL OUTPUTS | | | |
| Parallel Data Outputs | | | |
| Unipolar | Binary | * | See Note 7 |
| Bipolar | Offset Binary, 2's Complement | * | See Note 7 |
| Output Drive | 2TTL Loads | * | * |
| End of Conversion | Logic "1" During Conversion | * | * |
| Output Drive | 2TTL Loads | * | * |
| INTERNAL REFERENCE VOLTAGE | | | |
| External Load Current (Rated Performance) | +10V, ±0.3% 2mA max | * | * |
| POWER REQUIREMENTS | | | |
| Rated Voltages | ±15V (±3%), +5V (±5%) | * | * |
| Operating Voltages ^{8,9} | ±12V to ±17V, +4.75V to +5.25V | * | * |
| Supply Current Drain ±15V | ±15mA | * | * |
| +5V | 10mA | * | * |
| Total Power Consumption, V _S = ±15V | 500mW typ, 650mW max | * | * |
| TEMPERATURE RANGE | | | |
| Rated Performance | -25°C to +85°C | * | * |
| Operating | -25°C to +85°C | * | * |
| Storage | -40°C to +100°C | * | * |
| Relative Humidity | Meets MIL-STD-202E, Method 103B | * | * |
| Shielding | Electrostatic (RFI) 6 Sides Electromagnetic (EMI) 5 Sides | * | * |
| SIZE | 2" x 4" x 0.375" Metal Package | * | * |

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



ASSEMBLY INSTRUCTIONS

CAUTION: This module is not an embedded assembly and is not hermetically sealed. Do not subject to a solvent or water-wash process that would allow direct contact with free liquids or vapors. Entrapment of contaminants may occur, causing performance degradation and permanent damage. Install after any clean/wash process and then only spot clean by hand.

LETTE

NOTES

- *Specifications same as DAS1157
- **Specifications same as DAS1158
- ¹Measured in hold mode, input 20V pk-pk @ 10kHz.
- ²Worst-case summation of S/H and A/D nonlinearity errors.
- ³FSR means Full Scale Range.
- ⁴Differential Nonlinearity in the 0 to +5V input range is specified as ±0.003% typical for the DAS1157, DAS1158 and DAS1159.
- ⁵When connecting the Trigger and the S/H control terminals together, the pulse width must be long enough for the S/H amplifier to acquire the input signal to the required accuracy (5µs min). If the A/D converter only is used, the Trigger pulse width should be 1µs min (see Figure 3).

- ⁶Low Byte Enable pin connections are Bits 8 through 15; High Byte Enable pin connections are MSB, MSB or Bit 16 and Bits 2 through 7.
- ⁷DAS1159 unipolar coding is provided in a modified binary format (MSB complement) while bipolar coding is two's complement only. The MSB must be inverted for binary and offset binary codes.
- ⁸When the S/H section is required, -V_S must be at least 5 volts more negative than the most negative analog input voltage (example: V_S = ±12V dc, therefore, maximum analog input is +10 and -7V).
- ⁹Recommended Power Supply: Analog Devices Model 923. Specifications subject to change without notice.

Applying the DAS1157/DAS1158/DAS1159

OPERATION

For operation, the only connections necessary to the DAS1157/DAS1158/DAS1159 are the $\pm 15V$ and $+5V$ power supplies, analog input signal, trigger pulse, and the HI-ENABLE/LO-ENABLE tri-state controls. Analog input and digital output programming are user selectable via external jumper connections.

Input voltage ranges are selectable via user pin programming: 0 to $+5V$, 0 to $+10V$, $\pm 5V$ and $\pm 10V$. Unipolar coding is provided in true binary format with bipolar coding displayed in offset binary and two's complement (DAS1157 and DAS1158). DAS1159 unipolar coding is provided in a modified binary format (MSB complement) while bipolar coding is two's complement only.

ANALOG INPUT SECTION

The analog input can be applied to just the A/D converter or to the internal sample/hold amplifier ahead of the A/D converter.

When using just the A/D converter, apply the analog input per the voltage range pin programming shown in Table I. When using the sample/hold amplifier in conjunction with A/D converter, apply the analog input to the S/H INPUT terminal and connect the S/H OUTPUT terminal to the appropriate A/D converter analog input.

| Analog Voltage Input Range | Connect V_{IN} or S/H Out To | Connect Analog Common To | Connect Ref Out To |
|----------------------------|--------------------------------|--------------------------|--------------------|
| 0 to $+5V$ | ANA IN 1, ANA IN 2, ANA IN 3 | Ground | NC* |
| 0 to $+10V$ | ANA IN 2, ANA IN 3 | Ground, ANA IN 1 | NC* |
| $\pm 5V$ | ANA IN 1 | Ground, ANA IN 3 | ANA IN 2 |
| $\pm 10V$ | ANA IN 3 | Ground, ANA IN 1 | ANA IN 2 |

*No Connection

Table I. Analog Input Pin Programming

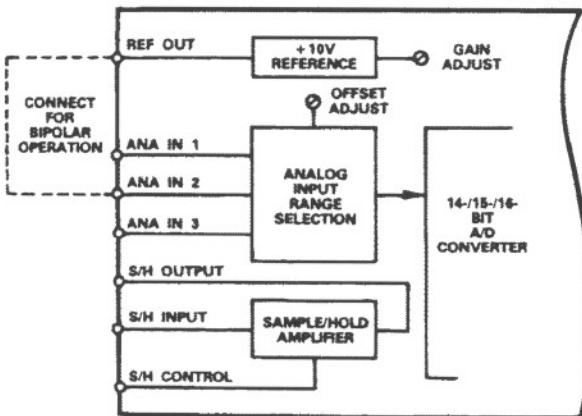


Figure 2. Analog Input Block Diagram

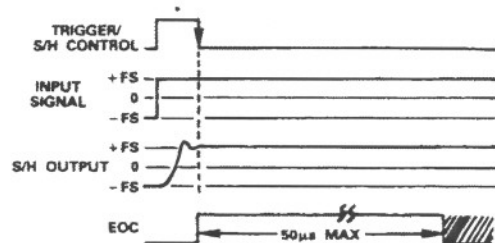
Errors due to source loading are eliminated since the sample/hold amplifier is a high-impedance unity-gain amplifier. High feed-through rejection is provided for either single-channel or multi-channel applications. Feedthrough rejection can be optimized, in multichannel applications, by changing channels at the rising or falling edge of the S/H control pulse.

TIMING DIAGRAM

The timing diagram for the DAS1157/DAS1158/DAS1159 is illustrated in Figure 3. This figure also includes the sample/hold amplifier acquisition time.

If the sample/hold amplifier is required, the TRIGGER input and S/H CONTROL terminal can be tied together providing only one conversion control signal. When the trigger pulse goes high, it places the sample/hold amplifier in the sample mode allowing it to acquire the present input signal. The trigger pulse must remain high for a minimum of $5\mu s$ to insure accuracy. If the sample/hold amplifier is not used, the trigger pulse needs to be $1\mu s$ (minimum) in length to satisfy the A/D converter trigger requirements. At the falling edge of the trigger pulse, the sample/hold amplifier is placed in the hold mode, all internal logic is reset and the A/D conversion begins. The conversion process can be retrIGGERED at any time, including during conversion.

With this negative edge of the trigger pulse, the MSB is set high with the remaining digital outputs set to logic low state, and the end of conversion is set high and remains high through the full conversion cycle. During conversion each bit, starting with the MSB, is sequentially switched high at the rising edge of the internal clock. The DAC output is then compared to the analog input and the bit decision is made. Each comparison lasts one clock cycle with the complete 14-/15-/16-bit conversion taking $50\mu s$ maximum. At this time, the end of conversion line goes low signifying that the conversion is complete. For microprocessor bus applications, the digital output can now be applied to the data bus by enabling the tri-state buffers. For maximum data throughput, the digital output data should be read while the sample/hold amplifier is acquiring the new analog input signal.



- NOTES
1. Output Data Valid.
 2. If S/H Control and Trigger are Tied Together, Pulse Width Must Be $5\mu s$ Min to Allow the S/H Amplifier to Acquire the Input Signal. If the ADC is Only Used, the Trigger Pulse Must Be $1\mu s$ Min.

Figure 3. DAS1157/DAS1158/DAS1159 Timing Diagram

DAS1157/DAS1158/DAS1159

GAIN AND OFFSET ADJUSTMENT

The DAS1157/DAS1158/DAS1159 contain internal gain and offset adjustment potentiometers. Each potentiometer has ample adjustment range so that gain and offset errors can be trimmed to zero.

Offset calibration is not affected by changes in gain calibration, and should be performed prior to gain calibration. Proper gain and offset calibration requires great care and the use of extremely sensitive and accurate reference instruments. The voltage standard used as a signal source must be very stable and be capable of being set to within $\pm 1/10\text{LSB}$ of the desired value at any point within its range.

OFFSET CALIBRATION

For a 0 to +10V unipolar range, set the input voltage precisely to +305 μV for the DAS1157, +153 μV for the DAS1158 and +76 μV for the DAS1159. For a 0 to +5V unipolar range, set the input to +153 μV for the DAS1157, +76 μV for the DAS1158 and +38 μV for the DAS1159. Then adjust the zero potentiometer until the converter is just on the verge of switching from 000.....000 to 000.....001 (DAS1157/DAS1158) or from 100.....000 to 100.....001 (DAS1159).

For the $\pm 5\text{V}$ bipolar range, set the input voltage precisely to +305 μV for the DAS1157, +153 μV for the DAS1158 and +76 μV for the DAS1159. For a $\pm 10\text{V}$ bipolar range, set the input voltage precisely to +610 μV for the DAS1157, +305 μV for the DAS1158 and +153 μV for the DAS1159. Adjust the zero potentiometer until the offset binary coded units are just on the verge of switching from 000.....000 to 000.....001 and the two's complement coded units are just on the verge of switching from 100.....000 to 100.....001.

GAIN CALIBRATION

Set the input voltage precisely to +9.99909V (DAS1157)/+9.99954V (DAS1158)/+9.99977V (DAS1159) for the 0 to +10V units, +4.99954V (DAS1157)/+4.99977V (DAS1158)/+4.99989V (DAS1159) for 0 to +5V units, +9.99817V (DAS1157)/+9.99909V (DAS1158)/+9.99954V (DAS1159) for $\pm 10\text{V}$ units, or +4.99909V (DAS1157)/+4.99954V (DAS1158)/+4.99977V (DAS1159) for $\pm 5\text{V}$ units. Note that these values are 1/2LSBs less than nominal full scale. Adjust the gain potentiometer until binary and offset binary coded units are just on the verge of switching from 11.....10 to 11.....11 or modified binary and two's complement coded units are just on the verge of switching from 011.....10 to 011.....11.

DAS1157/DAS1158/DAS1159 INPUT/OUTPUT RELATIONSHIPS

The DAS1157/DAS1158 produces a true binary coded output when configured as a unipolar device. Configured as a bipolar device, it can produce either offset binary or two's complement output codes. The most significant bit (MSB) is used to obtain the binary and offset binary codes while $\overline{\text{MSB}}$ is used to obtain two's complement coding. The DAS1159 produces a modified binary coded output when configured as a unipolar device. Configured as a bipolar device it can only produce two's complement output codes. The DAS1159 uses $\overline{\text{MSB}}$ to obtain the modified binary and two's complement output codes; the DAS1159 does not have an MSB output. Table II shows the DAS1157/DAS1158/DAS1159 unipolar analog input/digital output relationships. Table III shows the DAS1157/DAS1158/DAS1159 bipolar analog input/digital output relationships.

Input Voltage - Output Code Relationships

| Unipolar Input Voltages | | Digital Output |
|-------------------------|-----------------|---|
| Analog Input | 0 to +10V Range | |
| DAS1157 | | |
| +4.99969V | +9.99939V | Binary Code 11 1111 1111 1111 |
| +0.00000V | +0.00000V | 00 0000 0000 0000 |
| DAS1158 | | |
| +4.99985V | +9.99969V | Binary Code 111 1111 1111 1111 |
| +0.00000V | +0.00000V | 000 0000 0000 0000 |
| DAS1159 | | |
| +4.99992V | +9.99985V | Modified Binary Code 0111 1111 1111 1111 |
| +0.00000V | +0.00000V | 1000 0000 0000 0000 |

Table II. Unipolar Input-Output Relationships

| Bipolar Input Voltages | | Digital Output | |
|------------------------|------------------------|-----------------------|---------------------|
| Analog Input | Offset Binary Code | Two's Complement Code | |
| DAS1157 | | | |
| $\pm 5\text{V}$ Range | $\pm 10\text{V}$ Range | | |
| DAS1157 | | | |
| +4.99939V | +9.99878V | 11 1111 1111 1111 | 01 1111 1111 1111 |
| +0.00000V | +0.00000V | 10 0000 0000 0000 | 00 0000 0000 0000 |
| -5.00000V | -10.00000V | 00 0000 0000 0000 | 10 0000 0000 0000 |
| DAS1158 | | | |
| +4.99969V | +9.99939V | 111 1111 1111 1111 | 011 1111 1111 1111 |
| +0.00000V | +0.00000V | 100 0000 0000 0000 | 000 0000 0000 0000 |
| -5.00000V | -10.00000V | 000 0000 0000 0000 | 100 0000 0000 0000 |
| DAS1159 | | | |
| +4.99985V | +9.99969V | | 0111 1111 1111 1111 |
| +0.00000V | +0.00000V | | 0000 0000 0000 0000 |
| -5.00000V | -10.00000V | | 1000 0000 0000 0000 |

Table III. Bipolar Input-Output Relationships

TRI-STATE DIGITAL OUTPUT

The ADC digital outputs are provided in parallel format to the output tri-state buffers. The output information can be applied to a data bus in either a one-byte or a two-byte format by using the HIGH BYTE ENABLE and LOW BYTE ENABLE terminals. If the tri-state feature is not required, normal digital outputs can be obtained by connecting the enable pins to ground.

POWER SUPPLY AND GROUNDING CONNECTIONS

No power supply decoupling is required since the DAS1157/DAS1158/DAS1159 contain high quality tantalum capacitors on each of the power supply inputs to ground.

The analog and digital grounds are internally connected in the DAS1157/DAS1158/DAS1159. But in many applications, an external connection between the digital ground pin and analog ground pin is advisable for optimum performance.

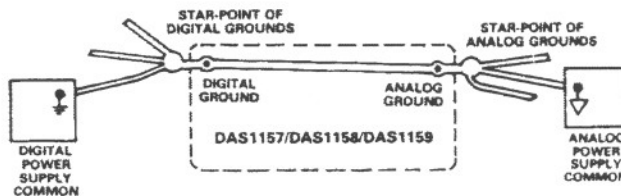


Figure 4. Typical Ground Layout for DAS1157/DAS1158/DAS1159