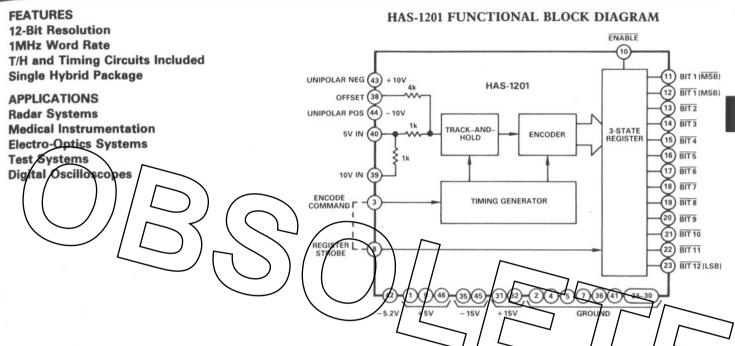


## 12-Bit, 1MHz Analog-to-Digital Converter

HAS-1201



#### GENERAL DESCRIPTION

The HAS-1201 A/D Converter combines high resolution and speed in a single hybrid package. This is a *complete* 12-bit, 1MHz unit which includes a track-and-hold and timing circuits. It's a total solution for the system designer who needs to perform the entire analog-to-digital conversion function in the smallest possible space.

This remarkable converter is a full answer to the question of digitizing analog signals into high-resolution data outputs and doing it in the most cost-effective way. The HAS-1201 is the ideal choice for the designer who needs state-of-the-art performance in high-resolution, high-speed A/D conversion.

Full-scale analog inputs are 5 or 10 volts; and the unit can operate with either bipolar or unipolar ranges. Analog input impedance is 1,000 ohms or 2,000 ohms and the three-state digital outputs are TTL compatible. The user needs to supply only an encode command and external power supplies for operation.

All models of the HAS-1201 A/D Converter are housed in 46-pin metal hybrid packages. The HAS-1201KM operates over a temperature range of 0 to +70°C. The HAS-1201SM is rated over an operating temperature range of -25°C to +85°C, but will operate with derated performance over a range of -55°C to +100°C. For units operating from -25°C to +85°C and military screening, order HAS-1201SMB; contact the factory for details about derated performance and military screening.

# **SPECIFICATIONS** (typical @ + 25°C with nominal power supplies unless otherwise noted)

### Compensation of Compensati	Parameter	Units HA	S-1201KM	HAS-1201SM/SMB	
March   Marc				*	·
ACCURACY Gain Properture Gain Properture Diff Nonlinearity N. Temp. Monotonicity Diff Nonlinearity N. Temp. Diff N. Dif				*	HAS-1201 PIN DESIGNATION
Gain v. Temperature	ACCURACY				IIAS-12011 IN DESIGNATION
Gailsty   Temperature	Gain		± 3	*	DIN FUNCTION DIN FUNCTION
DIFF				*	
Monotonicity				15	
DYNAMIC CHARACTERISTICS   1		ppm/ C			
In-Band Harmonics			Guaranteed		
Generation (1906Hz)   dis below PS (min)   80/75   *   dis below PS   75   *   dis below PS   distance of distance distan					
(1006Hz to 5000Hz)		dB below FS (min)	80 (75)	*	
Conversion Times				*	
Over Temperature				1.00	
Aperture Uncertainty (littler) ps, rms 30				1000	
Aperture Time (Delay)				*	
Transierri Response			25	*	34 NO CONNECTION 13 BIT 2
Over-rollage Recovery    1				*	
Topic Decided   MHz				*	
MHz		ns	1000		
Two-ToneLinetity		MHz	2	*	
Cys.Htz.plosskiz    Cys.Htz.plosskiz    Cys.Lept.plosskiz    Cys.Lept.			2	*	
NALOG KPUT			00		
NALIGGAPHO   2   BTT2 LIST   Companies   Complementary Offset   Co		dis below I'S	80	*	
Impedance (3V-N21 input)		(V CES)	F 0/100		
Impedance (SV-FsQL[pput)   Prince   P	Oltagerkanges	1 - 1	+15	*	
Impedance (SV   Imput)		v, max			PINS 2, 4, 5, 7, 24-30, 36 and 41 NEED TO BE CONNECTED
The content of the		Ω (max)	1000/2000 ( ± 1%)	/ / *	POSSIBLE. POWER SUPPLY VOLTAGES NEED TO BE
No.   Complementary		$\mathcal{L} \mathcal{L} \mathcal{L} \mathcal{L} \mathcal{L} \mathcal{L} \mathcal{L} \mathcal{L} $	24.10	11 = 1	
DIGITAL INPUTS				1 1 🖫 - 1	Tom Agron oscone
Logic Levels, TTL_Compatible		1 oppine s (max)	55(200)	<del>                                     </del>	NOTES -
Impedance		V	"0 -0 to + 0.4	L * /	<sup>1</sup> In-Band Harmonics expressed in terms of apur ous in-band signals
Impedance   LS TTL Loads   3		V	"1" = $+2.4$ to $+5$	/	generated at 1MHz encode rate at analog inputs shown in ( ).  Measured from leading edge of Encode Command to time associated
Frequency					data are valid.
Min				1.00	*For full-scale step input, 12-bit accuracy at ained in specified time.
Min Max         ns         50         *** (With analog input 40a Bladwer FS)           Register Strobe Width Min         ns         50         *** (With analog input 41a Bladwer FS)           Min         ns         50         *** (Part of the part of the pa		MITIZ, max	1.03	1.00	
Register Strobe Width   Min		ns	50	*	<sup>6</sup> With analog input 40dB below FS.
Min		ns	Encode Period - 350n	s *	
Max		22	50		<sup>8</sup> Externally adjustable to zero.
Enable Width Min				*	
Digital Loutputs	the state of the s	110	Elicode I eliou – 55011		range. Negative over-voltage inputs cause tri-state output to drift
Format	Min	ns	100	*	11 Case Temperature. Models HAS-1201SM/SMB will operate with
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$					derated performance over temperature range of -55°C to +100°C;
Logic Levels, TTL-Compatible   0	Format		2 C ND 7		<sup>12</sup> Maximum junction temperature is + 150°C.
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Logic Levels TTL -Compatible 10				
Time Skew   Delay: Register Strobe to   Output Data Validity   Delay: Register Strobe to   Output Data Validity   Output Data Validit	Logic Levels, 11 L-companie	*		*	Specifications subject to change without notice.
Delay: Register Strobe to Output Data Validity		TTL Loads	1	*	
Output Data Validity         Coding       30       *         Complementary Binary (CBIN)       *         Complementary Offset Binary (COB)       *         Complementary 2's Complement (C2SC)       *         POWER REQUIREMENTS       mA (max)       55 (70)       *         - 15V ± 5%       mA (max)       65 (80)       *         + 5V ± 5%       mA (max)       195 (2355)       *         - 5.2V ± 5%       mA (max)       35 (40)       *         Power Consumption       W (max)       3.0 (3.6)       *         TEMPERATURE RANGE <sup>11</sup> Operating       °C       0 to +70       -25 to +85         Storage       °C       -55 to +150       *         THERMAL RESISTANCE <sup>12</sup> Junction to Air, θja (Free Air)       °C/W       12       *         Junction to Case, θjc       °C/W       2.5       *         PACKAGE OPTION <sup>13</sup> HAS-1201KM       HAS-1201KM       HAS-1201KM		ns, max	10	*	
Complementary Binary (CBIN)         *           Complementary Offset Binary (COB)         *           Binary (COB)         *           Complementary 2's Complement (C2SC)         *           POWER REQUIREMENTS         *           + 15V ± 5%         mA (max)         55 (70)         *           - 15V ± 5%         mA (max)         65 (80)         *           + 5V ± 5%         mA (max)         195 (235)         *           - 5.2V ± 5%         mA (max)         35 (40)         *           Power Consumption         W (max)         3.0 (3.6)         *           TEMPERATURE RANGE <sup>11</sup> Operating         °C         0 to +70         -25 to +85           Storage         °C         0 to +70         -25 to +85           THERMAL RESISTANCE <sup>12</sup> Junction to Air, θja (Free Air)         °C/W         12         *           Junction to Case, θjc         °C/W         2.5         *           PACKAGE OPTION <sup>13</sup> HAS-1201KM         HAS-1201KM         HAS-1201SM		ns	30		
CBIN		ns		- v	
Binary (COB)   *   Complementary 2's   Complement (C2SC)   *				*	
Complementary 2's   Complement (C2SC)   *   POWER REQUIREMENTS				t	
Complement (C2SC)           POWER REQUIREMENTS           + 15V ± 5%         mA (max)         55 (70)         *           - 15V ± 5%         mA (max)         65 (80)         *           + 5V ± 5%         mA (max)         195 (235)         *           - 5.2V ± 5%         mA (max)         35 (40)         *           Power Consumption         W (max)         3.0 (3.6)         *           TEMPERATURE RANGE <sup>11</sup> Operating         °C         0 to +70         -25 to +85           Storage         °C         -55 to +150         *           THERMAL RESISTANCE <sup>12</sup> Junction to Air, θja (Free Air)         °C/W         12         *           Junction to Case, θjc         °C/W         2.5         *           PACKAGE OPTION <sup>13</sup> M-46         HAS-1201KM         HAS-1201KM				*	
POWER REQUIREMENTS         + 15V ± 5%       mA (max)       55 (70)       *         - 15V ± 5%       mA (max)       65 (80)       *         + 5V ± 5%       mA (max)       195 (235)       *         - 5.2V ± 5%       mA (max)       35 (40)       *         Power Consumption       W (max)       3.0 (3.6)       *         TEMPERATURE RANGE <sup>11</sup> Operating       °C       0 to +70       -25 to +85         Storage       °C       -55 to +150       *         THERMAL RESISTANCE <sup>12</sup> Junction to Air, θja (Free Air)       °C/W       12       *         Junction to Case, θjc       °C/W       2.5       *         PACKAGE OPTION <sup>13</sup> M-46       HAS-1201KM       HAS-1201KM       HAS-1201SM				*	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	POWER REQUIREMENTS		(0200)		
+5V ± 5%		mA (max)	55 (70)	*	
-5.2V ± 5% mA (max) 35 (40) *  Power Consumption W (max) 3.0 (3.6) *  TEMPERATURE RANGE <sup>11</sup> Operating °C 0 to +70 -25 to +85 Storage °C -55 to +150 *  THERMAL RESISTANCE <sup>12</sup> Junction to Air, θja (Free Air) °C/W 12 * Junction to Case, θjc °C/W 2.5 *  PACKAGE OPTION <sup>13</sup> M-46 HAS-1201KM HAS-1201SM		mA (max)	65 (80)	*	
Power Consumption         W (max)         3.0 (3.6)         ★           TEMPERATURE RANGE <sup>11</sup> °C         0 to +70         −25 to +85           Storage         °C         −55 to +150         ★           THERMAL RESISTANCE <sup>12</sup> Junction to Air, θja (Free Air)         °C/W         12         ★           Junction to Case, θjc         °C/W         2.5         ★           PACKAGE OPTION <sup>13</sup> HAS-1201KM         HAS-1201SM				*	
TEMPERATURE RANGE <sup>11</sup> Operating         °C         0 to +70         - 25 to +85           Storage         °C         - 55 to + 150         *           THERMAL RESISTANCE <sup>12</sup> Junction to Air, θja (Free Air)         °C/W         12         *           Junction to Case, θjc         °C/W         2.5         *           PACKAGE OPTION <sup>13</sup> M-46         HAS-1201KM         HAS-1201KM				*	
Operating Storage         °C or - 55 to + 150         - 25 to + 85 or - 25 to + 85 or - 25 to + 85 or - 25 to + 150           THERMAL RESISTANCE <sup>12</sup> Junction to Air, θja (Free Air) or C/W 12 * Junction to Case, θjc or C/W 2.5 * *           PACKAGE OPTION <sup>13</sup> M-46         HAS-1201KM         HAS-1201KM		+ (max)	3.0 (3.0)		
Storage		°C	0  to  + 70	-25 to + 85	
Junction to Air, θja (Free Air)       °C/W       12       *         Junction to Case, θjc       °C/W       2.5       *         PACKAGE OPTION¹³       HAS-1201KM       HAS-1201KM					
Junction to Case, θjc         °C/W         2.5         *           PACKAGE OPTION¹³         HAS-1201KM         HAS-1201KM	THERMAL RESISTANCE <sup>12</sup>				
PACKAGE OPTION <sup>13</sup> M-46 HAS-1201KM HAS-1201SM	Junction to Air, 0ja (Free Air)			*	
M-46 HAS-1201KM HAS-1201SM		°C/W	2.5	*	
HACIMICAN	M-46		HAS-1201KM		
HAS1201SMB				HAS1201SMB	

### **Theory of Operation**

#### THEORY OF OPERATION

Refer to the block diagram of the HAS-1201 A/D Converter.

This is a functional illustration of the HAS-1201 A/D Converter. Internally, the converter uses digitally corrected subranging (DCS) pioneered by Analog Devices to generate 14 bits of digital data. The two extra bits are used for digital correction to assure that the 12 bits of parallel output data are an accurate representation of the analog input signal present at the time of the encode command.

The analog signal to be digitized is applied to an internal track-and-hold (T/H), whose change between the "track" and "hold" modes is determined by the HAS-1201 internal timing circuits. Applying an encode command (at Pin 3) triggers these circuits and causes the required timing/signals to be generated.

Timing intervals for the various signals involved in the operation of the HAS-1201 A/D Converter are shown in Figure 1.

Understanding the operation of the HAS 201 is easiest when the timing of events is related to the leading edge of the Encode Command. Minimum width of that signal is 50ns; maximum width is the period of the encode rate less 350ns. A square wave is always an acceptable encode signal for the HAS-1201 converter.

For purposes of illustration, spacing between Encode Commands #1 and #2 in Figure 1 is approximately equal to a word rate of 500kHz.

When the encode command is applied, the unit switches to the hold mode for approximately 670 nanoseconds; the length of the track mode is a function of word rate. When operated at its maximum frequency, the HAS-1201 will remain in "track" 280

nanoseconds, the interval required for internal processing of data.

During the first 50 nanoseconds of each hold period, valid data resulting from the previous encode command continue to be applied to the output register. But then, internal switching within the HAS-1201 causes changes to occur until the conversion cycle initiated by the most recent encode command is completed.

Referenced to the leading edge of the encode command, minimum spacing on the Register Strobe is 950ns; maximum spacing is shown with the Register Strobe in dotted lines.

Output data at Pins 11-23 remain valid until updated by a Register Strobe. As noted, this validity interval is based on having the ENABLE connected to either digital "0" or ground.

In Figure 1, the timing of the signals labeled ENABLE and OUTPUT DATA are not referenced to the ENCODE COMMAND; their timing is related only to each other.

pulse is used to strobe output data into external the user must assure its arrival corresponds to the availability of valid data. When the ENABLE is at digital "1", output data present a high impedance to external circuits. Changing ABLE to a digital "0" causes the three-state logic outputs to impedances and makes them available for strobing. liagram, external connection of encode command (Pin 3) to the register strobe (Pin 8) is the connection which might be used if the HAS-1201 were operating at a tinuous maximum encode rate of 1.05MHz. Under these cumstances, the output data resulting from Encode Command #1 will be strobed out of the converter with the leading edge of Encode Command #2.

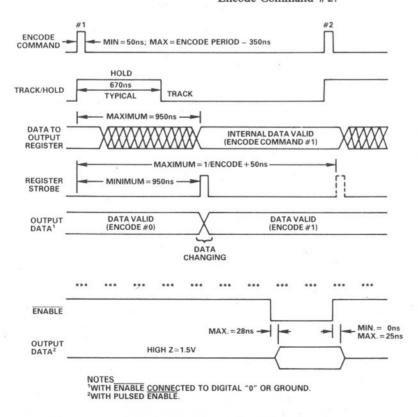


Figure 1. HAS-1201 Timing Diagram

### OPERATING HAS-1201 AT WORD RATES LESS THAN MAXIMUM

If encode commands are applied asynchronously, direct connection of these pins results in variations in the times when output data are available, because of pipeline delay through the converter and the differences in intervals between encode commands.

With Pins 3 and 8 connected, the leading edge of each encode command is the signal which strobes output data generated by the *preceding* encode command. There is no separate, designated output signal indicating data are valid.

As an example, assume the HAS-1201 encode rate varies around 500kHz, but with relatively large differences in the times between encode commands. Under these conditions, the availability of output data will vary; it is often preferable to have outputs available a specified interval after each encode command. A method to achieve this is shown in Figure 2.

The insertion of a delay circuit between the encode command input and the strobe input of the HAS-1201 makes it possible to use each digital output word at a precise time after its associated encode command, even when operating the converter asynchronously.

The delay circuit can take any of several forms. The user may opt to use a fixed delay line with a delay of 950ns or more; in other cases, shift registers could be used. Another possibility is a variable delay, such as multivibrators, adjusted to the optimum delay for each application.

In this latter approach, the period of the multivibrators can be set to any desired time between a minimum of 950ns (the period of 1.05MHz) and a maximum determined by the period of the highest word rate to be used.

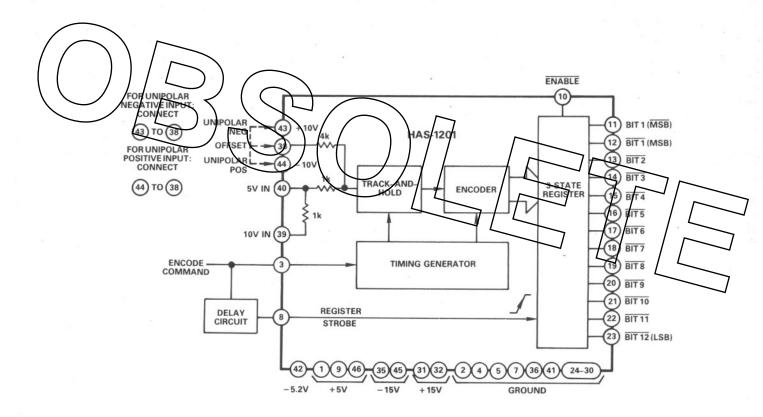
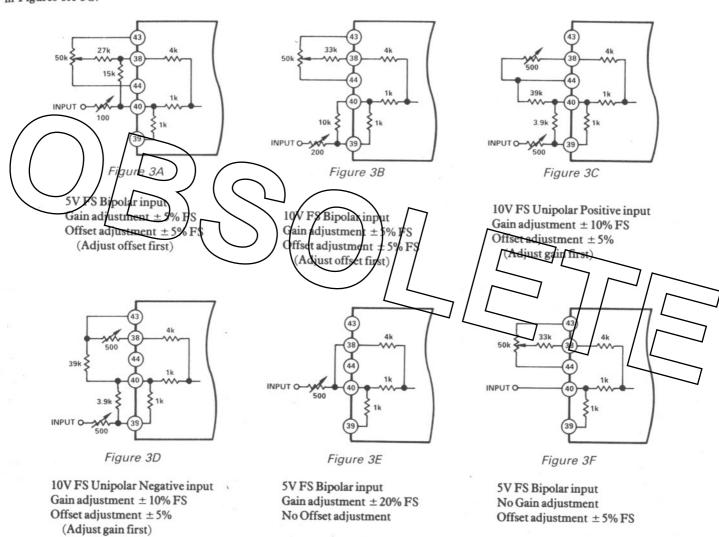


Figure 2. HAS-1201 Connection Diagram

#### **CONNECTING HAS-1201 A/D CONVERTER**

At the analog input, the user connects offset (Pin 38) externally to either Pin 43 or Pin 44 to obtain, respectively, unipolar negative or unipolar positive input ranging. The analog signal to be digitized is applied to Pin 39, the 10V input; or to Pin 40, the 5V input, depending upon the application. Examples are shown in Figures 3A-3G.

In Figure 3G, the recommended operational amplifier is an AD741. For 5V Unipolar Negative inputs using this circuit, connect Pin 43 to the positive input of the op amp and leave Pin 44 open.



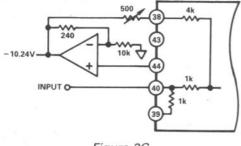


Figure 3G

5V Unipolar Positive input Offset adjustment ± 5% No Gain adjustment (see text) Various input ranges with fixed gain and offset are shown in Table I.

INPUT RANGE	CONNECT PINS	INPUT PIN
10V Bipolar	None	39
10V Uni. Pos.	38 to 44	39
10V Uni. Neg.	38 to 43	39
5V Bipolar	None	40
V Uni. Pos.	38 to 44	40
5V Uni. Neg.	38 to 43	40
V Bipolar	38 to 40	40
(800 ohms imped	dance)	

Table I.

Regardless of the input connection being used, certain basic rules of layout should be observed for any high-speed circuit; this is particularly important for high-resolution devices such as the HAS-1201.

Bypass capacitors are used internally, but all power supplies should be bypassed externally, with  $0.01\mu F$ – $0.1\mu F$  ceramic capacitors. Electrolytic capacitors of 10-22 microfarads should also be used on each supply; all capacitors should be connected as closely as possible to the supply pins.

A massive ground plane, careful component layout, and physically separating analog and digital signals are among other requirements for assuring the high-speed, high-resolution characteristics of the HAS-1201 A/D Converter.

Supply voltages must be applied to all pins for which they are designated. It is also extremely important to connect all grounds together, and to a solid, low-impedance ground plane.

Cooling air should be passed over the unit when it is being operated; it should be supplied at 300-500 linear feet per minute (LPPM).

The ENABLE signal at Pin 10 can be used for connecting the three-state logic outputs of the HAS-1201 to a bus. A logic "1" at this pin makes the logic outputs "float" at approximately 1.5 tolts and causes them to be high impedances during the time other signals are applied to the computer or microprocessor bus. If the HAS-1201 is not connected to a bus, i.e., it is being used as a system A/D, the ENABLE pin should be connected to logic "0" or ground.

When using the unit as a (free-standing) system A/D, the user should keep in mind the output characteristic noted in the footnotes of the Specifications table on Page 2 of this data sheet.

As a negative-going analog input is increased in value, the digital output of the HAS-1201 follows the changes until all outputs are at logic "1" (unit is operating with Complementary Offset Binary logic), indicating maximum negative analog input. Any further increase in negative input (overranging) will cause the tri-state digital outputs to "float".

The exception to this is the Bit  $1 (\overline{MSB})$  at Pin 11. Internal pulldown resistors cause it to go to logic "0" and remain.

When they are in an overrange condition, the digital outputs need to look "high". This means the load on the output must pull the open circuits to the "high" state; this requirement normally presents no problem when driving standard TTL or Schottky TTL inputs.

When driving low-power Schottky inputs, the change to "high" will have a slower rise time; it may require up to 100ns. For these, the user should avoid clocking the output data too soon.

CMOS circuits have no provision for pulling up the converter's outputs. In this situation, the recommended procedure is to use 2k pull-up resistors connected to +5 volts.

#### **TESTING HAS-1201 PERFORMANCE**

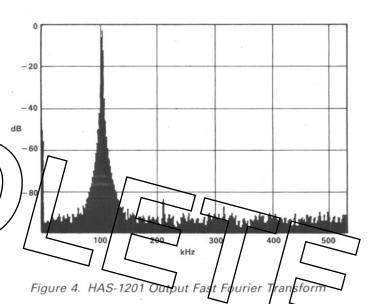
Sophisticated converters of the type represented by the HAS-1201 A/D Converter require sophisticated testing to assure they meet or exceed their specified performance parameters. One of these test methods is a Fast Fourier Transform (FFT) analysis of the converter output.

The results of that testing are shown in Figure 4.

This diagram is an average analysis, based on ten readings. In the test, a 104kHz sine wave is applied as the analog input (f<sub>o</sub>), at a level of 1dB below full scale; the HAS-1201 is operated at a word rate of 1.05MHz.

The FFT is based on 512 sample points, with Hanning weighting applied to the digital representations of the analog samples. The resulting spectrum demonstrates the exceptional performance of the converter, particularly in terms of low noise and harmonic distortion.

In Figure 4, the vertical scale is based on a full-scale input referenced as 0dB. In this way, all (frequency) energy cells can be calculated with respect to full-scale rms inputs.



Besides the plot shown, the computer testing also supplies numerical data stipulating the precise readings of the second and third harmonics; and the signal-to-noise ratio (SNR). These numbers have been replaced by a horizontal frequency scale for purposes of illustration.

The original numbers indicated the peak amplitude of the second harmonic (208kHz) was at a level of -81dB; the third harmonic (312kHz) was at -85dB. The signal-to-noise ratio was measured at 67.5dB, which corresponds to a noise floor of -68.5dB. All of these numbers, like the plot, are 10-run averages of 512 sample points in each run.

The harmonic distortion numbers include five energy cells on either side of the harmonics of  $2 \times f_o$ , and  $3 \times f_o$ . Including these cells helps negate the effects of side lobes caused by the Hanning weighting and non-coherent sampling used for testing.

Hanning, or cosine, weighting is one of several methods of generating FFT data; each method has certain characteristics which make it more or less appropriate for various applications.

#### **ORDERING INFORMATION**

Three models of the HAS-1201 A/D Converter are available. For commercial operating temperatures between 0 and  $+70^{\circ}$ C, order model number HAS-1201KM. The HAS-1201SM is rated over an operating temperature range of  $-25^{\circ}$ C to  $+85^{\circ}$ C, but will operate with derated performance over a range of  $-55^{\circ}$ C to  $+100^{\circ}$ C. For units operating from  $-25^{\circ}$ C to  $+85^{\circ}$ C and military screening, order HAS-1201SMB; contact the factory for details about derated performance and military screening.