1988 p2-335 0805

ANALOG DEVICES

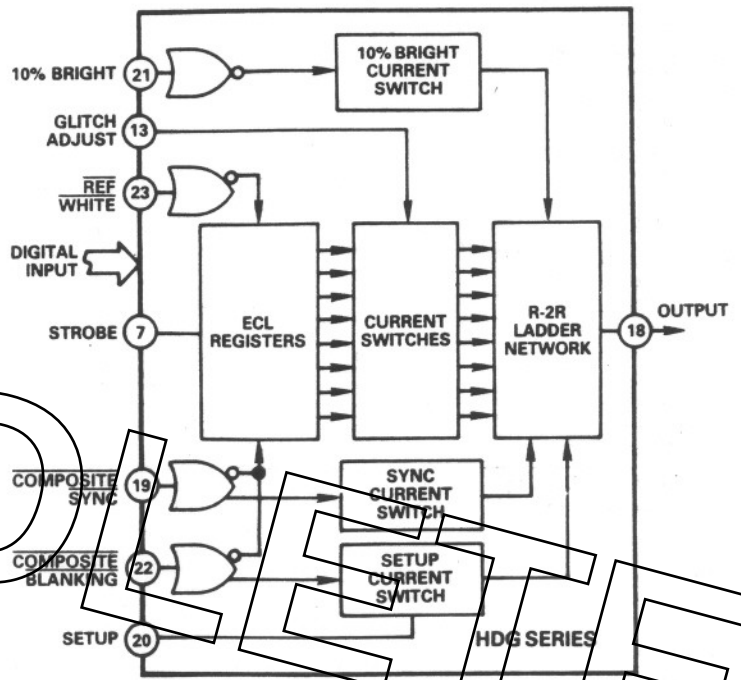
Hybrid Video Digital-to-Analog Converters

HDG SERIES

FEATURES
- Update Rates to 150MHz
- Low Glitch Energy
- Complete Composite Inputs
- Single −5.2V Power Supply
- Military Temperature Range Available

APPLICATIONS
- Raster Scan Displays
- Color Graphics
- Analytical Instrumentation
- TV Video Reconstruction

HDG SERIES FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The HDG-Series D/A Converters have become the standard of comparison for fast-settling D/A's with complete composite inputs.

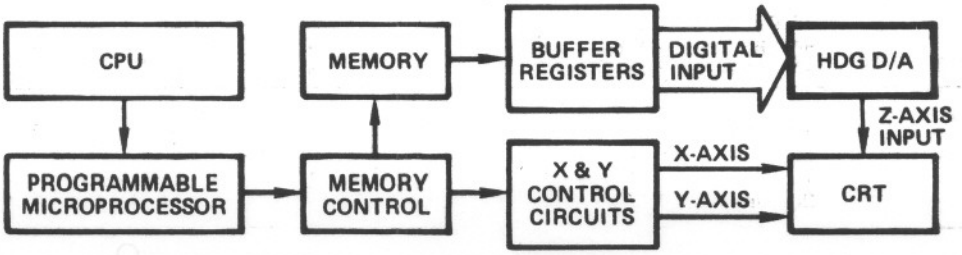
The units are available in three resolutions, or levels, of Gray Scale output. The HDG-0405 accepts four bits (16 levels) of digital input; the HDG-0605 has six bits (64 levels); and the HDG-0805 is an eight-bit (256 levels) device.

All versions have complete composite controls, including self-contained, digitally-controlled sync and blanking; and a reference white control input to help assure compatibility with EIA Standards RS-170, RS-330, and RS-343-A. Their performance is enhanced even more with a 10% bright input capability.

Output inpedance on all units is 75 ohms and their full-scale output current is capable of developing standard video levels across video loads. In addition to all of these characteristics which make them easy to incorporate into circuits, the need for a single −5.2V power supply also adds to their attractiveness.

Model numbers without suffixes designate the "original" HDG Series D/A Converters and are housed in 24-pin metal packages. Model numbers which include suffixes make use internally of the Analog Devices Model AD9700 to obtain better performance at a lower price; these devices are housed in ceramic DIP packages.

The "BD" and "BW" versions in the newer (suffixed) units are close equivalents to the original design, but a number of advantages accrue by using the newer units. Note particularly the parameters for linearity tempco; strobe input loading; Composite Sync and Composite Blanking outputs; Power Supply Rejection Ratio (PSRR); supply current; and power dissipation. Conversely, the original design is slightly better in terms of voltage settling time, glitch energy, and output compliance.



Typical Raster Scan Display System

Parameter	Units	HDG–0405	HDG–0605	HDG–0805	HDG–0405BD/ BW/SD	HDG–0605BD/ BW/SD	HDG–0805BD/ BW/SD
OUTPUT – REFERENCE WHITE[5]							
Current							
Logic "1"	mA (±4%)	Normal Operation	*	*	*	*	*
Logic "0"	mA (±4%)	0 or −1.9	*	*	*	*	*
Voltage							
Logic "1"	mV (±4%)	Normal Operation	*	*	*	*	*
Logic "0"	mV (±4%)	0 or −71					
OUTPUT – 10% BRIGHT[6]							
Current							
Logic "1"	mA (±5%)	−1.9	*	*	*	*	*
Logic "0"	mA (±5%)	0	*	*	*	*	*
Voltage							
Logic "1"	mV (±5%)	−71	*	*	*	*	*
Logic "0"	mV (±5%)	0	*	*	*	*	*
OUTPUT – COMPOSITE SYNC[6,7]							
Current							
Logic "1"	mA (±4%)	0	*	*	*	*	*
Logic "0"	mA (±4%)	−7.6	*	*	−8.6	−7.8	−7.6
Voltage							
Logic "1"	mV (±4%)	0	*	*	*	*	*
Logic "0"	mV (±4%)	−285	*	*	−322.5	−292.5	−285
OUTPUT – COMPOSITE BLANKING[6,7] (Assumes Setup is Open, Which is Equiavalent to 10 IRE Units)							
Current							
Logic "1"	mA (±4%)	0	*	*	*	*	*
Logic "0"	mA (±4%)	−1.9	*	*	−2.9	−2.1	−1.9
Voltage							
Logic "1"	mV (±4%)	0	*	*	*	*	*
Logic "0"	mV (±4%)	−71	*	*	−108.7	−78.7	−71
POWER REQUIREMENTS							
−5.2V ±0.25V[8]	mA (max)	200 (225)	260 (290)	320 (360)	125 (140)	**	**
Power Supply Rejection Ratio	%/%	1/1	*	*	0.005/1	**	**
Power Dissipation	mW (max)	1040 (1170)	1350 (1510)	1665 (1875)	650 (730)	**	**
TEMPERATURE RANGE							
Operating (Case)[9]	°C	−25 to +85	*	*	* (BD and BW)	* (BD and BW)	* (BD and BW)
Operating ("SD" Case)	°C				−55 to +125	−55 to +125	−55 to +125
Storage	°C	−55 to +150	*	*	*	*	*
THERMAL RESISTANCE[10]							
Junction to Air, θ_{ja} (free air)	°C/W, max	45	*	*	*	*	*
Junction to Case, θ_{jc}	°C/W, max	12	*	*	*	*	*
MTBF[11] Mean Time Between Failures	Hours						3.23×10^5
PACKAGE OPTIONS[12]							
M–24A		HDG-0405	HDG-0605	HDG-0805			
DH-24B					HDG-0405BD	HDG-0605BD	HDG-0805BD
					HDG-0405BW	HDG-0605BW	HDG-0805BW
					HDG–0405SD	HDG-0605SD	HDG-0805SD

NOTES
[1]Settling to GS percentage includes FS and MSB transitions. Inherent 3ns register delay (50%) points) is not included.
[2]Minimum update rates limited by full-scale settling time for useable number of bits for each converter.
Units can be updated to 150MHz with settling degradation.
[3]Glitch can be reduced with glitch adjustment.
[4]LSB value used for calibration causes Gray Scale output to be 637.5mV rather than 643mV shown in idealized composite waveform; both values are well within the output and EIA Standard RS-170 tolerances.
[5]Effect on analog output of logic "0" at Reference White input depends on 10% Bright signal input (See Table I).
[6]10% Bright, Composite Sync, and Composite Blanking outputs shown add to Gray scale analog output at Pin 18 (See Table I).
[7]Composite Sync or Composite Blanking control signals reset input registers. Composite Sync or Composite Blanking should not be operated simultaneously with Reference White.
[8]Power supply must have less than 5mV p-p ripple.
[9]Operating temperature −55°C to +125°C on "SD" units.
[10]Maximum junction temperature = 150°C.
[11]Calculated for HDG-0805SDB using MIL HNBK-217; Ground Fixed; +25°C Ambient.
[12]See Section 13 for package outline information.
* Specification same as HDG-0405.
** Specification same as HDG-0405BD/BW/SD.
Specifications subject to change without notice.

SPECIFICATIONS (typical @ + 25°C with nominal power supplies unless otherwise noted)

Parameter	Units	HDG–0405	HDG–0605	HDG–0805	HDG–0405BD/ BW/SD	HDG–0605BD/ BW/SD	HDG–0805BD/ BW/SD
RESOLUTION	Bits	4	6	8	4	6	8
LEAST SIGNIFICANT BIT (LSB) WEIGHT							
Voltage (adjustable)	mV	40	10	2.5	40	10	2.5
Current (adjustable)	μA	1067	267	67	1067	267	67
ACCURACY							
(GS = Gray Scale; FS = Full-Scale)							
Linearity	± % GS	3.2	0.8	0.2	3.2	0.8	0.2
Differential Linearity	± % GS, max	3.2	0.8	0.2	3.2	0.8	0.2
Zero Offset (Initial)							
Voltage	mV, max	0.9	*	*	*	*	*
Monotonicity		Guaranteed	*	*	*	*	*
TEMPERATURE COEFFICIENTS							
Linearity	ppm/°C (max)	20 (35)	*	*	15 (30)	**	**
Gain	ppm/°C (max)	50 (125)	*	*	*	*	*
Zero Offset	ppm/°C (max)	10 (15)	*	*	*	*	*
DYNAMIC CHARACTERISTICS – GRAY SCALE OUTPUT[1]							
Settling Time (0V to FS GS change)	% GS;	6.4	1.6	0.4	6.4	1.6	0.4
Voltage	ns (max)	4 (5)	6 (8)	8 (10)	5 (6)	7 (9)	9 (11)
Update Rate[2]	MHz (min)	150 (125)	*	*	*	*	*
Slew Rate	V/μs	200	*	*	*	*	*
Rise Time	ns	2	*	*	*	*	*
Glitch Energy[3]	pV-s	50	*	*	80	**	**
DIGITAL DATA INPUTS							
Logic Compatibility		ECL	*	*	*	*	*
Coding		Complementary Binary (CBN)	*	*	*	*	*
Logic Levels							
"1"	V (min/max)	−0.9 (−1.1/−0.6)	*	*	*	*	*
"0"	V (min/max)	−1.7 (−2.0/−1.5)	*	*	*	*	*
Loading (each bit)		5pF and 50kΩ to −5.2V	*	*	*	*	*
STROBE INPUT							
Logic Compatibility		ECL	*	*	*	*	*
Logic Levels							
"1"	V (min/max)	−0.9 (−1.1/−0.6)	*	*	*	*	*
"0"	V (min/max)	−1.7 (−2.0/−1.5)	*	*	*	*	*
Loading		50pF and 5kΩ to −5.2V	*	*	5pF and 50kΩ to −5.2V	**	**
Setup Time (Data)	ns, min	2.5	*	*	*	*	*
Hold Time (Data)	ns, min	1.5	*	*	*	*	*
Propagation Delay	ns (max)	3 (4)	*	*	*	*	*
10% BRIGHT, REFERENCE WHITE, COMPOSITE SYNC, AND COMPOSITE BLANKING INPUTS							
Logic Compatibility		ECL	*	*	*	*	*
Logic Levels							
"1"	V (min/max)	−0.9 (−1.1/−0.6)	*	*	*	*	*
"0"	V (min/max)	−1.7 (−2.0/−1.5)	*	*	*	*	*
Loading		5pF and 50kΩ to −5.2V	*	*	*	*	*
SPEED PERFORMANCE – CONTROL INPUTS							
Settling Time to 10% of Final Value for:							
10% Bright	ns (max)	8 (10)	*	*	*	*	*
Reference White	ns (max)	8 (10)	*	*	*	*	*
Composite Sync	ns (max)	8 (10)	*	*	*	*	*
Composite Blanking	ns (max)	8 (10)	*	*	*	*	*
SETUP CONTROL							
Ground	mV (IRE Units)	0 (0)	*	*	*	*	*
Open	mV (IRE Units)	71 (10)	*	*	*	*	*
−5.2V	mV (IRE Units)	142 (20)	*	*	*	*	*
ANALOG OUTPUT							
GS Current	mA (± 1%)	0 to −16	0 to −16.8	0 to −17	0 to −16	0 to −16.8	0 to −17
GS Voltage[4]	mV	0 to −600	0 to −630	0 to −637.5	0 to −600	0 to −630	0 to −637.5
Compliance	V	−1.1 to +1.1	*	*	−1.2 to +0.1	**	**
Internal Impedance	Ω (min/max)	75 (71/79)	*	*	*	*	*

PIN DESIGNATIONS

Pin	Function	Pin	Function
12	GROUND	13	GLITCH ADJUST
11	BIT 8 (LSB)	14	GROUND
10	BIT 7	15	GROUND
9	BIT 6	16	GROUND
8	BIT 5	17	GROUND
7	STROBE	18	ANALOG OUTPUT
6	BIT 4	19	COMPOSITE SYNC
5	BIT 3	20	SETUP
4	BIT 2	21	10% BRIGHT
3	BIT 1 (MSB)	22	COMPOSITE BLANKING
2	−5.2V	23	REFERENCE WHITE
1	GROUND	24	−5.2V

NOTES: For HDG-0605 units, Pin 9 is LSB; Pins 10 and 11 are present but not used. For HDG-0405 units, Pin 6 is LSB; Pins 8, 9, 10, and 11 are present but not used. Connect Pins 1, 12, and 14–17 together and to low-impedance ground plane as close to case as possible.

USING HDG-SERIES UNIT FOR RASTER SCAN

Refer to the block diagram of the HDG-Series D/A Converter and the idealized composite output waveform.

The digital input bits represent the Gray Scale values (the discrete levels between Reference Black and Reference White) in a composite video signal. For HDG-0405 units, there are 16 (2^4) of these levels; for the HDG-0605, 64 (2^6) levels; and for the HDG-0805, 256 (2^8) levels.

The input bits are applied to Pins 3–6 (only, for the HDG-0405), and Pins 8 and 9 for the HDG-0605; or Pins 8–11 for the HDG-0805.

The output analog signal (at Pin 18) will be a function of these digital inputs. The output will also be affected by the ECL levels at the control inputs of 10% Bright, Reference White, Composite Sync, and Composite Blanking; and the level of the control signal (expressed in terms of IRE units) at the Setup input.

The total effect of these combined signals can be illustrated in a truth table format if arbitrary values are assigned for Gray scale inputs, and various combinations of control inputs are selected.

Refer to Table I.

DIGITAL INPUTS VS. ANALOG OUTPUT

BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	BIT 8	10% BRIGHT	REF. WHITE	BLANKING	COMP. SYNC	ANALOG OUTPUT IN mV[1] (HDG-0805BD/BW/SD)
1	1	1	1	1	1	1	1	0	1	1	1	0
1	1	1	1	1	1	1	1	1	1	1	1	−71
1	0	0	0	0	0	0	0	0	1	1	1	−320
0	0	0	0	0	0	0	0	0	1	1	1	−637.5
0	0	0	0	0	0	0	0	1	1	1	1	−708.5
X	X	X	X	X	X	X	X	0	0	1	1	0
X	X	X	X	X	X	X	X	1	0	1	1	−71
X	X	X	X	X	X	X	X	0	1	0	1	−637.5[2]
X	X	X	X	X	X	X	X	0	1	0	1	−708.5mV[3]
X	X	X	X	X	X	X	X	0	1	0	1	−779.5mV[4]
X	X	X	X	X	X	X	X	0	1	0	0	−922.5mV[2]
X	X	X	X	X	X	X	X	0	1	0	0	−993.5mV[3]
X	X	X	X	X	X	X	X	0	1	0	0	−1064.5mV[4]
X	X	X	X	X	X	X	X	1	1	0	0	−993.5mV[2]
X	X	X	X	X	X	X	X	1	1	0	0	−1064.5mV[3]
X	X	X	X	X	X	X	X	1	1	0	0	−1135.5mV[4]

NOTES

[1]Values are for Gray Scale output of 8-bit D/A's. To determine full-scale Gray Scale output for 4-bit units, subtract total value of 4 LSB's (37.5mV) from 8-bit output shown. To determine output of 6-bit units, subtract total value of 2 LSB's (7.5mV) from 8-bit output shown.

[2]Setup (Pin 20) grounded. (0 IRE units)

[3]Setup (Pin 20) open. (10 IRE units)

[4]Setup (Pin 20) to −5.2V (20 IRE units)

Actual analog output value of −637.5mV is different from ideal value of −643mV because of LSB value used in calibration.

Table I. Digital Inputs vs. Analog Output

As the footnote to the table points out, the actual full-scale (−637.5mV) output of the HDG units is different from the ideal −643mV output shown in the composite waveform.

The two are different because Analog Devices uses 2.5mV for weighting the LSB during calibration of the converter. The disparity does not cause any problems in using the device, since both the ideal value and the actual value are well within the tolerances of the output and the RS-343 standard.

Referring again to the block diagram, the Strobe input applied to the HDG D/A clocks the input registers when the strobe signal makes the transition from a logic "0" to a logic "1". The purpose of the registers is to remove time skew from the digital input bits and minimize perturbations or "glitches" in the analog output signal.

A logic "0" applied to either the $\overline{\text{Composite Sync}}$ or $\overline{\text{Composite Blanking}}$ input (on the HDG-0805) resets the input registers to 00/000 000. The analog output at Pin 18 will be −922.5mV (−637.5mV plus −285mV) if the $\overline{\text{Composite Sync}}$ input is operated; this is not affected by the value of IRE units at the Setup input.

A logic "0" signal applied to the $\overline{\text{Reference White}}$ input sets the input registers, thereby overriding the video input word. When this occurs, the analog output of the converter goes to 0V or to −71mV, depending upon whether or not the 10% Bright signal is also operated.

When $\overline{\text{Composite Blanking}}$ is operated, the analog output will go to its full-scale value of −637.5mV plus some additional amount, as determined by the voltage at Setup. The −71mV example used in the Specifications section of the data sheet is based on the Setup input floating, which is equivalent to 10 IRE units. (For this example, the analog output would be 708.5mV.)

Details on the connections for using a Model HDG-0805 D/A Converter in composite video applications are shown in Figure 2.

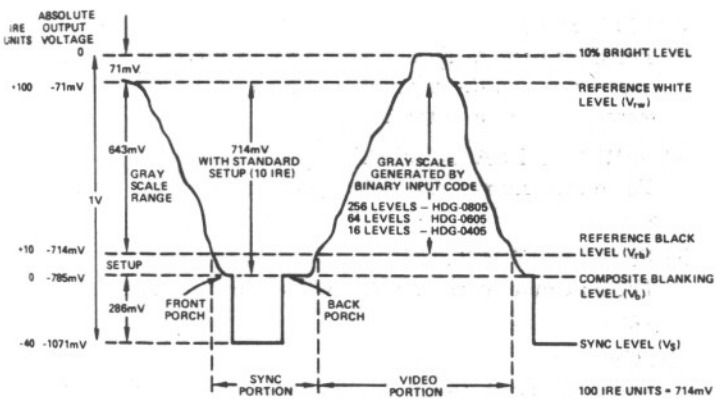


Figure 1. Composite Output Waveform

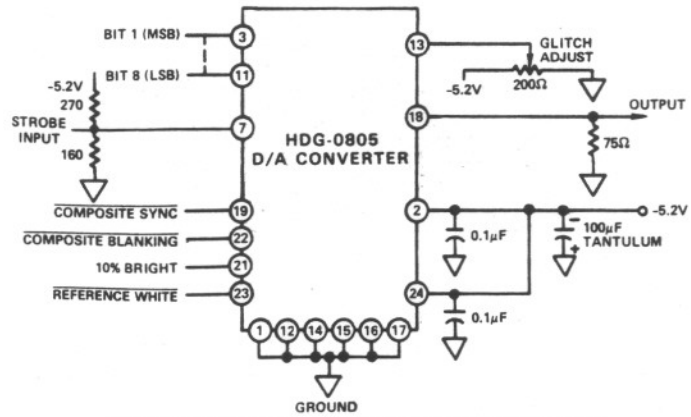


Figure 2. HDG-0805 Typical Connection Diagram

Ground pins 1,12, and 14 – 17 are shown connected together and to ground near the unit; this is the recommended procedure for obtaining optimum performance, especially in high-speed applications. A large ground plane is a "must."

The performance of the HDG devices can be enhanced with external bypass capacitors which will supplement the internal components. Low-frequency bypassing should be provided with a 1μF (or larger) tantalum capacitor between the −5.2V supply pin and ground. High-frequency bypassing can be provided with ceramic capacitors of 0.1μF or larger. All bypass capacitors should be tied as closely as possible to the −5.2V supply pins on the hybrid.

The external potentiometer shown connected to Pin 13 changes the threshold of the internal current switches and can reduce the amount of glitch from its typical 50pV-s to a lesser value for those applications which require it.

Figure 3 is a photo of the mid-scale glitch of a Model HDG-0805 D/A Converter; the measurement was made using the 50-ohm input of a sampling scope as the termination for the D/A.

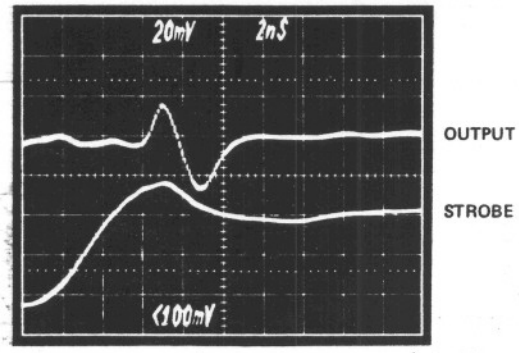


Figure 3. Midscale Glitch

The output of the converter was connected directly to the scope, using appropriate BNC fittings, rather than a scope probe. As shown, positive and negative glitch excursions are approximately equal and opposite with values of 30 picovolt-seconds each; net glitch energy is approximately zero. In those instances where the two are unequal, the glitch adjust circuit shown in Figure 1 can be used to compensate for differences between them.

For best performance, standard 24-pin hybrid sockets should be avoided. Individual pin sockets are preferable for evaluating devices; in final designs, the D/A should be soldered directly into the printed circuit board without sockets.

If it is necessary to route digital signals and/or strobe signals for distances greater than one inch (2.54cm), microstrip techniques should be used. Otherwise, the performance of the D/A converter may be affected adversely.

The power supply rejection ratio (PSRR) of the basic HDG-Series units is 1:1; in the units bearing suffix designators, it is 0.005/1. In the basic units, their PSRR means a 1% change in the −5.2V power supply voltage will cause a 1% change at the output of the converter. This usually presents no problems in using the HDG-0405 or HDG-0605 devices, since even a 5mV ripple on the power supply translates into less than 1/2LSB error at the output of those units.

If regulation is desired or needed for 8-bit converters, use an LM120 or equivalent 3-terminal negative regulator. When the −5.2V supply is highly regulated, it may help counteract changes in output caused by time and temperature.

Figure 4 shows a circuit capable of supplying a precise −5.2V supply for the HDG-Series converters.

This circuit uses an AD584 and AD OP-07 to achieve an ultra stable −5.2V power supply input to the D/A.

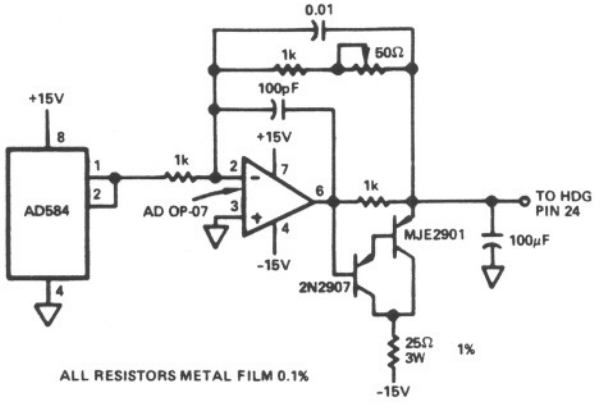


Figure 4. Precision −5.2V Supply

ORDERING INFORMATION

There are 12 versions of converters in the standard HDG-Series of D/A's. For a temperature range of −25°C to +85°C, specify the HDG-0405, HDG-0405BD, or HDG-0405BW; HDG-0605, HDG-0605BD, or HDG-0605BW; or the HDG-0805, HDG-0805BD, or HDG-0805BW. For a military temperature range of −55°C to +125°C, specify HDG-0405SD, HDG-0605SD, or HDG-0805SD. In these model numbers, the "D" in the suffix indicates a ceramic, hermetically-sealed DIP; and the "W" indicates a non-hermetic ceramic DIP. Units without suffixes are housed in 24-pin metal packages.

Versions are available screened to military requirements, with an "SDB" suffix on the model number; contact the factory for details. In addition, it is also possible to order HDG units with synchronous functions on a "special order" basis; these are available only for those devices containing suffixes in the part number.

DEFINITION OF VIDEO TERMS

BLANKING LEVEL
: The level separating the SYNC portion from the Video portion of the waveform. Usually referred to as the Front Porch or Back Porch. At 0 IRE Units, it is the level which will shut off the picture tube, resulting in the blackest possible picture.

COLOR VIDEO (RGB)
: This usually refers to the technique of combining the three primary colors of Red, Green, and Blue to produce color pictures within the usual spectrum. In RGB monitors, three HDG Series DACs would be required, one for each color.

COMPOSITE SYNC SIGNAL (SYNC)
: The portion of the composite video signal which synchronizes the scanning process.

COMPOSITE VIDEO SIGNAL
: The video signal with or without setup, plus the composite SYNC signal.

GRAY SCALE
: The discrete levels of video signal between Reference Black and Reference White levels. A 10-bit DAC contains 1,024 different levels, while an 8-bit DAC contains 256 (2^N).

RASTER SCAN
: The most basic method of sweeping a CRT one line at a time to generate and display images. This method is used in commercial television in the USA.

REFERENCE BLACK LEVEL
: The maximum negative polarity amplitude of the video signal.

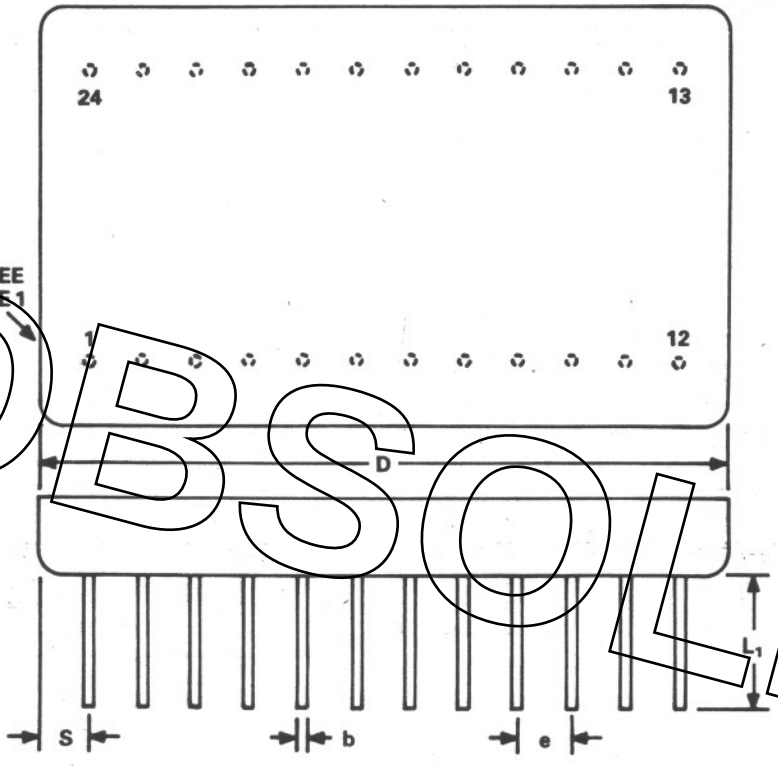
REFERENCE WHITE LEVEL
: The maximum positive polarity amplitude of the video signal.

SETUP
: The difference between the Reference Black level and the blanking level. This should not be confused with setup as used with digital logic.

SYNC LEVEL
: The peak level of the composite SYNC signal.

VIDEO SIGNAL
: That portion of the composite video signal which varies in gray scale levels between Reference White and Reference Black. Also referred to as the picture signal, this is the portion which may be visually observed.

M-24A
24-Lead Metal Platform DIP



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
b	0.014	0.023	0.36	0.58	
D	1.265	1.280	32.131	32.51	
E	0.765	0.780	19.431	19.80	
E_1	0.590	0.620	12.95	15.75	3
e	0.090	0.110	2.29	2.79	4
L_1	0.230	0.270	5.84	6.85	
S		0.090		2.29	2

NOTES
1. Index area; a notch or a lead one identification mark is located adjacent to lead one.
2. Applies to all four corners.
3. E_1 shall be measured at the centerline of the leads.
7. Twenty-two spaces.