Hybrid Video Digital-to-Analog Converters

HDL-3805/3806

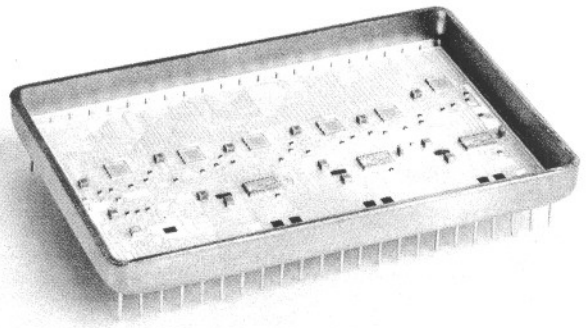
PRELIMINARY DATA

FEATURES

- Triple 8-Bit D/A with LUTs
- 115MHz Update Rates
- RGB Composite Functions
- Small Size (2.3″ × 1.5″)
- Latched Composite Functions (HDL-3806)

APPLICATIONS

- Raster Scan Displays
- Color Graphics Systems



GENERAL DESCRIPTION

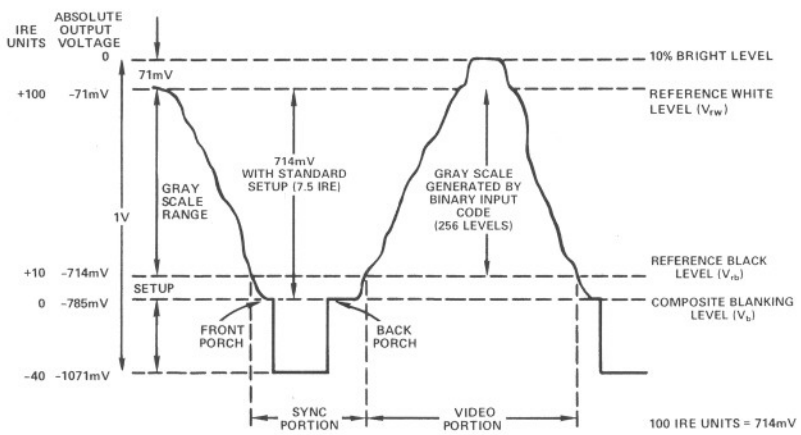
The HDL-3805 D/A Converter is a thick-film hybrid which includes three AD9700 IC D/A converters and three ECL random access memory (RAM) look-up tables in a single package. It is the smallest, lowest-power RGB (red, green, blue) video generator available to video designers of high-resolution raster scan graphics displays.

With eight bits of Gray scale resolution per channel, the user has a total palette of 16.7 million colors. Since each of the three DACs has a 256 × 8 RAM, a total of 256 colors is available on each sweep. The write speed of the RAMS is sufficiently high to rewrite the color map completely during vertical retrace, or update smaller blocks of data during horizontal retrace.

Composite functions in the HDL units include $\overline{\text{Red Sync}}$, $\overline{\text{Green Sync}}$, $\overline{\text{Blue Sync}}$, Composite Blanking, Reference White, and 10% Bright. The ability of the devices to drive 75Ω loads directly with a 1V composite signal combines with these functions to assure the outputs will be compatible with the general requirements of EIA Standards RS-170 and RS-343.

The model HDL-3806 D/A Converter is a variation of the HDL-3805 which includes synchronous composite functions and offers increased flexibility for the designer in a pin-for-pin compatible package.

All models of the HDL-3805 and HDL-3806 are housed in 46-pin metal hybrid packages. Standard versions are rated over an operating temperature range of −25°C to +85°C; for units with this range and military screening, consult factory.



Idealized Composite Output Waveform

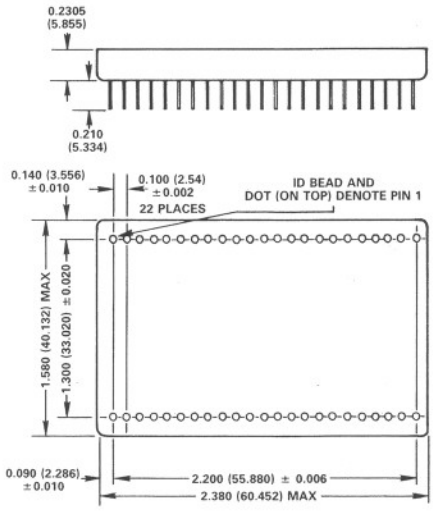
Route 1 Industrial Park; P.O. Box 280; Norwood, Mass. 02062
Tel: 617/329-4700 **TWX: 710/394-6577**
West Coast 714/641-9391 **Mid-West 312/653-5000** **Texas 214/231-5094**

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Parameter	Units	HDL-3805BM	HDL-3806BM	HDL-3806CM
RESOLUTION	Bits	8	*	*
LEAST SIGNIFICANT BIT (LSB) WEIGHT				
Voltage	mV	2.5	*	*
Current	µA	67	*	*
ACCURACY				
(GS = Gray Scale; FS = Full-Scale)				
Linearity	± % GS	0.2	*	*
Differential Linearity	± % GS	0.2	*	*
Integral Linearity	± % GS, max	0.2	*	*
Zero Offset (Initial)	mV, max	1.5	*	*
Monotonicity		Guaranteed		
TEMPERATURE COEFFICIENTS				
Linearity	ppm/°C (max)	30	*	*
Gain	ppm/°C (max)	125	*	*
Zero Offset	ppm/°C (max)	15	*	*
DYNAMIC CHARACTERISTICS – GRAY SCALE OUTPUT[1]				
Settling Time to 0.4% GS; 0V to 637.5mV GS Change				
Voltage	ns (max)	10 (12)	*	*
Output Time Skew				
(Among RGB Outputs)	ns, max	2	*	*
Update Rate	MHz (min)	100 (85)	*	(115)
Slew Rate	V/µs, min	300	*	*
Rise Time	ns (max)	2 (3)	*	*
Glitch Energy	pV-s	80	*	*
Crosstalk				
(Among RGB Outputs)	± % GS	0.2	*	*
Clock Noise on RGB Outputs				
(With 100MHz Filter)	mV	10	*	*
DIGITAL DATA INPUTS				
Logic Compatibility		ECL	*	*
Coding		Complementary Binary (CBT)	*	*
Logic Levels				
"1"	V (min/max)	−0.9 (−1.1/−0.6)	*	*
"0"	V (min/max)	−1.7 (−2.0/−1.5)	*	*
Loading				
Data and Address	µA/pF	650/45	*	*
$\overline{\text{RGB Chip Select}}$	µA/pF	880/18	*	*
$\overline{\text{Write Enable}}$	µA/pF	650/65	*	*
$\overline{\text{RGB Sync}}$, $\overline{\text{Composite Blanking}}$ Reference White, or 10% Bright	µA/pF	290/10	*	*
Strobe	µA/pF	50/5	*	*
SPEED PERFORMANCE – CONTROL INPUTS				
(Standard Setup Control = 7.5 IRE Units = 53.25mV)				
Settling Time to 10% of Final Value for:				
10% Bright	ns, max	10	*	*
$\overline{\text{Reference White}}$	ns, max	10	*	*
$\overline{\text{RGB Sync}}$	ns, max	10	*	*
$\overline{\text{Composite Blanking}}$	ns, max	10	*	*
ANALOG OUTPUTS (Red, Green, and Blue)				
GS Current[2]	mA	0 to −17	*	*
GS Voltage[3]	mV (±1%)	0 to −637.5	*	*
Compliance	V	−1.2 to +0.1	*	*
Internal Impedance	Ω (min/max)	75 (71/79)	*	*
REFERENCE WHITE[4]				
Current				
Logic "1"	mA (±5%)	Normal Operation	*	*
Logic "0"	mA (±5%)	0 or −1.9	*	*
Voltage				
Logic "1"	mV (±5%)	Normal Operation	*	*
Logic "0"	mV (±5%)	0 or −71	*	*
10% BRIGHT[5]				
Current				
Logic "1"	mA (±5%)	−1.9	*	*
Logic "0"	mA (±5%)	0	*	*
Voltage				
Logic "1"	mV (±5%)	−71	*	*
Logic "0"	mV (±5%)	0	*	*

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



PIN DESIGNATIONS

(Bottom View)

PIN	FUNCTION	PIN	FUNCTION
44	$\overline{\text{RED CHIP SELECT}}$	1	$\overline{\text{WRITE ENABLE}}$
45	DIGITAL GROUND	2	ADDRESS A_7 (MSB)
44	$\overline{\text{RED OUT}}$	3	ADDRESS A_6
43	V_{EE} (−5.2V)	4	ADDRESS A_5
42	$\overline{\text{RED OUT}}$	5	ADDRESS A_4
41	$\overline{\text{RED RETURN}}$	6	V_{EE} (−5.2V)
40	$\overline{\text{GREEN CHIP SELECT}}$	7	ADDRESS A_3
39	DIGITAL GROUND	8	ADDRESS A_2
38	$\overline{\text{GREEN OUT}}$	9	ADDRESS A_1
37	V_{EE} (−5.2V)	10	ADDRESS A_0 (LSB)
36	$\overline{\text{GREEN OUT}}$	11	DIGITAL GROUND
35	$\overline{\text{GREEN RETURN}}$	12	DATA IN D_7 (MSB)
34	DIGITAL GROUND	13	DATA IN D_6
33	$\overline{\text{BLUE OUT}}$	14	DATA IN D_5
32	V_{EE} (−5.2V)	15	DATA IN D_4
31	$\overline{\text{BLUE OUT}}$	16	DATA IN D_3
30	$\overline{\text{BLUE RETURN}}$	17	DATA IN D_2
29	$\overline{\text{RED SYNC}}$	18	V_{EE} (−5.2V)
28	$\overline{\text{GREEN SYNC}}$	19	DATA IN D_1
27	$\overline{\text{BLUE SYNC}}$	20	DATA IN D_0 (LSB)
26	10% BRIGHT	21	$\overline{\text{BLUE CHIP SELECT}}$
25	$\overline{\text{REFERENCE WHITE}}$	22	STROBE
24	COMPOSITE BLANKING	23	DIGITAL GROUND

NOTES: GROUNDS ARE NOT CONNECTED INTERNALLY. CONNECT PINS 11, 23, 30, 34, 35, 39, 41, AND 45 TOGETHER AND TO GROUND AS CLOSE TO CASE AS POSSIBLE. −5.2V MUST BE APPLIED TO ALL DESIGNATED PINS.

Parameter	Units	HDL–3805BM	HDL-3806BM	HDL–3806CM
COMPOSITE SYNC[5,6]				
(Applied to RED SYNC, GREEN SYNC, or BLUE SYNC Input Pins)				
Current				
Logic "1"	mA (±4%)	0	*	*
Logic "0"	mA (±4%)	−7.6	*	*
Voltage				
Logic "1"	mV (±4%)	0	*	*
Logic "0"	mV (±4%)	−285	*	*
COMPOSITE BLANKING[5,6]				
(Standard Setup Control = 7.5 IRE Units = 53.25mV)				
Current				
Logic "1"	mA (±4%)	0	*	*
Logic "0"	mA (±4%)	−1.4	*	*
Voltage				
Logic "1"	mV (±4%)	0	*	*
Logic "0"	mV (±4%)	−53.25		
POWER REQUIREMENTS				
−5.2V ±0.25V	mA, max	1450	*	*
Power Dissipation[7]	W, max	7.55	*	*
Power Supply Rejection Ratio	%GS/V	0.025/0.25	*	*
TEMPERATURE RANGE				
Operating (Case)	°C	−25 to +85	*	*
Storage	°C	−55 to +150	*	*
THERMAL RESISTANCE[8]				
Junction to Air, θ_{ja} (Free Air)	°C/W, max	12	*	*
Junction to Case, θ_{jc}	°C/W, max	2.5	*	*
PRICES				
1–4	$	430	463	512

For applications assistance, phone Computer Labs Division at (919) 668-9516

NOTES

[1]Settling to GS percentage includes FS and MSB transitions. Inherent 3ns register delay (3.9% points) is not included.

[2]GS current = FS current − video functions.

[3]LSB value of 2.5mV used for calibration. This causes Gray Scale output to be 637.5mV rather than 643mV shown in idealized composite waveform elsewhere in this data sheet; both values are well within the output and EIA Standard RS-343 tolerances.

[4]Effect on analog output of Logic "0" at Reference White input depends on 10% Bright signal input.

[5]10% Bright, Composite Sync, and Composite Blanking outputs shown add to Gray scale analog output at Pin 31, 36, or 42.

[6]Red Sync, Green Sync, Blue Sync, or Composite Sync control signals reset input registers. Neither the RGB Sync signals nor the Composite Sync should be operated simultaneously with Reference White.

[7]Air flow of 500 LFPM required when operating unit.

[8]Maximum junction temperature = 150°C.

*Specification same as HDL-3805BM.

Specifications subject to change without notice.

Theory of Operation

Refer to the block diagram of the HDL-3805/3806 D/A Converter.

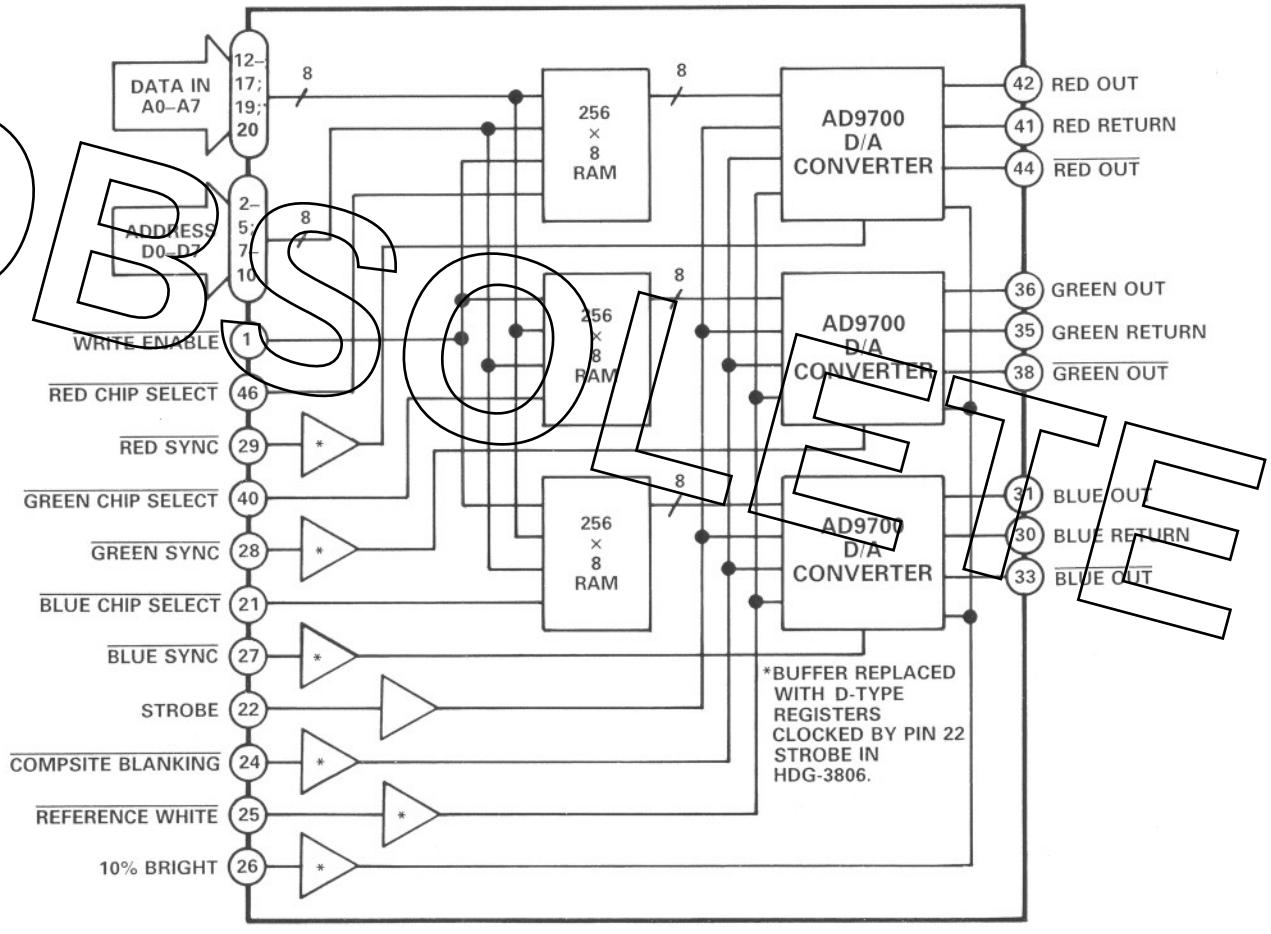
As shown, the unit is comprised of three each random access memories (RAMs) and AD9700 current output D/A converters. These components operate as three pairs in controlling the red, green, and blue (RGB) analog outputs of the device; and greatly simplify the interface between the frame buffers and the monitor in raster scan graphics systems.

RGB digital data information can be loaded into the RAMs during retrace periods. During horizontal retrace intervals, small blocks of data can be entered; the complete color map can be rewritten during the longer vertical retrace times.

Intensities for the RGB outputs are updated by a single 8-bit address word and a Strobe signal during the RAM read operations.

The routing of the digital data to the correct RAM and its associated D/A is controlled by the digital Address input Signals; and by the $\overline{\text{Red Chip Select}}$, $\overline{\text{Green Chip Select}}$, $\overline{\text{Blue Chip Select}}$, and $\overline{\text{Write Enable}}$ signals.

In addition to digital input and address information, the user of the HDl-3805/3806 also has control over composite functions with $\overline{\text{Red Sync}}$, $\overline{\text{Green Sync}}$, $\overline{\text{Blue Sync}}$, $\overline{\text{Composite Blanking}}$, $\overline{\text{Reference White}}$, and 10% Bright.



HLD-3805/3806 Block Diagram

The sequence and timing intervals associated with the write cycle are shown in Figure 1, the HDL-3805/3806 Write Mode illustration.

$\overline{\text{RGB Chip Select}}$ on the top line of Figure 1 illustrates any one of the three $\overline{\text{Chip Select}}$ control signals. For the purposes of discussion, assume it represents $\overline{\text{Red Chip Select}}$.

Note all timing is measured from the 50% points of the various signals. Various signals involved in the write mode may, or may not, occur simultaneously; all, however, must be completed a minimum of two nanoseconds prior to the $\overline{\text{Write Enable}}$ pulse.

Under the assumed conditions, the $\overline{\text{Red Chip Select}}$ (only) changes state to a digital "0" and causes the digital data to be routed, via the Address information, to the RAM associated with the Red analog output. Digital data establishing the intensity of the Red signal are also applied and the $\overline{\text{Write Enable}}$ occurs 2ns later.

The change from digital "1" to digital "0" on the $\overline{\text{Write Enable}}$ input stores the digital input data in memory during the 6ns time of this change. The steps outlined here continue to be repeated until all data for the "red" RAM are loaded; and all data for the RGB inputs are stored in the three RAMS, ready to be read out of memory.

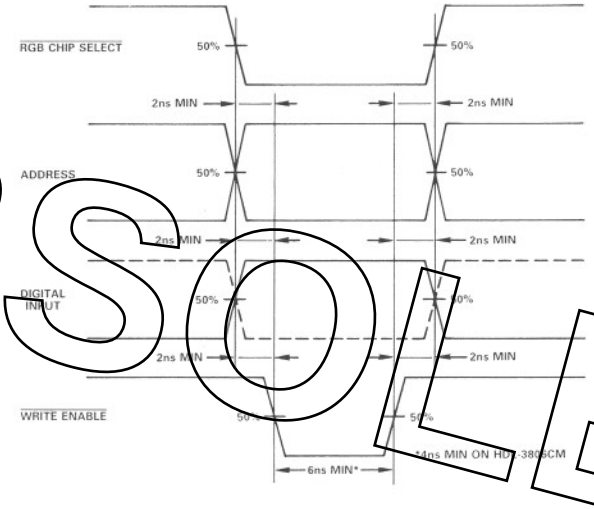


Figure 1. HDL-3805/3806 Write Mode

Figure 2 illustrates the sequence involved in reading out the stored data.

During the read cycle, digital "0" is applied to all three $\overline{\text{Chip Select}}$ inputs, as contrasted to only one of these inputs during the write cycle. Address information applied to the RGB RAMs causes their stored red, green, and blue digital data to be applied to the associated AD9700 D/A converters. The strobe which is then applied simultaneously to all three converters via Pin 22 triggers RGB analog signals out of the unit.

The minimum time between the application of the address and the application of the strobe signal is slightly different among the three models of the converter. As shown, this interval is 12.5ns for the HDL-3805BM and HDL-3806BM; and 8.7ns for the HDL-3806CM. The times are different because of the differences in the required intervals for memory address and register setups.

Reading the RGB data out of memory continues as necessary until all appropriate pixels have been illuminated.

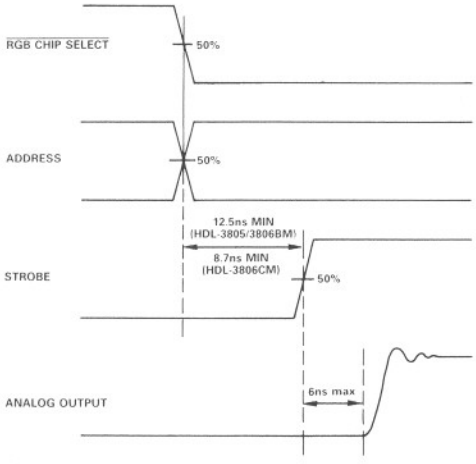


Figure 2. HDL-3805/3806 Read Mode

SYNCHRONOUS VS. ASYNCHRONOUS OPERATION

Asynchronous composite operation is possible with the HDL-3805 because its composite inputs are unlatched; the HDL-3806, on the other hand, offers synchronous operation with latched composite inputs.

There are two situations which require synchronous composite operation for best display quality.

The first of these is for applications in which the raster field is smaller than the visible face of the display tube. If operated asynchronously, any timing mismatch between the pixel clock (strobe input) and the composite blanking control could cause the pixel at the end of each line to be partially illuminated.

The second situation occurs when the 10% bright function is used for overlay on the display. If this overbright signal is used at pixel rates, it must be synchronized with the pixel clock.

Figure 3, the $\overline{\text{Composite Blanking}}$ Timing Diagram, illustrates the timing for both synchronous and asynchronous composite inputs.

When operating synchronously, the $\overline{\text{Composite Blanking}}$ input must return to the digital "1" logic level one pixel clock period before the display line begins. This is necessary because of the delay time of the composite function register. The timing of the change to Logic "1" is important to avoid the possibility of losing the first pixel of the new line.

In Figure 3, some strobe pulses are shown as "first" or "last" strobes to help illustrate synchronous vs. asynchronous operation. The user needs to remember it is the leading edge of the strobe which causes the edge-triggered AD9700 converters to operate.

The D/A inputs shown in Figure 3 are the digital inputs applied to the built-in registers of the internal AD9700 D/A converters. These are asynchronous for the HDL-3805; and synchronous for both models of the HDL-3806.

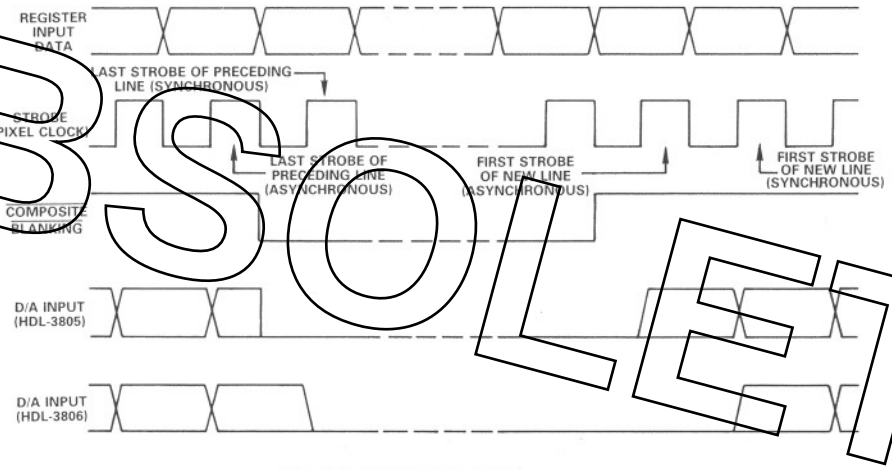


Figure 3. $\overline{\text{Composite Blanking}}$ Timing Diagram

ORDERING INFORMATION

There is one standard model of the HDL-3805 D/A converter, and two model numbers for the HDL-3806 version. Specifically, the designations are HDL-3805BM; and HDL-3806BM and HDL-3806CM. The HDL-3805 unit operates with unlatched asynchronous composite inputs; and both models of the HDL-3806 operate with latched synchronous signals.

In terms of speed, the HDL-3805BM and HDL-3806BM are identical with minimum update rates of 85MHz, and typical word rates of 100MHz. The HDL-3806CM is specified at a minimum update rate of 115MHz.

Standard units operate over a case temperature range of −25°C to +85°C; units with the same temperature range and military screening are also available. For these, consult the factory.

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