

Hybrid Video Digital-to-Analog Converters

PRELIMINARY DATA

FEATURES Triple 8-Bit D/A with LUTs 115MHz Update Rates **RGB Composite Functions** Small Size (2.3" × 1.5") Latched Composite Functions (HDL-3806)

APPLICATIONS

Raster Scan Displays Color Graphics Systems



The HDL-3805 D/A Converter is a thick-film hybrid which includes three AD9700 IC D/A converters and three ECL random access memory (RAM) look-up tables in a single package. It is the smallest, lowest-power RGB (red, green, blue) video generator available to video designers of high-resolution raster scan graphics displays.

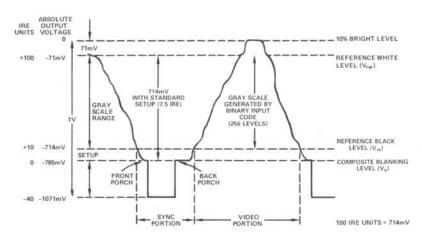
With eight bits of Gray scale resolution per channel, the user has a total palette of 16.7 million colors. Since each of the three DACs has a 256 × 8 RAM, a total of 256 colors is available on each sweep. The write speed of the RAMS is sufficiently high to rewrite the color map completely during vertical retrace, or update smaller blocks of data during horizontal retrace.



osite functions in the HDL units include Red Sync, Green Sync, Blue Sync, Composite Blanking, Reference White, and 0% Bright. The ability of the devices to drive 75Ω loads directly with a 1V composite signal combines with these functions to assure the outputs will be compatible with the general requirement of EIA Standards RS-170 and RS-343.

The model HDL-3806 D/A Converter is a variation of the HDL-3805 which includes synchronous composite functions and offers increased flexibility for the designer in a pin-for-pin compatible package.

All models of the HDL-3805 and HDL-3806 are housed in 46pin metal hybrid packages. Standard versions are rated over an operating temperature range of -25°C to +85°C; for units with this range and military screening, consult factory.



Idealized Composite Output Waveform

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SPECIFICATIONS (typical @ + 25°C with nominal power supplies unless otherwise noted)

Parameter	Units	HDL-3805BM	HDL-3806BM	HDL-3806CM	OUTLINE DIMENSIONS
RESOLUTION	Bits	8	*	*	Dimensions shown in inches and (mm).
LEAST SIGNIFICANT BIT (LSB) WEI					0.2305
Voltage	mV	2.5	*	*	(5.855)
Current	μА	67		*	1
ACCURACY					
(GS = Gray Scale; FS = Full-Scale) Linearity	± % GS	0.2	*	*	<u> </u>
Differential Linearity	± % GS	0.2	*	*	0.210
Integral Linearity	± % GS, max	0.2	*	*	(5.334)
Zero Offset (Initial)	mV, max	1.5	*	*	0.140 (3.556) ± 0.010 0.100 (2.54) ID BEAD AND
Monotonicity		Guaranteed			±0.002 DOT (ON TOP) DENOTE PIN 1
TEMPERATURE COEFFICIENTS					1-000-00-00-00-00-00-00-0
Linearity	ppm/°C (max)	30	*	*	
Gain	ppm/°C (max)	125	*	*	# 0.020 #
Zero Offset	ppm/°C (max)	15	*	*	(2 0) + 0
DYNAMIC CHARACTERISTICS -					(33.020) (33.020)
GRAY SCALE OUTPUT	WOO Ch				
Settling Time to 0.4% GS; 0V to 637.5m Voltage	ns (max)	10(12)	*	*	1.300 (5
Output Time Skew	ns (max)	10(12)			
(Among RGB Outputs)	ns, max	2	*	*	-000-00-00-00-00-00-00-00-00-00-00-00-0
Update Rate	MHz (min)	100 (85)	*	(115)	
Slow Rate	V/As, min	300	*	*	0.090 (2.286) ± 0.010
Rise Time	ns (max)	2(3)	*	*	2.380 (60.452) MAX
Glitch Energy	7 pV-1 / /	_80	*	*	
Crosstalk (Among RGB Output)	₹%GS	0.2	*	*	DENI DEGLOSIA TRONG
Clock Noise on KGB Outputs	1 7,000	0.2	\sim	_	PIN DESIGNATIONS
(With 100MHz Filter)	mt/	10	*)	<i>F</i> 7	(Bottom View)
DIGITAL DATA INPUTS	/ / /	\\\\\\	2200000 - 04.5 (170000)	1-1	
Logic Compatibility	_ (\	ECL /	*	/ * /	PIN FUNCTION PIN FUNCTION
Coding		Complementary	* / / /	*	46 RED SHIP SELECT 1 WRITE ENABLE
5.0 (0.0004) (0.0004)	_	Binary (CBN)	ノ / /	1	45 DIGITAL GROUND 2 ADDRESS A ₇ (MSB)
Logic Levels	***	00/ 11/0		I	44 REDOUT 3 ADDRESS A. 43 V _{EE} (-7.2V) 4 ADDRESS A ₅
"1" "0"	V (min/max)	-0.9(-1.1/-0.6)	* [· /	42 RED OUT 5 ADDRESS A.
Loading	V (min/max)	-1.7(-2.0/-1.5)		\sim 71	41 RED RETURN 6 V _{EE} (-5.2V) 40 GREEN CHIP SELECT 7 ADDRESS A ₃
Data and Address	μA/pF	650/45	*	* — [39 DIGITAL GROUND 8 ADDRESS A ₂
RGB Chip Select	μA/pF	880/18	*	*	38 GREENOUT 9 ADDRESS A ₁ 37 V _{SE} (+5.2V) 10 ADDRESS A ₀ (LSB)
Write Enable	μA/pF	650/65	*	*	36 GREEN OUT 11 DIGITAL GROUND
RGB Sync, Composite Blanking					35 GREEN RETURN 12 DATA IN D ₇ (MSB) 34 DIGITAL GROUND 13 DATA IN D ₆
Reference White, or 10% Bright Strobe	μΑ/pF μΑ/pF	290/10 50/5	*	*	33 BLUEOUT 14 DATAIN D ₅
		30/3		***************************************	32 V _{EE} (-5.2V) 15 DATA IN D ₄ 31 BLUE OUT 16 DATA IN D ₃
SPEED PERFORMANCE - CONTROL (Standard Setup Control = 7.5 IRE Uni					30 BLUERETURN 17 DATAIN D ₂
Settling Time to 10% of Final Value for					29 RED SYNC 18 V _{EE} (-5.2V) 28 GREEN SYNC 19 DATA IN D ₁
10% Bright	ns, max	10	*	*	27 BLUE SYNC 20 DATA IN D ₀ (LSB)
Reference White	ns, max	10	*	*	26 10% BRIGHT 21 BLUE CHIP SELECT 25 REFERENCE WHITE 22 STROBE
RGB Sync	ns, max	10	*	*	24 COMPOSITE BLANKING 23 DIGITAL GROUND
Composite Blanking	ns, max	10	*	*	NOTES: GROUNDS ARE NOT CONNECTED INTERNALLY.
ANALOG OUTPUTS (Red, Green, and E	Blue)				CONNECT PINS 11, 23, 30, 34, 35, 39, 41, AND 45
GS Current ²	mA	0 to -17	*	*	TOGETHER AND TO GROUND AS CLOSE TO CASE AS POSSIBLE. – 5.2V MUST BE APPLIED TO ALL
GS Voltage ³	mV (± 1%)	0 to -637.5	*	*	DESIGNATED PINS.
Compliance Internal Impedance	V O (min/max)	- 1.2 to + 0.1 75 (71/79)	*	*	
	Ω (min/max)	13 (11/19)			
REFERENCE WHITE ⁴ Current					
Logic "1"	mA (±5%)	Normal	*	*	
	(= 3 /0)	Operation			
Logic "0"	mA (± 5%)	0 or -1.9	*	*	
Voltage					
Logic "1"	mV (\pm 5%)	Normal	*	*	
Logic "0"	mV(+50/)	Operation	*		
	mV (± 5%)	0 or -71		P	
10% BRIGHT ⁵					
Current Logic "1"	m A (+ 50/)	-1.9	*	*	
	$mA(\pm 5\%)$			1	
	mA(+5%)				
Logic "0"	$mA (\pm 5\%)$	0	^	•	
	mA (±5%) mV (±5%)	-71	*	*	

Parameter	Units	HDL-3805BM	HDL-3806BM	HDL-3806CM	
COMPOSITE SYNC ^{5,6}					
(Applied to RED SYNC, GREEN SYNC	,				
or BLUE SYNC Input Pins)					
Current	A (. 40/)	0			
Logic "1"	mA (±4%)	0			
Logic "0"	$mA(\pm 4\%)$	-7.6		4	
Voltage	777 . 4075	0	1		
Logic "1"	mV (±4%)	0	1	1	
Logic "0"	mV (±4%)	- 285	*		
COMPOSITE BLANKING ^{5,6}					
(Standard Setup Control = 7.5 IRE Units	s = 53.25 mV				
Current					
Logic "1"	$mA(\pm 4\%)$	0	*	*	
Logic "0"	mA (±4%)	-1.4	*	*	
Voltage					
Logic "1"	$mV(\pm 4\%)$	0	*	*	
Logic "0"	mV (±4%)	-53.25			
POWER REQUIREMENTS					nerine
$-5.2V \pm 0.25V$	mA, max	1450	*	*	
Power Dissipation ⁷	W, max	7.55	*	*	
Power Supply					
Rejection Ratio	%GS/V	0.025/0.25	*	*	
TEMPERATURE RANGE					959
Operating (Case)	×	-25 to + 85	*	*	
Storage (Case)	·d	-55 to +150	*	*	
	7/-				maker .
THERMAL RESISTANCE8	/) -	_		
Junction to Air, 9 _{ja}	°C/W, max		*		
(Free Air)	OC AVI		$\overline{}$	<u></u>	
Junction to Case, θ _{ja}	°C/W, max	4.5			inter a second s
PRICES	/	\mathcal{L}	1 1 /	1	
1-4	\$ \	430	463	512	
For applications assistance, p	hone Computer	Labs Division at (919) 6	668-9516	1 1	
NOTES Settling to GS percentage includes FS and MSB t	manaitiana Inhanan	2no register delay \$00()	points) is not included.	1 1	7 . 1 .
² GS current = FS current – video functions.	ransitions. Inneren	ons register delay (50%)	points) is not included.	L I	
³ LSB value of 2.5mV used for calibration. This ca	uses Gray Scale ou	put to be 637.5mV rather	than 643mV shown in		
idealized composite waveform elsewhere in this da	ata sheet; both valu	es are well within the outp	out and EIA Standard	<u> </u>	
RS-343 tolerances.	NAME OF TAXABLE PARTY.			\sim [
⁴ Effect on analog output of Logic "0" at Reference ⁵ 10% Bright, Composite Sync, and Composite Blan				- 42	<u> </u>
⁶ Red Sync, Green Sync, Blue Sync, or Composite				1 42.	~ / / / / / · / ·
signals nor the Composite Sync should be operate	d simultaneously w				\smile
Air flow of 500 LFPM required when operating u	ınit.				· 1
⁸ Maximum junction temperature = 150°C.					
*Specification same as HDL-3805BM.					
Specifications subject to change without notice.					_

Theory of Operation

Refer to the block diagram of the HDL-3805/3806 D/A Converter.

As shown, the unit is comprised of three each random access memories (RAMs) and AD9700 current output D/A converters. These components operate as three pairs in controlling the red, green, and blue (RGB) analog outputs of the device; and greatly simplify the interface between the frame buffers and the monitor in raster scan graphics systems.

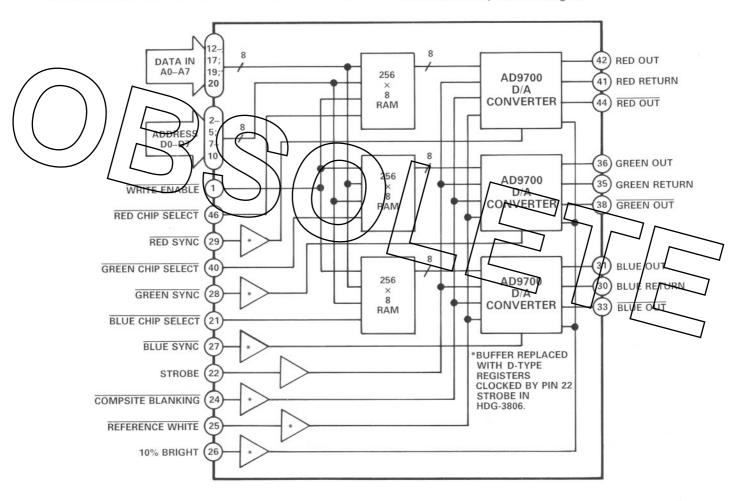
RGB digital data information can be loaded into the RAMs during retrace periods. During horizontal retrace intervals,

small blocks of data can be entered; the complete color map can be rewritten during the longer vertical retrace times.

Intensities for the RGB outputs are updated by a single 8-bit address word and a Strobe signal during the RAM read operations.

The routing of the digital data to the correct RAM and its associated D/A is controlled by the digital Address input Signals; and by the Red Chip Select, Green Chip Select, Blue Chip Select, and Write Enable signals.

In addition to digital input and address information, the user of the HDI-3805/3806 also has control over composite functions with Red Sync, Green Sync, Blue Sync, Composite Blanking, Reference White, and 10% Bright.



HLD-3805/3806 Block Diagram

The sequence and timing intervals associated with the write cycle are shown in Figure 1, the HDL-3805/3806 Write Mode illustration.

RGB Chip Select on the top line of Figure 1 illustrates any one of the three Chip Select control signals. For the purposes of discussion, assume it represents Red Chip Select.

Note all timing is measured from the 50% points of the various signals. Various signals involved in the write mode may, or may not, occur simultaneously; all, however, must be completed a minimum of two nanoseconds prior to the Write Enable pulse.

Under the assumed conditions, the Red Chip Select (only) changes

state to a digital "0" and causes the digital data to be routed, via the Address information, to the RAM associated with the Red analog output. Digital data establishing the intensity of the Red signal are also applied and the Write Enable occurs 2ns later.

The change from digital "1" to digital "0" on the Write Enable input stores the digital input data in memory during the 6ns time of this change. The steps outlined here continue to be repeated until all data for the "red" RAM are loaded; and all data for the RGB inputs are stored in the three RAMS, ready to be read out of memory.

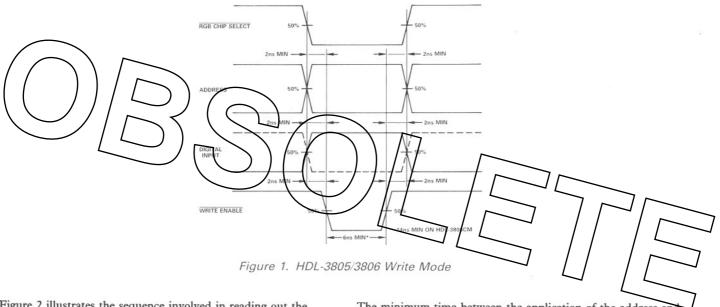


Figure 2 illustrates the sequence involved in reading out the stored data.

During the read cycle, digital "0" is applied to all three Chip Select inputs, as contrasted to only one of these inputs during the write cycle. Address information applied to the RGB RAMs causes their stored red, green, and blue digital data to be applied to the associated AD9700 D/A converters. The strobe which is then applied simultaneously to all three converters via Pin 22 triggers RGB analog signals out of the unit.

The minimum time between the application of the address and the application of the strobe signal is slightly different among the three models of the converter. As shown, this interval is 12.5ns for the HDL-3805BM and HDL-3806BM; and 8.7ns for the HDL-3806CM. The times are different because of the differences in the required intervals for memory address and register setups.

Reading the RGB data out of memory continues as necessary until all appropriate pixels have been illuminated.

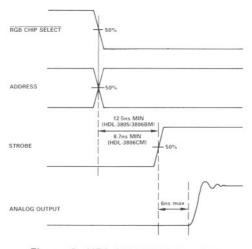


Figure 2. HDL-3805/3806 Read Mode

SYNCHRONOUS VS. ASYNCHRONOUS OPERATION

Asynchronous composite operation is possible with the HDL-3805 because its composite inputs are unlatched; the HDL-3806, on the other hand, offers synchronous operation with latched composite inputs.

There are two situations which require synchronous composite operation for best display quality.

The first of these is for applications in which the raster field is smaller than the visible face of the display tube. If operated asynchronously, any timing mismatch between the pixel clock (strobe input) and the composite blanking control could cause the pixel at the end of each line to be partially illuminated.

The second situation occurs when the 10% bright function is used for overlay on the display. If this overbright signal is used at pixel rates, it must be synchronized with the pixel clock.

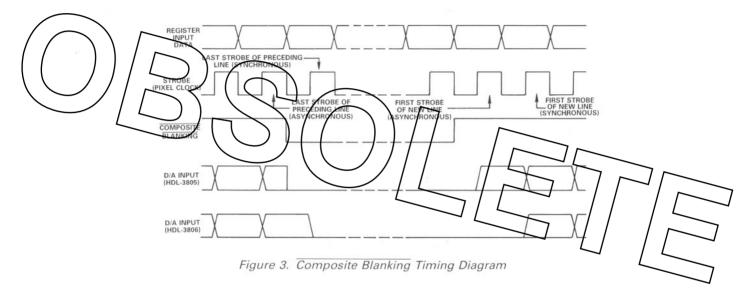
Figure 3, the Composite Blanking Timing Diagram, illustrates

the timing for both synchronous and asynchronous composite inputs.

When operating synchronously, the Composite Blanking input must return to the digital "1" logic level one pixel clock period before the display line begins. This is necessary because of the delay time of the composite function register. The timing of the change to Logic "1" is important to avoid the possibility of losing the first pixel of the new line.

In Figure 3, some strobe pulses are shown as "first" or "last" strobes to help illustrate synchronous vs. asynchronous operation. The user needs to remember it is the leading edge of the strobe which causes the edge-triggered AD9700 converters to operate.

The D/A inputs shown in Figure 3 are the digital inputs applied to the built-in registers of the internal AD9700 D/A converters. These are asynchronous for the HDL-3805; and synchronous for both models of the HDL-3806.



ORDERING INFORMATION

There is one standard model of the HDL-3805 D/A converter, and two model numbers for the HDL-3806 version. Specifically, the designations are HDL-3805BM; and HDL-3806BM and HDL-3806CM. The HDL-3805 unit operates with unlatched asynchronous composite inputs; and both models of the HDL-3806 operate with latched synchronous signals.

In terms of speed, the HDL-3805BM and HDL-3806BM are identical with minimum update rates of 85MHz, and typical word rates of 100MHz. The HDL-3806CM is specified at a minimum update rate of 115MHz.

Standard units operate over a case temperature range of -25° C to $+85^{\circ}$ C; units with the same temperature range and military screening are also available. For these, consult the factory.