HMC-C060

v02.0711

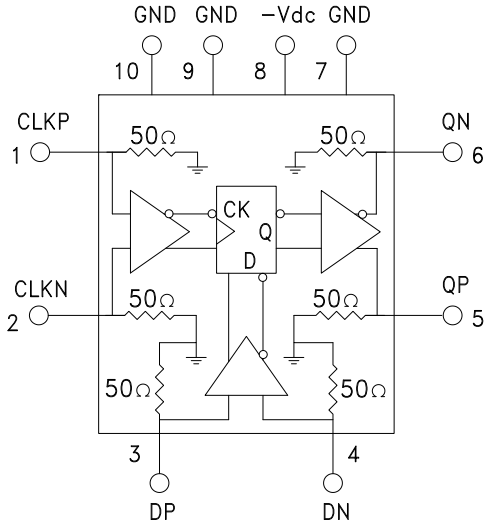
43 Gbps, D-TYPE FLIP-FLOP MODULE

Typical Applications

The HMC-C060 is ideal for:

- OC-768 and SDH STM-256 Equipment
- Serial Data Transmission up to 43 Gbps
- Digital Logic Systems up to 43 Gbps
- Broadband Test and Measurement

Functional Diagram



Features

Supports Data Rates up to 43 Gbps

Inputs Terminated Internally in 50 ohms

Supports Single-Ended or Differential Operation

Low Power Consumption: 580mW

Less than 200 fs Additive RMS Jitter

Fast Rise and Fall Times: <10 ps

Single -3.3 V Power Supply

Hermetically Sealed Module: 1.85mm Connectors

-40°C to +70°C Operating Temperature

General Description

The HMC-C060 is a D-type Flip Flop designed to support data transmission rates of up to 43 Gbps and clock frequencies as high as 43 GHz. During normal operation, data is transferred to the outputs on the positive edge of the clock. Reversing the clock inputs allows for negative-edge triggered applications. All input signals to the HMC-C060 are terminated with 50 Ohms to ground on-chip, and may be either AC or DC coupled. The differential outputs of the HMC-C060 may be either AC or DC coupled. Outputs can be connected directly to a 50 Ohm to ground terminated system, while DC blocking capacitors may be used if the terminating system is 50 Ohms to a non-ground DC voltage. The HMC-C060 operates from a single -3.3V DC supply, and is housed in a hermetically sealed module with 1.85mm connectors.

Electrical Specifications, T_A = +25°C, -Vdc = Vee = -3.3V

Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage	±10% Tolerance	-3.6	-3.3	-3	V
Power Supply Current			175	225	mA
Maximum Data Rate	NRZ Format	43			Gbps
Maximum Clock Rate		43			GHz
Deterministic Jitter [1]			1.5		ps p-p
Additive Random Jitter [2]			0.2		ps rms
Clock Phase Margin	@ 43 Gbps		280		degree
Rise Time, tr	20% - 80%		9		ps
Fall Time, tf	20% - 80%		10		ps
Data Output Swing	Differential Output Swing	420	500		mV p-p

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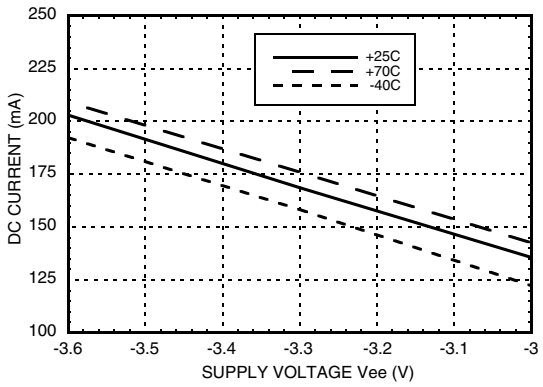
Electrical Specifications, (continued)

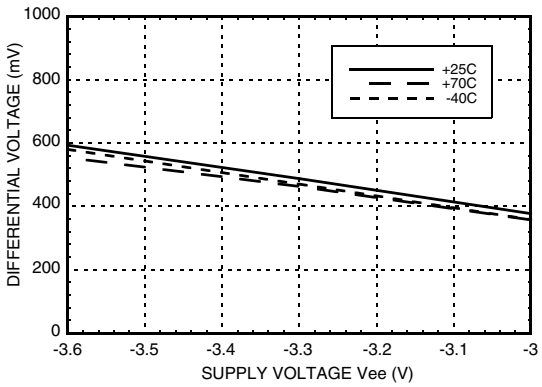
Parameter	Conditions	Min.	Typ.	Max	Units
Input Return Loss	Data input up to 25 GHz		10		dB
	Clock input up to 40 GHz		10		dB
Output Return Loss	Data output up to 25 GHz		10		dB
Propagation Delay, td			200		ps
Input Amplitude (Data & Clock)	Single-Ended Amplitude	100		800	mV p-p
	Differential Amplitude	100		2000	mV p-p
Input High Voltage (Data & Clock)		-0.5		0.5	V
Input Low Voltage (Data & Clock)		-1		0	V
Output High Voltage			-10		mV
Output Low Voltage			-300		mV

[1] Deterministic jitter measured at 43 Gbps with PRBS 2^{13}-1 pattern. It is the peak to peak deviation from the ideal time crossing
[2] Random jitter is measured with 43 Gbps 10101… pattern

DC Current vs. Supply Voltage



Differential Output vs. Supply Voltage



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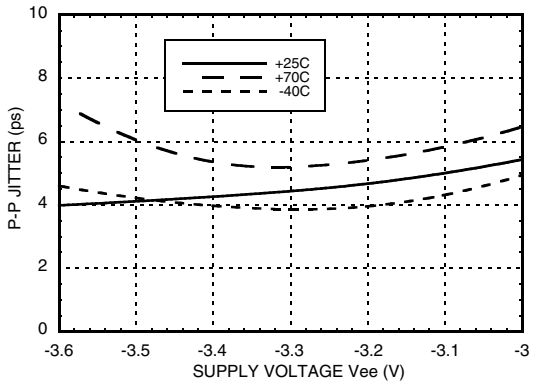
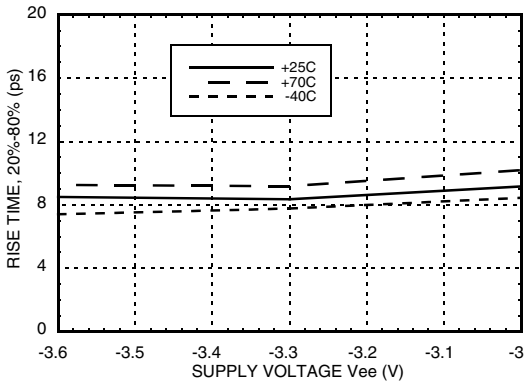
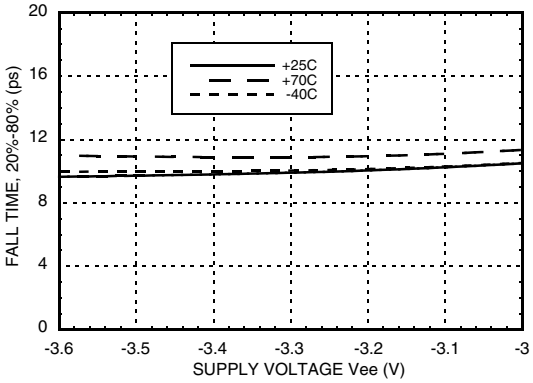
Peak-to-Peak Jitter vs. Supply Voltage [1] [2]



Rise Time vs. Supply Voltage [1]



Fall Time vs. Supply Voltage [1]



[1] Data input = 43Gbps PRBS 2^{23}-1 [2] Source jitter was not deembedded.

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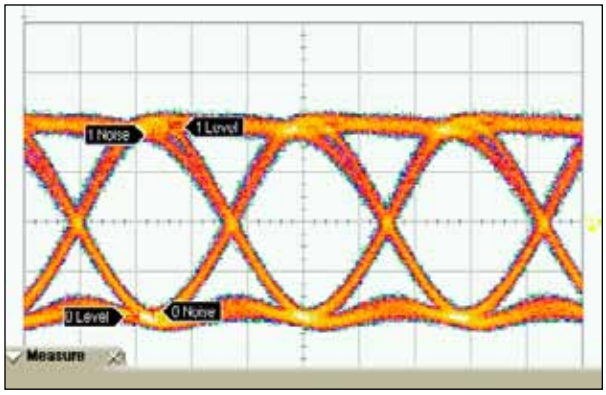
Eye Diagram

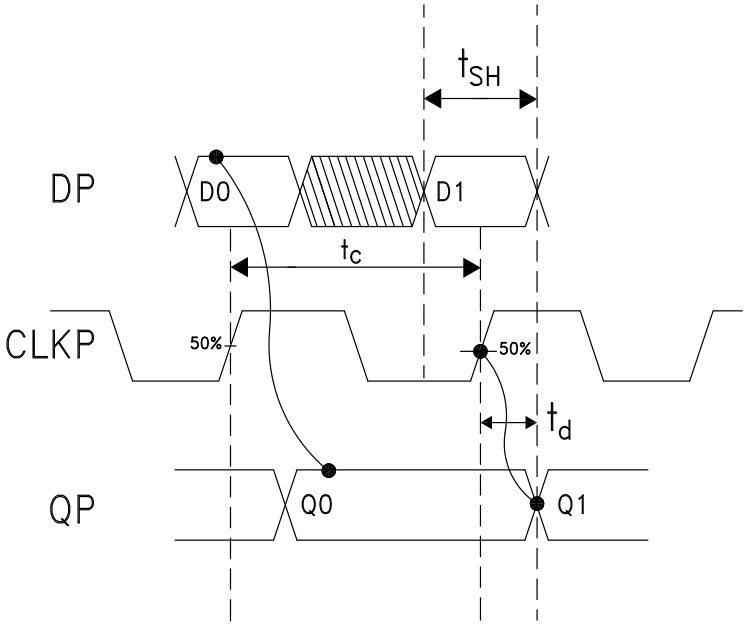


[1] Test Conditions:
Eye diagram data presented on an Infinium DCA 86100A
Rate = 43 GB/s
Pseudo Random Code = 2^{23} -1
Vin = 500 mVpp differential

	Current	Minimum	Maximum	Total Meas
Jitter p-p (f1)	3.600 ps	3.000 ps	3.800 ps	30
Rise Time (f1)	9.60 ps	9.60 ps	9.80 ps	30
Fall Time (f1)	11.40 ps	11.00 ps	11.40 ps	30
Eye S/N (f1)	14.69	14.54	14.68	30

Vertical Scale	132.6 mV / div
Horizontal Scale	9.0 ps / div

Timing Diagram



Truth Table

Input		Outputs
D	CLK	Q
L	L -> H	L
H	L -> H	H
Notes: D = DP - DN CLK = CLKP - CLKN Q = QP - QN	H - Negative voltage level L - Positive voltage level	

$t_c = \frac{1}{f_{clock}}$

t_{SH} = Setup and Hold Time

CPM = Clock Phase Margin = 360° $\frac{t_c - t_{SH}}{t_c}$

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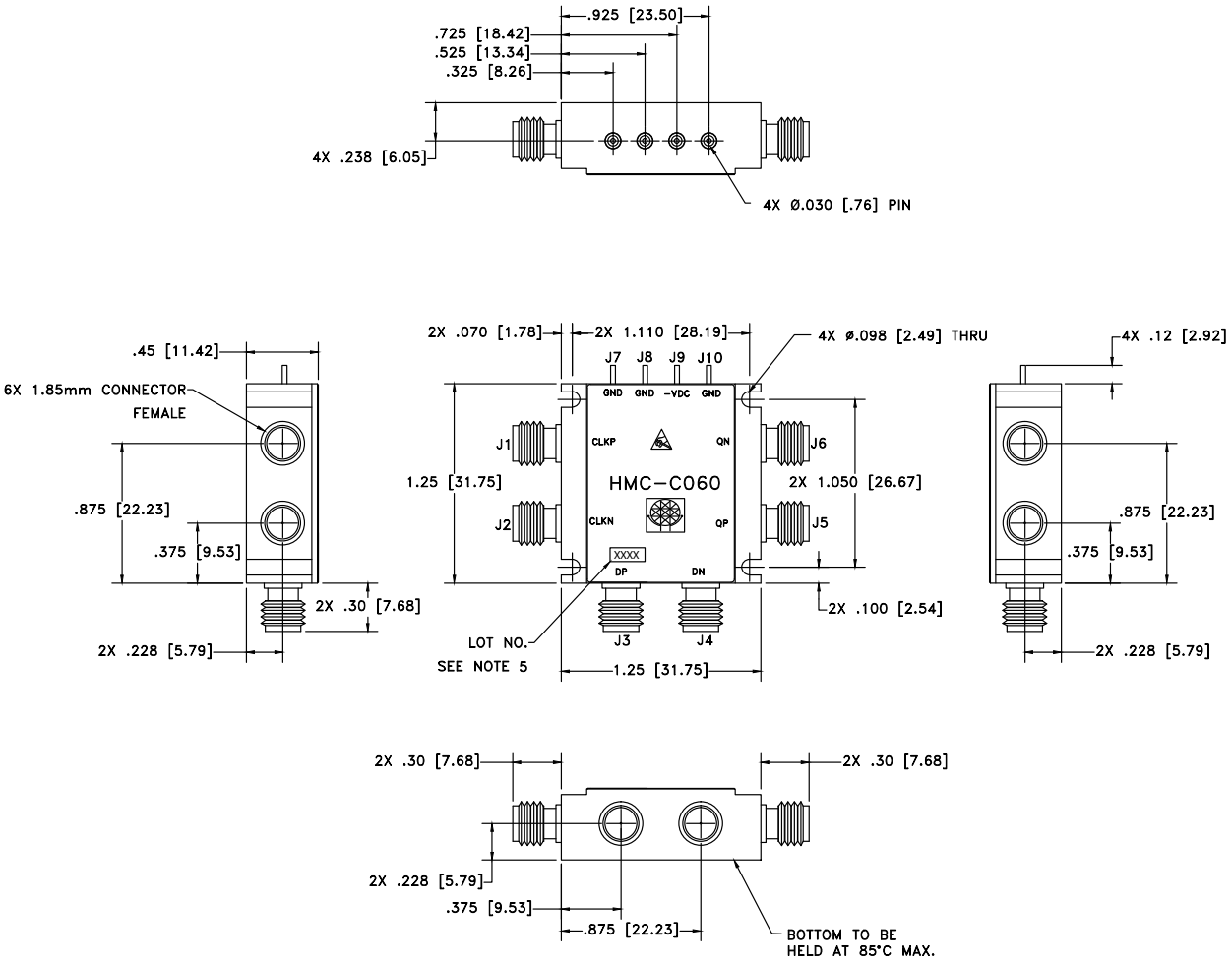
Absolute Maximum Ratings

Power Supply Voltage (Vee)	-3.6 to +0.5V
Input Signals	-1.5V to +0.5V
Output Signals	-1.5V to +0.5V
Junction Temperature	125°C
Storage Temperature	-65°C to +125°C
Operating Temperature	-40°C to 70°C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1 PACKAGE, LEADS, COVER MATERIAL: KOVAR
2 FINISH: GOLD PLATE OVER NICKEL PLATE.
3 ALL DIMENSIONS ARE IN INCHES [MILLIMETERS]
4 TOLERANCES:
  4.1 .XX = ± .02
  4.2 XXX = ±.010
5 MARK LOT NUMBER ON 0.080 X 0.250 LABEL WHERE SHOWN, WITH 0.030" MIN. TEXT HEIGHT.

Package Information

Package Type	C-13
Package Weight [1]	59.5 gms

[1] Includes the connectors

[2] ±1 gms Tolerance

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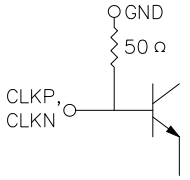
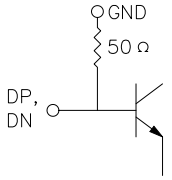
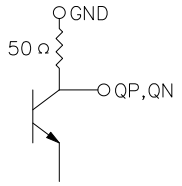
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 2	CLKP, CLKN	Differential clock inputs.	
3, 4	DP, DN	Differential data inputs.	
5, 6	QP, QN	Differential data outputs.	
7, 9, 10	GND	Signal and supply ground.	
8	-Vdc	Negative Supply	

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