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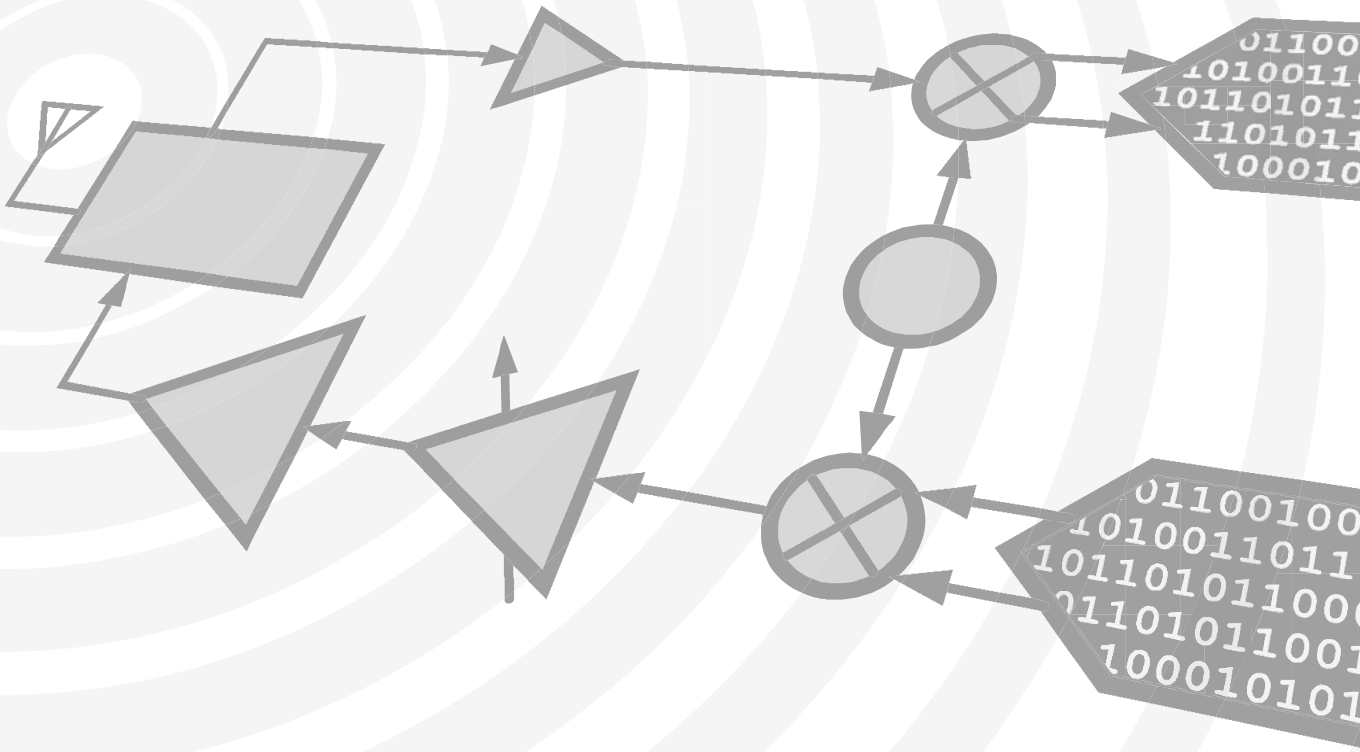

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Frequency Hopping with Hittite PLLVCOs

Application Note

1 Table of Contents

Revision History

Revision	Date	Description
Rev 1.0	August, 2013	First pre-release
Rev 2.0	May 2014	First release

2 Overview

The application note applies to frequency hopping and other time sensitive frequency tuning applications using Hittite's narrowband, triband or wideband PLLVCOs.

Typically applications using Hittite PLLVCOs use the built-in VCO frequency calibration function to lock to a new frequency. However, in many cases there are limitations on the time available to hop to a new frequency or between selected frequencies.

This application note describes the methods to implement fast frequency hopping. Hittite recommends that customers with settling time requirements faster than 1msec contact Hittite Applications Support. Hittite PLLVCOs are capable of very fast settling times, well under 100usec in many cases, however, certain conditions on performance do exist. Our Applications Support team can advise how best to get the required performance.

3 Selecting the target frequency

The Hittite PLLVCOs have one or more VCO cores, depending on the total frequency range covered by the product. Each VCO core has an array of switched capacitors (often 5 capacitors, providing total of 2^5 or 32 possible capacitor settings per VCO core). The VCO auto-calibration routine selects the suitable capacitor setting for optimal VCO performance. This capacitor setting does not change for a given frequency, and is used across the whole operating temperature range.

There are applications that need control over the time it takes to switch frequencies. For these applications, it is recommended to use a manual calibration routine. In manual calibration mode the user generates a look-up table (LUT) that stores the capacitor settings for each frequency of interest. The LUT can be generated at production test, or at bring-up of the system card. Upon frequency changes these settings are written directly to the device registers, thereby eliminating the need to run the auto-calibration routine.

3.1 Applicable Products

This note applies to the following products:

HMC820LP6CE	HMC821LP6CE	HMC822LP6CE	HMC824LP6CE
HMC826LP6CE	HMC828LP6CE	HMC829LP6GE	HMC830LP6GE
HMC831LP6CE	HMC832LP6GE	HMC833LP6GE	HMC834LP6GE
HMC835LP6GE	HMC836LP6CE	HMC837LP6CE	HMC838LP6CE
HMC839LP6CE	HMC840LP6CE	HMC1190LP6GE	HMC1197LP7FE

4 Manual VCO Calibration Options

Prior to use, a device-specific LUT is created in the host controller, which associates all required frequencies to VCO capacitor settings. The manual calibration can be a one-time calibration occurring during the customer's production test, supported by non-volatile memory in the host system. Alternatively, the system can be designed to perform a self-calibration on every power-up, supported by regular static memory in the host system. Both techniques offer reliable operation at all operating temperatures and over time, including aging effects.

When the system needs to change frequency during regular operation, the correct VCO capacitor setting is selected from the LUT. The system then programs the required capacitor value into the VCO and programs the PLL divider registers as required for the frequency change. The frequency hop time using manual calibration is defined by the number of SPI writes, SPI clock speed and the normal PLL settling behavior.

The look-up-table can be created in two ways:

1. Manual calibration with direct LUT, which captures and stores settings for all required frequencies
2. Manual calibration with LUT extrapolation, which captures and stores settings for limited number of frequencies, and uses extrapolation to determine settings between these frequencies

4.1 Manual Calibration with Direct LUT

1. Program the required frequency with Auto-calibration enabled
2. Wait for the Auto-calibration to complete
3. Read the VCO capacitor setting selected by the Auto-calibration for that frequency
4. Record the Frequency and Capacitor setting in the LUT
5. Repeat 1 thru 4 for all required frequencies
6. Once the LUT is completed, disable the VCO Auto-calibration

Use the table to select the appropriate VCO capacitor setting for the desired VCO frequency;

4.2 Manual Calibration with LUT Extrapolation

1. Program the VCO open loop with the internal preset voltage applied to the varactor. This centers the VCO at mid-tuning voltage on each capacitor setting
2. Program the required VCO capacitor setting
3. Record the frequency of the VCO capacitor setting by using the error count feature
4. Repeat steps 1 thru 3 for all possible capacitor settings
5. Calculate the frequency half way between each VCO cap setting measured above, and store the frequency in the LUT as the switching point between VCO capacitor settings

When complete, use the LUT to select the appropriate VCO capacitor setting for any desired VCO frequency, (fvco).

5 Calibration with Direct LUT

Information below describes the calibration method in detail.

5.1 Divider Configuration

In addition, to performing the Manual Calibration, two register setting changes are required for proper operation:

1. Reg08h[8]=1 to “Disable Synchronous VCO Divider Reset”
2. Reg0Bh[18:17]=10 to set “Mcounter (VCO Divider) Clock Gating” for N<1023

5.2 Setting up the LUT table

Apply power to FPGA/microcontroller while keeping PLL+VCO product unpowered. Configure SPI signals going to PLL+VCO product and set all SPI digital signals low. Apply power to PLL+VCO product and cycle either SCK or SEN to configure the correct SPI programming protocol (not required for HMC835, HMC1190 and HMC1197). Then follow the steps outlined in the table below.

Table 1. Calibration with Direct LUT

Step	Action	Comments
1	Initialize	Initialize the device for normal operation with VCO Auto-calibration enabled
2	Program the first frequency via Reg03h and Reg04h	If the frequency requires the use of the VCO Output Divider, the divider must be set prior to programming to ensure correct VCO and VCO capacitor selection
3	Wait until the device has locked to the specified frequency	Poll the LD register to ensure device is locked to selected frequency
4	Read Reg10h & manipulate data for storage in the LUT	For Wideband PLL+VCO & Clock Generation devices (HMC829, HMC830, HMC832, HMC833, HMC834, HMC1032, HMC1033, HMC1034, HMC1035): [Reg10h x 2^8] For Wideband PLL+VCO HMC835 and Wideband PLL+VCO with Integrated Mixer devices HMC1190, HMC1197: [Reg10h[8:1] x 2] + E4A00h For Narrowband, Triband devices (HMC820, HMC821, HMC822, HMC824, HMC826, HMC828, HMC831, HMC836, HMC837, HMC838, HMC839, HMC840); [Reg10h x 2^8] + 5
5	Store the calculated value in the look-up data table with the specific frequency as the address	
6	Repeat steps 2 through 5 for each frequency required	
7	Write Reg0Ah[11] =1	This disables the VCO Auto-calibration

5.3 Programming the LUT frequency during operation

1. Address look-up table with the frequency, output data is the VCO and VCO capacitor setting
2. Program the VCO settings into Reg05h (all devices except HMC835 and HMC119x) or Reg15h (HMC835 and HMC119x)
3. If other VCO states are to be configured, they should be programmed now (for example, VCO Output Divider, output power, muting)
4. Program Reg03h and Reg04h to configure the PLL

6 Calibration with LUT Extrapolation

An alternative approach to a complete frequency LUT is to create a look-up table which specifies the nominal center frequency of each of the VCO and VCO capacitor settings.

When a frequency is to be programmed, the software will execute a search through the look-up table to identify the best VCO capacitor setting which is closest to the desired frequency.

6.1 Divider Configuration

In addition, to performing the Manual Calibration, two register setting changes are required for proper operation:

1. Reg08h[8]=1 to “Disable Synchronous VCO Divider Reset”
2. Reg0Bh[18:17]=10 to set “Mcounter (VCO Divider) Clock Gating” for N<1023

6.2 Setting up the LUT table

Apply power to FPGA/microcontroller while keeping PLL+VCO product unpowered. Configure SPI signals going to PLL+VCO product and set all digital signals low. Apply power to PLL+VCO product and cycle either SCK or SEN to configure the correct SPI programming protocol (not required for HMC835, and HMC119x). Then follow the steps outlined in the table below.

Table 2. Calibration with LUT Extrapolation

Step	Action	Comments
1	Write Reg0Ah = 2047h and Reg02h = 1h	Initialize the device for normal operation with VCO Auto-calibration enabled
2	Write Reg03h = 32h and Reg04h = 0h	Set the VCO divide value to 50

Step	Action	Comments
3	Program the first VCO and VCO sub-band via Reg05h or Reg15h (HMC835 and HMC119x) with VCO Vtune Preset enabled	For Wideband PLL+VCO & Clock Generation devices (HMC829, HMC830, HMC832, HMC833, HMC834, HMC1032, HMC1033, HMC1034, HMC1035): Reg05h = 80h For Wideband PLL+VCO HMC835 and Wideband PLL+VCO with Integrated Mixer devices HMC1190, HMC1197; Reg15h = E4A01h Reg15h[0] = 1 & Reg15h[9] = 1 are required for all calibration measurements. For Narrowband, Triband devices (HMC820, HMC821, HMC822, HMC824, HMC826, HMC828, HMC831, HMC836, HMC837, HMC838, HMC839, HMC840); Reg05h = 85h
	Write Reg05h = 1h	Prevents VCO Auto-calibration from manipulating and changing the VCO and VCO sub-band when Reg04h is programmed. Not required for HMC835, HMC1190, HMC1197.
4	Write Reg04h = 0h	this causes the VCO Auto-calibration to run but it will not change the VCO and VCO sub-band setting so the result in Reg11h will be the frequency error of the selected VCO and VCO sub-band.
5	Read Reg11h[19:0]	Reg11h[19] is the sign bit. This data is used to calculate the measured frequency of the VCO
6	Calculate VCO frequency: [12800 +/- Reg11h]/[256 x Tpd] Hz	This calculation assumes R=1 and Reg0Ah = 2047h. Other settings require different expression. Refer to datasheet or Operating Guide.
7	Store this value in the look-up table for the VCO setting	

Step	Action	Comments
8	Repeat steps 3 through 7 for each VCO setting in sequence	For HMC829, HMC830, HMC832, HMC833, HMC834, HMC1032, HMC1033, HMC1034, HMC1035 Reg05h=080h,180h,280h,380h,480h... (lower 8 bits must always be 80h). 2080h through 3F80, 6080h through 7F80h & A080 through BF80h do not need to be included in the calibration because these are repeated settings are due to the VCO_Reg00h[6] "don't care" bit. For Narrowband, Triband devices HMC820, HMC821, HMC822, HMC824, HMC826, HMC828, HMC831, HMC836, HMC837, HMC838, HMC839, HMC840; Reg05h=85h, 185h, 285h, 385h, 485h to 1F85h (lower 8 bits must always be 85h). Reg15h=E4A01h,E4A03h,E4A05h,E4A07h...E4A3FFh. During the calibration the LSB Reg15h[0] must always be 1 to keep Vtune Preset enabled and Reg15h[9] must always be 1 to prevent Auto-calibration from changing the VCO and VCO sub-band setting. Look-up table needs to mask Reg15h[0]=0 to disable Vtune Preset when in normal operating mode (non-calibration mode) for HMC835 and HMC119x. Note that the devices may have multiple VCO cores so there are overlapping VCO sub-bands when transitioning from one VCO core to the next VCO core. Any calibration VCO and VCO sub-band setting near VCO core transitions that do not provide a monotonic calibration look-up table should be rejected.
10	Repeat with VCO output divider enabled, if required	If the frequency requires the use of the VCO Output Divider, the calibration must be executed a second time with the VCO Output Divider enabled (this can be done on one divider setting only. It does not need to be implemented for every divider setting)
11	Reg0Ah[11] =1	Disable VCO Auto-calibration

6.3 Programming the LUT frequency during operation

1. Scan through the look-up table to locate the closest VCO and VCO sub-band setting
2. Program this value into Reg05h for all devices except HMC835, HMC1190, HMC1197. Reg15h for HMC835, HMC1190, HMC1197.
3. If other VCO states are to be configured, they should be programmed now (for example, VCO Output Divider, output power, muting)
4. Program Reg03h/Reg04h to configure the PLL

7 Frequently Asked Questions

Q1. How often does the Manual VCO Calibration need to be run?

Once. This must be done at the customer's production test time. The system should be at a stable temperature when the calibration is executed.

Alternatively, the calibration could be implemented every time the system is powered-up because all necessary calibration hardware resides inside the PLL+VCO device.

Q2. Will the calibration hold over temperature?

Yes.

Q3. Will the calibration be accurate as aging takes effect over long time periods?

Yes.

Q4. What about frequency over-lap on devices with multiple VCO cores?

If populating the look-up table for the large number of frequency case on PLL+VCO products with multiple VCO cores, it is necessary to eliminate some VCO settings otherwise the resulting look-up table will exhibit non-monotonic behavior.

This is normal because frequency 'over-lap' has been designed into multi-VCO core sub-systems.