ANALOG DEVICES

Reliability Report

Report Title: **GaAs PHEMT-L Process Cumulative Reliability**

Report Number: **2013-00266**

Revision: **4**

Date: **27 September 2018**

Summary

This report summarizes the process qualification testing of the GaAs PHEMT-L process.

Table 1: Process Characteristics

Fabrication Details

Wafer Fabrication Process	PHEMT L
Passivation Layer	SiN
Bond Pad Metal Composition	Au

Description / Results of Tests Performed

The following tables provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Table 1. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

Table 2: Process Qualification Test Results

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
High Temperature Operating Life (HTOL)	JESD22-A108	$T_{j\text{-stress}}$=175°C, Biased, 1,000 Hrs	HMC1040	QTR2012-00327	81	0
			HMC1065	QTR2013-00194	78	0
		$T_{j\text{-stress}}$=150°C, Biased, 1,000 Hrs[1]	HMC6782	Q12586	41	0
High Temperature Storage Life (HTSL)	JESD22-A103	150°C, 1,000 Hours	HMC1040	QTR2012-00327	77	0
			HMC1065	QTR2013-00194	77	0
Low Temperature Storage Life (HTSL)	JESD22-A119	-55°C, 1,000 Hours	HMC1049	Q13960.LS1	77	0
			HMC1049	Q13960.LS1	77	0
			HMC1049	Q13960.LS1	77	0

[1] These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on Analog Devices' web site.

Approvals

Reliability Engineer: Tom Wood

Additional Information

Data sheets and other additional information are available on Analog Devices' web site

Appendix

GaAs PHEMT-L Failure Rate Estimate

The failure rate estimation was determined using the process HTOL test results and the parameters shown below:

- Die Use Junction Temperature, $T_{j\text{-use}}$ = 85°C
- GaAs PHEMT-L Activation Energy = 1.16 eV

- Acceleration Factor (AF):

$$AF = \exp\left[\left(\frac{E_A}{k}\right) \cdot \left(\left(\frac{1}{T_{USE}}\right) - \left(\frac{1}{T_{STRESS}}\right)\right)\right]$$

- Equivalent hours = Device hours x Acceleration Factor

Device	Qual Number	Equivalent Device Hours
HMC1040	QTR2012-00327	1.57×10^8
HMC1065	QTR2013-00194	1.51×10^8
HMC6782	Q12586	1.34×10^7
Total Equivalent Device Hours =		3.21×10^8

The failure rate was calculated using Chi Square Statistic:

Since there were no failures and the tests were time terminated, F=0, and R = 2F+2 = 2

$$\lambda_{CL} = \frac{\chi^2{}_{(\%CL, 2\mathcal{F}+2)} \cdot 10^9}{2 \cdot (Equiv.\ Device\ Hours)}$$ at 60% and 90% Confidence Level (CL) and a die use junction temp, $T_{j\text{-use}}$=85°C;

Failure Rate:

λ_{60} = [$(\chi^2)_{60,2}$]/(2X 3.21x10^8)] = 1.8/ 6.43x10^8 = 2.85x10^{-9} failures/hour or 2.8 FIT or MTTF = 3.51x10^8 Hours

λ_{90} = [$(\chi^2)_{90,2}$]/(2X 3.21x10^8)] = 4.6/ 6.43x10^8 = 7.17x10^{-9} failures/hour or 7.2 FIT or MTTF = 1.39x10^8 Hours