PCB DESIGN CHECKLIST

PROJECT ID 2012618

Engineer:	HIEU NGUYEN	Part Number:	600-00419-00-
PCB Designer:	VINH LY	Revision:	2
MECH Designer:	N/A	Board Name:	EVAL, 75 OHM
Checker:	M. LYONS	Review Date:	5/9/12

Designer	Checker		
		Layout Verification	
☑	☒	Spacing and Connectivity	NO ERRORS FOUND
☑	☒	Impedance Control Rules	75 OHMS 28/20
☑	☒	Power Planes	(PWR current capacities/GND plane around strip-line VAIS)
☑	☒	VIA types	(Blind/Back-drilled/FILLED/HOT VIAS/ Mask for MTG vias)
☑	☒	GND VIAS	(IC centers/SMA pattern/RF Shielding/cover wall centers/antennas)
☑	☒	IC center GND slugs	(VIAS placed/Solder-mask/Paste-mask copper)
☐ N/A	☐	Printed Components	(Layer 20/Solder-mask/Keep-out/VIAS inside & outside keep-out)
☐ N/A	☐	Unused pads	(If removing-preserve via pads on start/end layers)
☑	☒	Soldermask	(10mil solder dam/no silkscreen in solder-able area)
☑	☒	Silkscreen review	(Polarities/board #/HMC logo/Connector labels/Omitted Ref Des)
☐ N/A	☐	Fiducials	(Omit Ref Des from silkscreen/add to stencil for Assy. house)
☐	☐		
		Mechanical	
☐ N/A	☐	Cover Wall	(Thickness/keep-out/solder-mask size)
☐ N/A	☐	Cover & Mounting holes	(Sizes and locations)
☐ N/A	☐	Critical comp. locations	(Connectors/Substrates/Dimensions/Bottom layer clearances)
☑	☒	Keep-out areas	(Verify keep-outs per components, VIAS, GND pour, etc)
☑	☒	Solder-mask openings	(screws-washers/Cover wall oversize/Bottom around connectors)
☐ N/A	☐	**DXF BACKCHECK WITH MECHANICAL DESIGNER!**	
☐	☐		
		Fabrication	
☑	☒	Specify IPC standard	600 & 6012 CLASS 2
☑	☒	PCB Dimensions	(overall/cutouts/radius/angles/Edge plating/coupons)
☑	☒	Layer stack-up detail	(VIA cross-section/Layers/Thickness as Critical Dimension)
☐ N/A	☒	Material, copper weight	(Stack-up to match notes)
☑	☒	Finish plating requirements	(Multi-finish/Wire-bonding/OSP)
☐ N/A	☒	Special requirements	(Impedance-line widths/Blind or Back-drilled VIAS/Edge plate)
☑	☐	VIA fill requirements	(Shown in cross-section detail and/or in notes)
☑	☒ 7.5	Verify Minimum annular ring	(VIAS and thru holes)
☑	☒	Hole Chart	(Match drill files/Partials/Merge drill sizes/Tolerances)
☐	☐		
		Gerber, Drill Data	
☑	☒	Artwork, output files	(Appropriate labels & RS-274X output format)
☐ N/A	☐	Printed Components	(Proper size shapes and gaps/Metal-01 layer 20)
☑	☒	Soldermask	(Oversize 8 mils/If POSITIVE Image-it must be clearly labeled)
☑	☒	Stencil/Paste-mask	(Undersize 2 mils/omit printed components/)
☑	☒	NCDrill data for Thru & Partial VIAS	(3 files for each: .rep, .drl, .lst)
☑	☒	GC-Prevue file review	(Engineer check/Design Review)
☑	☒	ZIP file	(Readme.txt/Output files /FAB PDF/ IPC Netlist/aperture.rep/ ASCII file V5.0/Component X-Y list/GC-Prevue)
☐	☐		
		Assembly (as applicable)	
☑	☒	Ref Des readable/ NOTES/Detail views/Electrostatic note & symbols/DEPOP components	
☐	☐		
☐	☐	Design Review	

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