



# Analog Devices Welcomes Hittite Microwave Corporation

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Report Title: Report Type: Date:

**Qualification Test Report** 

See Attached

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# QUALIFICATION TEST REPORTWafer Process: pHEMT-JQTR: 2012-00042

HMC6484 HMC284A



**Rev: 02** 

#### Hittite Microwave Corporation is committed to:

- Supplying products of the highest quality
- Advance in state-of-the-art technology that supports our products
- · Enhance our competitive position with superior product standards



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#### Hittite's employees recognize the responsibility to:

- Take the initiative to ensure product quality
- Create an environment where the highest standards are maintained
- Continue to improve quality practices

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#### Introduction

This Reliability test is designed to satisfy the reliability requirements designated by Hittite Microwave Corporation. The testing is devised to simulate exposure to environments the product may experience during assembly, test, and life in the end user application. The pass/fail criteria are dependent upon DC and critical RF parameters determined by the appropriate catalog specifications.

The IC Process Reliability Plan for the pHEMT-J process is as follows:

#### **IC Process Reliability**



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**Sample Selection:** All devices used were from finished goods and met acceptance test requirements. 160 parts were obtained from stock and divided to perform the following test.

#### **IC Process Reliability**

<u>High Temperature Operating Life (HTOL)</u> - Devices are subjected to 1000 hours of accelerated operating life test at Tj=125°C with a DC bias applied. The supply current ( $I_{dd}$ ) is periodically monitored. A significant decrease or increase in current indicates a potential device failure. This test is in accordance with JESD22-A108.

High Temperature Storage Life (HTSL) - Devices are subjected to 1000 hours at 150°C per JESD22-A103.

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#### **Summary of Results/Conclusions**

All testing is complete. There were no failures detected. The device meets the requirements for Hittite Reliability Testing.

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial electrical Test	160	160	Pass	
HTSL	80	80	Pass	
Post HTSL - Final Electrical Test	80	80	Pass	
HTOL	80	80	Pass	
Post HTOL - Final Electrical test	80	80	Pass	

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## QUALIFICATION TEST REPORT Wafer Process: pHEMT-J QTR: 2012-00042 Rev: 02

### FIT / MTTF Calculation

Stress conditions:

Qty of Parts Tested = 80 Qty of parts out of spec = 0 Stress Die Junction Temp = 125°C Max Use Die Junction Temp = 85°C Activation Energy = 1.6eV

$$AF = \exp\left[\left(\frac{E_A}{k}\right) \cdot \left(\left(\frac{1}{T_{USE}}\right) - \left(\frac{1}{T_{STRESS}}\right)\right)\right], \text{ AF=185.5}$$

Acceleration Factor (AF):

Calculating the Upper Confidence Bound Failure Rate at 90% CL:

$$\lambda_{CL} = \frac{\chi^2_{\% CL, 2f+2} \cdot 10^9}{2 \cdot t \cdot ss \cdot AF}, \text{ at 90\% CL and with 0 units out of spec,}$$

 $\lambda_{90\%} = -$ 

155 FIT, or  $6.4 \times 10^6$  hours or 735 years.

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