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Floating The HMC307QS16G For Positive Bias Operation

General Description

The HMC307QS16G is a broadband 5-bit GaAs IC digital attenuator mounted in a 16 lead QSOP surface mountable plastic package. This attenuator covers a frequency range from DC to 4 GHz with a typical insertion loss of less than 2 dB. It also achieves excellent attenuation accuracy with a typical ± 0.5 dB at an IIP3 of up to 44 dBm. The attenuator provides 32 (2^5) states of attenuation from 1 dB (LSB) to 16 dB (MSB) for a total attenuation of 31 dB. Five bit control voltage input, toggled between 0 and -5V, is used to select each attenuation state at less than 50 uA current consumption each. A single Vee bias of -5V allows operation down to DC. However, implementation of a “Floating Ground” on the PCB allows for positive bias operation. This product note will discuss implementation of this modification.

Application Problem

In a typical base station (BTS) receiver, shown in Figure 1, both high and low frequency digital attenuators (DATT) are used. RF digital attenuators typically cover from 700 MHz to 2.2 GHz while the IF frequency digital attenuators

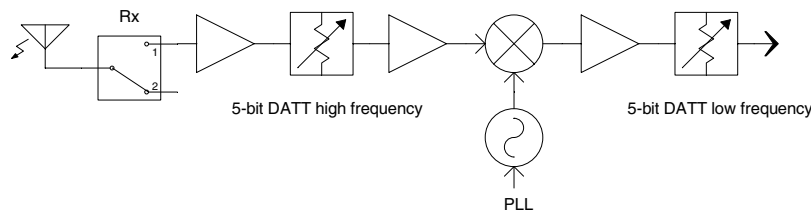


Figure 1. BTS receiver diagram

typically cover from 50 MHz to 700 MHz and operate with a negative bias. Since most positive bias RF digital attenuators have a lower frequency limit greater than 700 MHz, they cannot be used at these IF frequencies. This can be seen in Figure 2, which shows the normalized attenuation levels for a 5-bit positive biased digital attenuator, the HMC273MS10G, which operates from 0.7 to 3.7 GHz.

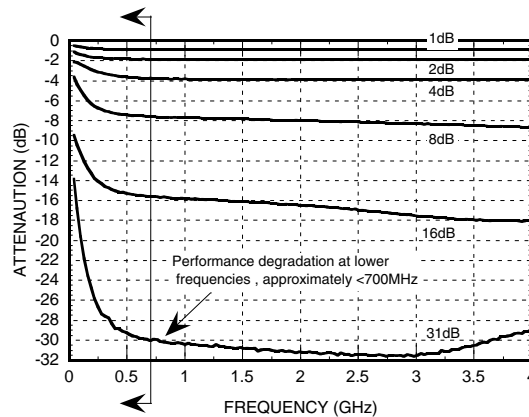


Figure 2. HMC273MS10G normalized attenuation

Application Solution

A typical digital attenuator is comprised of multiple FET’s in either series or shunt configuration. These FET’s are subsequently used to switch in/out various resistive networks, which provide the required attenuation. Because the FET’s are N-channel, a 0 volt potential on the gate is required to turn the FET “on” and -5V to turn the FET “off”. It is the potential difference between the gate and drain-source channel, which turn the FET “on” and “off”. By isolating the ground, or “floating” it, it is possible to create the same potential difference using a positive

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voltage. A positive bias attenuator employs this technique by placing on-chip capacitors between the shunt FET's and ground. The ideal reactance of a capacitor is determined by the equation:

$$X_c := 1/j\omega C$$

$$\omega = 2\pi f$$

From the equation, it can be seen that as the reactance increases the frequency decreases. This increased reactance at lower frequencies is what affects the performance of the attenuator. The solution to this problem would be to use a larger capacitor or a combination of capacitors to minimize this reactance at the lower frequencies. However, this would be difficult if not impossible, on-chip, due to physical constraints.

A negative bias attenuator has no on-chip capacitors between ground and the shunt FET's to restrict low frequency performance. By using the same technique of floating the ground off chip, a negative bias attenuator can be made into a positive bias attenuator. Furthermore, since the capacitance is off chip it will be possible to make adjustments to achieve the desired frequency response.

Since GaAs FET's require the gate voltage to be negative with respect to the drain-source to pinch-off the FET, DC ground must be isolated from RF ground. This is accomplished with the use of external capacitors and by applying +5V to the drain-source terminals through a resistor (R1), as shown in Figure 3. The increasing reactance of the capacitors (C3, C4) at low frequency will determine the lowest frequency of operation while the parasitic components of these capacitors determine the resonant frequency and therefore the upper frequency

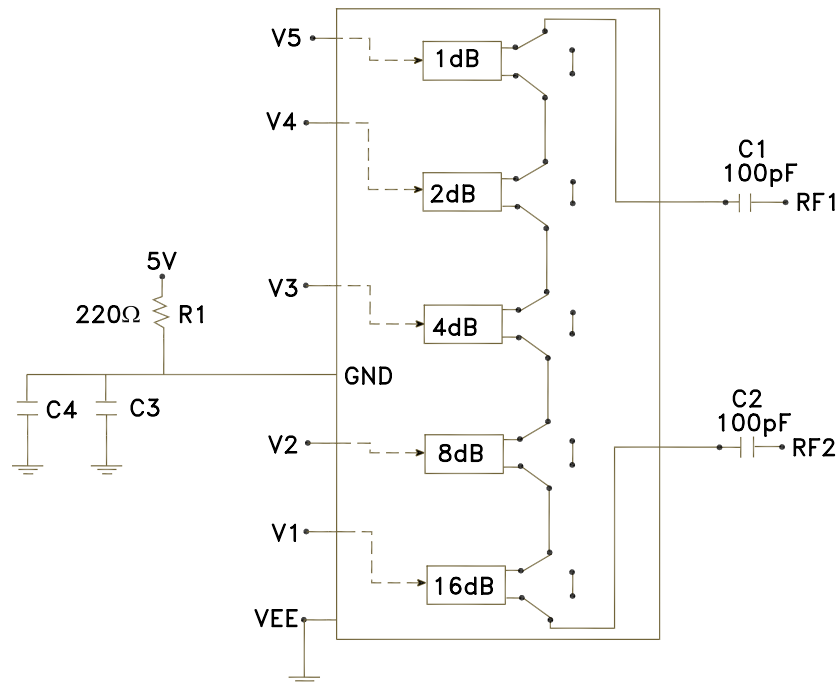


Figure 3. Positive bias application circuit

limit of operation (Beyond resonance a capacitor becomes inductive). In order to provide a symmetric path to ground for the digital attenuator, two capacitors will be used to float the ground plane.

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For this application the HMC307QS16G, a negative bias (-5V), 5-bit digital attenuator, which operates from DC to 4 GHz, is used. Figure 4 shows the application circuit for the HMC307QS16G operated with negative bias. C1 and

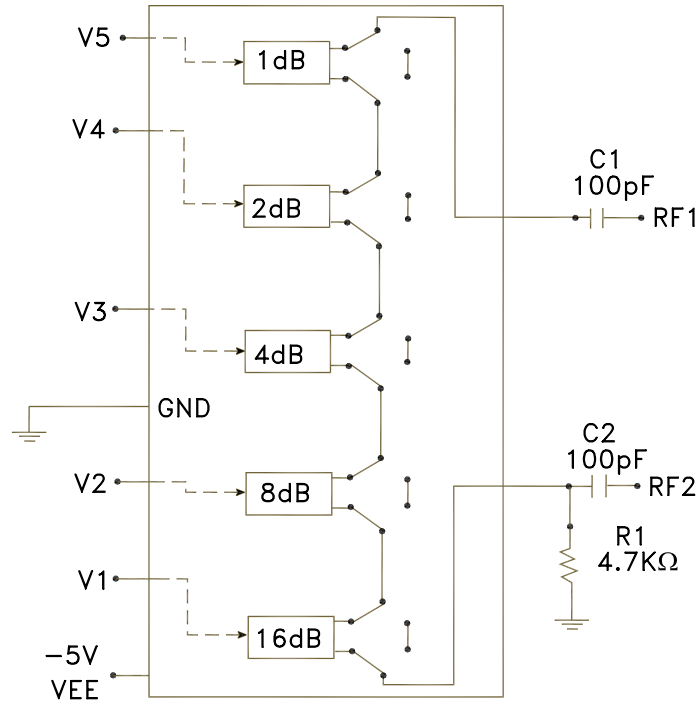


Figure 4. Negative bias application circuit

C2 represent DC-blocking capacitors and R1 functions as a pull-down resistor. Figure 5 shows the normalized attenuation of the HMC307QS16G operated with negative bias. Notice the improved performance at the lower frequencies. Again, this improvement is due to the absence of the shunt capacitance to ground. The remainder of this product note will discuss implementation of a positive bias by floating the ground plane using off chip shunt capacitors.

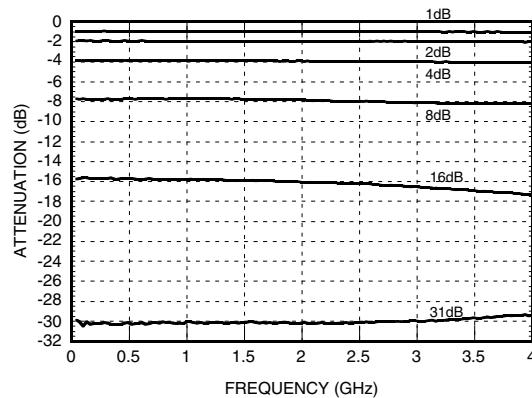


Figure 5. HMC307QS16G normalized attenuation

External Circuit Design

Figure 6 shows the HMC307 with positive bias/floating ground network implemented on the PCB. The board material is Rogers 4350 at a thickness of 10 mil. Coplanar lines are utilized to minimize radiation from the RF traces. Via holes are used to connect the top metal to the RF ground plane. To provide stiffness additional board material is used under the Rogers material. The attenuator is located on a pad, which is isolated from ground (no vias). To provide DC isolation to ground and an RF ground to the pad, the pad is floated to ground using capacitors C3 and C4. Bias is applied to the ground pad from the Vdd pin through R1. If 0V and 5V are to be used to control the attenuator then 5V should be applied to pin Vdd. This will provide a negative potential when 0V is applied to the control pin, hence turning off the related FET. 5V establishes zero potential, thus turning the FET on. The board uses six 220 Ω resistors to isolate the control lines and Vdd. It is not recommended to utilize Vdd as an RF ground since this will provide a sneak path for noise.

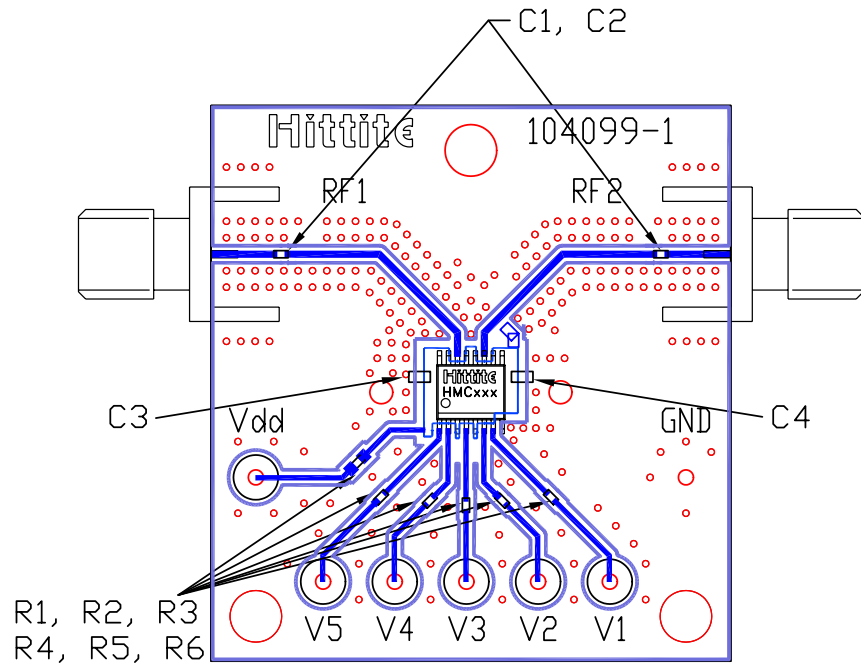


Figure 6. Positive bias evaluation board

For low frequency performance, the capacitors to ground should present a low reactance to ground at the low end of the frequency spectrum. For this example, the frequency of operation is limited from 50 MHz to 350 MHz. Therefore the lowest frequency of operation, 50 MHz, will determine the capacitance value. By the formula, $X = 1/(\omega c)$, the impedance of 0.027 μF capacitor at 50 MHz is approximately 0.12 Ω which is suitable for this example. Figures 7 and 8 shows a comparison of measured performances between two 0.027 μF and two 0.5 pF capacitors.

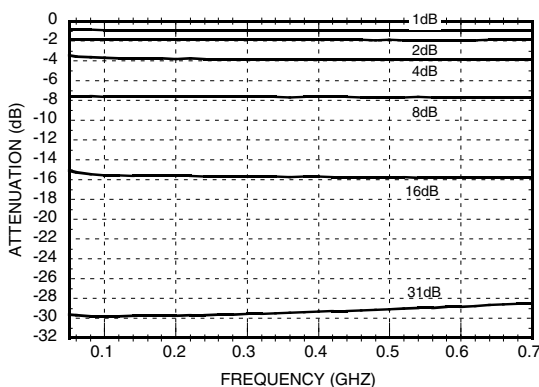


Figure 7. Measured normalized attenuation with two 0.027 μF capacitors

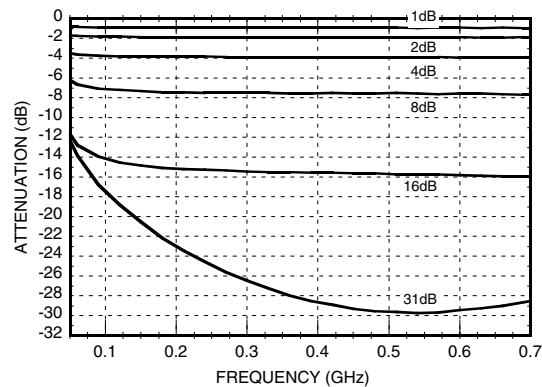


Figure 8. Measured normalized attenuation with two 0.5 pF capacitors

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The measured results clearly show optimum performance at low frequencies when the 0.027 μF capacitors are implemented.

In a perfect world, the reactance of a capacitor would be purely capacitive from DC to infinity. Unfortunately, in the real world, this is not the case. To provide insight, a model with the associated board and capacitor parasitics is created for the “floating ground” board. The model is shown in Figure 9¹.

A two-port network containing S-parameters data for HMC307QS16G is used with its reference node terminated with the board and capacitor parasitics. The S-parameters are obtained from Hittite’s web site, www.hittite.com. Inductor L1 represents the parasitic inductance from the package to the shunt capacitors C2 and C3. Inductor L4 is the inductance from the via to ground. C1 is the capacitance of the floating ground plane, which is calculated using the parallel plate equation for capacitance, $C = \epsilon A/d$,

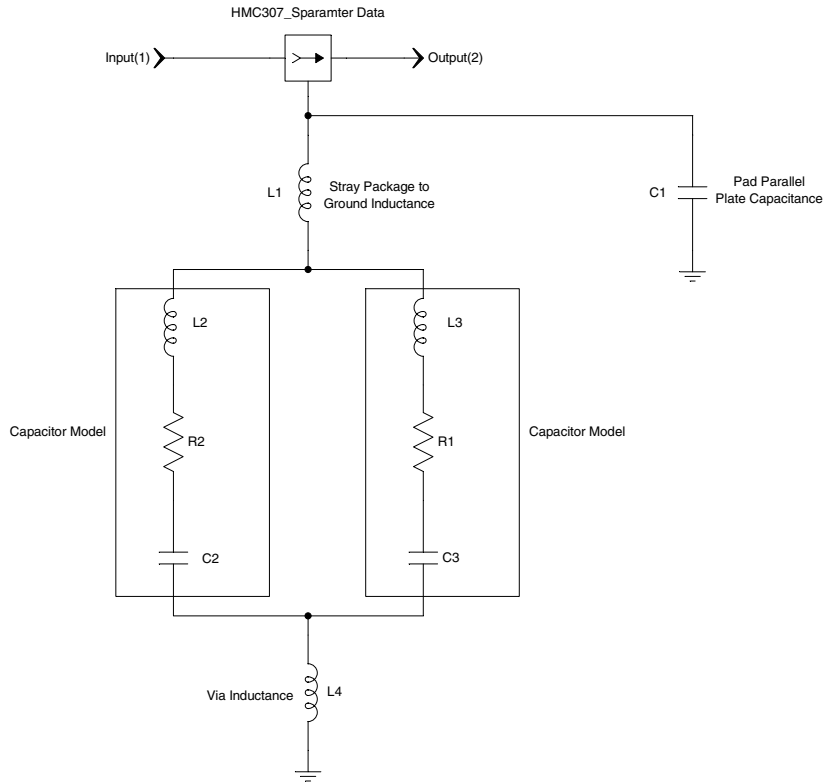


Figure 9. HMC307QS16G floated ground model

where $\epsilon = (\epsilon_0)(\epsilon_r)$, $\epsilon_r = 3.48$, $\epsilon_0 = 8.851 \times 10^{-12}$ F/M, $A = 0.046$ in² and $d = 0.010$ in. The physical capacitor consists of a series inductance (L2, L3), resistance (R1, R2), and capacitance (C2, C3). The values of the series resistor and inductor are available from vendor specifications.

The simulated results are compared to the measured results in Figure 10¹. As shown in Figure 10, the simulated data is in close agreement with the measured data. In fact, more than 29.7 dB of maximum attenuation is achieved, which is approximately the same attenuation obtained with negative bias operation. Moreover, attenuation flatness is good across the frequency range up to 0.7 GHz, which exceeds the initial target for the upper frequency limit. The above model, or similar model, can be used to predict performance over various frequency bands or capacitor values.

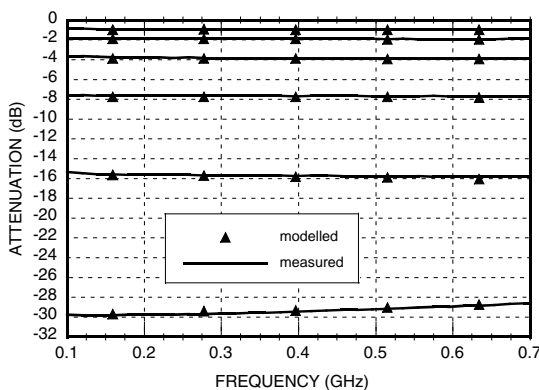


Figure 10. Modeled and measured normalized attenuation with two 0.027 μF capacitors

Limitations and Trade-offs

High frequency operation is limited by the self-resonance value of the capacitors used. Above the resonance frequency, the inductive reactance will dominate limiting operation of the attenuator. This effect is shown in Figure 11.

Covering a wider band will require more capacitors of different or same values, and subsequently higher resonant frequencies. Figure 12 shows measured results using five 0.010 μF capacitors. The operating band is substantially increased due to the higher overall capacitance but more importantly lower inductance.

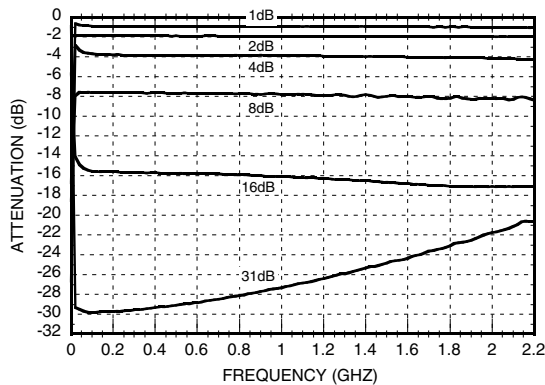


Figure 11. Attenuator performance using two 0.027 μF capacitors

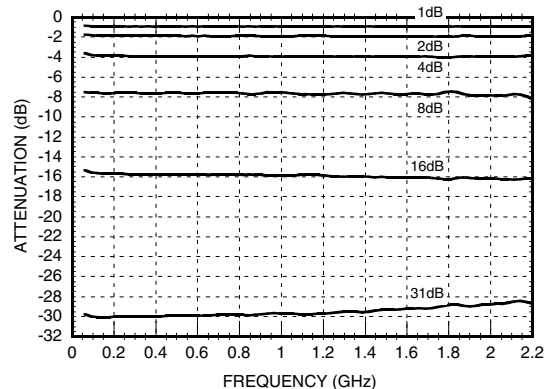


Figure 12. Attenuator performance using five 0.010 μF capacitors

Conclusion

By using two 0.027 μF capacitors, the HMC307QS16G is transformed from a negative bias attenuator to a positive bias attenuator operating from 50 to 350 MHz. The performance is comparable with the original, negative-bias operation over this frequency range. By increasing the number of capacitors, and changing the value, the operating range can be extended to 2 GHz.

As a result a “floated”, positive bias HMC307QS16G can be used in a BTS receiver system as a low frequency 5 bit digital attenuator with nearly 30 dB attenuation range and a frequency response from 50 MHz to 700 MHz.

Evaluation board is available from Hittite Microwave Corporation upon request.

References:

1 and 2: Simulation performed using Genesys V2002.09, By Eagleware Corporation

Notes: