



# ***Reliability Report***

<b>Report Title:</b>	<b>GaAs HBT-A Process Cumulative Reliability</b>
<b>Report Number:</b>	<b>2013-00228</b>
<b>Revision:</b>	<b>11</b>
<b>Date:</b>	<b>25 March 2021</b>

## Summary

This report summarizes the process qualification testing of the GaAs HBT-A process.

**Table 1: Process Characteristics**

**Fabrication Details**

Wafer Fabrication Process	GaAs HBT-A
Passivation Layer	SiN
Bond Pad Metal Composition	Au

## Description / Results of Tests Performed

The following tables provide a description of the qualification tests conducted and the associated test results for products manufactured on the same technologies as described in Table 1. All devices were electrically tested before and after each stress. Any device that did not meet all electrical data sheet limits following stressing would be considered a valid (stress-attributable) failure unless there was conclusive evidence to indicate otherwise.

**Table 2: Process Qualification Test Results**

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
High Temperature Operating Life (HTOL)	JESD22-A108	T <sub>j-stress</sub> =125°C, Biased, 1,240 Hrs	HMC365	QTR2004-00001	12	0
		T <sub>j-stress</sub> =125°C, Biased, 1,000 Hrs	HMC510	QTR2011-00004	12	0
		T <sub>j-stress</sub> =135°C, Biased, 1,000 Hrs	HMC511	QTR2011-00013	159	0
		T <sub>j-stress</sub> =175°C, Biased, 1,000 Hrs	HMC416	QTR2012-00198	24	0
		T <sub>j-stress</sub> =165°C, Biased, 240 Hrs	HMC361	QTR2012-00255	80	0

Test Name	Specification	Conditions	Device	Lot #	Sample Size	Qty. Failures
		T <sub>j-stress</sub> =165°C, Biased, 1,000 Hrs	HMC361	QTR2012-00255	12	0
		T <sub>j-stress</sub> =143°C, Biased, 5039 Hrs	HMC6XXX	QTR2013-00340	6	0
		T <sub>j-stress</sub> =143°C, Biased, 2,000 Hrs	HMC6XXX	QTR2013-00340	14	0
		T <sub>j-stress</sub> =150°C, Biased, 1,000 Hrs <sup>1</sup>	HMC8362	Q13356	82	0
		T <sub>j-stress</sub> =148°C, Biased, 1,000 Hrs <sup>1</sup>	HMC8362	Q15090.11	82	0
		T <sub>j-stress</sub> =125°C, Biased, 1,000 Hrs <sup>1</sup>	ADH363S	Q14676	45	0
		T <sub>j-stress</sub> =148°C, Biased, 1,000 Hrs <sup>1</sup>	HMC8362	Q17319.4	81	0

<sup>1</sup> These samples were subjected to preconditioning (per J-STD-020 Level 3) prior to the start of the stress test. Level 3 preconditioning consists of the following: Bake: 24 hrs @ 125°C, Unbiased Soak: 192 hrs @ 30°C, 60%RH, Reflow: 3 passes through an oven with a peak temperature of 260°C.

Samples of the many devices manufactured with these package and process technologies are continuously undergoing reliability evaluation as part of the ADI Reliability Monitor Program. Additional qualification data is available on [Analog Devices' web site](#).

## Approvals

Reliability Engineer: Tom Wood

## Additional Information

Data sheets and other additional information are available on [Analog Devices' web site](#)

## Appendix

### GaAs HBT-A Failure Rate Estimate

The failure rate estimation was determined using the process HTOL test results and the parameters shown below:

- Die Use Junction Temperature,  $T_{j-use} = 85^{\circ}\text{C}$
- Activation Energy = 1.1 eV

• Acceleration Factor (AF):

$$AF = \exp\left[\left(\frac{E_A}{k}\right) \cdot \left(\left(\frac{1}{T_{USE}}\right) - \left(\frac{1}{T_{STRESS}}\right)\right)\right]$$

- Equivalent hours = Device hours x Acceleration Factor

Device	Qual Number	Equivalent Device Hours
HMC365	QTR2004-00001	$5.40 \times 10^5$
HMC510	QTR2011-00004	$4.35 \times 10^5$
HMC511	QTR2011-00013	$1.27 \times 10^7$
HMC416	QTR2012-00198	$3.14 \times 10^7$
HMC361	QTR2012-00255	$2.13 \times 10^7$
HMC6XXX	QTR2013-00340	$8.48 \times 10^6$
HMC8362	Q13356	$1.99 \times 10^7$
HMC8362	Q15090.11	$1.72 \times 10^7$
ADH363S	Q14676	$1.63 \times 10^7$
HMC8362	Q17319.4	$1.70 \times 10^7$
Total Equivalent Device Hours =		$1.31 \times 10^8$

The failure rate was calculated using Chi Square Statistic:

Since there were no failures and the tests were time terminated,  $F=0$ , and  $R = 2F+2 = 2$

$$\lambda_{CL} = \frac{\chi^2_{(%CL, 2F+2)} \cdot 10^9}{2 \cdot (\text{Equiv. Device Hours})}$$

at 60% and 90% Confidence Level (CL) and a die use junction temp,

$$T_j = 85^\circ\text{C};$$

Failure Rate:

$$\lambda_{60} = [(\chi^2)_{60,2}] / (2 \times 1.31 \times 10^8) = 1.8 / 2.61 \times 10^8 = 7.01 \times 10^{-9} \text{ failures/hour or } 7.0 \text{ FIT or MTTF} = 1.43 \times 10^8 \text{ Hours}$$

$$\lambda_{90} = [(\chi^2)_{90,2}] / (2 \times 1.31 \times 10^8) = 4.6 / 2.61 \times 10^8 = 1.77 \times 10^{-8} \text{ failures/hour or } 17.7 \text{ FIT or MTTF} = 5.66 \times 10^7 \text{ Hours}$$