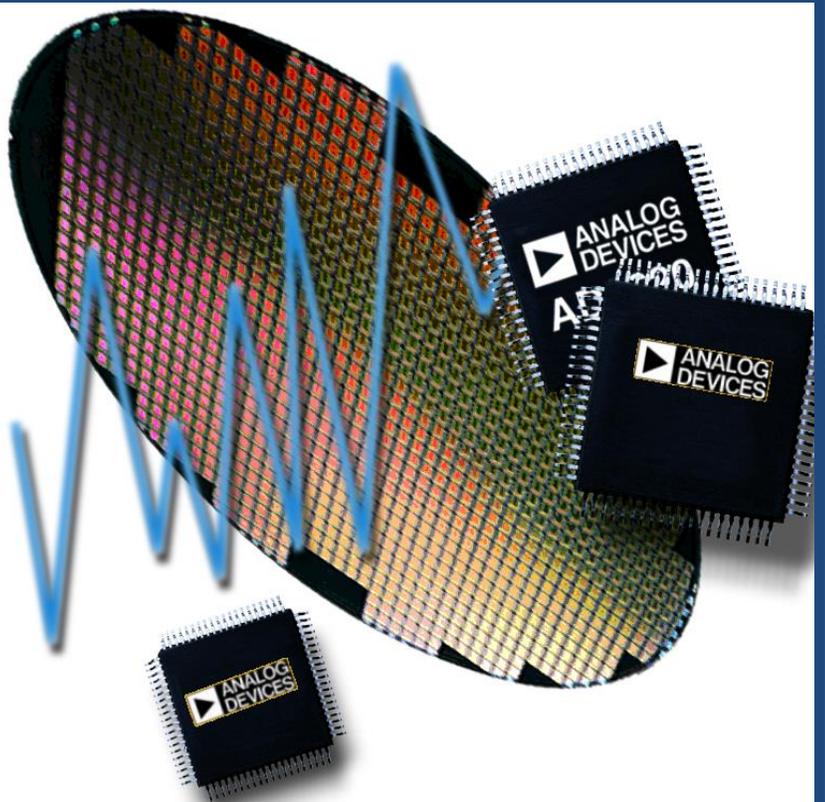


# Analog Devices Welcomes Hittite Microwave Corporation

NO CONTENT ON THE ATTACHED DOCUMENT HAS CHANGED





# ***Reliability Report***

**Report Title:** Qualification Test Report

**Report Type:** See Attached

**Date:** See Attached

# Process FIT Rate Report

**QTR: 2013- 00261**

**Rev: 02**

**Wafer Process: CMOS-A**

HMC596

HMC645

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## Introduction

The testing performed for this report is designed to accelerate the predominant failure mode, electro-migration (EM), for the devices under test. The devices are stressed at high temperature and DC biased to simulate a lifetime of use at typical operating temperatures. Using the Arrhenius equation, the acceleration factor (AF) is calculated for the stress testing based on the stress temperature and the typical use operating temperature.

This report is intended to summarize all of the High Temperature Operating Life Test (HTOL) data for the CMOS-A process. The FIT/MTTF data contained in this report includes all the stress testing performed on this process to date and will be updated periodically as additional data becomes available. Data sheets for the tested devices can be found at [www.hittite.com](http://www.hittite.com).

## Glossary of Terms & Definitions:

- HAST:** Highly Accelerated Stress Test (biased). Devices are subjected to 96 hours of 85% relative humidity at a temperature of 130°C and pressure (15 PSIG), while DC biased. This test is performed in accordance with JESD22-A110.
- HTOL:** High Temperature Operating Life. This test is used to determine the effects of bias conditions and temperature on semiconductor devices over time. It simulates the devices' operating condition in an accelerated way, through high temperature and/or bias voltage, and is primarily for device qualification and reliability monitoring. This test was performed in accordance with JEDEC JESD22-A108.
- MSL:** Moisture sensitivity level pre-conditioning is performed per JESD22-A113.
- Operating Junction Temp ( $T_{oj}$ ):** Temperature of the die active circuitry during typical operation.
- Stress Junction Temp ( $T_{sj}$ ):** Temperature of the die active circuitry during stress testing.

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## Qualification Sample Selection:

All qualification devices used were manufactured and tested on standard production processes and met pre-stress acceptance test requirements.

## Summary of Qualification Tests:

### HMC596 (QTR08004)

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial Electrical	234	234	Complete	
HTOL, 1000 hours	80	80	Complete	
Post HTOL Electrical Test	80	80	Pass	
MSL1 260°C Preconditioning	154	154	Complete	
Temperature Cycle	77	77	Complete	
Post Temperature Cycle Electrical Test	77	77	Pass	
Autoclave Exposure	77	77	Complete	
Post Autoclave Electrical Test	77	77	Pass	
Bond Pull	10	10	Pass	
Die Shear	10	10	Pass	
Metal and Dielectric Thickness	5	5	Pass	
SEM Inspection	5	5	Pass	

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## HMC625 (QTR11011)

TEST	QTY IN	QTY OUT	PASS / FAIL	NOTES
Initial Electrical	48	48	Complete	
HTOL, 1000 hours	48	48	Complete	
Post HTOL Electrical Test	48	48	Pass	

## HMC625 (QTR2012-00185)

TEST	QTY IN	QTY OUT	PASS / FAIL	NOTES
Initial Electrical	184	184	Complete	
HTOL, 1033 hours	24	24	Complete	
Post HTOL Electrical Test	24	24	Pass	
Temperature Cycle	80	80	Complete	
Post Temperature Cycle Electrical Test	80	80	Pass	
Temperature Humidity (85°C/85% RH, unbiased)	80	80	Complete	
Post Temperature Humidity Electrical Test	80	80	Pass	

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## HMC625 (QTR2012-00279)

TEST	QTY IN	QTY OUT	PASS / FAIL	NOTES
Initial Electrical	184	184	Complete	
HTOL, 1033 hours	24	24	Complete	
Post HTOL Electrical Test	24	24	Pass	
Temperature Cycle	80	80	Complete	
Post Temperature Cycle Electrical Test	80	80	Pass	
Temperature Humidity (85°C/85% RH, unbiased)	80	80	Complete	
Post Temperature Humidity Electrical Test	80	80	Pass	

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**HMC625 (QTR2012-00430)**

TEST	QTY IN	QTY OUT	PASS / FAIL	NOTES
Initial Electrical	184	184	Complete	
HTOL, 1033 hours	72	72	Complete	
Post HTOL Electrical Test	72	72	Pass	
Temperature Cycle	240	240	Complete	
Post Temperature Cycle Electrical Test	240	240	Pass	
Temperature Humidity (85°C/85% RH, unbiased)	240	240	Complete	
Post Temperature Humidity Electrical Test	240	240	Pass	
MSL 1 Preconditioning	239	239	Complete	
Post MSL 1 Electrical Test	239	239	Pass	
HAST (preconditioned)	239	239	Complete	
Post HAST Electrical Test	239	239	Pass	

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# Process FIT Rate Report

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**Rev: 02**

**Wafer Process: CMOS-A**

## HMC2166 (QTR2013-00339)

TEST	QTY IN	QTY OUT	PASS / FAIL	NOTES
Initial Electrical	243	243	Complete	
HTOL, 1000 hours	243	243	Complete	
Post HTOL Electrical Test	243	243	Pass	

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## CMOS-A Failure Rate Estimate

Based on the HTOL test results, a failure rate estimation was determined using the following parameters:

With device ambient case temp,  $T_c = 60^\circ\text{C}$

HMC596 (QTR08004)

Operating Junction Temp ( $T_{oj}$ ) =  $60^\circ\text{C}$ ( $333^\circ\text{K}$ )

Stress Junction Temp ( $T_{sj}$ ) =  $125^\circ\text{C}$ ( $398^\circ\text{K}$ )

HMC625 (QTR11011)

Operating Junction Temp ( $T_{oj}$ ) =  $89^\circ\text{C}$ ( $362^\circ\text{K}$ )

Stress Junction Temp ( $T_{sj}$ ) =  $150^\circ\text{C}$ ( $423^\circ\text{K}$ )

HMC625 (QTR2012-00185)

Operating Junction Temp ( $T_{oj}$ ) =  $89^\circ\text{C}$ ( $362^\circ\text{K}$ )

Stress Junction Temp ( $T_{sj}$ ) =  $150^\circ\text{C}$ ( $423^\circ\text{K}$ )

HMC625 (QTR2012-00279)

Operating Junction Temp ( $T_{oj}$ ) =  $89^\circ\text{C}$ ( $362^\circ\text{K}$ )

Stress Junction Temp ( $T_{sj}$ ) =  $150^\circ\text{C}$ ( $423^\circ\text{K}$ )

HMC625 (QTR2012-00430)

Operating Junction Temp ( $T_{oj}$ ) =  $89^\circ\text{C}$ ( $362^\circ\text{K}$ )

Stress Junction Temp ( $T_{sj}$ ) =  $150^\circ\text{C}$ ( $423^\circ\text{K}$ )

HMC2166 (QTR2013-00339)

Operating Junction Temp ( $T_{oj}$ ) =  $62^\circ\text{C}$ ( $335^\circ\text{K}$ )

Stress Junction Temp ( $T_{sj}$ ) =  $106^\circ\text{C}$ ( $379^\circ\text{K}$ )

Device hours:

HMC596 (QTR08004) = (80 X 1000hrs) = 80,000 hours

HMC625 (QTR11011) = (54 X 1000hrs) = 54,000 hours

HMC625 (QTR2012-00185) = (48 X 1000hrs) = 48,000 hours

HMC625 (QTR2012-00279) = (24 X 1000hrs) = 24,000 hours

HMC625 (QTR2012-00430) = (72 X 1000hrs) = 72,000 hours

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HMC2166 (QTR2013-00339) = (243 X 1000hrs) = 243,000 hours

For CMOS-A MMIC, Activation Energy = 0.7 eV

$$AF = \exp\left[\left(\frac{E_A}{k}\right) \cdot \left(\left(\frac{1}{T_{USE}}\right) - \left(\frac{1}{T_{STRESS}}\right)\right)\right]$$

Acceleration Factor (AF):

HMC596 (QTR08004) Acceleration Factor =  $\exp[0.7/8.6 \text{ e-}5(1/333-1/398)] = 54.2$

HMC625 (QTR11011) Acceleration Factor =  $\exp[0.7/8.6 \text{ e-}5(1/362-1/423)] = 25.6$

HMC625 (QTR2012-00185) Acceleration Factor =  $\exp[0.7/8.6 \text{ e-}5(1/362-1/423)] = 25.6$

HMC625 (QTR2012-00279) Acceleration Factor =  $\exp[0.7/8.6 \text{ e-}5(1/362-1/423)] = 25.6$

HMC625 (QTR2012-00430) Acceleration Factor =  $\exp[0.7/8.6 \text{ e-}5(1/362-1/423)] = 25.6$

HMC2166 (QTR2013-00339) Acceleration Factor =  $\exp[0.7/8.6 \text{ e-}5(1/335-1/379)] = 16.8$

Equivalent hours = Device hours x Acceleration Factor

Equivalent hours = (80,000x54.2)+(54,000x25.6)+(48,000x25.6)+(24,000x25.6)+(72,000x25.6)+(243,000x16.8)  
=  $1.35 \times 10^7$  hours

Since there were no failures and we used a time terminated test, F=0, and R = 2F+2 = 2

The failure rate was calculated using Chi Square Statistic:

$\lambda_{CL} = \frac{\chi^2_{\%CL, 2f+2} \cdot 10^9}{2 \cdot t \cdot SS \cdot AF}$  at 60% and 90% Confidence Level (CL), with 0 units out of spec and a 60°C package backside temp;

Failure Rate

$\lambda_{60} = [(\chi^2)_{60,2}]/(2X 1.35 \times 10^7)] = 1.8/ 2.70 \times 10^7 = 6.79 \times 10^{-8}$  failures/hour or 68 FIT or MTTF =  $1.47 \times 10^7$  Hours

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$$\lambda_{90} = [(\chi^2)_{90,2}]/(2X \ 1.35 \times 10^7) = 4.6/ \ 2.70 \times 10^7 = 1.71 \times 10^{-7} \text{ failures/hour or } 171 \text{ FIT or MTTF} = 5.85 \times 10^6 \text{ Hours}$$

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