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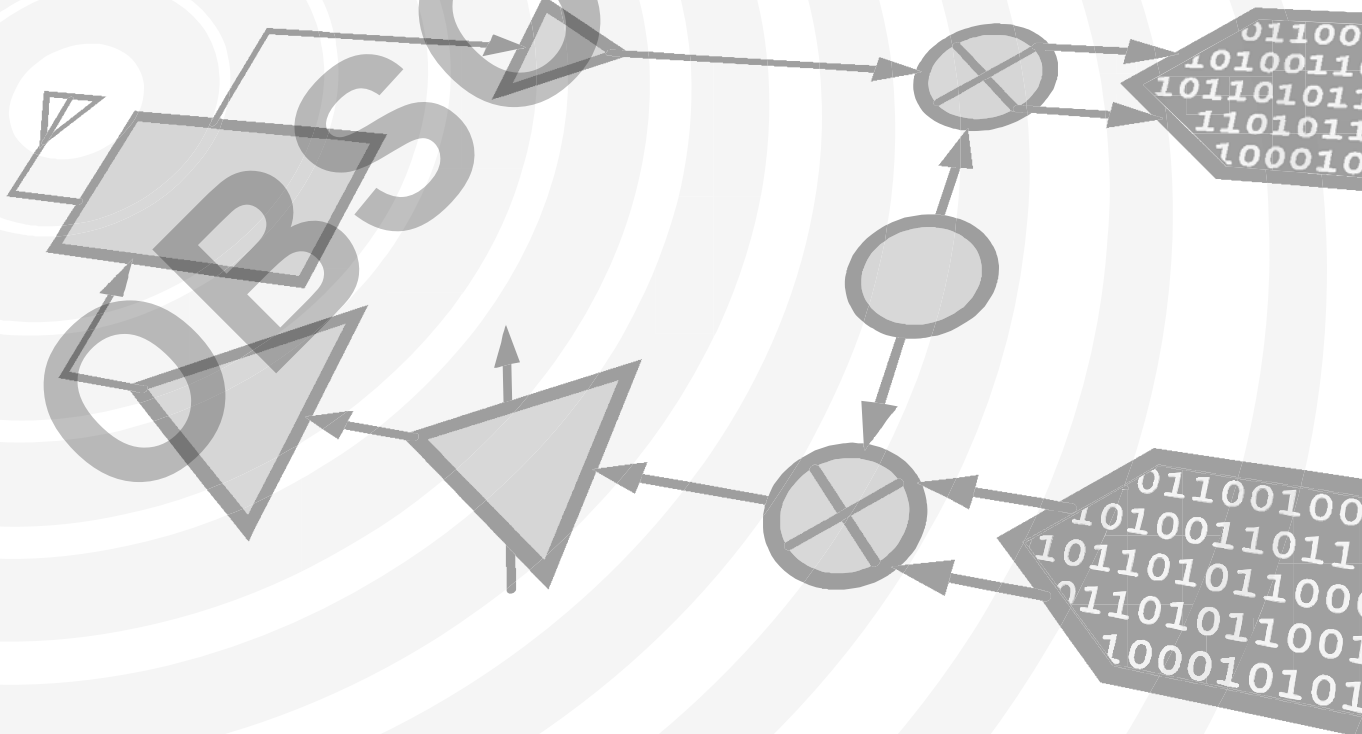
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HMC6000

v02.0514

MILLIMETERWAVE TRANSMITTER IC
*57 - 64 GHz*

Typical Applications

The HMC6000 is ideal for:

• WiGig Single Carrier Modulations

• 60 GHz ISM Band Data Transmitter

• Multi-Gbps Data Communications

• High Definition Video Transmission

• RFID

Features

Support for IEEE Channel Plan

Output Power: 12 dBm

Max Gain: 38 dB

Gain Control Range: 17 dB

Integrated Frequency Synthesizer

Integrated Image Reject Filter

Programmable IF Gain Block

Universal Analog I/Q Baseband Interface

Three-Wire Serial Digital Interface

Die Size: 4.082 x 1.814 mm

Functional Diagram
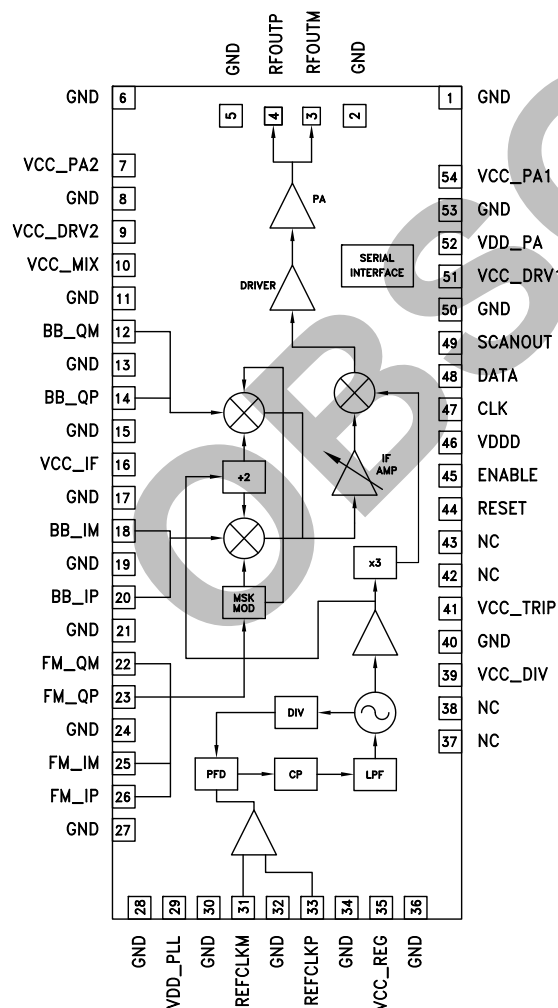
General Description

The HMC6000 is a complete mmWave transmitter on a chip operating from 57 to 64 GHz with 1.8 GHz of modulation bandwidth. An integrated synthesizer provides tuning in 500 or 540 MHz step sizes depending on the choice of external reference clock. Support for a wide variety of modulation formats is provided through a universal analog baseband IQ interface. The transmitter chip supports all single carrier WiGig modulations and optionally supports dedicated FSK/MSK modulation formats for lower cost and lower power serial data links without the need for high speed data converters. A differential output provides up to 12 dBm linear output power into a 100 ohm load. Together with the HMC6001, a complete transmit/receive chipset is provided for multi-Gbps operation in the unlicensed 60 GHz ISM band.

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Table 1. Electrical Specifications, TA = +25° C, See Test Conditions

Parameter	Condition	Min.	Typ.	Max.	Units
Frequency Range		57		64	GHz
Frequency Step Size	308.5714 MHz Ref Clk		0.54		GHz
Frequency Step Size	285.714 MHz Ref Clk		0.50		GHz
Modulation Bandwidth	3dB BW, double-sided		1.8		GHz
Max Gain	Pout minus total Pin of all 4 baseband inputs	33	36.5	40	dB
Gain Control Range			17		dB
Gain Step Size			1.3		dB
P1dB			12		dBm
Psat			17		dBm
Image Rejection			34		dB
Sideband Suppression		14	20		dB
Carrier Suppression [1]		11	20		dB
3xLO Suppression			32		dBc
Phase Noise @ 100 kHz			-72		dBc/Hz
Phase Noise @ 1 MHz			-86		dBc/Hz
Phase Noise @ 10 MHz			-111		dBc/Hz
Phase Noise @ 100 MHz			-125		dBc/Hz
Phase Noise @ 1 GHz			-127		dBc/Hz
TX Noise Floor	Max Gain		-125		dBm/Hz
PLL Loop BW	Internal Loop Ffilter		200		kHz
Synthesizer Settling Time			< 6		µs
Power Dissipation			0.8		W

[1] Single point calibration can be used to improve carrier suppression.

Table 2. Test Conditions

Reference frequency	308.5714 MHz
Temperature	+25°C
Gain Setting	Max
Input Signal Level	-31 dBm @ each of the 4 baseband inputs
IF Bandwidth	Max
Input Impedance	100Ω Differential
Output Impedance	100Ω Differential

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2

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Table 3. Recommended Operation Conditions

Description	Symbol	Min	Typical	Max	Units
Analog Ground	GND		0		Vdc
	VCC_PA1 VCC_PA2	3.9	4.0	4.1	Vdc
Power Supplies	VDD_PA VCC_DRV VCC_TRIP VCC_DIV VCC_REG VCC_IF VCC_MIX	2.565	2.7	2.835	Vdc
	VDD_PLL	1.3	1.35	1.48	Vdc
	VDDD				
Input Voltage Ranges					
Serial Digital Interface – Logic High	DATA ENABLE CLK RESET	0.9	1.2	1.4	V
Serial Digital Interface – Logic Low	DATA ENABLE CLK RESET	-0.05	0.1	0.3	V
Reference Clock	REFCLKP REFCLKM		3.3 or 2.5V LVPECL/LVDS 1.2V CMOS		V
Baseband I and Q [1] [2]	BB_IM BB_IP BB_QM BB_QP	5	25	100	mVp-p
Baseband I and Q Common mode			1.6		V
MSK Data [3]	FM_IM FM_IP FM_QM FM_QP	200	500	750	mVp-p
MSK Common mode			1.1		V
RF Output [4]	RFOUTP RFOUTM			17	dBm
Input Resistance	DATA ENABLE CLK RESET		>50		kOhms
	REFCLKP / M		50		Ohm
Temperature		-40		+85	C

[1] Values above 25 mVp-p are to be used only with IF attenuation to keep the Pout below 16 dBm

[2] 25mVp-p is applied at each of the 4 Baseband Inputs

[3] 500mVp-p is applied at each of the 4 FM Inputs

[4] 4.0Vdc present at the TX RF output pads. To avoid damaging the Power Amplifier the pads must be AC coupled to any other DC voltage including ground

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3

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Table 4. Power Consumption

Voltage		Typical Current (mA)	Typical Power Consumption (Watts)
VCC_PA1	(4.0Vdc)	33	0.27
VCC_PA2	(4.0Vdc)	33	
VCC_REG	(2.7Vdc)	12	0.53
VCC_DRV1	(2.7Vdc)	16	
VCC_DRV2	(2.7Vdc)	16	
VCC_MIX	(2.7Vdc)	29	
VCC_IF	(2.7Vdc)	31	
VCC_TRIP	(2.7Vdc)	48	
VCC_DIV	(2.7Vdc)	35	
VDD_PA	(2.7Vdc)	6	
VDDD	(1.35Vdc)	<1	0.01
VDD_PLL	(1.35Vdc)	8	

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4

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Figure 1. Output Power vs. Frequency at Maximum Gain[1]
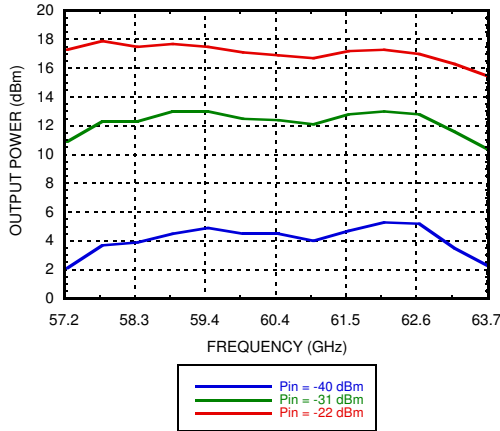
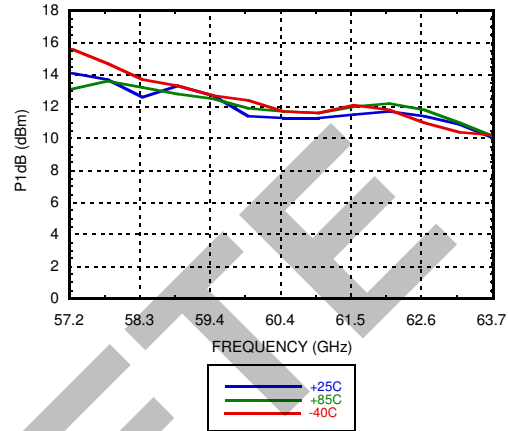### Figure 2. Output P1dB vs. Frequency Over Temperature[2]

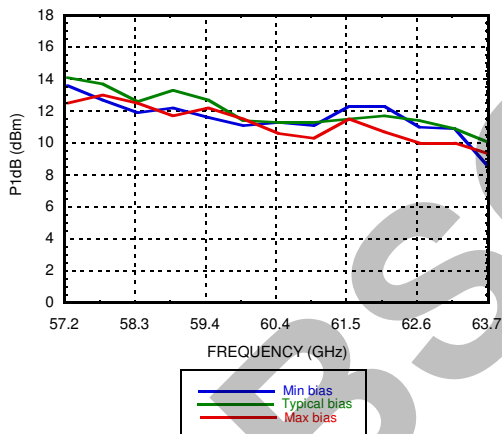### Figure 3. Output P1dB vs. Frequency Across Voltage

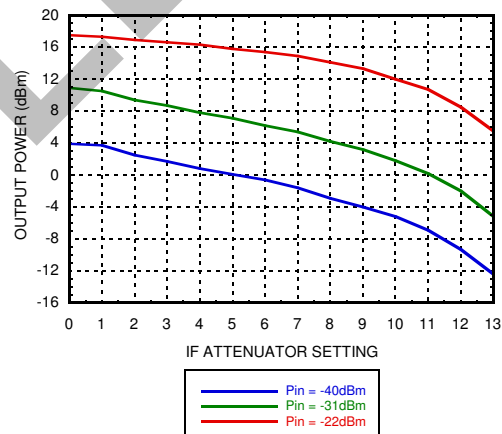### Figure 4. 58.32 GHz (IEEE CH-1) Output Power vs. IF Gain Setting[1]

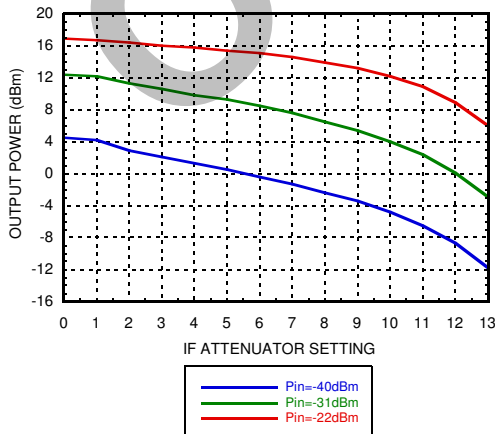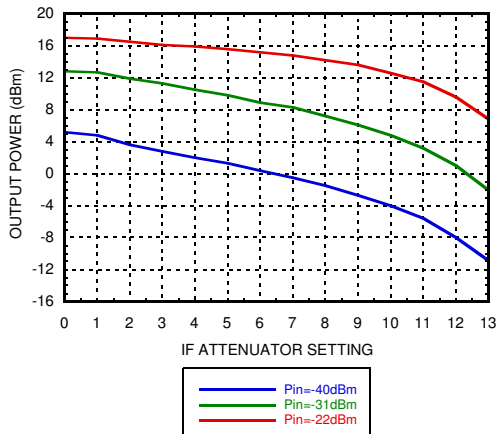### Figure 5. 60.48 GHz (IEEE CH-2) Output Power vs. IF Gain Setting[1]

Figure 6. 62.64 GHz (IEEE CH-3) Output Power vs. IF Gain Setting[1]

[1] Input power of -40, -31 and -22dBm applied at each of the 4 baseband inputs
[2] Maximum gain

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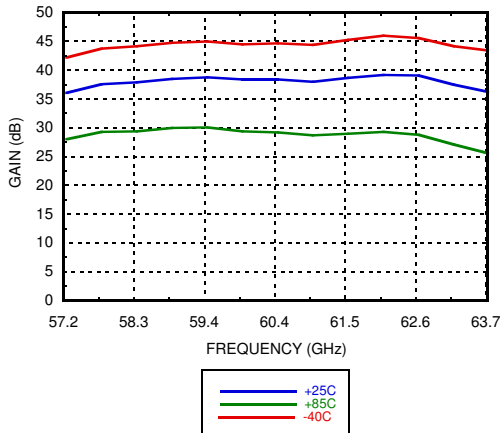### Figure 7. Gain vs. Frequency Over Temperature[3]

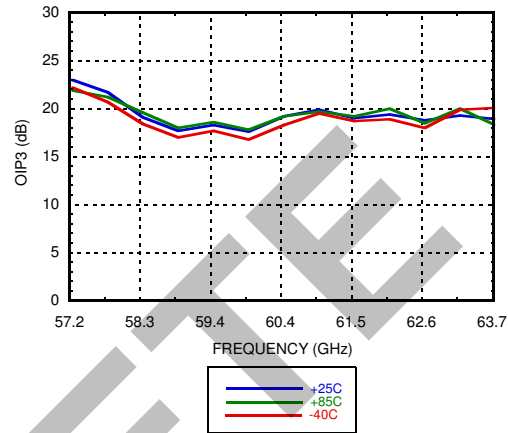### Figure 8. OIP3 vs. Frequency over Temperature[2]

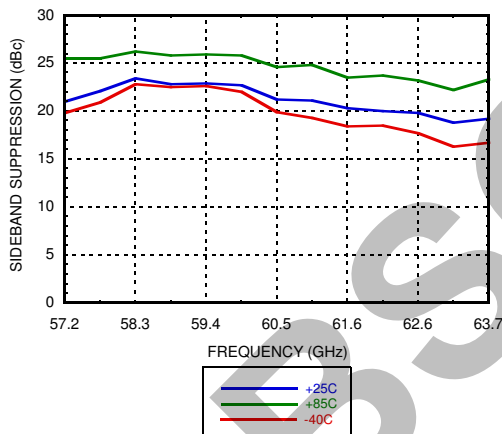### Figure 9. Sideband Suppression vs. Frequency Over Temperature[4]

Figure 10. Sideband Suppression vs. Frequency Across Voltage[4]
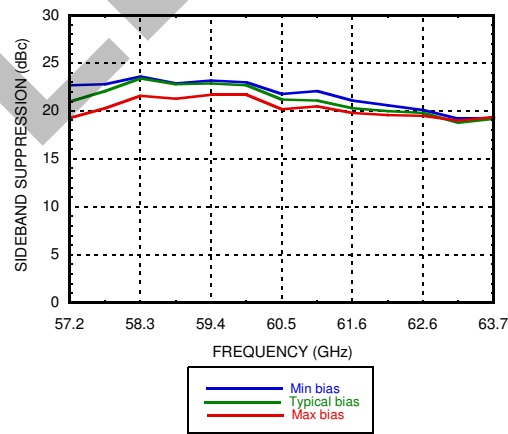
Figure 11. Image Rejection vs. Frequency Over Temperature[4]
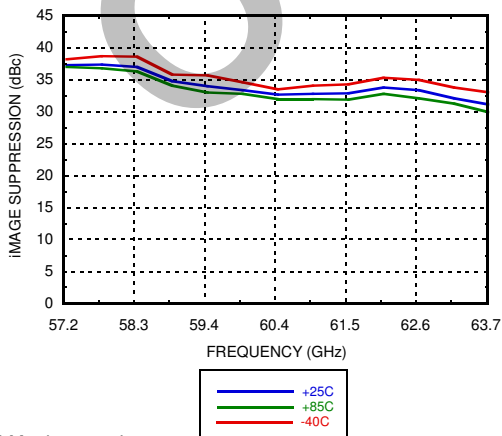
Figure 12. Image Rejection vs. Frequency Across IF Gain[5]
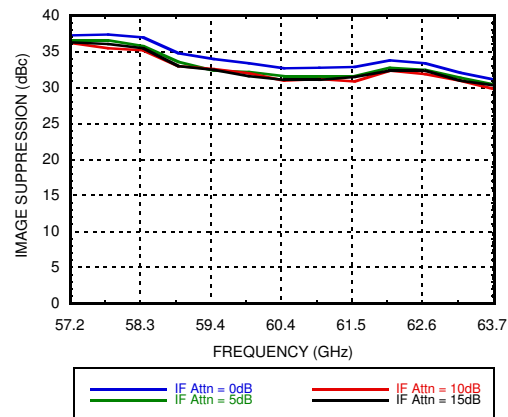
[2] Maximum gain
[3] Input power of -40dBm applied at each of the 4 baseband inputs, Gain = Pout minus total Pin of all 4 baseband inputs
[4] Max gain, sideband offset = 100MHz, input power of -31dBm applied to each of the 4 baseband inputs @ +25C, -22dBm @ +85C and -40dBm @ -40C
[5] Input power of -31dBm applied to each of the 4 baseband inputs

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6

Figure 13. Carrier Suppression vs. Frequency Over Temperature[6]
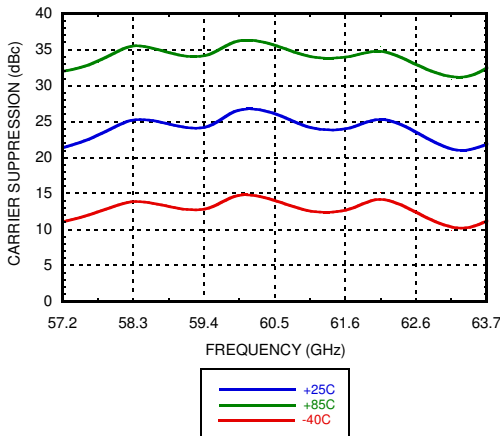
Figure 14. 3x LO Suppression vs. Frequency Over Temperature[6]
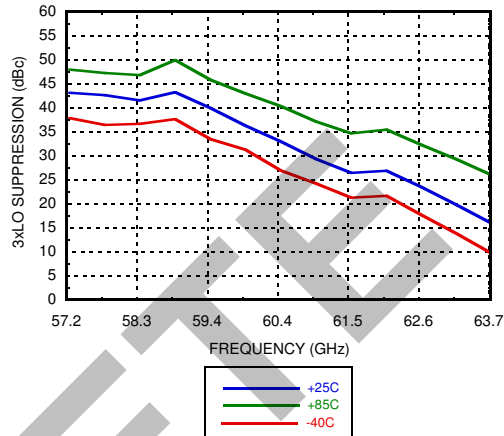
Figure 15. 3x LO Suppression vs. Frequency Across IF Gain[5]
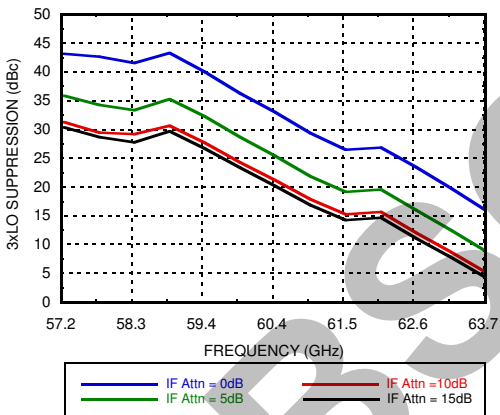
Figure 16. 2xLO vs. Frequency Across IF Gain[5]
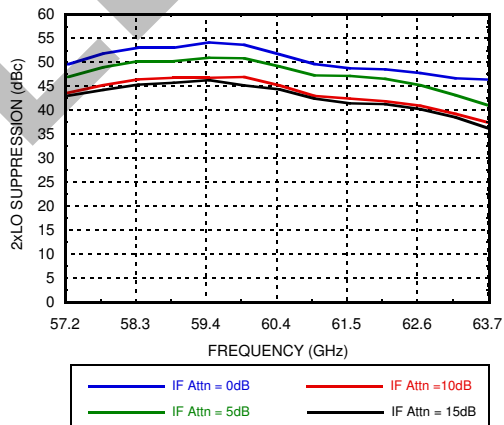
Figure 17. Phase Noise vs. Frequency Offset Over Temperature[7]
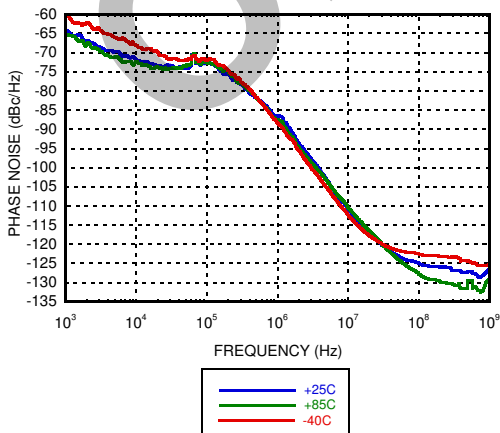
Figure 18. Phase Noise vs. Frequency Offset Over Voltage[7]
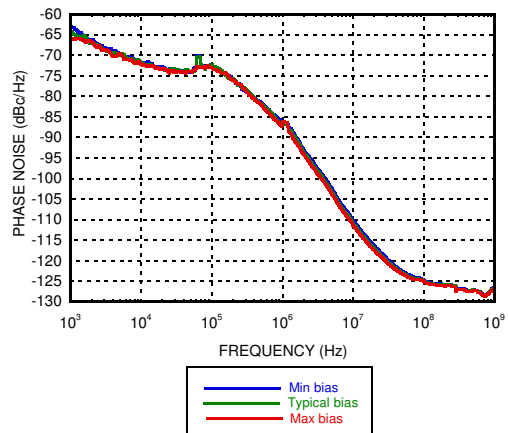
[5] *Input power of -31dBm applied to each of the 4 baseband inputs*
[6] *Max gain, input power of -31dBm applied to each of the 4 baseband inputs*
[7] *60.48 GHz Carrier*

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Figure 19. Passband Response vs. Frequency Offset by Channel[7]
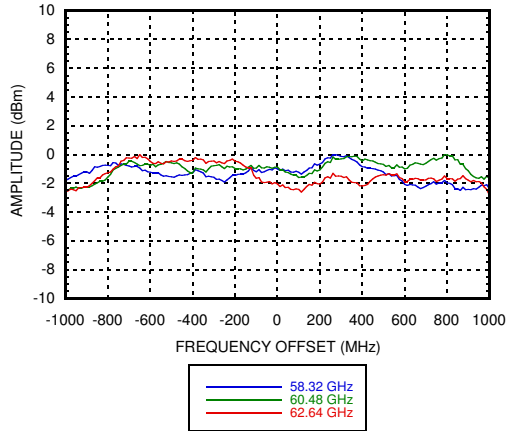
Figure 20. 60.48 GHz MCS1 WiGig waveform @ 16dBm vs. WiGig Mask[8]
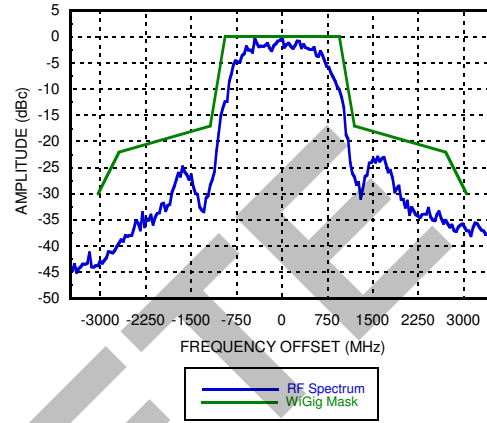
Figure 21. 60.48 GHz MCS1 WiGig waveform @ 14dBm vs. IEEE 802.15.3c Mask[9]

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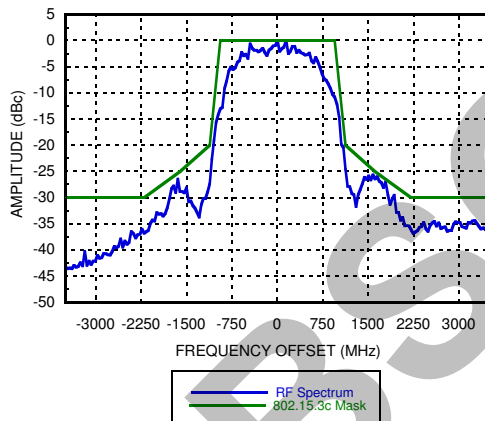
[7] Max gain, reference Table 12 for IF VGA and IF Up-Mixer Filter Settings
[8] Max gain, Input power of -24 dBm applied to each of the 4 baseband inputs
[9] Max gain, Input power of -27 dBm applied to each of the 4 baseband inputs

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8

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Table 5. Absolute Maximum Ratings

VCC_PA = 4 V	4.2 Vdc
VDD = 2.7 V	2.85 Vdc
VCC = 2.7 V	2.85 Vdc
VDD_PLL = 1.35 V	1.6 Vdc
VDDD = 1.35 V	1.6 Vdc
GND	0± 50 mV
Power Dissipation (Combined Pdiss of VCC_PA1 and VCC_PA2)	27 C/W (1.1W total Pdiss) 0.36W (at 85 baseplate)
Serial Digital Interface Input Voltage	1.5 Vdc
Ref CLK Input (AC coupled)(each)	0.75 Vp-p
Baseband Inputs (BB, FM)(each)	0.75 Vp-p
Storage Temperature	-55°C to 150°C
Operating Temperature	-40°C to 85°C

Outline Drawing
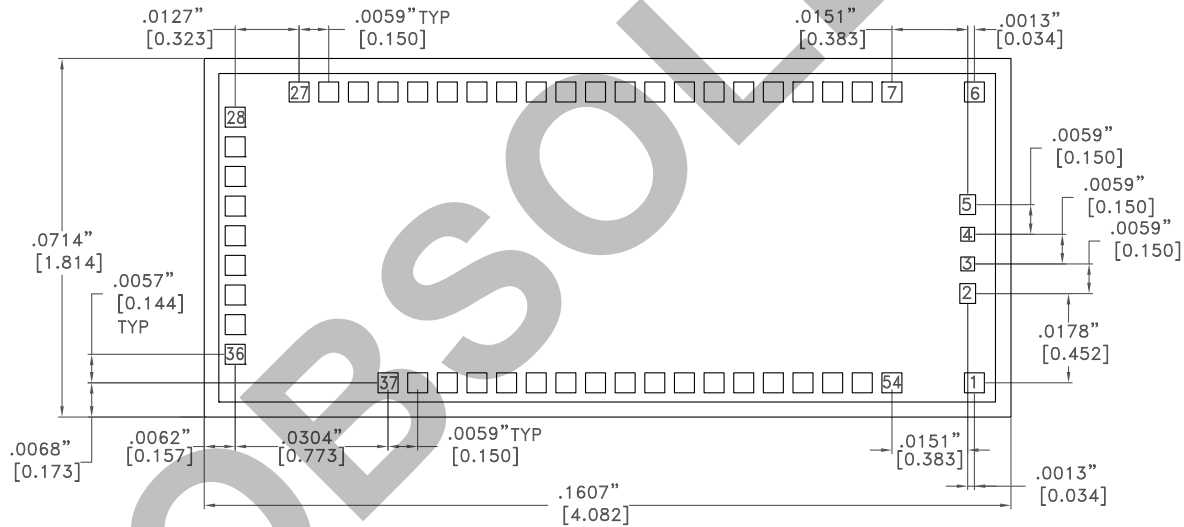
NOTES:
1. ALL DIMENSIONS ARE IN INCHES [MM]
2. DIE THICKNESS IS .028 [0.711] ± .001 [.025]
3. BOND PAD METALLIZATION: AL
4. OVERALL DIE SIZE ± .002 [.051]

Table 6. Die Packaging Information

Standard	Alternate
VR-33CC-02-X4 GEL_PAK	[1]

[1] For alternate packaging information contact Hittite Microwave Corporation.

Table 7. Die Pad Dimensions

Pads	Pad Size	Pad Opening
1, 6, 7 - 54	0.0040 [0.101] x 0.0040 [0.101]	0.0037 [0.095] x 0.0037 [0.095]
3, 4	0.0028 [0.070] x 0.0028 [0.070]	0.0025 [0.064] x 0.0025 [0.064]
2, 5	0.0046 [0.118] x 0.0059 [0.150]	0.0028 [0.070] x 0.0036 [0.090]

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9

Table 8. Pad Descriptions

Pad Number	Function	Description
1, 2, 5, 6, 8, 11, 13, 15, 17, 19, 21, 24, 27, 28, 30, 32, 34, 36, 40, 50, 53	GND	Analog Ground
3	RFOUTM	RF negative output – DC coupled – diff match to 100Ω [1]
4	RFOUTP	RF positive output – DC coupled – diff match to 100Ω [1]
7	VCC_PA2	4.0V supply (PA)
9	VCC_DRV2	2.7V supply (Driver)
10	VCC_MIX	2.7V (Mixer)
12	BB_QM	Baseband negative quadrature input – DC coupled - 50Ω
14	BB_QP	Baseband positive quadrature input – DC coupled - 50Ω
16	VCC_IF	2.7V supply (IF)
18	BB_IM	Baseband negative in-phase input – DC coupled - 50Ω
20	BB_IP	Baseband positive in-phase input – DC coupled - 50Ω
22	FM_QM	FSK negative quadrature input – DC coupled - 50Ω
23	FM_QP	FSK positive quadrature input – DC coupled - 50Ω
25	FM_IM	FSK negative in-phase input – DC coupled - 50Ω
26	FM_IP	FSK positive in-phase input – DC coupled - 50Ω
29	VDD_PLL	1.35V supply (VCO)
31	REFCLKM	Xtal REF CLK Minus - AC or DC coupled - 50Ω
33	REFCLKP	Xtal REF CLK Plus - AC or DC coupled - 50Ω
35	VCC_REG	2.7V supply (VCO)
37, 38, 42, 43	NC	Factory test points. Leave floating. Do not connect.
39	VCC_DIV	2.7V supply (Divider)
41	VCC_TRIP	2.7V supply (Tripler)
44	RESET	Asynchronous reset-all registers (1.2V CMOS, active high)
45	ENABLE	Serial digital interface enable (1.2V CMOS) - 50kΩ
46	VDDD	1.35V supply (serial digital interface)
47	CLK	Serial digital interface clock (1.2V CMOS) - 50kΩ
48	DATA	Serial digital interface data (1.2V CMOS) - 50kΩ
49	SCANOUT	Serial digital interface out (1.2V CMOS) - 50kΩ
51	VCC_DRV1	2.7V supply (Driver)
52	VDD_PA	2.7V supply (PA)
54	VDD_PA1	4.0V supply (PA)

[1] 4.0Vdc present at the TX RF output pads. To avoid damaging the Power Amplifier the pads must be AC coupled to any other DC voltage including ground

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10

Theory of Operation

An integrated frequency synthesizer creates a low-phase noise LO between 16.3 and 18.3 GHz. This is divided by 2, split into quadrature components and used to modulate differential baseband I and Q signals onto an 8 to 9.1 GHz sliding IF. This signal is then filtered and amplified with 17 dB of variable gain, then mixed with three times the LO frequency to upconvert to an RF frequency between 57 and 64 GHz. The step size of the synthesizer equates to 540MHz steps at RF when used with 308.5714 MHz reference crystal (compatible with the IEEE channels of the ISM band) or 500 MHz steps if used with a 285.714 MHz reference crystal. Integrated notch filters attenuate the lower mixing product at 40-46GHz. Two RF amplifier stages provide gain to allow up to 12 dBm differential output.

The phase noise and quadrature balance of the HMC6000 is sufficient to carry up to 16QAM modulation.

There are no special power sequencing requirements for the HMC6000; all voltages are to be applied simultaneously.

Register Array Assignments and Serial Interface

The register arrays for both the transmitter and receiver are organized into 16 rows of 8 bits. Using the serial interface, the arrays are written or read one row at a time as shown in Figure 22 and Figure 23, respectively. Figure 22 shows the sequence of signals on the ENABLE, CLK, and DATA lines to write one 8-bit row of the register array. The ENABLE line goes low, the first of 18 data bits (bit 0) is placed on the DATA line, and 2 ns or more after the DATA line stabilizes, the CLK line goes high to clock in data bit 0. The DATA line should remain stable for at least 2 ns after the rising edge of CLK.

The Tx IC will support a serial interface running up to several hundred MHz, and the interface is 1.2V CMOS levels. A write operation requires 18 data bits and 18 clock pulses, as shown in Figure 22. The 18 data bits contain the 8-bit register array row data (LSB is clocked in first), followed by the register array row address (ROW0 through ROW15, 000000 to 001111, LSB first), the Read/Write bit (set to 1 to write), and finally the Tx chip address 110, LSB first).

Note that the register array row address is 6 bits, but only four are used to designate 16 rows, the two MSBs are 0.

After the 18th clock pulse of the write operation, the ENABLE line returns high to load the register array on the IC; prior to the rising edge of the ENABLE line, no data is written to the array. The CLK line should have stabilized in the low state at least 2 ns prior to the rising edge of the ENABLE line.
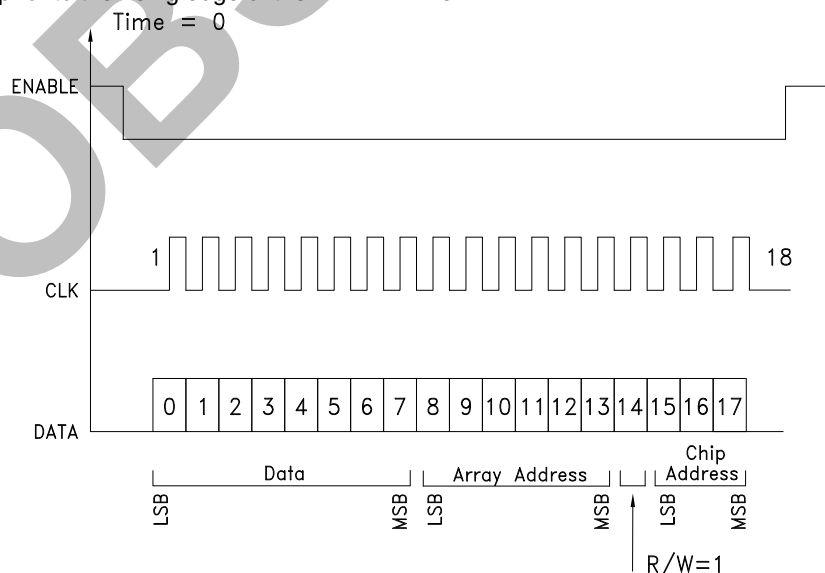
Figure 22. Timing Diagram for writing a row of the Transmitter Serial Interface

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11
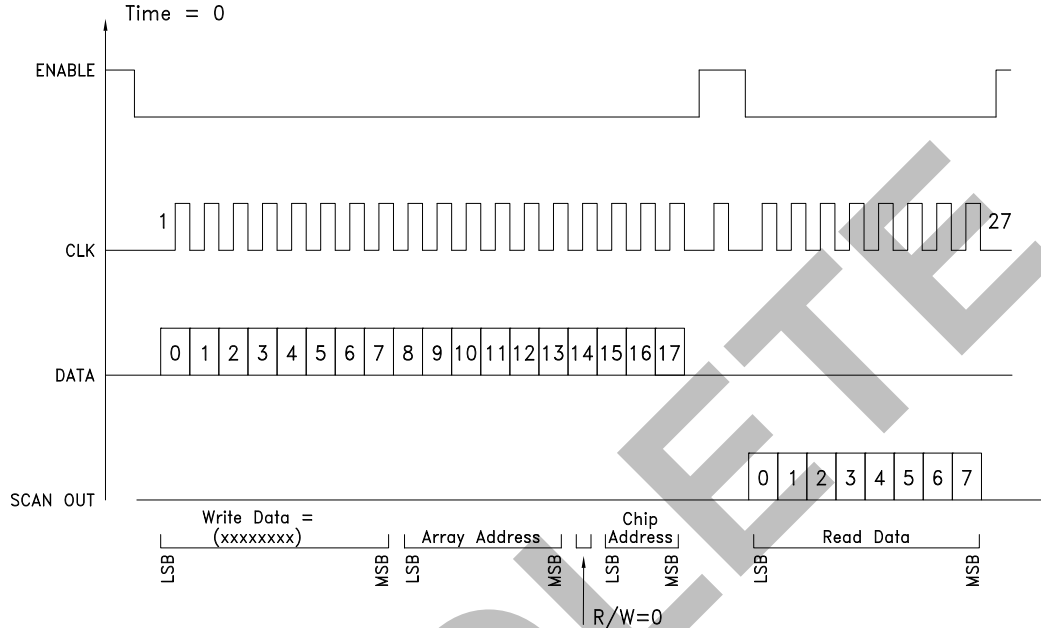
Figure 23. Timing Diagram for reading a row of the Transmitter Serial Interface

Table 9. Transmitter Register Array Assignments

Register Array Row & Bit	Internal Signal Name	Signal Function
ROW0		
ROW0<7>	pa_pwrdn	Active high to power down most other PA circuits not controlled by ROW0<6>
ROW0<6>	pa_pwrdn_fast	Active high to power down the PA core in < 1 µs
ROW0<5>	upmixer_pwrdn	Active high to power down IF to RF upmixer
ROW0<4>	divider_pwrdn	Active high to power down local oscillator divider
ROW0<3>	if_bgmux_pwrdn	Active high to power down one of three on-chip bandgap refs (IF) and associated mux
ROW0<2>	if_upmixer_pwrdn	Active high to power down baseband to IF upmixer
ROW0<1>	driver_pwrdn	Active high to power down PA predriver
ROW0<0>	ifvga_pwrdn	Active high to power down IF variable gain amplifier
ROW1		
ROW1<7>	ipc_pwrdn	Active high to power down on chip current reference generator
ROW1<6>	tripler_pwrdn	Active high to power down frequency tripler
ROW1<5>	ifvga_q_cntrl<2>	These bits control the Q of the IF filter in the baseband to IF upmixer; ROW1<5:3> = 000 for highest Q and highest gain. To reduce Q and widen bandwidth, increment ROW1<5:3> in the sequence 001 100 101 111
ROW1<4>	ifvga_q_cntrl<1>	
ROW1<3>	ifvga_q_cntrl<0>	
ROW1<2>	not used	ROW1<2:0> = xxx - not used
ROW1<1>	not used	
ROW1<0>	not used	

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12

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Table 9. Transmitter Register Array Assignments

Register Array Row & Bit	Internal Signal Name	Signal Function
ROW2		
ROW2<7>	FDB<11>	Factory Diagnostics; ROW2<7:4> = 1111 for normal operation
ROW2<6>	FDB<10>	
ROW2<5>	FDB<9>	
ROW2<4>	FDB<8>	
ROW2<3>	pa_sel_vgbs<3>	Controls the regulator for the base voltage of the PA output transistors; ROW2<3:0> = 0000 for normal operation
ROW2<2>	pa_sel_vgbs<2>	
ROW2<1>	pa_sel_vgbs<1>	
ROW2<0>	pa_sel_vgbs<0>	
ROW3		
ROW3<7>	FDB<7>	Factory Diagnostics; ROW4<7:4> = 0001 for normal operation
ROW3<6>	FDB<6>	
ROW3<5>	FDB<5>	
ROW3<4>	FDB<4>	
ROW3<3>	FDB<3>	Factory Diagnostics; ROW4<3:0> = 1111 for normal operation
ROW3<2>	FDB<2>	
ROW3<1>	FDB<1>	
ROW3<0>	FDB<0>	
ROW4		
ROW4<7>	pa_sel_vref<3>	Controls the bias current for the PA output transistors; ROW4<7:4> = 0011 for normal operation
ROW4<6>	pa_sel_vref<2>	
ROW4<5>	pa_sel_vref<1>	
ROW4<4>	pa_sel_vref<0>	
ROW4<3>	driver_bias<2>	Controls the bias current for the PA predriver; ROW4<3:1> = 111 for normal operation
ROW4<2>	driver_bias<1>	
ROW4<1>	driver_bias<0>	
ROW4<0>	driver_bias2<2>	Controls the bias current for the PA predriver2; ROW4<0> = 1 for normal operation
ROW5		
ROW5<7>	not used	ROW5<7:4> = x - not used
ROW5<6>	not used	
ROW5<5>	not used	
ROW5<4>	not used	
ROW5<3>	bg_monitor_sel	These bits are for reserved for diagnostic purposes; ROW5<3:2> = 01 for normal operation
ROW5<2>	if_refsel	
ROW5<1>	enable_fm	Active high to enable the FSK/MSK modulator inputs. ROW5<1> = 0 for normal I/Q operation
ROW5<0>	not used	ROW5<0> = x - not used
ROW6		
ROW6<7>	ifvga_bias<3>	Controls the bias current of the IF variable gain amplifier; ROW6<7:4> = 1000 for normal operation
ROW6<6>	ifvga_bias<2>	
ROW6<5>	ifvga_bias<1>	
ROW6<4>	ifvga_bias<0>	

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13

v02.0514

Table 9. Transmitter Register Array Assignments

Register Array Row & Bit	Internal Signal Name	Signal Function
ROW6<3>	ifvga_tune<3>	Controls the tuning of the IF filter for the variable gain amplifier; ROW6<3:0> = 1111 for normal operation
ROW6<2>	ifvga_tune<2>	
ROW6<1>	ifvga_tune<1>	
ROW6<0>	ifvga_tune<0>	
ROW7		
ROW7<7>	ifvga_vga_adj<3>	IF variable gain amplifier gain control bits; ROW7<7:4> = 0000 is highest gain 1101 is lowest gain Attenuation is ≈ 1.3 dB / step, ≈ 17 dB maximum
ROW7<6>	ifvga_vga_adj<2>	
ROW7<5>	ifvga_vga_adj<1>	
ROW7<4>	ifvga_vga_adj<0>	
ROW7<3>	if_upmixer_tune<3>	Controls the tuning of the IF filter for the IF to RF upmixer; ROW7<3:0> = 1111 for normal operation
ROW7<2>	if_upmixer_tune<2>	
ROW7<1>	if_upmixer_tune<1>	
ROW7<0>	if_upmixer_tune<0>	
ROW8		
ROW8<7>	tripler_bias<13>	These bits control the biasing of the frequency tripler; ROW8<7:0> = 10111111 for normal operation
ROW8<6>	tripler_bias<12>	
ROW8<5>	tripler_bias<11>	
ROW8<4>	tripler_bias<10>	
ROW8<3>	tripler_bias<9>	
ROW8<2>	tripler_bias<8>	
ROW8<1>	tripler_bias<7>	
ROW8<0>	tripler_bias<6>	
ROW9		
ROW9<7>	tripler_bias<5>	These bits control the biasing of the frequency tripler; ROW9<7:2> = 011011 for normal operation
ROW9<6>	tripler_bias<4>	
ROW9<5>	tripler_bias<3>	
ROW9<4>	tripler_bias<2>	
ROW9<3>	tripler_bias<1>	
ROW9<2>	tripler_bias<0>	
ROW9<1>	driver_bias2<1>	Controls the bias current for the PA predriver2; ROW9<1:0> = 11 for normal operation
ROW9<0>	driver_bias2<0>	
ROW10		
ROW10<7>	RDACIN<5>	VCO amplitude adjustment DAC; ROW10<7:2> = 111100 for normal operation
ROW10<6>	RDACIN<4>	
ROW10<5>	RDACIN<3>	
ROW10<4>	RDACIN<2>	
ROW10<3>	RDACIN<1>	
ROW10<2>	RDACIN<0>	
ROW10<1>	SYNRESET	ROW10<1> = 0 for normal operation

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Table 9. Transmitter Register Array Assignments

Register Array Row & Bit	Internal Signal Name	Signal Function
ROW10<0>	DIVRATIO<4>	ROW10<0> Control the synthesizer divider ratio and output frequency. Refer to Tables 10 and 11 for synthesizer control details.
ROW11		
ROW11<7>	DIVRATIO<3>	ROW11<7:4> Control the synthesizer divider ratio and output frequency. Refer to Tables 10 and 11 for synthesizer control details.
ROW11<6>	DIVRATIO<2>	
ROW11<5>	DIVRATIO<1>	
ROW11<4>	DIVRATIO<0>	
ROW11<3>	BAND<2>	ROW11<3:1> Control the VCO band, and must be changed when tuning the synthesizer output frequency. Refer to Tables 10 and 11 for synthesizer control details.
ROW11<2>	BAND<1>	
ROW11<1>	BAND<0>	
ROW11<0>	REFSELDIV	These bits are for reserved for diagnostic purposes; ROW11<0> = 1 for normal operation
ROW12		
ROW12<7>	CPBIAS<2>	These bits control the synthesizer charge pump bias. ROW12<7:5> = 010 for normal operation
ROW12<6>	CPBIAS<1>	
ROW12<5>	CPBIAS<0>	
ROW12<4>	VRSEL<3>	These bits control the width of the lock window for the synthesizer lock detector. ROW12<4:1> = 1111 specifies the widest lock window for normal operation
ROW12<3>	VRSEL<2>	
ROW12<2>	VRSEL<1>	
ROW12<1>	VRSEL<0>	
ROW12<0>	REFSELVCO	This bit is for reserved for diagnostic purposes; ROW12<0> = 1 for normal operation
ROW13		
ROW13<7>	MUXREF	These bit are reserved for diagnostic purposes; ROW13<7> = 1 for normal operation
ROW13<6>	DIV4	ROW13<6> = 0 for normal operation
ROW13<5>	ENDC	Active high to enable DC coupling on synthesizer reference input; ROW13<5> = 0 for normal operation
ROW13<4>	INI	This bit is for reserved for diagnostic purposes; ROW13<4> = 0 for normal operation
ROW13<3>	PDDIV12	Active high to power down 1.2V circuits in synthesizer divider
ROW13<2>	PDDIV27	Active high to power down 2.7V circuits in synthesizer divider
ROW13<1>	PDQP	Active high to power down synthesizer charge pump
ROW13<0>	PDVCO	Active high to power down synthesizer VCO
ROW14		
ROW14<7>	PDCAL	Active high to power down VCO calibration comparators; ROW14<7> = 0 for normal operation
ROW14<6>	MUXOUT	Controls multiplexing of diagnostic bits, high to read Row15<7:0> ROW14<6> = 1 for normal operation
ROW14<5>	PDALC12	Active high to power down VCO automatic level control (ALC); ROW14<5> = 1 for normal operation
ROW14<4>	PLOAD	Active high to load external amplitude adjustment bits for VCO ROW14<4> = 1 for normal operation

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15

Table 9. Transmitter Register Array Assignments

Register Array Row & Bit	Internal Signal Name	Signal Function
ROW14<3>	WIDE<1>	Control bits for VCO ALC loop;
ROW14<2>	WIDE<0>	ROW14<3:2> = 01 for normal operation
ROW14<1>	SLEW<1>	Controls slew rate in sub-integer N divider
ROW14<0>	SLEW<0>	ROW14<1:0> = 10 for normal operation
ROW15		
ROW15<7>	COMPP	Read only bits to indicate synthesizer lock: ROW15<7:6> = 01 indicates that the VCO control voltage is within the lock window and the synthesizer is locked.
ROW15<6>	COMPN	11 indicates the VCO control voltage above lock window 00 below lock window 10 is a disallowed state indicating an error
ROW15<5>	RDACMSB<2>	
ROW15<4>	RDACMSB<1>	These bits are read only and reserved for factory diagnostic purposes.
ROW15<3>	RDACMSB<0>	
ROW15<2>	RDACMUX<0>	
ROW15<1>	RDACMUX<1>	These bits are read only and reserved for factory diagnostic purposes.
ROW15<0>	RDACMUX<2>	

Synthesizer Settings

Table 10. IEEE Channels Using 308.5714 MHz Reference

Frequency (GHz)	Divider Setting	Typical Band Setting
57.24	10101	001
57.78	10100	001
58.32 (IEEE CH 1)	10011	010
58.86	10010	010
59.40	10001	011
59.94	10000	011
60.48 (IEEE CH 2)	11111	100
61.02	00000	100
61.56	00001	101
62.10	00010	101
62.64 (IEEE CH 3)	00011	110
63.18	00100	110
63.72	00101	111

Divide Ratio settings consist of registers ROW10 bit <0> (MSB) and ROW11 bits <4:7> (4 LSBs)

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16

Table 11. 500 MHz Channels Using 285.7143 MHz Reference

Frequency (GHz)	Divider Setting	Typical Band Setting
57	00001	000
57.5	00010	000
58	00011	001
58.5	00100	001
59	00101	010
59.5	00110	010
60	00111	011
60.5	01000	011
61	01001	100
61.5	01010	100
62	01011	101
62.5	01100	101
63	01101	110
63.5	01110	110
64	01111	111

Divide Ratio settings consist of registers ROW10 bit <0> (MSB) and ROW11 bits <4:7> (4 LSBs)

Table 12. Typical IF VGA and IF Upmixer Filter Settings

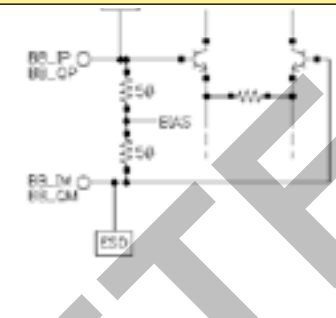| Frequency (GHz)	IF VGA Filter Setting (ifvga_tune)	IF UPMIXER Filter Setting (if_upmixer_tune)
57-60	1000	1010
60-62	1011	1111
62-64	1111	1111

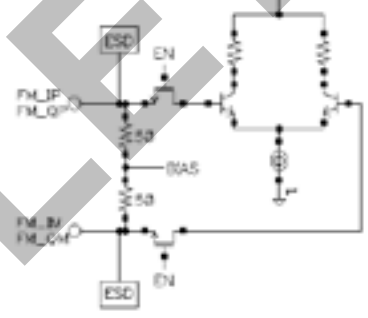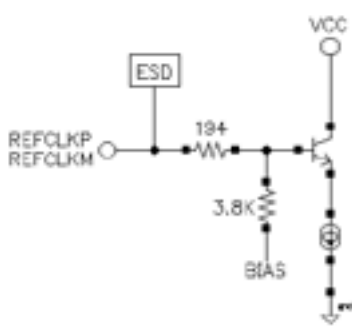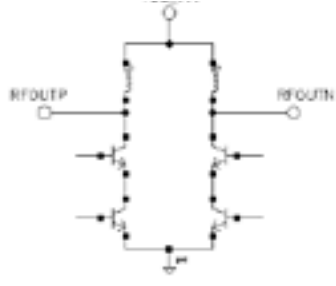*if_vga_tune settings consist of registers ROW6 bit <3:0> (4 MSBs)*
if_upmixer_tune settings consist of registers ROW7 <3:0> (4 MSBs)

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17

Table 13. Pad Discriptions

Item	Function	Pad Description	Interface Schematic
12,14,18,20	BB_QM BB_QP BB_IM BB_IP	Pads are DC coupled, matched to 50Ω (100Ω differential)	
22,23,25,26	FM_QM FM_QP Fm_IM FM_IP	Pads are DC coupled, matched to 50Ω (100Ω differential)	
31,33	REFCLKM REFCLKP	Pads are DC coupled, matched to 50Ω (100Ω differential)	
3,4	RFOUTM RFOUTP	Pads are DC coupled, matched to 50Ω (100Ω differential)	

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18

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Table 14. Evaluation Kit Order Information

Item	Part Number	Description
1	EKIT01-HMC6450	60 GHz Antenna in Package Transceiver Evaluation Kit

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19

v02.0514

Mounting & Bonding Techniques for Millimeterwave SiGe Die

The die should be attached directly to the ground plane with conductive epoxy (see HMC general Handling, Mounting, Bonding Note).

Handling Precautions

Follow these precautions to avoid permanent damage.

Storage: All bare die are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

Static Sensitivity: Follow ESD precautions to protect against ESD strikes.

Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.

General Handling: Handle the chip along the edges with a sharp pair of bent tweezers or use a top side vacuum tool to pick and place. The surface should not be touched with tweezers or fingers.

Mounting

The chip should be mounted with electrically conductive epoxy. The mounting surface should be clean and flat.

Epoxy Die Attach: Apply a minimum amount of epoxy to the mounting surface so that a fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer's recommendation.

Wire Bonding

RF bonds made with 0.003" (0.076mm) x 0.0005" (0.012mm) ribbon are recommended and should be thermosonically bonded. DC bonds of 0.001" (0.025 mm) diameter are recommended and should also be thermosonically bonded. All bonds should be made with a nominal stage temperature of 150 °C. A minimum amount of ultrasonic energy should be applied to achieve reliable bonds. All bonds should be as short as possible.

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20