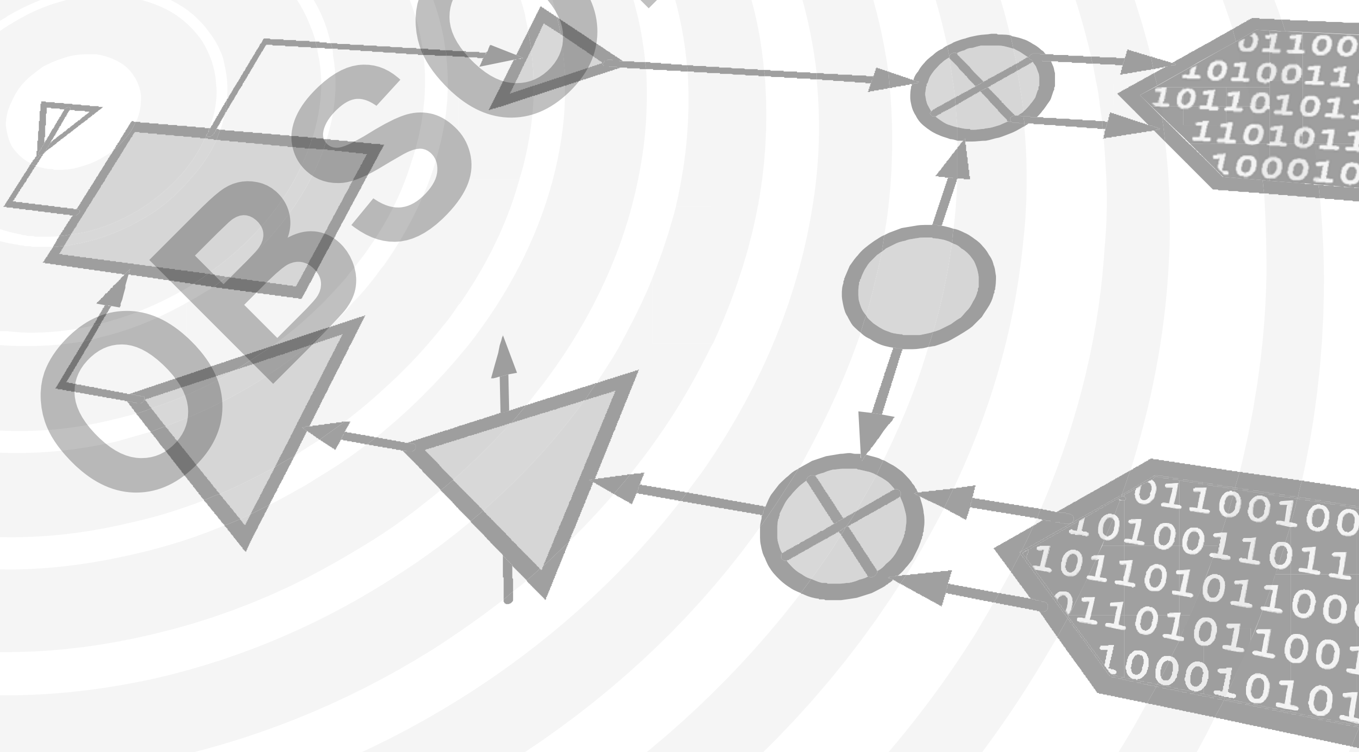
Analog Devices Welcomes Hittite Microwave Corporation



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MILLIMETERWAVE RECEIVER IC
57 - 64 GHz

Typical Applications

The HMC6001 is ideal for:

- WiGig Single Carrier Modulations
- 60 GHz ISM Band Data Transmitter
- Multi-Gbps Data Communications
- High Definition Video Transmission
- RFID

Features

Support for IEEE Channel Plan

Receiver Gain: 2 - 67 dB

Noise Figure: 6.0 dB

Integrated Image Reject Filter

Integrated Frequency Synthesizer

Programmable IF Gain Blocks

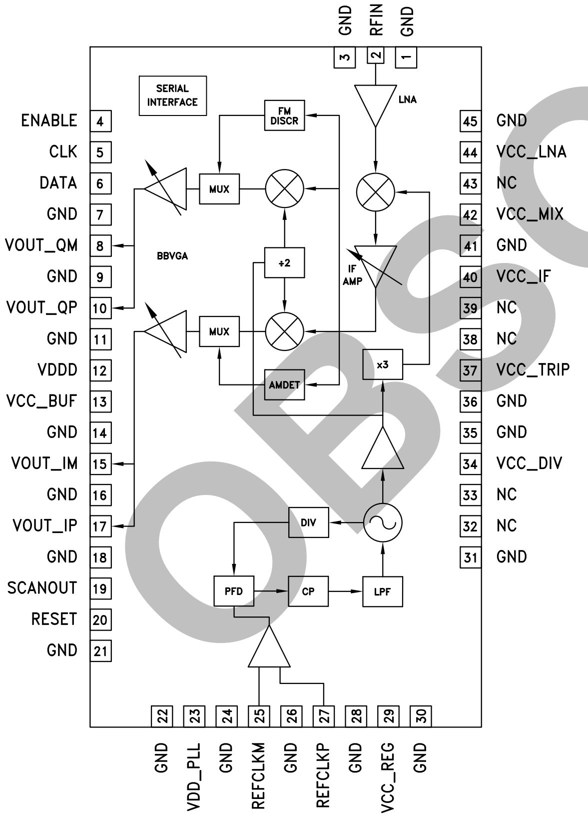
Universal Analog I/Q Baseband Interface

Integrated AM and FM Demodulator

Three-Wire Serial Digital Interface

Die Size: 3.452 x 1.852 mm

Functional Diagram



General Description

The HMC6001 is a complete mmWave super-heterodyne receiver chip including LNA, image reject filter, RF to IF downconverter, IF filter, I/Q downconverter, and frequency synthesizer. The receiver operates from 57 to 64 GHz with up to 1.8 GHz of double sided modulation bandwidth. An integrated synthesizer provides tuning in 500 or 540 MHz step sizes depending on the choice of external reference clock. Support for a wide variety of modulation formats is provided through a universal analog baseband IQ interface. The receiver chip supports all single carrier WiGig modulations and optionally supports dedicated FSK/MSK modulation formats for lower cost and lower power serial data links without the need for high speed data converters. LNA and adjustable gain IF stages provide 6 dB typical noise figure with AGC support. Together with the HMC6000, a complete transmit/receive chipset is provided for multi-Gbps operation in the unlicensed 60 GHz ISM band.

Table 1. Electrical Specifications, TA = +25° C, See Test Conditions

Parameter	Condition	Min.	Typ.	Max.	Units
Frequency Range		57		64	GHz
Frequency Step Size	308.5714 MHz Ref Clk		0.54		GHz
Frequency Step Size	285.714 MHz Ref Clk		0.50		GHz
Modulation Bandwidth	Max BW setting, 5dB BW, double-sided		1.8		GHz
Max Gain	Pout of all 4 baseband outputs minus Pin	63	67	69	dB
Gain Control Range			65		dB
Gain Step Size			1		dB
Gain Change Settling Time			3		µs
Noise Figure (<57.5 GHz)	at Max Gain	6	7	8	dB
Noise Figure (>57.5 GHz)	at Max Gain	5	6	7	dB
Input IP3	at Min Gain		-27		dBm
Input P1dB	at Min Gain		-36		dBm
Image Rejection			>35		dB
Sideband Suppression		14	27		dBc
Phase Noise @ 100 kHz			-72		dBc/Hz
Phase Noise @ 1 MHz			-86		dBc/Hz
Phase Noise @ 10 MHz			-111		dBc/Hz
Phase Noise @ 100 MHz			-125		dBc/Hz
Phase Noise @ 1 GHz			-127		dBc/Hz
PLL Loop BW	Internal Loop Filter		200		kHz
Synthesizer Settling Time			< 6		µs
Power Dissipation			0.610		W

Table 2. Test Conditions

Reference frequency	308.5714 MHz
Temperature	+25°C
Gain Setting	Max
Input Signal Level	-65 dBm
IF Bandwidth	Max
Input Impedance	50Ω Single-Ended
Output Impedance	100Ω Differential

Table 3. Recommended Operation Conditions

Description	Symbol	Min	Typical	Max	Units
Analog Ground	GND		0		Vdc
Power Supplies	VCC_BUF VCC_REG VCC_IF VCC_TRIP VCC_DIV VCC_MIX VCC_LNA	2.565	2.7	2.835	Vdc
	VDDD VDD_PLL	1.3	1.35	1.48	Vdc
Input Voltage Ranges					
Serial Digital Interface – Logic High	DATA ENABLE CLK RESET	0.9	1.2	1.4	V
Serial Digital Interface – Logic Low	DATA ENABLE CLK RESET	-0.05	0.1	0.3	V
Reference Clock	REFCLKP REFCLKM		3.3 or 2.5V LVPECL/LVDS 1.2V CMOS		V
Baseband I and Q [1]	BB_IM BB_IP BB_QM BB_QP	10	50	200	mVp-p
Baseband I and Q Common Mode [4]			1.3		V
Temperature		-40		+85	C

[1] Baseband voltage at each of the 4 baseband outputs

[2] DC voltage present at all 4 baseband outputs

Table 4. Power Consumption

Voltage	Typical Current (mA)	Typical Power Consumption (Watts)
VCC_BUF (2.7Vdc)	67	0.60
VCC_REG (2.7Vdc)	13	
VCC_IF (2.7Vdc)	37	
VCC_TRIP (2.7Vdc)	47	
VCC_DIV (2.7Vdc)	34	
VCC_MIX (2.7Vdc)	15	
VDD_LNA (2.7Vdc)	11	
VDDD (1.35Vdc)	1	0.01
VDD_PLL (1.35Vdc)	7	

Figure 1. Gain vs. Frequency Across Voltage[1]

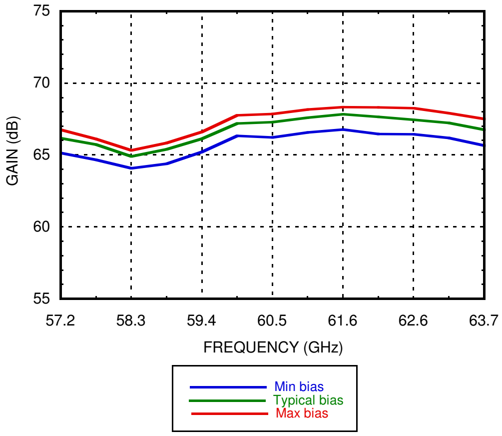


Figure 2. Gain vs. Frequency Over Temperature[1]

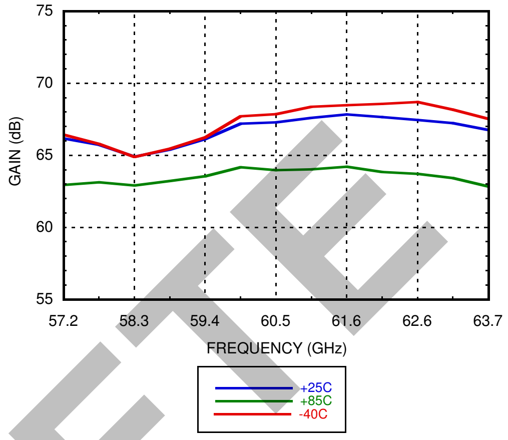


Figure 3. Noise Figure vs. Gain @ 60.48GHz[2]

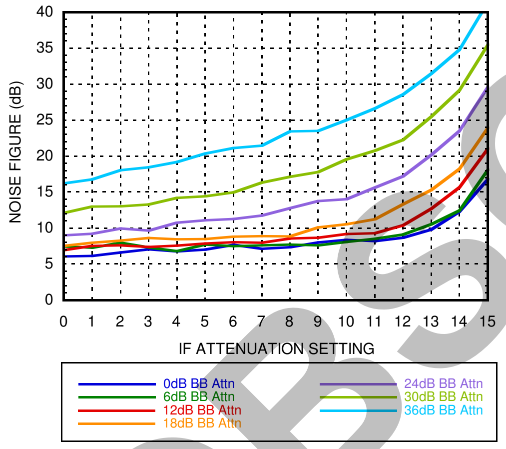


Figure 4. Noise Figure vs. Frequency Over Temperature[1]

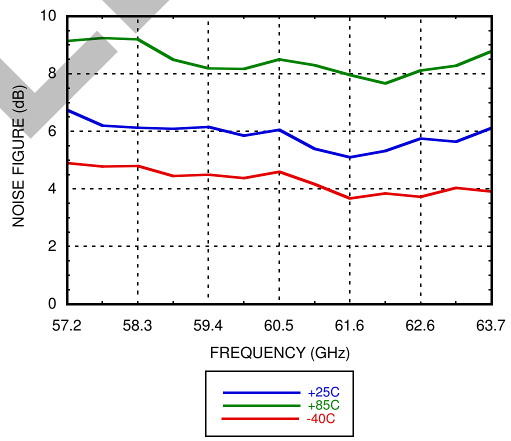


Figure 5. Noise Figure vs. Frequency Across Voltage[1]

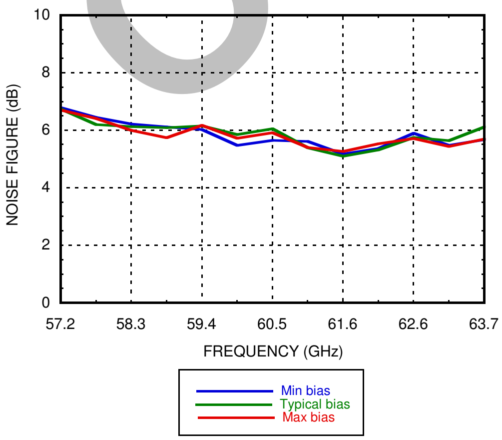
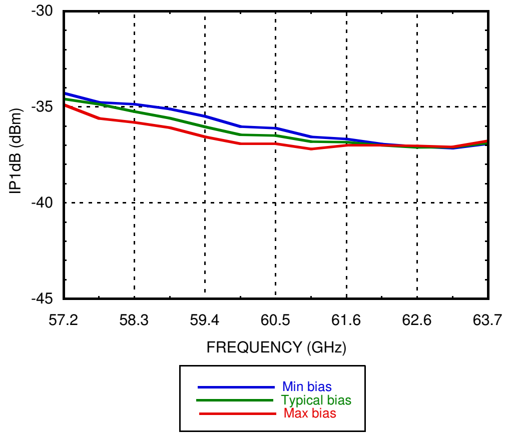


Figure 6. Input P1dB vs. Frequency Across Voltage[1]



[1] Maximum gain setting
[2] Fine BB Attn = 0dB

Figure 7. Input P1dB vs. Frequency Over Temperature[1]

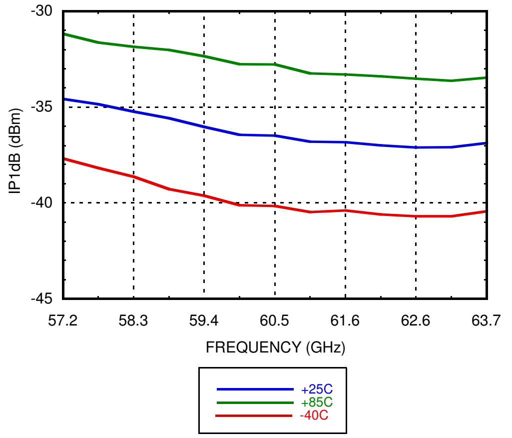


Figure 8. Input P1dB vs. Frequency and Gain

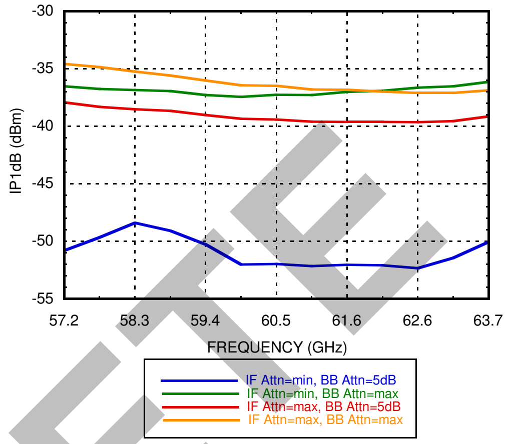


Figure 9. Input IP3 vs. Frequency Across Voltage[1]

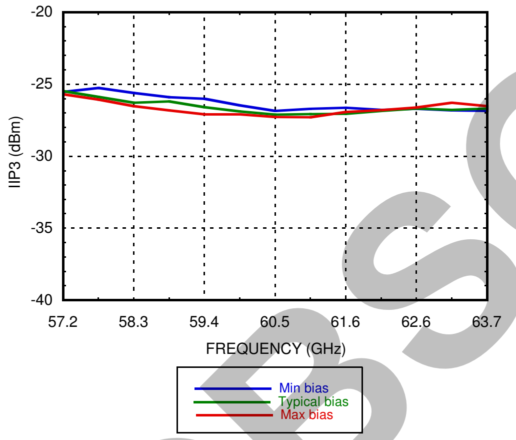


Figure 10. Input IP3 vs. Frequency Over Temperature[1]

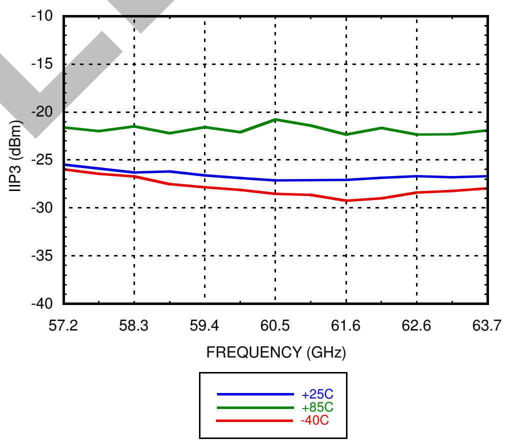


Figure 11. Input IP3 vs. Gain @ 60.48 GHz[2]

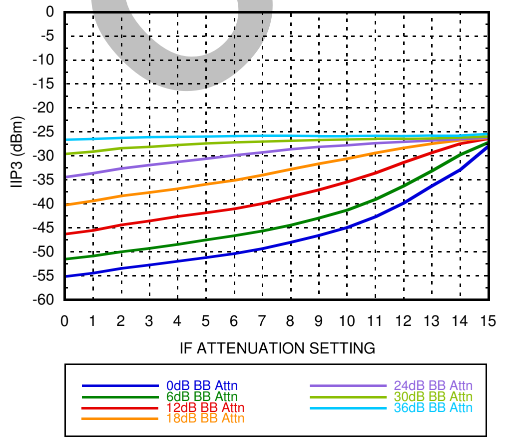
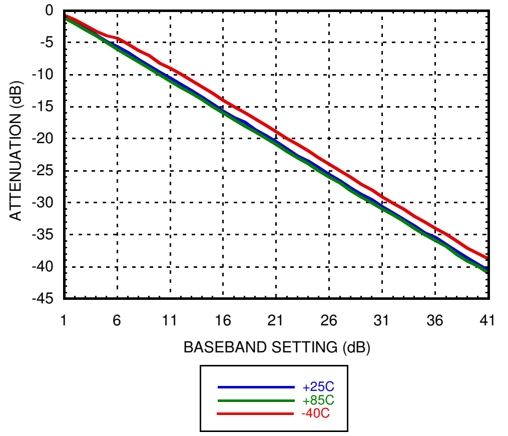


Figure 12. Baseband Attenuation Over Temperature



[1] Maximum gain setting
[2] Fine BB Attn = 0dB

Figure 13. IF Attenuation vs. Attenuator Setting vs Frequency

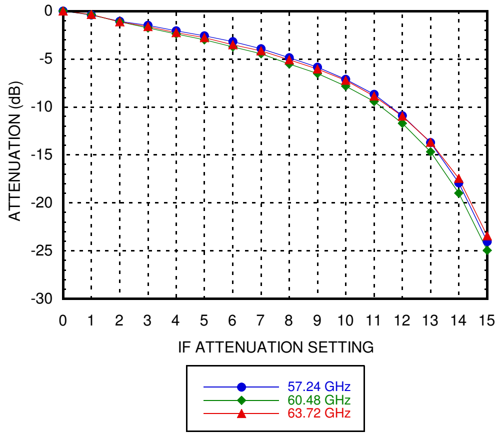


Figure 14. IF Attenuation vs. Attenuator Setting over Temperature[3]

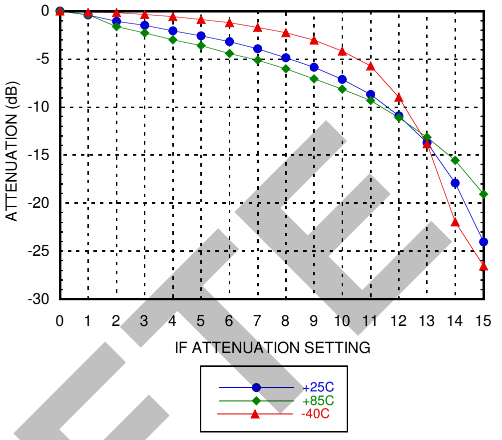


Figure 15. Single Sided Passband Response vs. Voltage[4]

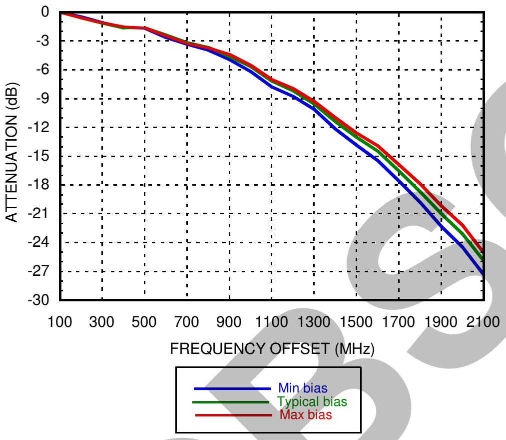


Figure 16. Single Sided Passband Response vs. Temperature[4]

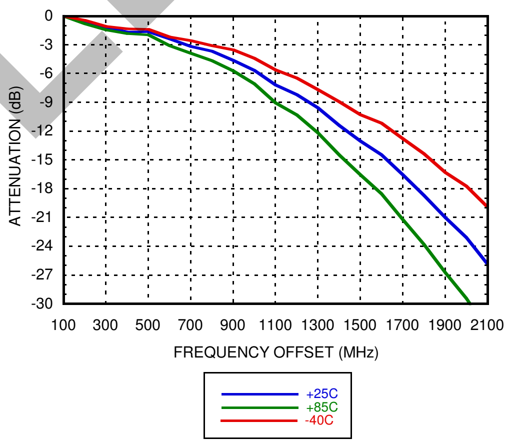


Figure 17. Single Sided Passband Response vs. IF Gain[4]

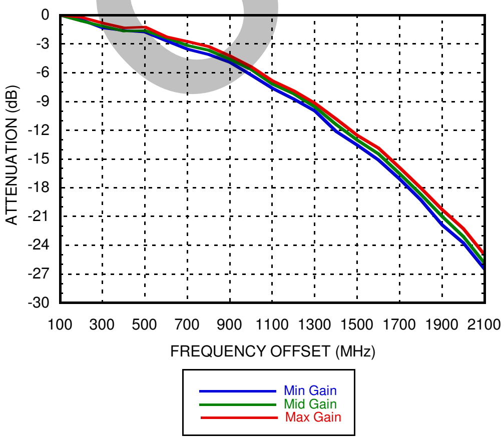
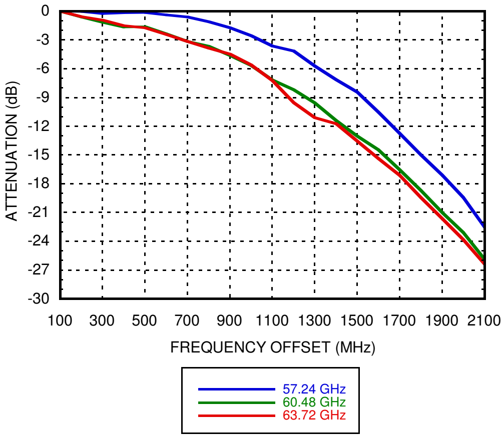


Figure 18. Single Sided Passband Response vs. Frequency[5]



[3] 60.48 GHz Carrier

[4] 60.48 GHz Carrier, Maximum BW

[5] Maximum BW

Figure 19. Single Sided Passband Response BW vs. BW Setting[3]

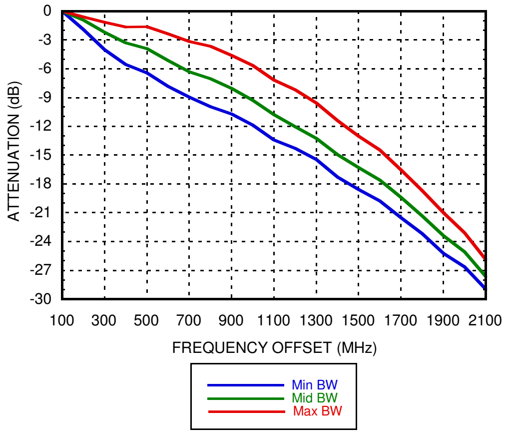


Figure 20. Single Sided High Pass Filter Response vs. HPF Setting[3]

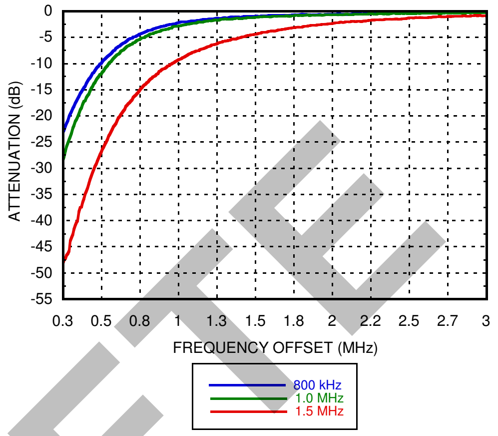


Figure 21. Single Sided High Pass Filter Response vs Temperature[6]

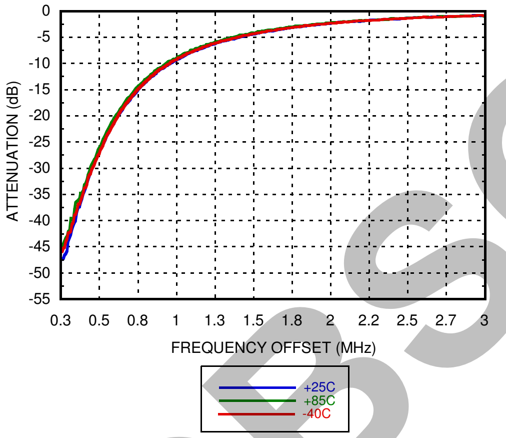


Figure 22. Sideband Suppression vs. Frequency across Voltage[1]

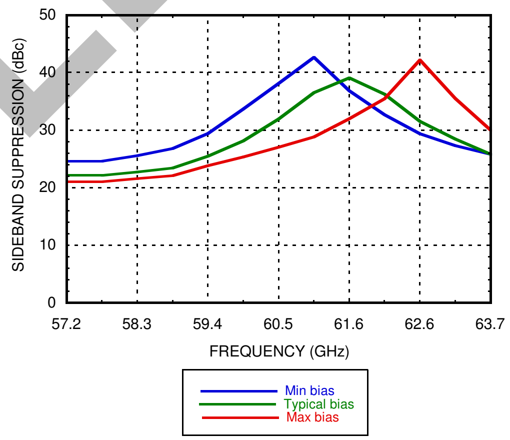


Figure 23. Sideband Suppression vs. Frequency over Temperature[1]

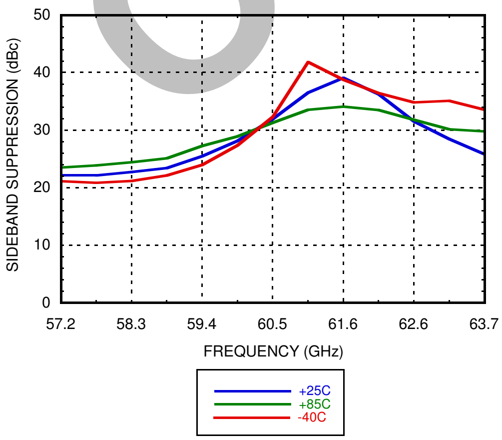
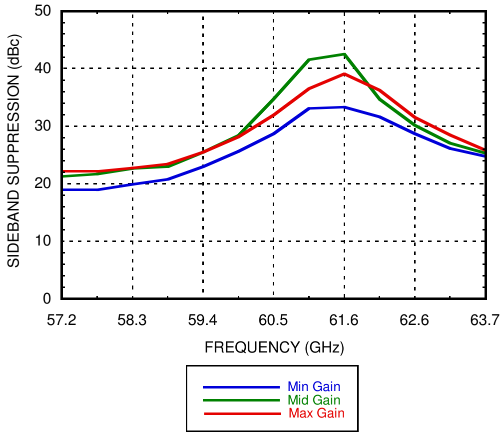


Figure 24. Sideband Suppression vs. Frequency and IF Gain



[1] Maximum gain setting
[3] 60.48 GHz Carrier
[6] 60.48 GHz Carrier, 1.5MHz HPF Setting

Figure 25. I/Q Amplitude and Phase during Fine Baseband Attenuator change[7]

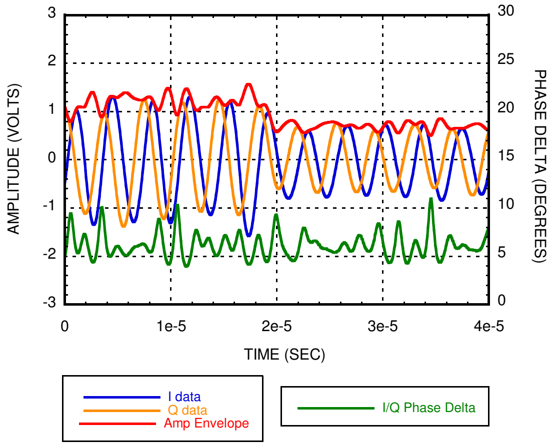


Figure 26. I/Q Amplitude and Phase during Coarse Baseband Attenuator change[8]

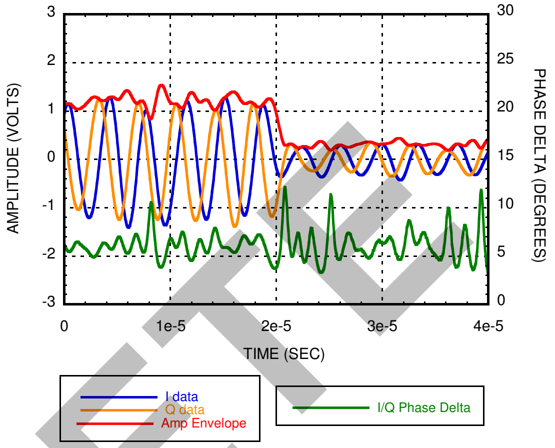
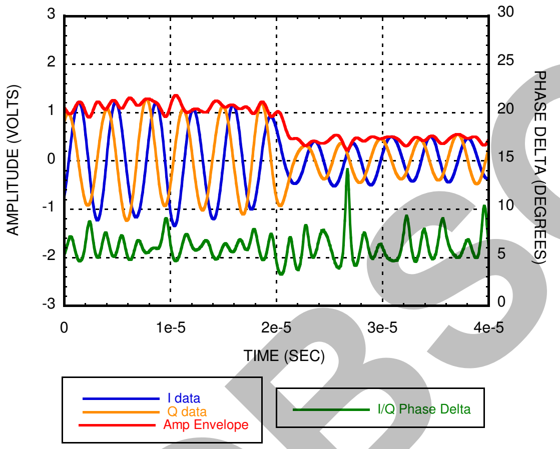


Figure 27. I/Q Amplitude and Phase during IF Attenuator change[9]

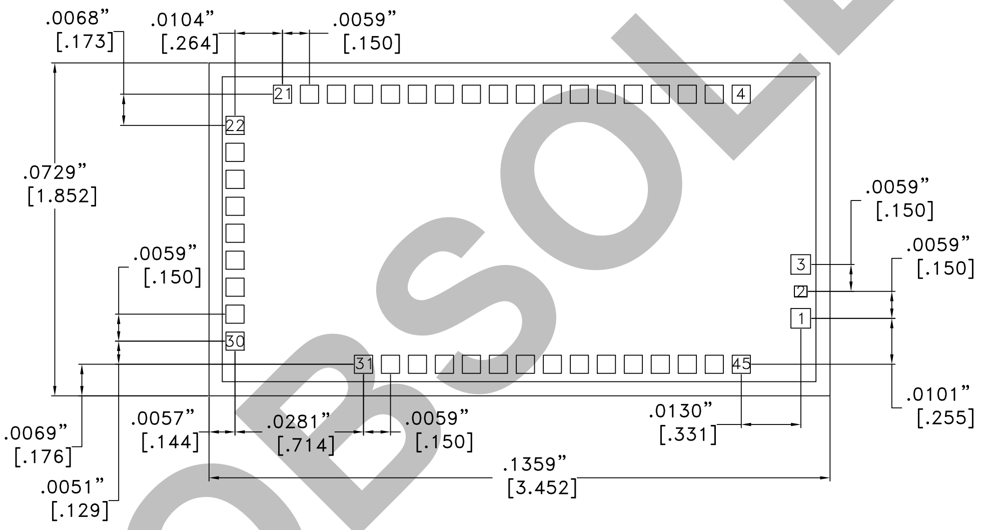


[7] 60.48 GHz Carrier, fine baseband attenuator change from 0 to 5dB
[8] 60.48 GHz Carrier, coarse baseband attenuator change from 12 to 24dB
[9] 60.48 GHz Carrier, IF attenuator change from setting 0 to 7

Table 5. Absolute Maximum Ratings

RF Input Power	0 dBm
RF DC Input	3.8 Vdc
VDD = 2.7 V	2.85 Vdc
VCC = 2.7 V	2.85 Vdc
VDD_PLL = 1.35 V	1.6 Vdc
VDDD = 1.35 V	1.6 Vdc
GND	0± 50 mV
Power Dissipation	0.760 W
Serial Digital Interface Input Voltage	1.5 Vdc
Ref CLK Input (AC coupled)(each)	0.75 Vp-p
Baseband Outputs (BB, FM)	0.75 Vp-p
Storage Temperature	-55°C to 150°C
Operating Temperature	-40°C to 85°C

Outline Drawing



NOTES:
1. ALL DIMENSIONS ARE IN INCHES [MM]
2. DIE THICKNESS IS .028" [0.711] +/- .001" [.025]
3. BOND PAD METALLIZATION: AL
4. OVERALL DIE SIZE ± .002 [0.051]

Table 6. Die Packaging Information

Standard	Alternate
VR-33CC-02-X4 GEL_PAK	[1]

[1] For alternate packaging information contact Hittite Microwave Corporation.

Table 7. Die Pad Dimensions

Pads	Pad Size	Pad Opening
1, 3	0.0043 [0.109] x 0.0043 [0.109]	0.0041 [0.103] x 0.0041 [0.103]
2	0.0028 [0.070] x 0.0024 [0.060]	0.0025 [0.064] x 0.0021 [0.054]
4 - 45	0.0040 [0.101] x 0.0040 [0.101]	0.0037 [0.095] x 0.0037 [0.095]

Table 8. Pad Descriptions

Pad Number	Function	Description
1, 3, 7, 9, 11, 14 16, 18, 21, 22, 24, 26, 28, 30, 31, 35, 36, 41, 45	GND	Analog Ground
2	RFIN	LNA input - AC coupled - matched to 50Ω
4	ENABLE	Serial digital interface enable (1.2V CMOS) - 50kΩ
5	CLK	Serial digital interface clock (1.2V CMOS) - 50kΩ
6	DATA	Serial digital interface data (1.2V CMOS) - 50kΩ
8	VOUT_QM	Baseband negative quadrature output – DC coupled 1.3Vcm - 50Ω
10	VOUT_QP	Baseband positive quadrature output – DC coupled 1.3Vcm - 50Ω
12	VDDD	1.35 supply (serial data interface)
13	VCC_BUF	2.7V supply (BB VGA and output buffers)
15	VOUT_IM	Baseband negative in-phase output – DC coupled 1.3Vcm - 50Ω
17	VOUT_IP	Baseband positive in-phase output – DC coupled 1.3Vcm - 50Ω
19	SCANOUT	Serial digital interface out (1.2V CMOS) - 50kΩ
20	RESET	Asynchronous reset-all registers (1.2V CMOS, active high) - 50kΩ
23	VDD_PLL	1.35 supply (VCO)
25	REFCLKM	Xtal REF CLK Minus - AC or DC coupled - 50Ω
27	REFCLKP	Xtal REF CLK Minus - AC or DC coupled - 50Ω
29	VCC_REG	2.7V supply (VCO)
32, 33, 38, 39, 43	NC	Factory test points. Leave floating. Do not connect.
34	VCC_DIV	2.7V supply (Divider)
37	VCC_TRIP	2.7V supply (Tripler)
40	VCC_IF	2.7V supply (IF)
42	VCC_MIX	2.7V supply (Mixer)
44	VCC_LNA	2.7V supply (LNA)

Theory of Operation

An integrated frequency synthesizer creates a low-phase noise LO between 16.3 and 18.3 GHz. The step size of the synthesizer equates to 540MHz steps at RF when used with 308.5714 MHz reference crystal (compatible with the IEEE channels of the ISM band) or 500 MHz steps if used with a 285.714 MHz reference crystal. A 57 to 64 GHz signal enters the chip through a single-ended LNA input. The LO is multiplied by three and mixed with the LNA output to downconvert to an 8 to 9.1 GHz sliding IF. An integrated notch filter removes the image frequency. The IF signal is filtered and amplified with 17 dB of variable gain. If the chip is configured for IQ baseband output, the IF signal is feds into a quadrature demodulator using the LO/2 to downconvert to baseband. There are also options to use on-chip demodulators capable of to demodulating AM/FM/FSK/MSK waveforms. Contact Hittite application support for further guidance and application notes if interested in these modes.

The phase noise and quadrature balance of the HMC6001 is sufficient to demodulate up to 16QAM modulation for high data rate operation.

There are no special power sequencing requirements for the HMC6001; all voltages are to be applied simultaneously.

Register Array Assignments and Serial Interface

The register arrays for both the receiver and transmitter are organized into 16 rows of 8 bits. Using the serial interface, the arrays are written or read one row at a time as shown in Figure 28 and Figure 29, respectively. Figure 28 shows the sequence of signals on the ENABLE, CLK, and DATA lines to write one 8-bit row of the register array. The ENABLE line goes low, the first of 18 data bits (bit 0) is placed on the DATA line, and 2 ns or more after the DATA line stabilizes, the CLK line goes high to clock in data bit 0. The DATA line should remain stable for at least 2 ns after the rising edge of CLK.

The Rx IC will support a serial interface running up to several hundred MHz, and the interface is 1.2V CMOS levels. A write operation requires 18 data bits and 18 clock pulses, as shown in Figure 29. The 18 data bits contain the 8-bit register array row data (LSB is clocked in first), followed by the register array row address (ROW0 through ROW15, 000000 to 001111, LSB first), the Read/Write bit (set to 1 to write), and finally the Rx chip address 111, LSB first).

Note that the register array row address is 6 bits, but only four are used to designate 16 rows, the two MSBs are 0.

After the 18th clock pulse of the write operation, the ENABLE line returns high to load the register array on the IC; prior to the rising edge of the ENABLE line, no data is written to the array. The CLK line should have stabilized in the low state at least 2 ns prior to the rising edge of the ENABLE line.

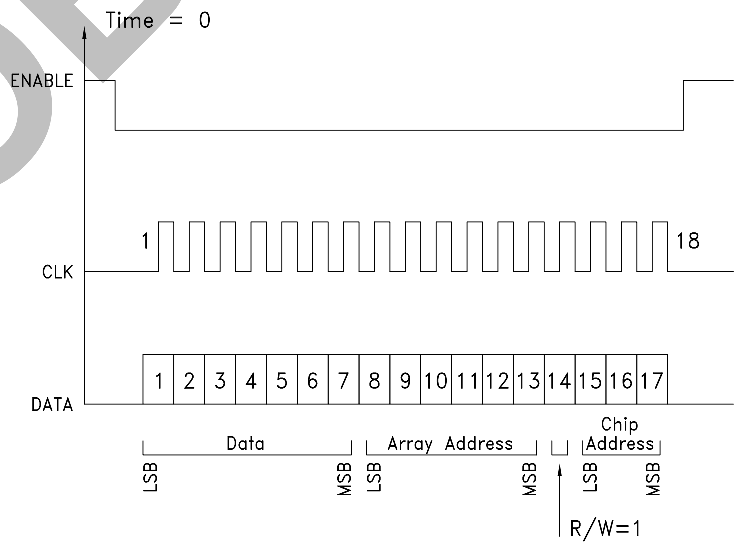


Figure 28. *Timing Diagram for writing a row of the Receiver Serial Interface*

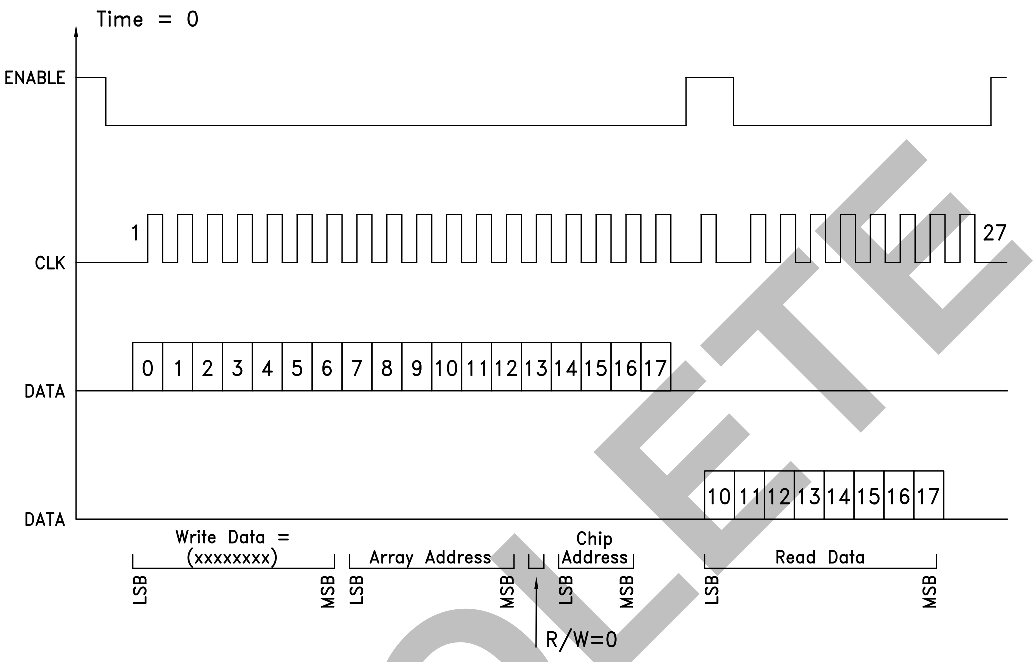


Figure 29. *Timing Diagram for reading a row of the Receiver Serial Interface*

Table 9. Receiver Register Array Assignments

Register Array Row & Bit	Internal Signal Name	Signal Function
ROW0		
ROW0<7>	ask_pwrdn	Active high to power down ASK demodulator
ROW0<6>	bbamp_pwrdn_i	Active high to power down I-channel baseband amplifier
ROW0<5>	bbamp_pwrdn_q	Active high to power down Q-channel baseband amplifier
ROW0<4>	divider_pwrdn	Active high to power down local oscillator divider
ROW0<3>	if_bgmux_pwrdn	Active high to power down one of three on-chip bandgap refs (IF) and associated mux
ROW0<2>	ifmix_pwrdn_i	Active high to power down I-channel IF to baseband mixer
ROW0<1>	ifmix_pwrdn_q	Active high to power down Q-channel IF to baseband mixer
ROW0<0>	ifvga_pwrdn	Active high to power down IF variable gain amplifier
ROW1		
ROW1<7>	ipc_pwrdn	Active high to power down on chip current reference generator
ROW1<6>	lna_pwrdn	Active high to power down low noise amplifier and reference
ROW1<5>	rfmix_pwrdn	Active high to power down RF to IF mixer
ROW1<4>	tripler_pwrdn	Active high to power down frequency tripler
ROW1<3>	bbamp_atten1_0	First baseband attenuator; ROW1<2:3> = 11 is 18 dB attenuation 10 is 12 dB attenuation 01 is 6 dB attenuation 00 is 0 dB attenuation
ROW1<2>	bbamp_atten1_1	

Table 9. Receiver Register Array Assignments

Register Array Row & Bit	Internal Signal Name	Signal Function
ROW1<1>	bbamp_atten2_0	Second baseband attenuator; ROW1<0:1> = 11 is 18 dB attenuation 10 is 12 dB attenuation 01 is 6 dB attenuation 00 is 0 dB attenuation
ROW1<0>	bbamp_atten2_1	
ROW2		
ROW2<7>	bbamp_attenfi_0	I Channel baseband fine attenuator; ROW2<5:7> ≥ 101 is 5 dB attenuation 100 is 4 dB attenuation 011 is 3 dB attenuation 010 is 2 dB attenuation 001 is 1 dB attenuation 000 is 0 dB attenuation
ROW2<6>	bbamp_attenfi_1	
ROW2<5>	bbamp_attenfi_2	
ROW2<4>	bbamp_attenfq_0	Q Channel baseband fine attenuator; ROW2<2:4> ≥ 101 is 5 dB attenuation 100 is 4 dB attenuation 011 is 3 dB attenuation 010 is 2 dB attenuation 001 is 1 dB attenuation 000 is 0 dB attenuation
ROW2<3>	bbamp_attenfq_1	
ROW2<2>	bbamp_attenfq_2	
ROW2<1>	bbamp_selask	Active high to multiplex the AM detector output into the I channel baseband amplifier input
ROW2<0>	bbamp_sigshort	Active high to short the input to the I and Q channel baseband amplifiers
ROW3		
ROW3<7>	bbamp_selbw0	Selects the low pass corner of the baseband amplifiers; ROW3<6:7> = 00 is ≈ 1.4 GHz 01 is ≈ 500 MHz 10 is ≈ 300 MHz 11 is ≈ 200 MHz
ROW3<6>	bbamp_selbw1	
ROW3<5>	bbamp_selfastrec	Selects the high pass corner of the baseband amplifiers; ROW3<4:5> = 00 is ≈ 800 kHz 01 is ≈ 1 MHz 10 is ≈ 1.5 MHz
ROW3<4>	bbamp_selfastrec2	
ROW3<3>	bg_monitor_sel<1>	These bits are for reserved for diagnostic purposes; ROW3<3:0> = 0011 for normal operation
ROW3<2>	bg_monitor_sel<0>	
ROW3<1>	if_refsel	
ROW3<0>	lna_refsel	
ROW4		

Table 9. Receiver Register Array Assignments

Register Array Row & Bit	Internal Signal Name	Signal Function
ROW4<7>	ifvga_bias<2>	These bits are for biasing and IF filter alignment in the IF variable gain amplifier; ROW4<7:0> = 1001111x for normal operation
ROW4<6>	ifvga_bias<1>	
ROW4<5>	ifvga_bias<0>	
ROW4<4>	ifvga_tune<4>	
ROW4<3>	ifvga_tune<3>	
ROW4<2>	ifvga_tune<2>	
ROW4<1>	ifvga_tune<1>	
ROW4<0>	not used	
ROW5		
ROW5<7>	ifvga_vga_adj<3>	IF variable gain amplifier gain control bits; ROW5<7:4> = 0000 is highest gain 1111 is lowest gain Attenuation is ≈ 1 dB / step, ≈ 20 dB maximum
ROW5<6>	ifvga_vga_adj<2>	
ROW5<5>	ifvga_vga_adj<1>	
ROW5<4>	ifvga_vga_adj<0>	
ROW5<3>	rfmix_tune<4>	These bits control IF filter alignment in the RF mixer; ROW5<3:0> = 1111 for normal operation
ROW5<2>	rfmix_tune<3>	
ROW5<1>	rfmix_tune<2>	
ROW5<0>	rfmix_tune<1>	
ROW6		
ROW6<7>	tripler_bias<13>	These bits control the biasing of the frequency tripler; ROW6<7:0> = 10111111 for normal operation
ROW6<6>	tripler_bias<12>	
ROW6<5>	tripler_bias<11>	
ROW6<4>	tripler_bias<10>	
ROW6<3>	tripler_bias<9>	
ROW6<2>	tripler_bias<8>	
ROW6<1>	tripler_bias<7>	
ROW6<0>	tripler_bias<6>	
ROW7		
ROW7<7>	tripler_bias<5>	These bits control the biasing of the frequency tripler; ROW7<7:2> = 011011 for normal operation
ROW7<6>	tripler_bias<4>	
ROW7<5>	tripler_bias<3>	
ROW7<4>	tripler_bias<2>	
ROW7<3>	tripler_bias<1>	
ROW7<2>	tripler_bias<0>	
ROW7<1>	bbamp_selfm	Active high to multiplex the FM detector output into the Q channel baseband amplifier input
ROW7<0>	fm_pwrdn	Active high to power down FM demodulator
ROW8		
ROW8<7>	lna_bias<2>	These bits control biasing of the low noise amplifier; ROW8<7:5> = 100 for normal operation
ROW8<6>	lna_bias<1>	
ROW8<5>	lna_bias<0>	

Table 9. Receiver Register Array Assignments

Register Array Row & Bit	Internal Signal Name	Signal Function
ROW8<4>	not used	ROW8<4:3> = xx - not used
ROW8<3>	not used	
ROW8<2>	ifvga_q_cntrl<2>	These bits control the Q of the IF filter in the IF variable gain amplifier; ROW8<2:0> = 000 for highest Q and highest gain. To reduce Q and widen bandwidth, increment ROW8<2:0> in the sequence: 001 100 101 111
ROW8<1>	ifvga_q_cntrl<1>	
ROW8<0>	ifvga_q_cntrl<0>	
ROW9		
ROW9<7>	not used	ROW9<7:0> = xxxxxxxx - not used
ROW9<6>	not used	
ROW9<5>	not used	
ROW9<4>	not used	
ROW9<3>	not used	
ROW9<2>	not used	
ROW9<1>	not used	
ROW9<0>	not used	
ROW10		
ROW10<7>	RDACIN<5>	VCO amplitude adjustment DAC; ROW10<7:2> = 111100 for normal operation
ROW10<6>	RDACIN<4>	
ROW10<5>	RDACIN<3>	
ROW10<4>	RDACIN<2>	
ROW10<3>	RDACIN<1>	
ROW10<2>	RDACIN<0>	
ROW10<1>	SYNRESET	ROW10<1> = 0 for normal operation
ROW10<0>	DIVRATIO<4>	ROW10<0> Control the synthesizer divider ratio and output frequency. Refer to Tables 10 and 11 for synthesizer control details
ROW11		
ROW11<7>	DIVRATIO<3>	ROW11<7:4> Control the synthesizer divider ratio and output frequency. Refer to Tables 10 and 11 for synthesizer control details.
ROW11<6>	DIVRATIO<2>	
ROW11<5>	DIVRATIO<1>	
ROW11<4>	DIVRATIO<0>	
ROW11<3>	BAND<2>	ROW11<3:1> Control the VCO band, and must be changed when tuning the synthesizer output frequency. Refer to Tables 10 and 11 for synthesizer control details.
ROW11<2>	BAND<1>	
ROW11<1>	BAND<0>	
ROW11<0>	REFSELDIV	These bits are for reserved for diagnostic purposes; ROW11<0> = 1 for normal operation
ROW12		
ROW12<7>	CPBIAS<2>	These bits control the synthesizer charge pump bias. ROW12<7:5> = 010 for normal operation
ROW12<6>	CPBIAS<1>	
ROW12<5>	CPBIAS<0>	

Table 9. Receiver Register Array Assignments

Register Array Row & Bit	Internal Signal Name	Signal Function
ROW12<4>	VRSEL<3>	These bits control the width of the lock window for the synthesizer lock detector. ROW12<4:1> = 1111 specifies the widest lock window for normal operation
ROW12<3>	VRSEL<2>	
ROW12<2>	VRSEL<1>	
ROW12<1>	VRSEL<0>	
ROW12<0>	REFSELVCO	This bit is reserved for diagnostic purposes; ROW12<0> = 1 for normal operation
ROW13		
ROW13<7>	MUXREF	This bit is reserved for diagnostic purposes; ROW13<7> = 1 for normal operation
ROW13<6>	DIV4	ROW13<6> = 0 for normal operation
ROW13<5>	ENDC	Active high to enable DC coupling on synthesizer reference input; ROW13<5> = 0 for normal operation
ROW13<4>	INI	This bit is reserved for diagnostic purposes; ROW13<4> = 0 for normal operation
ROW13<3>	PDDIV12	Active high to power down 1.2V circuits in synthesizer divider
ROW13<2>	PDDIV27	Active high to power down 2.7V circuits in synthesizer divider
ROW13<1>	PDQP	Active high to power down synthesizer charge pump
ROW13<0>	PDVCO	Active high to power down synthesizer VCO
ROW14		
ROW14<7>	PDCAL	Active high to power down VCO calibration comparators; ROW14<7> = 0 for normal operation
ROW14<6>	MUXOUT	Controls multiplexing of diagnostic bits, high to read Row15<7:0> ROW14<6> = 1 for normal operation
ROW14<5>	PDALC12	Active high to power down VCO automatic level control (ALC); ROW14<5> = 1 for normal operation
ROW14<4>	PLOAD	Active high to load external amplitude adjustment bits for VCO ROW14<4> = 1 for normal operation
ROW14<3>	WIDE<1>	Control bits for VCO ALC loop; ROW14<3:2> = 01 for normal operation
ROW14<2>	WIDE<0>	
ROW14<1>	SLEW<1>	Controls slew rate in sub-integer N divider ROW14<1:0> = 10 for normal operation
ROW14<0>	SLEW<0>	
ROW15		
ROW15<7>	COMPP	Read only bits to indicate synthesizer lock: ROW15<7:6> = 01 indicates that the VCO control voltage is within the lock window and the synthesizer is locked. 11 indicates the VCO control voltage above lock window 00 below lock window 10 is a disallowed state indicating an error
ROW15<6>	COMPN	
ROW15<5>	RDACMSB<2>	These bits are read only and reserved for factory diagnostic purposes.
ROW15<4>	RDACMSB<1>	
ROW15<3>	RDACMSB<0>	
ROW15<2>	RDACMUX<0>	These bits are read only and reserved for factory diagnostic purposes.
ROW15<1>	RDACMUX<1>	
ROW15<0>	RDACMUX<2>	

Synthesizer Settings

Table 10. IEEE Channels Using 308.5714 MHz Reference

Frequency (GHz)	Divider Setting	Typical Band Setting
57.24	10101	001
57.78	10100	001
58.32 (IEEE CH 1)	10011	010
58.86	10010	010
59.40	10001	011
59.94	10000	011
60.48 (IEEE CH 2)	11111	100
61.02	00000	100
61.56	00001	101
62.10	00010	101
62.64 (IEEE CH 3)	00011	110
63.18	00100	110
63.72	00101	111

Divide Ratio settings consist of registers ROW10 bit <0> (MSB) and ROW11 bits <4:7> (4 LSBs)

Table 11. 500 MHz Channels Using 285.7143 MHz Reference

Frequency (GHz)	Divider Setting	Typical Band Setting
57	00001	000
57.5	00010	000
58	00011	001
58.5	00100	001
59	00101	010
59.5	00110	010
60	00111	011
60.5	01000	011
61	01001	100
61.5	01010	100
62	01011	101
62.5	01100	101
63	01101	110
63.5	01110	110
64	01111	111

Divide Ratio settings consist of registers ROW10 bit <0> (MSB) and ROW11 bits <4:7> (4 LSBs)

Table 12. Pad Descriptions

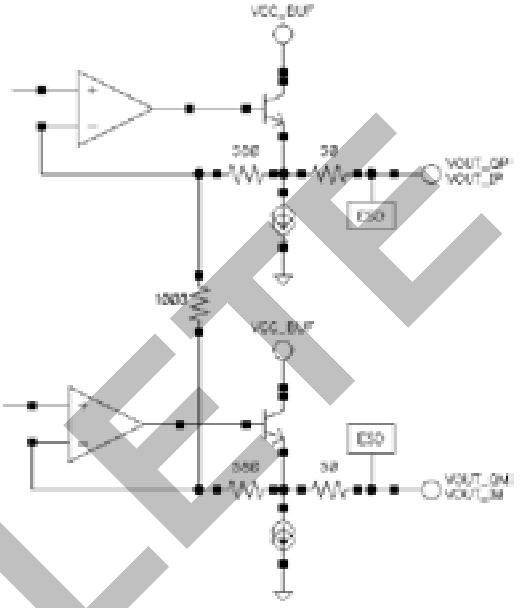
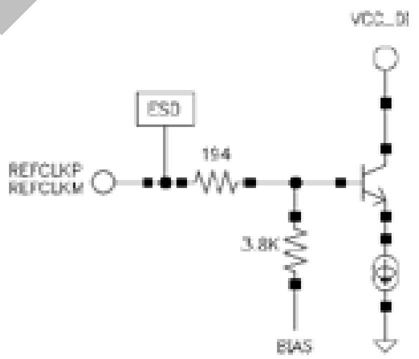
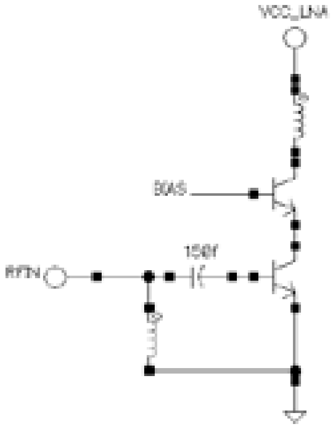
Item	Function	Pad Description	Interface Schematic
8, 10,13,15	VOUT_QM VOUT_QP VOUT_IM VOUT_IP	Pads are DC Coupled, matched to 50Ω (100Ω differential)	
25, 27	REFLKM REFCLKP	Pads are AC or DC coupled. matched to 50Ω (100Ω differential)	
2	RFIN	Pad is AC Coupled, matched to 50Ω	

Table 13. Evaluation Kit Order Options

Item	Part Number	Description
1	EKIT01-HMC6450	60 GHz Antenna in Package Transceiver Evaluation Kit

Mounting & Bonding Techniques for Millimeterwave SiGe Die

The die should be attached directly to the ground plane with conductive epoxy (see HMC general Handling, Mounting, Bonding Note).

Handling Precautions

Follow these precautions to avoid permanent damage.

Storage: All bare die are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

Static Sensitivity: Follow ESD precautions to protect against ESD strikes.

Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.

General Handling: Handle the chip along the edges with a sharp pair of bent tweezers or use a top side vacuum tool to pick and place. The surface should not be touched with tweezers or fingers.

Mounting

The chip should be mounted with electrically conductive epoxy. The mounting surface should be clean and flat.

Epoxy Die Attach: Apply a minimum amount of epoxy to the mounting surface so that a fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer's recommendation.

Wire Bonding

RF bonds made with 0.003” (0.076mm) x 0.0005” (0.012mm) ribbon are recommended and should be thermosonically bonded. DC bonds of 0.001” (0.025 mm) diameter are recommended and should also be thermosonically bonded. All bonds should be made with a nominal stage temperature of 150 °C. A minimum amount of ultrasonic energy should be applied to achieve reliable bonds. All bonds should be as short as possible.