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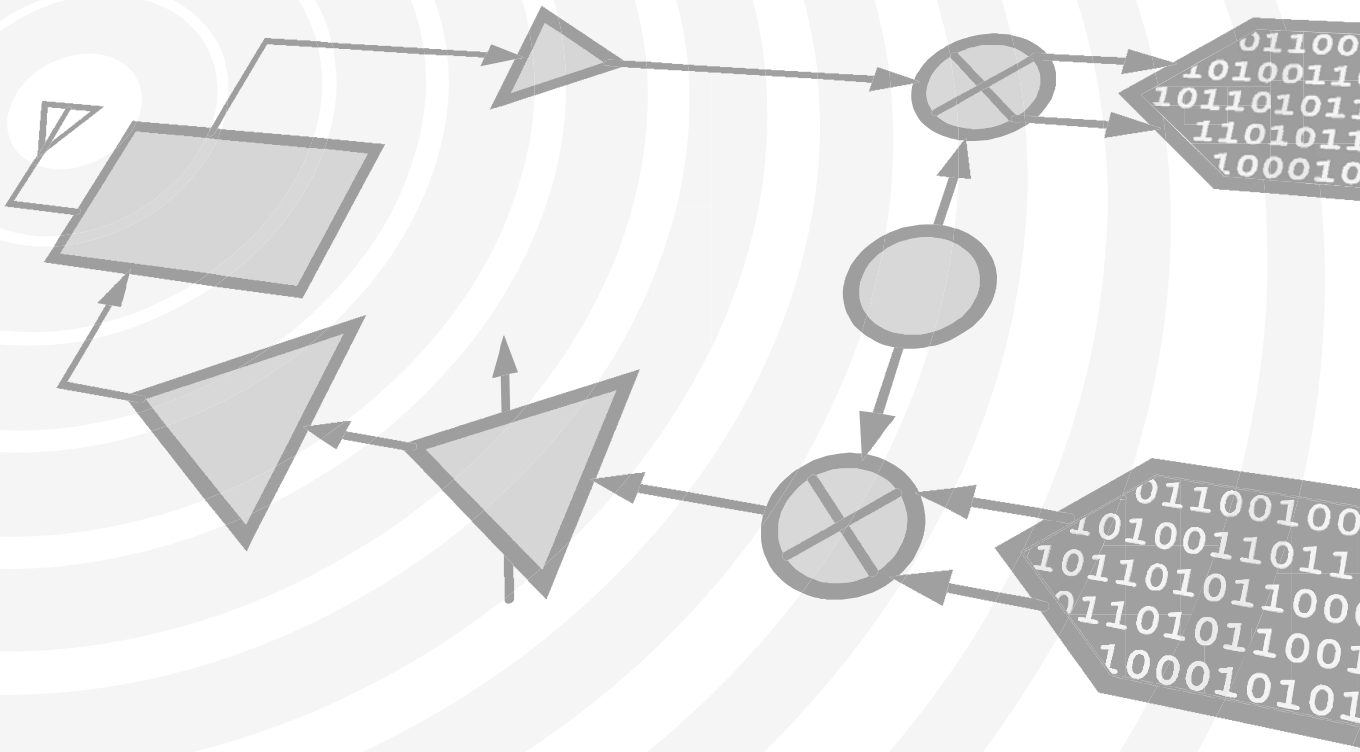

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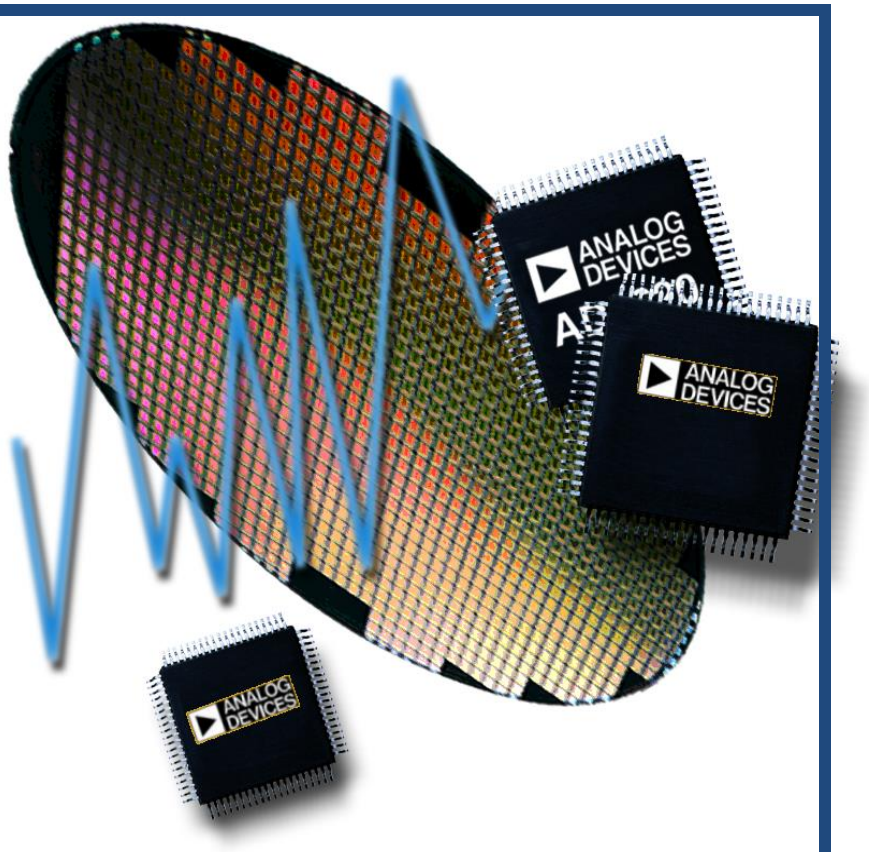

Reliability Report

Report Title: Qualification Test Report

Report Type: See Attached

Date: See Attached

Process FIT Rate Report

QTR: 2013-00500 **Rev: 05**

Wafer Process: PHEMT-K

HMC637A
HMC6981
HMC7091
HMC7144
HMC7150
HMC7229
HMC7441
HMC5XXX

Hittite MICROWAVE CORPORATION
20 Alpha Road, Chelmsford, MA 01824
Ph: 978.250.3343 Fax: 978.250.3373
www.hittite.com

Process FIT Rate Report

QTR: 2013-00500 **Rev: 05**

Wafer Process: PHEMT-K

Introduction

The testing performed for this report is designed to accelerate the predominant failure mode, electro-migration (EM), for the devices under test. The devices are stressed at high temperature and DC biased to simulate a lifetime of use at typical operating temperatures. Using the Arrhenius equation, the acceleration factor (AF) is calculated for the stress testing based on the stress temperature and the typical use operating temperature.

This report is intended to summarize all of the High Temperature Operating Life Test (HTOL) data for the PHEMT-K process. The FIT/MTTF data contained in this report includes all the stress testing performed on this process to date and will be updated periodically as additional data becomes available. Data sheets for the tested devices can be found at www.hittite.com.

Glossary of Terms & Definitions:

1. **CDM:** Charged Device Model. A specified ESD testing circuit characterizing an event that occurs when a device acquires charge through some triboelectric (frictional) or electrostatic induction processes and then abruptly touches a grounded object or surface. This test was performed in accordance with JEDEC 22-C101.
2. **ESD:** Electro-Static Discharge. A sudden transfer of electrostatic charge between bodies or surfaces at different electrostatic potentials.
3. **HBM:** Human Body Model. A specified ESD testing circuit characterizing an event that occurs when a device is subjected to an electro-static charge stored in the human body and discharged through handling of the electronic device. This test was performed in accordance with JEDEC 22-A114.
4. **HTOL:** High Temperature Operating Life. This test is used to determine the effects of bias conditions and temperature on semiconductor devices over time. It simulates the devices' operating condition in an accelerated way, through high temperature and/or bias voltage, and is primarily for device qualification and reliability monitoring. This test was performed in accordance with JEDEC JESD22-A108.
5. **HTSL:** High Temperature Storage Life. Devices are subjected to 1000 hours at 150ºC per JESD22-A103.
6. **MSL:** Moisture sensitivity level pre-conditioning is performed per JESD22-A113.
7. **Operating Junction Temp (T_{oj}):** Temperature of the die active circuitry during typical operation.
8. **Stress Junction Temp (T_{sj}):** Temperature of the die active circuitry during stress testing.
9. **UHAST:** Unbiased Highly Accelerated Stress Test. Devices are subjected to 96 hours of 85% relative humidity at a temperature of 130°C and pressure (15 PSIG). This test is performed in accordance with JESD22-A118.

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Qualification Sample Selection:

All qualification devices used were manufactured and tested on standard production processes and met pre-stress acceptance test requirements.

Summary of Qualification Tests:

HMC7150 (QTR2013-00338)

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial Electrical Test	356	356	Pass	
MSL-1 Preconditioning	160	160	Pass	
Post MSL-1 Electrical Test	160	160	Pass	
UHAST (Preconditioned)	80	80	Pass	
Post UHAST Electrical Test	80	80	Pass	
Temp. Cycle (Preconditioned)	80	80	Pass	
Post Temp Cycle Electrical Test	80	80	Pass	
HTSL	80	80	Pass	
Post HTSL Electrical Test	80	80	Pass	
HTOL	80	80	Pass	
Post HTOL Electrical test	80	80	Pass	
ESD Exposure	36	36	Pass	
Post ESD Electrical Test	36	36	Pass	HBM = Class 1A CDM = Passed 1500V MM = Passed 75V

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HMC7144 (QTR2013-00361)

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial Electrical Test	351	351	Pass	
MSL-1 Preconditioning	156	156	Pass	
Post MSL-1 Electrical Test	156	156	Pass	
UHAST (Preconditioned)	78	78	Pass	
Post UHAST Electrical Test	78	78	Pass	
Temp. Cycle (Preconditioned)	78	78	Pass	
Post Temp Cycle Electrical Test	78	78	Pass	
HTSL	78	78	Pass	
Post HTSL Electrical Test	78	78	Pass	
HTOL	81	81	Pass	
Post HTOL Electrical test	81	81	Pass	
ESD Exposure	36	36	Pass	
Post ESD Electrical Test	36	36	Pass	HBM = Class 1A CDM = Passed 1500V MM = Passed 75V

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HMC6981 (QTR2012-00517)

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial Electrical Test	267	267	Pass	
MSL-3 Preconditioning	80	80	Pass	
Post MSL-3 Electrical Test	80	80	Pass	
Temp. Cycle (Preconditioned)	80	80	Pass	
Post Temp Cycle Electrical Test	80	80	Pass	
HTSL	80	80	Pass	
Post HTSL Electrical Test	80	80	Pass	
HTOL	80	80	Pass	
Post HTOL Electrical test	80	80	Pass	
ESD Exposure	27	27	Pass	
Post ESD Electrical Test	27	27	Pass	HBM = Passed, 125V CDM = Passed 2000V

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HMC7091 (QTR2013-00071)

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial Electrical Test	80	80	Pass	
Post HTOL Electrical test	80	80	Pass	

HMC7441 (Q11662)

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial Electrical Test	225	225	Pass	
HTSL	90	90	Pass	2 lots of 45 units
Post HTSL Electrical Test	90	90	Pass	
HTOL	135	135	Pass	3 lots of 45 units
Post HTOL Electrical test	135	135	Pass	

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HMC5XXX (Q11814)

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial Electrical Test	396	396	Pass	
HTOL	231	231	Pass	3 Lots of 77 units
Post HTOL Electrical Test	231	231	Pass	
HTSL	135	135	Pass	3 Lots of 45 units
Post HTSL Electrical test	135	135	Pass	
ESD Exposure	30	30	Pass	
Post ESD Electrical Test	30	30	Pass	HBM = Passed 250V CDM = Passed 1000V

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PHEMT-K Failure Rate Estimate

Based on the HTOL test results, a failure rate estimation was determined using the following parameters:

With device back-side case temp, Tc = 85°C

HMC7150 (QTR2013-00338)
Operating Junction Temp (T_{oj}) = 96°C(369°K)
Stress Junction Temp (T_{sj}) = 175°C(448°K)

HMC7144 (QTR2013-00361)
Operating Junction Temp (T_{oj}) = 96°C(369°K)
Stress Junction Temp (T_{sj}) = 175°C(448°K)

HMC6981 (QTR2012-00517)
Operating Junction Temp (T_{oj}) = 136°C(409°K)
Stress Junction Temp (T_{sj}) = 160°C(433°K)

HMC7091 (QTR2013-00071)
Operating Junction Temp (T_{oj}) = 136°C(409°K)
Stress Junction Temp (T_{sj}) = 150°C(448°K)

HMC7441 (Q11662)
Operating Junction Temp (T_{oj}) = 133°C(406°K)
Stress Junction Temp (T_{sj}) = 150°C(423°K)

HMC5XXX (Q11814)
Operating Junction Temp (T_{oj}) = 140°C(413°K)
Stress Junction Temp (T_{sj}) = 175°C(448°K)

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Device hours:

HMC7150 (QTR2013-00338) = (80 X 1000hrs) = 80,000 hours
HMC7144 (QTR2013-00361) = (81 X 1000hrs) = 81,000 hours
HMC6981 (QTR2012-00517) = (80 X 1000hrs) = 80,000 hours
HMC7091 (QTR2013-00071) = (80 X 1000hrs) = 80,000 hours
HMC7441 (Q11662) = (135 X 1000hrs) = 135,000 hours
HMC5XXX (Q11814) = (231 X 1000hrs) = 231,000 hours

For PHEMT-K MMIC, Activation Energy = 1.43 eV

Acceleration Factor (AF): $$AF = \exp\left[\left(\frac{E_A}{k}\right)\cdot\left(\left(\frac{1}{T_{USE}}\right)-\left(\frac{1}{T_{STRESS}}\right)\right)\right]$$

HMC7150 (QTR2013-00338) Acceleration Factor = exp[1.43/8.6 e-5(1/369-1/448)] = 2824.9
HMC7144 (QTR2013-00361) Acceleration Factor = exp[1.43/8.6 e-5(1/369-1/448)] = 2824.9
HMC6981 (QTR2012-00517) Acceleration Factor = exp[1.43/8.6 e-5(1/409-1/433)] = 9.5
HMC7091 (QTR2013-00071) Acceleration Factor = exp[1.43/8.6 e-5(1/409-1/448)] = 3.8
HMC7441 (Q11662) Acceleration Factor = exp[1.43/8.6 e-5(1/406-1/433)] = 5.2
HMC5XXX (Q11814) Acceleration Factor = exp[1.43/8.6 e-5(1/413-1/448)] = 23.2

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Equivalent hours = Device hours x Acceleration Factor

Equivalent hours = (80,000x2824.9)+(81,000x2824.9)+(80,000x9.5)+(80,000x9.5)+(135,000x3.8)+(231,000x23.2) = 4.69×10^8 hours

Since there was no failures and we used a time terminated test, F=0, and R = 2F+2 = 2

The failure rate was calculated using Chi Square Statistic:

$$\lambda_{CL} = \frac{\chi^2_{\%CL,2f+2} \cdot 10^9}{2 \cdot t \cdot ss \cdot AF}$$ at 60% and 90% Confidence Level (CL), with 0 units out of spec and a 85°C device case temp;

Failure Rate

$\lambda_{60} = [(\chi^2)_{60,2}]/(2X \quad 4.69 \times 10^8 \quad)] = 1.8/ \quad 9.39 \times 10^8 = \quad 1.95 \times 10^{-9}$ failures/hour or 1.9 FIT or MTTF = 5.13×10^8 Hours

$\lambda_{90} = [(\chi^2)_{90,2}]/(2X \quad 4.69 \times 10^8 \quad)] = 4.6/ \quad 9.39 \times 10^8 = \quad 4.91 \times 10^{-9}$ failures/hour or 4.9 FIT or MTTF = 2.04×10^8 Hours

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