

D

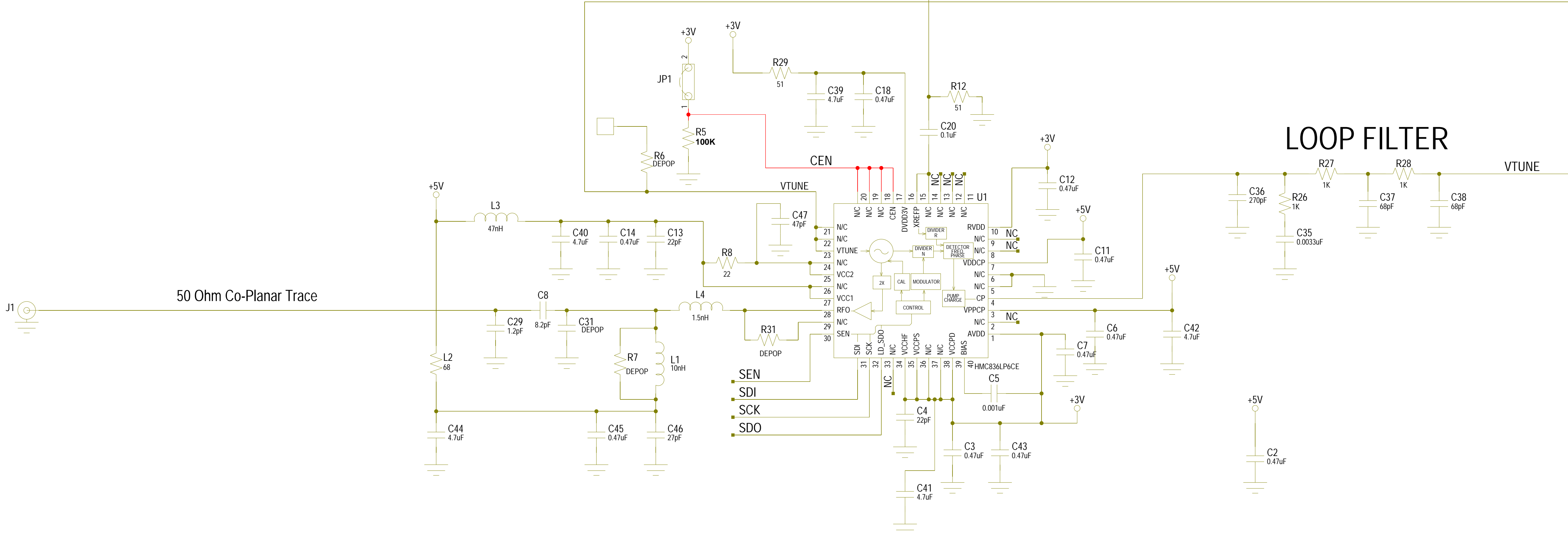
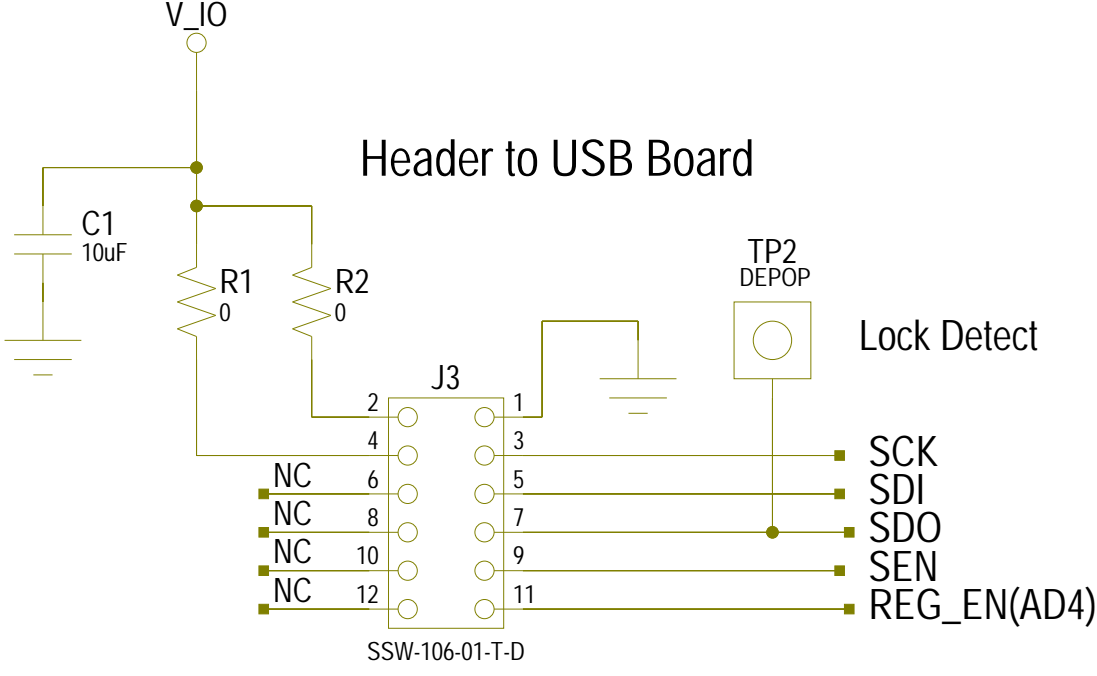
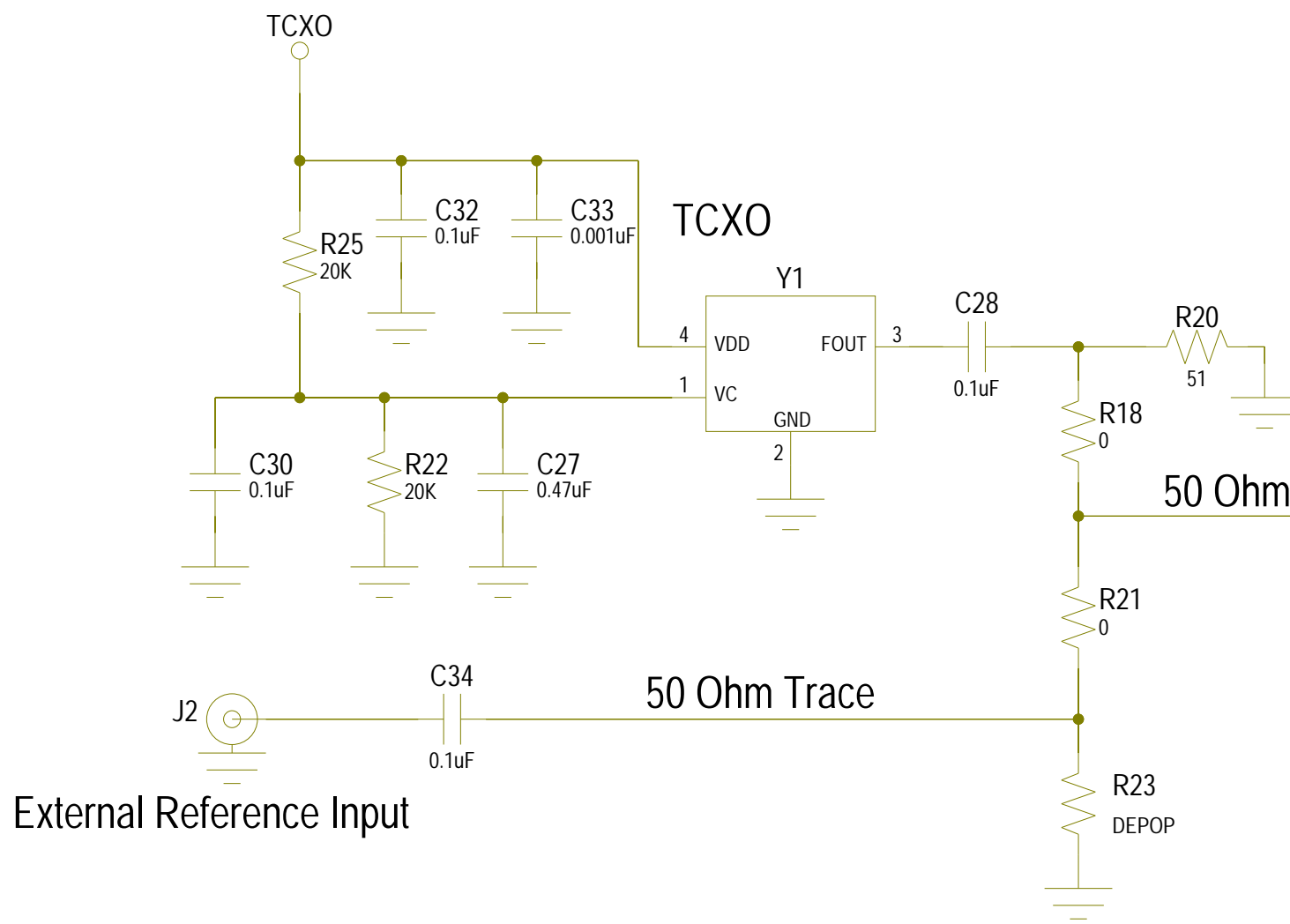
C

B

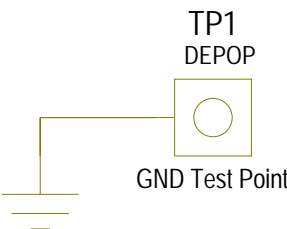
A


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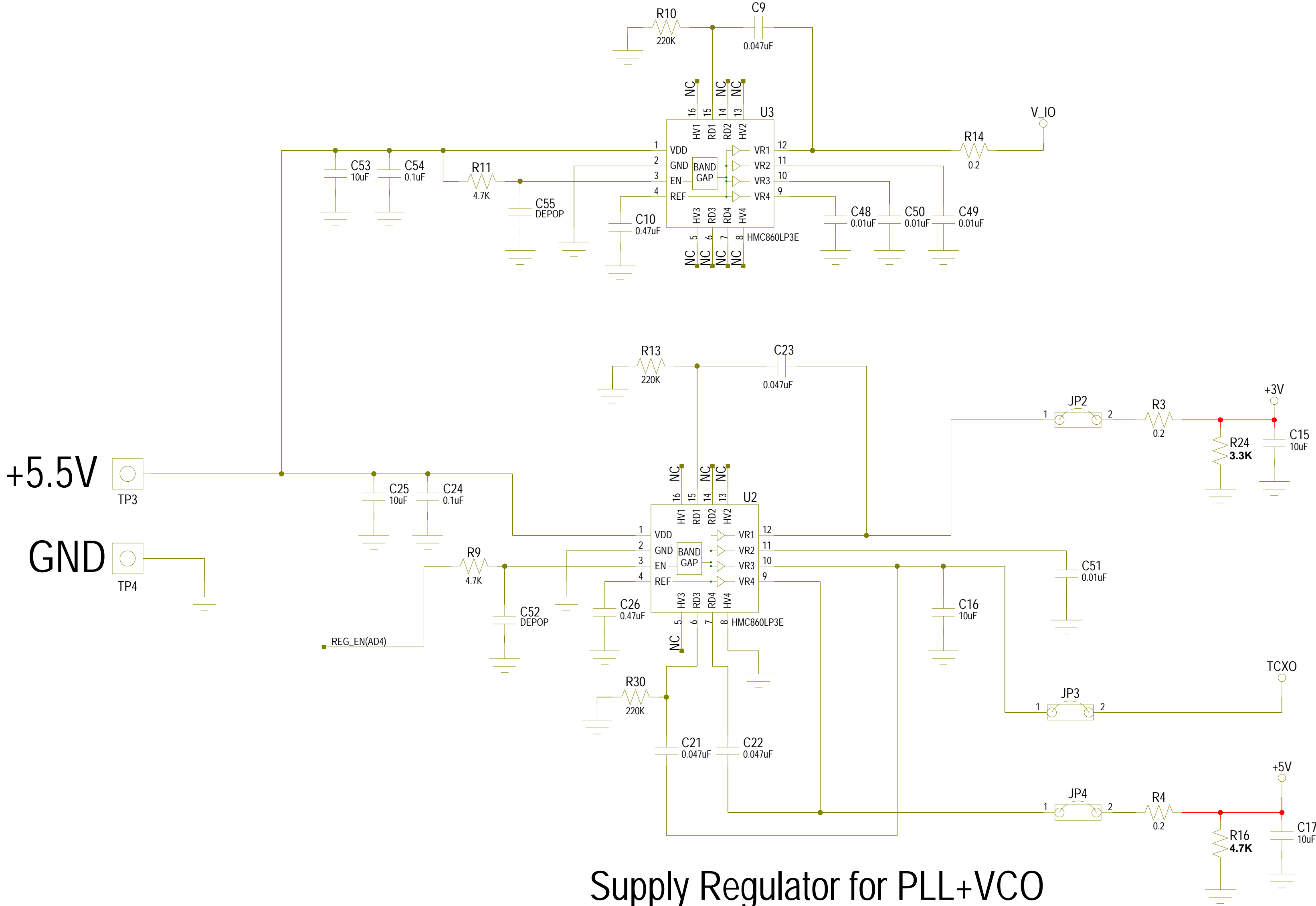
REVISIONS					
REV	ECN#	ZONE	DESCRIPTION	NAME	DATE
A	20100115	PRODUCTION RELEASE PER ECN 20100115	D. YOUNG	24/01/10
B	CP121275	PRODUCTION CHANGE PER CP 121275	V. VADUVA	09/14/2012



HMC836LP6CE Integrated PLL & VCO Eval



 HITTITE MICROWAVE CORPORATION 20 Alpha Rd Chelmsford, MA 01824					
TITLE SCH, CUSTOMER EVALALUATION PLL & VCO					
PROJECT					
DRAWING #: 129272			SHEET CODE ID NO. 1CN88		1 OF 2 SIZE D
DRAWN BY D.YOUNG		DATE 10/01/2010		REV B	



A recommended design practice is to connect the regulator Enable Pin #3 through a 4.7kOhm resistor to the system microcontroller/FPGA for power management control
Small series resistors required in VR1 and VR4 output paths, as shown