REVISIONS					
REV	ECN#	ZONE	DESCRIPTION	NAME	DATE
A	20100319	-----	ENGINEERING RELEASE ECN 20100319	D. YOUNG	2010/03/09
B	CP121275	-----	ENGINEERING RELEASE CP121275	V. VADUVA	09/14/2012

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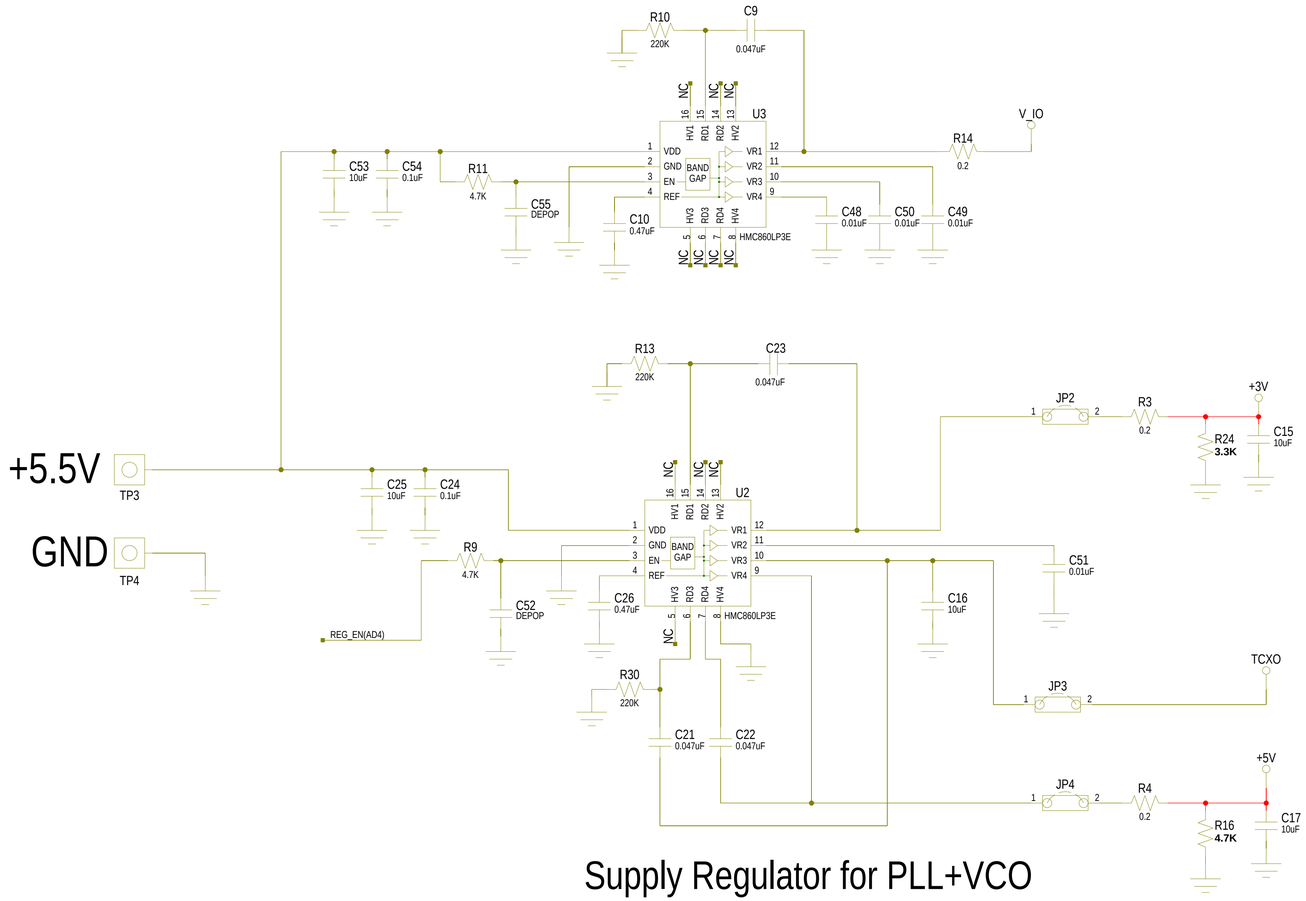
TCXO
R25 20K
C32 0.1uF
C33 0.001uF
TCXO
Y1
VDD
VC
FOUT
GND
4
1
3
2
C28 0.1uF
R20 51
R18 0
C30 0.1uF
R22 20K
C27 0.47uF
50 Ohm Co-Planar Trace
R21 0
R19 0
R17 DEPOP 0
R15 0
J2
C34 0.1uF
50 Ohm Trace
External Reference Input
R23 51 DEPOP

V_IO
C1 10uF
R1 0
R2 0
Header to USB Board
TP2 DEPOP
Lock Detect
J3
SCK
SDI
SDO
SEN
REG_EN(AD4)
NC
SSW-106-01-T-D

+3V
+3V
JP1
R29 51
C39 4.7uF
C18 0.47uF
R12 51
C20 0.1uF
R5 100K
R6 DEPOP
CEN
VTUNE
+5V
L3 47nH
C40 4.7uF
C14 0.47uF
C13 22pF
C47 47pF
R8 0
J1
50 Ohm Co-Planar Trace
C8 8.2pF
C29 1pF
C31 DEPOP
L4 1nH
R31 0
L2 47nH
R7 DEPOP
L1 10nH
C44 4.7uF
C45 0.47uF
C46 27pF
SEN
SDI
SCK
SDO
U1
HMC838LP6CE
N/C
VTUNE
VCC2
VCC1
RF_N
RF_P
SEN
SDI
SCK
LD_SDO
VCDHF
VCDPS
VCDPD
BIAS
DVDD3V
XREFP
RVDD
VDDCP
VPPCP
AVDD
CP
DIVIDER R
DIVIDER N
DETECTOR FREQ. PHASE
OR 2X /2 /1
CAL
MODULATOR
PUMP CHARGE
CONTROL
C4 22pF
C5 0.001uF
C41 4.7uF
C3 0.47uF
C43 0.47uF
C12 0.47uF
C11 0.47uF
C6 0.47uF
C7 0.47uF
C42 4.7uF
C2 0.47uF
+5V
+3V
LOOP FILTER
R27 1K
R28 1K
R26 1K
C36 270pF
C37 68pF
C38 68pF
C35 0.0033uF
TP1 DEPOP
GND Test Point

HMC838 2xFo
Integrated PLL & VCO
Eval

HITTITE MICROWAVE CORPORATION	20 Alpha Rd Chelmsford, MA 01824
TITLE	SCH, CUSTOMER EVALUATIONC PLL & VCO 2 X FO
PROJECT	
DRAWING #:	129506
DRAWN BY	D.YOUNG
DATE	10/01/2010
SHEET	1 OF 2
CODE ID NO.	1CN88
SIZE	D
REV	B



Supply Regulator for PLL+VCO

A recommended design practice is to connect the regulator Enable Pin #3 through a 4.7kOhm resistor to the system microcontroller/FPGA for power management control

Small series resistors required in VR1 and VR4 output paths, as shown

HITTITE MICROWAVE CORPORATION
20 Alpha Rd Chelmsford, MA 01824

TITLE: SCH, CUSTOMER EVALUATIONC PLL & VCO 2 X FO

PROJECT

DRAWING #: 129506

SHEET 2 OF 2

DRAWN BY: D.YOUNG

DATE: 10/01/2010

CODE ID NO.: 1CN88

SIZE: D

REV: B