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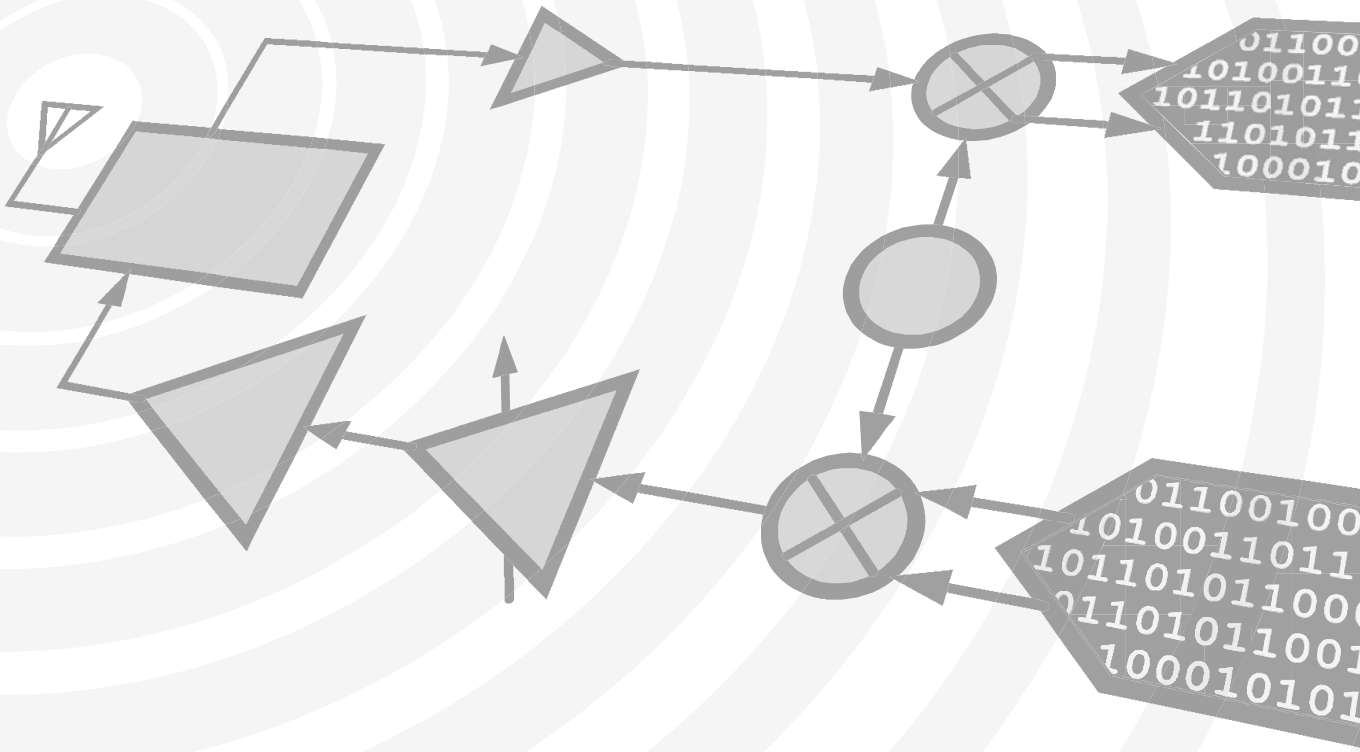

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70 dB Extended Dynamic Range SDLVA Using HMC913LC4B

Introduction

The HMC913LC4B is a Successive Detection Logarithmic Video Amplifier (SDLVA) which operates from 0.6 to 20 GHz. The HMC913LC4B provides ±3dB logging range of 59 dB and ±1dB log linearity between -50 dBm and +3 dBm of RF input. This device offers typical fast rise/fall times of 5/10 ns and an excellent delay time of only 14 ns. The HMC913LC4B log video output slope is typically 14 mV/dB. Maximum recovery times are less than 30 ns. The HMC913LC4B is available in a highly compact 4 x 4 mm SMT ceramic package and is ideal for high speed channelized receiver applications.

This application note discusses the system design to extend the dynamic range of the HMC913LC4B.

Design Concept

The sensitivity of the HMC913LC4B can be increased with an amplifier preceding the SDLVA. This allows for the detection of lower power levels with the SDLVA. Similarly, higher power levels can be detected with an attenuator preceding the SDLVA. The effect of the amplification and attenuation is illustrated in Figure 1.

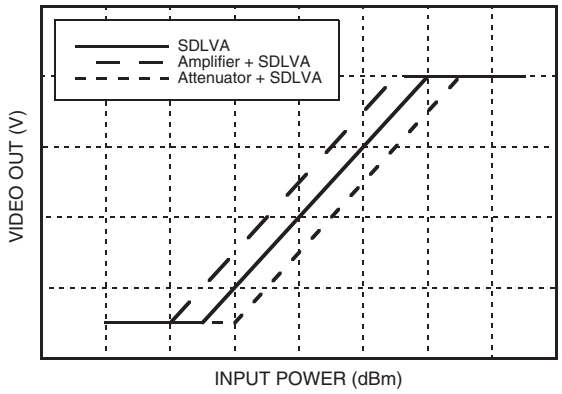

Figure 1: Effect of Amplifier and Attenuator Preceding SDLVA

As shown in Figure 1 the amplifier and the attenuator alone do not increase the range, but simply shift the response to the input power by the amount of amplification or attenuation. The low power detection with the amplified configuration and high power response of the attenuated configuration can then be combined to extend the SDLVA's dynamic range. The block diagram of the proposed system is shown in Figure 2.

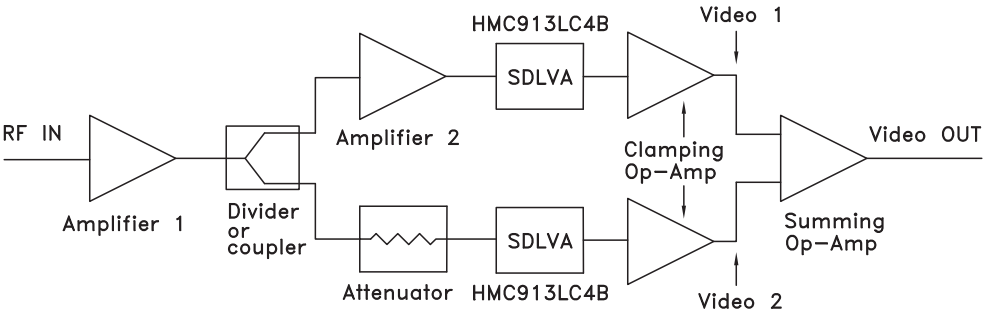

Figure 2: Block Diagram of the Extended Range SDLVA System

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In Figure 2, Amplifier 1 should be a low-noise amplifier, as it defines the minimum detectable signal of the system. The divider diverts the input signal to an amplified path and an attenuated path. A coupler can also be used instead of divider. The sensitivity of the HMC913LC4B is increased in the amplified path, while the attenuated branch is responsible for high power detection. Since the SDLVA is a wideband component, all components from RF IN up to the input of the SDLVAs should have sufficient bandwidth and frequency flatness. Also, the implementation should follow RF system circuit design principles.

Each HMC913LC4B converts the RF signals to video voltages corresponding to the RF power levels, and the results of the two branches should be combined in the correct fashion. For example, adding the output voltages of the two branches directly would double the slope of the detection system due to overlapping log detection in the amplified and attenuated branches. In order to avoid overlapping log detection, SDLVA output voltages are clamped at proper levels to maintain constant log detection slope. Therefore, only one branch logs at any power level. The effect of the clamping operation and the resulting summed Video output is shown in Figure 3.

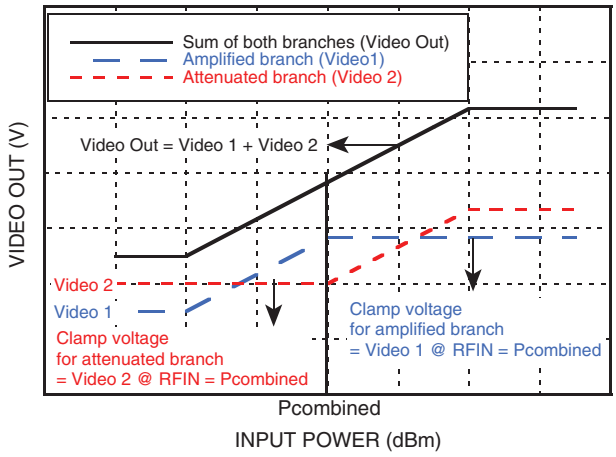

Figure 3: The Effect of Clamping for Amplified and Attenuated Branches and the Sum of Both Branches

The attenuated branch is clamped below a set voltage to eliminate its effect for low power levels. Correspondingly, the amplified branch is clamped above a set voltage to eliminate its effect for high power levels. The clamp voltages should be set as indicated in Figure 3.

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Implementation

The design is implemented as shown in Figure 4. Important design parameters are indicated in the figure. Please refer to the Appendices on page 10 and 11 for a complete schematic and a list of materials.

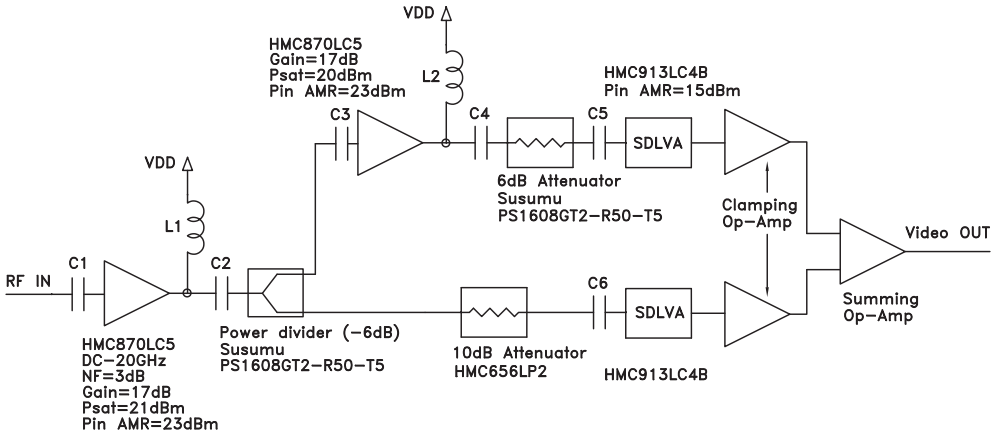

Figure 4: Extended Range SDLVA Implementation

The HMC870LC5 distributed amplifier is chosen for its wideband operation, gain flatness, low noise figure, and high input power handling capability. The input amplifier is followed by a wideband power divider. In the amplified branch, after the second HMC870LC5, a 6dB attenuator is implemented to prevent HMC913LC4B input power from exceeding the AMR (Absolute Maximum Rated) value.

The HMC870LC5 amplifiers are supplied with +5V. The gate control voltages (Vgg) of the HMC870LC5 amplifiers are set to achieve Icc=133mA each. The amplitude control voltages (Vctl) of the input amplifier and the second amplifier are set to 0.5V and 0V respectively. The HMC913LC4B SDLVAs are supplied with +3.3V.

The design is manufactured on a four layer PCB adhering to RF circuit design principles.

The amplified and attenuated branches are optimized for frequency flatness by tuning the passive input/output component values. In addition, the frequency response profile of the amplified and attenuated branches should be matched to minimize log linearity errors.

The results of the optimization process is illustrated in Figure 5. In Figure 5, the frequency response of both SDLVAs are plotted for Pin = -40 dBm. Trace 1 and Trace 3 correspond to the initial design point of the amplified and attenuated responses respectively. The frequency flatness of the amplified branch is improved by changing the C23 capacitor value from 120 pF to 0.5 pF (refer to detailed schematic in Appendix-1). This creates a high-pass filter effect, resulting in Trace 2. At this point, the frequency flatness of the amplified branch is improved. However, the log linearity at 2 GHz is distorted. At 2 GHz the dip at the amplified branch will lower the video output at this frequency. When the amplified branch is combined with the attenuated branch, the peak at 2 GHz on Trace 3 will boost the video output. This results in a discontinuity at the junction of the amplified and attenuated branches which causes a distortion of the log linearity. Therefore, for low frequencies, the attenuated branch video out response is also attenuated to minimize log linearity error. The input matching capacitors of the attenuated branch, C36 and C37, are reduced from 33 pF to 1 pF and 0.8 pF respectively. This results in Trace 4, which is optimized for the attenuated branch.

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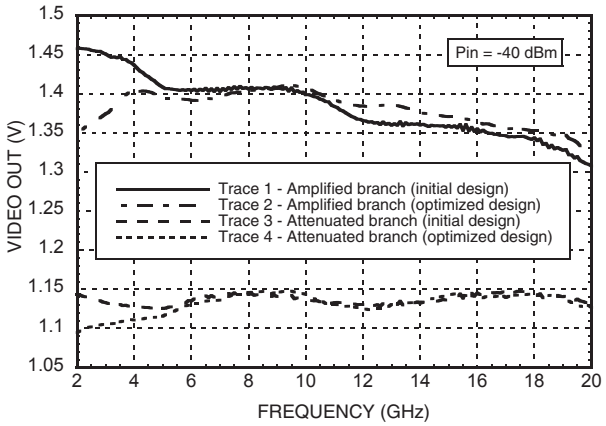

Figure 5: Frequency Response of the Amplified and Attenuated Branches

Following the HMC913LC4Bs, op-amps are used to clamp the HMC913LC4B outputs. The power level of -40 dBm is selected to combine the two branches. The summing op-amp adds the resulting voltages of both branches. The input bandwidth and slew rate of the clamping and summing op-amps should be carefully considered so as to avoid limiting the pulse response of the HMC913LC4B SDLVAs. Figure 6 shows the clamped video out responses of the amplified and attenuated branches as well as the summed video out response. The input frequency is swept from 2 GHz to 20 GHz. The amplified and attenuated branches are combined at -40 dBm.

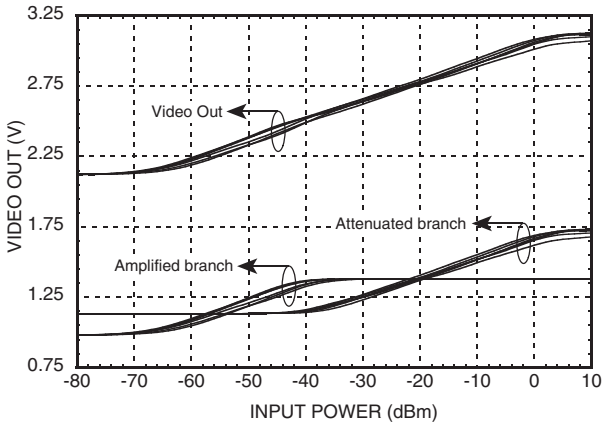

Figure 6: Video Out and Clamped Branch Outputs swept from 2 GHz to 20 GHz

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Extended Range Performance Parameters

The electrical specifications of the HMC913LC4B and the measured Extended Range SDLVA system are compared in Table 1.

Table-1: Electrical Specifications Comparing the HMC913LC4B with the Extended Range SDLVA System

Parameter	Conditions		HMC913LC4B	Extended Range SDLVA	Units
Input Frequency Range			0.6-20	2-18	GHz
Frequency Flatness			±2	±2	dB
Log Error			±1	±1.5	dB
Log Error over Temperature*			±1	±1	dB
Minimum Logging Range			-54	-68	dBm
Maximum Logging Range			+5	+5	dBm
Tangential Signal Sensitivity	@ 10 GHz		-56	-74	dBm
Log Video Minimum Output Voltage			1	2.12	V
Log Video Maximum Output Voltage			1.8	3.12	V
Log Video Output Slope			14	14	mV/dB
Log Video Output Rise Time	10% to 90%	Slope = 14 mV/dB	5	7.5	ns
		Slope = 25 mV/dB	-	9.6	ns
Log Video Output Fall Time	90% to 10%	Slope = 14 mV/dB	10	15.7	ns
		Slope = 25 mV/dB	-	16.8	ns

* Temperature error with respect to 25°C.

Video out and error of the extended range SDLVA system for various frequencies and temperatures are presented in Figure 7 through Figure 11. The frequency response of the system for various power levels and temperatures is presented in Figure 12.

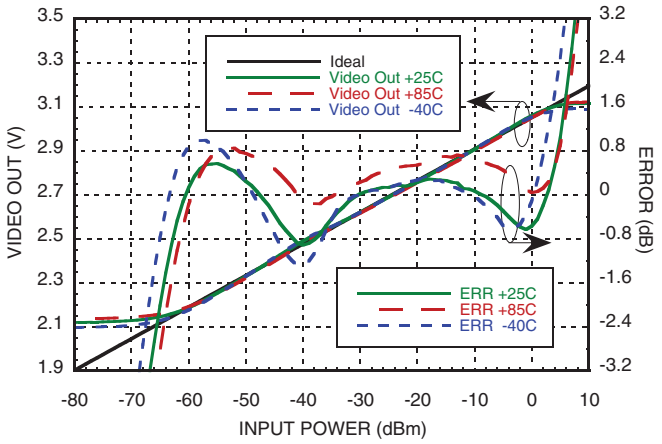


Figure 7: Extended Range Video Out & Error vs. Input Power, Fin = 2 GHz

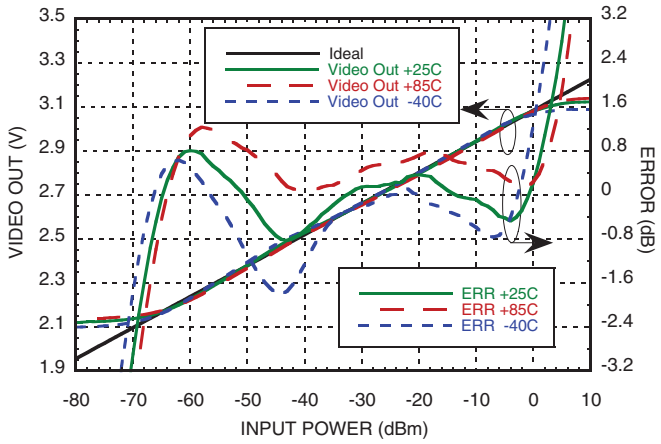


Figure 8: Extended Range Video Out & Error vs. Input Power, Fin = 6 GHz

70 dB Extended Dynamic Range SDLVA Using HMC913LC4B

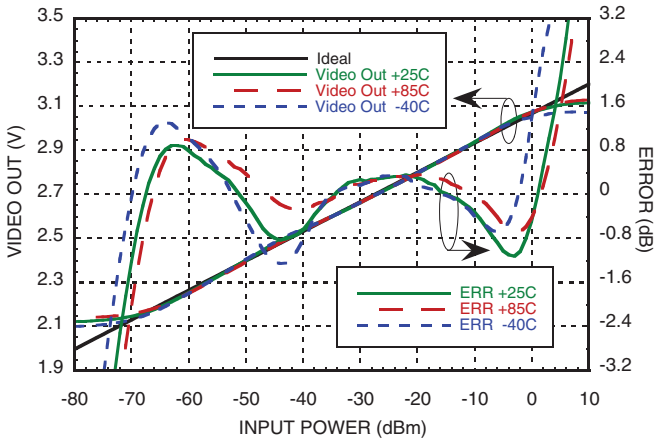


Figure 9: Extended Range Video Out & Error vs. Input Power, Fin = 10 GHz

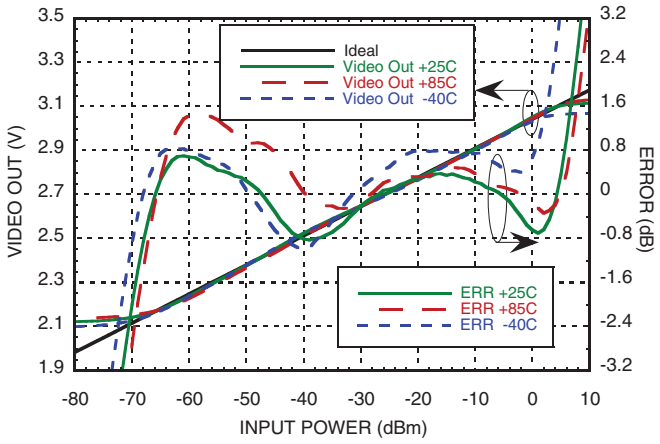


Figure 10: Extended Range Video Out & Error vs. Input Power, Fin = 14 GHz

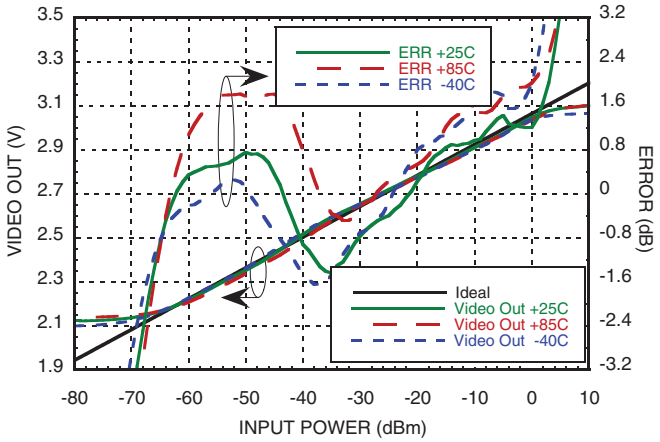


Figure 11: Extended Range Video Out & Error vs. Input Power, Fin = 18 GHz

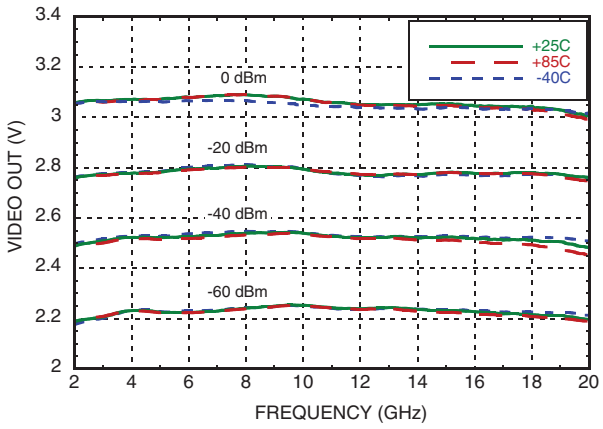


Figure 12: Extended Range Video Out vs. Frequency over Input Power & Temperature

Video Signal Shaping (Offset and Slope adjustment)

The Extended Range SDLVA system provides configuration flexibility to provide desired log detection slope and offset at the summing op-amp node. The log slope of the extended range SDLVA system can be scaled up and down by changing the gain of the summing op-amp stage without affecting the clipping mechanism implemented in previous stages. Similarly, the video output can be shifted up and down with an external offset voltage on the summing op-amp stage.

The log slope of the extended range SDLVA system is adjusted by changing the gain of the summing op-amp. For example, in order to double the log slope of the extended range SDLVA, the gain of the summing op-amp should be doubled. The gain of the summing op-amp can be adjusted with the R15 resistor.

In order to adjust the video base-line, a DC current should be injected to the inverting node of the summing op-amp. To realize this current injection, R16 is installed between VOFFSET and the inverting node of the summing op-amp on the extended range SDLVA board. In the default configuration, VOFFSET is shorted to GND, which results in direct summation of the amplified and attenuated branch outputs yielding a video base-line close to 2.1 V. Increasing the VOFFSET voltage lowers the video base-line; reducing VOFFSET increases the video base-line voltage.

In order to illustrate the video signal shaping, R15 is changed to 604 Ohm and an offset voltage of 1.69 V is applied to VOFFSET. In this configuration the log slope of the extended range SDLVA is increased to 25 mV/dB and the base-line voltage is reduced to 100 mV.

The effect of the video signal shaping is presented with the pulse responses of both the default and the adjusted configurations in Figure 13 and Figure 14.

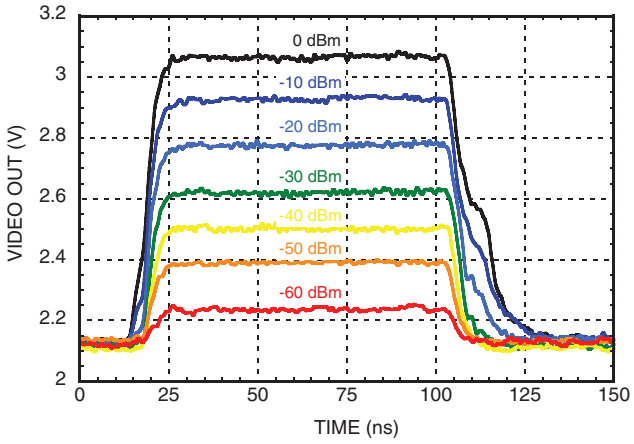


Figure 13: RF Pulse Response @ 5 GHz with 14 mV/dB slope

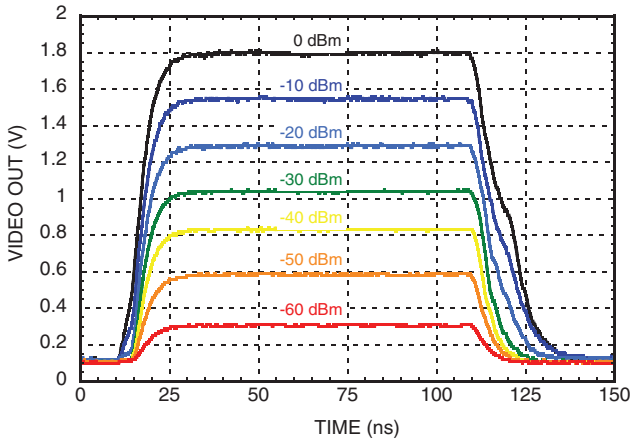


Figure 14: RF Pulse Response @ 5 GHz with offset adjusted 25 mV/dB slope

The video out and error of the extended range SDLVA system after slope and offset adjustment is presented for various frequencies and temperatures in Figures 15 to 17.

Similarly, the pulse responses of this configuration are presented in Figures 18 to 21.

70 dB Extended Dynamic Range SDLVA Using HMC913LC4B

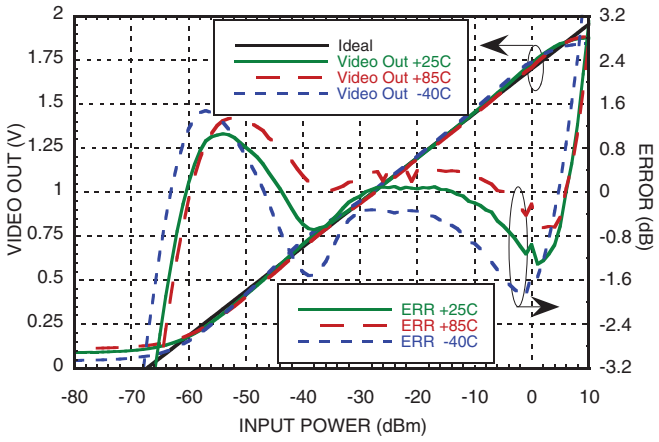


Figure 15: Log-conformance of ER-SDLVA after offset and slope adjustment @ 2 GHz

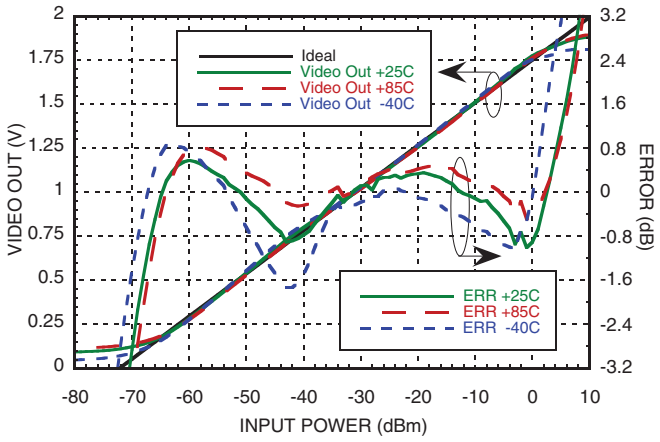


Figure 16: Log-conformance of ER-SDLVA after offset and slope adjustment @ 10 GHz

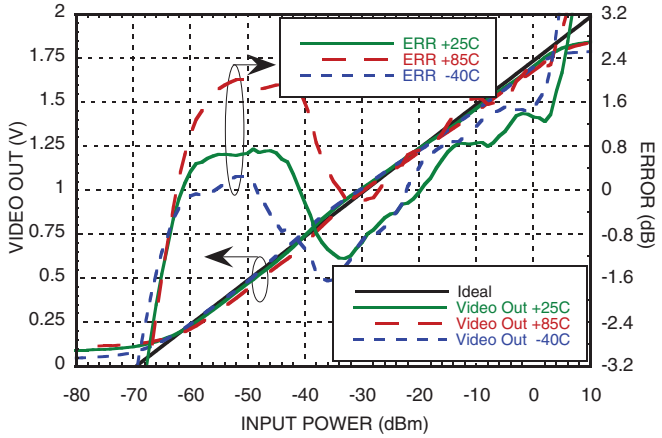


Figure 17: Log-conformance of ER-SDLVA after offset and slope adjustment @ 18 GHz

70 dB Extended Dynamic Range SDLVA Using HMC913LC4B

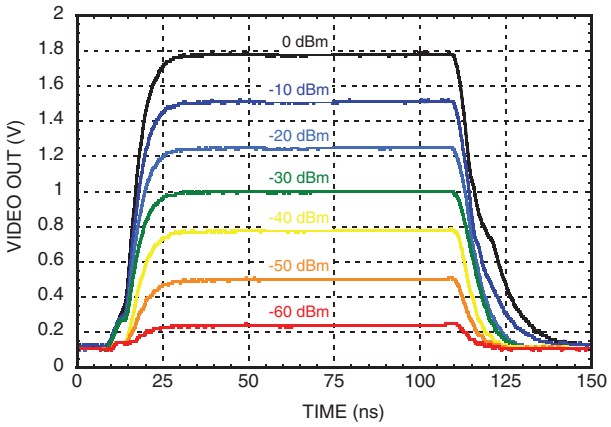


Figure 18: Pulse Response of ER-SDLVA after offset and slope adjustment @ 2 GHz

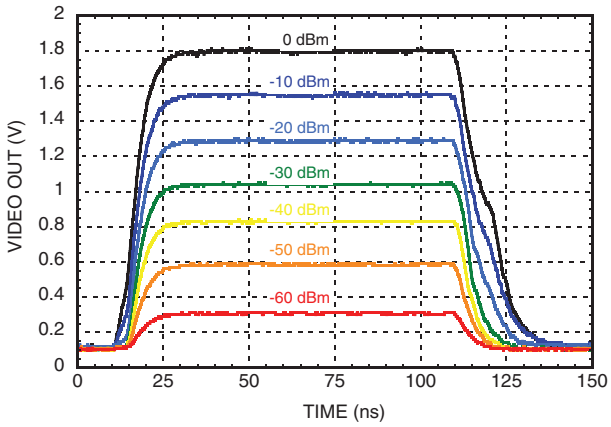


Figure 19: Pulse Response of ER-SDLVA after offset and slope adjustment @ 5 GHz

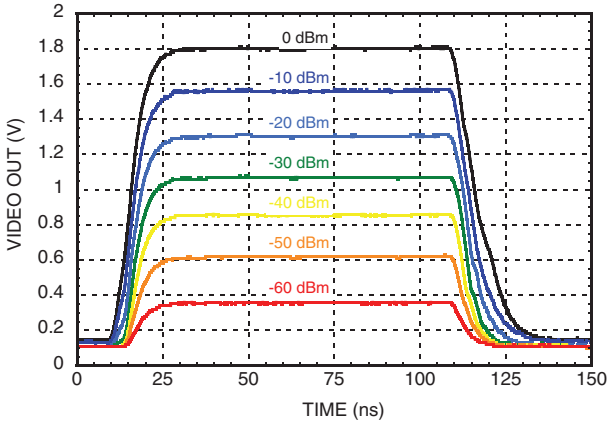


Figure 20: Pulse Response of ER-SDLVA after offset and slope adjustment @ 10 GHz

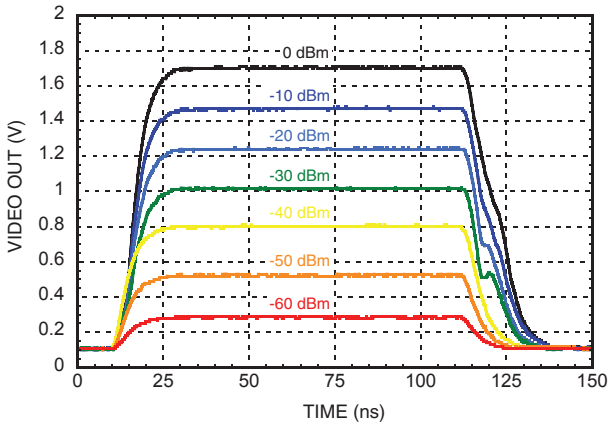
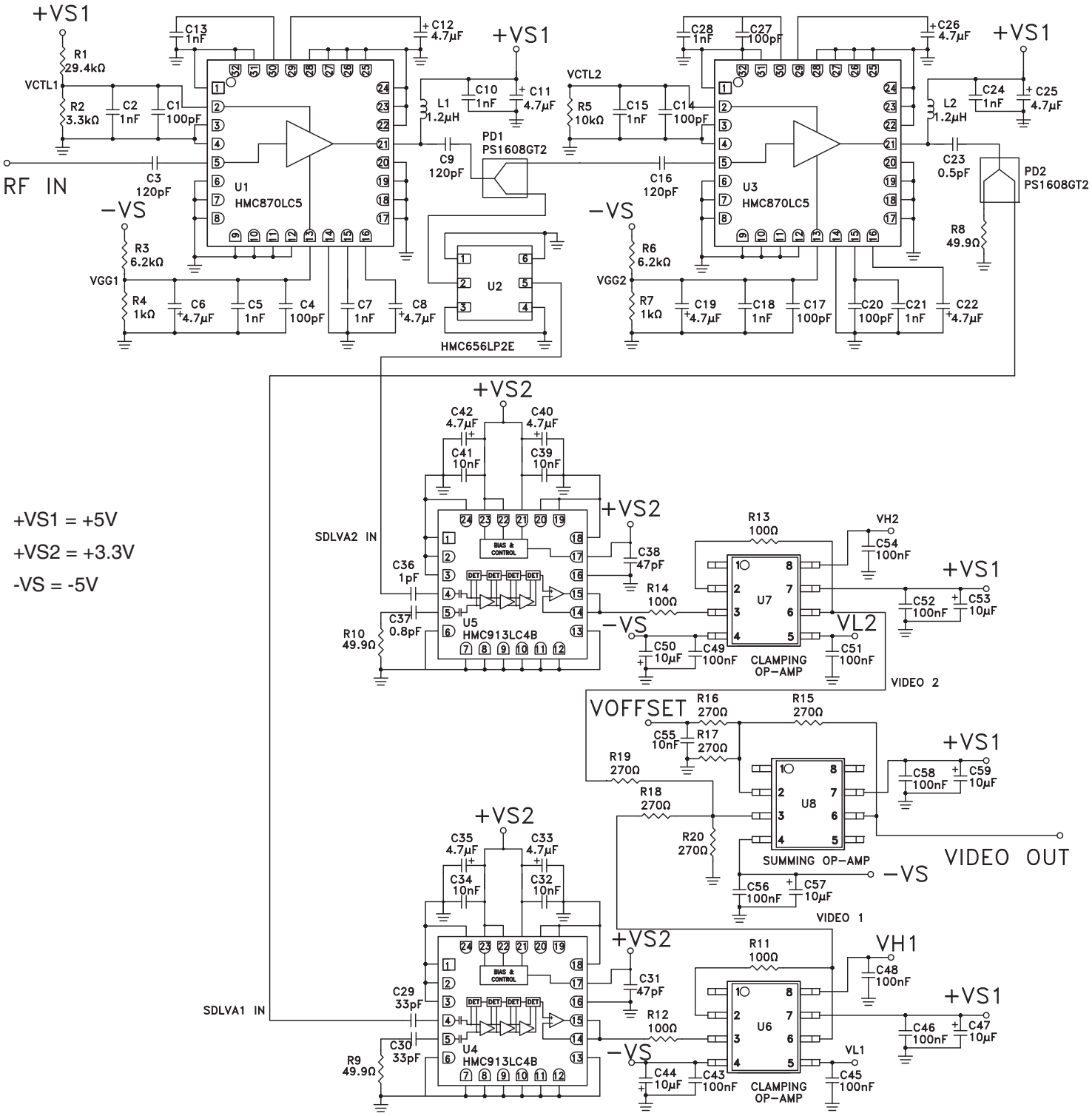


Figure 21: Pulse Response of ER-SDLVA after offset and slope adjustment @ 18 GHz

70 dB Extended Dynamic Range SDLVA Using HMC913LC4B

Appendix-1 - Application Circuit



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Appendix-2 - List of Materials

Item	Description
C1, C4, C14, C17, C20, C27	100 pF Capacitor, 0402 Pkg.
C2, C5, C7, C10, C13, C15, C18, C21, C24, C28	1 nF Capacitor, 0402 Pkg.
C3, C9, C16	120 pF Capacitor, 0402 Pkg.
C6, C8, C11, C12, C19, C22, C25-C26, C33, C35, C40, C42	4.7 µF Capacitor, Tantalum
C23	0.5 pF Capacitor, 0402 Pkg.
C29, C30	33 pF Capacitor, 0402 Pkg.
C31, C38	47 pF Capacitor, 0402 Pkg.
C32, C34, C39, C41, C55	10 nF Capacitor, 0402 Pkg.
C36	1 pF Capacitor, 0402 Pkg.
C37	0.8 pF Capacitor, 0402 Pkg.
C43, C45, C46, C48, C49, C51,C52, C54, C56, C58	100 nF Capacitor, 0402 Pkg.
C44, C47, C50, C53, C57, C59	10 µF Capacitor, Tantalum
L1-L2	1.2 µH Inductor, Conical
R1	29.4 kΩ Resistor, 0402 Pkg.
R2	3.3 kΩ Resistor, 0402 Pkg.
R3, R6	6.2 kΩ Resistor, 0402 Pkg.
R4, R7	1 kΩ Resistor, 0402 Pkg.
R5	10 kΩ Resistor, 0402 Pkg.
R8 - R10	49.9 Ω Resistor, 0402 Pkg.
R11 - R14	100 Ω Resistor, 0603 Pkg.
R15 - R20	270 Ω Resistor, 0402 Pkg.
PD1, PD2	PS1608GT2, High Precision Power Splitter
U1, U3	HMC870LC5, Modulator Driver
U2	HMC656LP2E, Passive Attenuator
U4, U5	HMC913LC4B, SDLVA
U6, U7	Clamping Op-Amp
U8	Summing Op-Amp