REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY MM DD 17-11-22	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, LINEAR-DIGITAL, 0.1 GHz TO 33 GHz, 1 dB LEAST SIGNIFICANT BIT (LSB), 5-Bit, DIGITAL ATTENUATOR, GALLIUM ARSENIDE (GaAs)
	APPROVED BY Thomas M. Hess	
	SIZE **A** / **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/17616**
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AMSC N/A

5962-V007-18

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance 0.1 GHz to 33 GHz, 1 dB LSB, 5 Bit, GaAs Digital Attenuator microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/17616	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	HMC939ATCPZ –EP	0.1 GHz to 33 GHz, 1 dB LSB, 5 Bit, GaAs Digital Attenuator

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	24	JEDEC MO-220-VGGD-8	Lead Frame Chip Scale Package [LFCSP]

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA)
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage:
- Positive ..... 7.0 V
- Negative ..... -7.0 V

Digital Control Input voltage, V_{CTL} ..... V_{DD} + 0.5 V
RF Input Power (All Attenuation States, f = 0.1 GHz to 33 GHz, T_{CASE} = 85°C)..... 27 dBm
Continuous Power Dissipation, P_{DISS}:
- (T_{CASE} = 85°C) ..... 0.453 W 2/
- (T_{CASE} = 105°C) ..... 0.314 W 2/
- (T_{CASE} = 125°C) ..... 0.174 W 2/

Temperature:
- Junction, T_J ..... 150°C
- Case, T_{CASE} ..... -55°C to +125°C
- Storage ..... -65°C to 150°C
- Reflow 3/ (Moisture Sensitivity Level 3 (MSL3) Rating ..... 260°C

Electrostatic Discharge (ESD) Sensitivity:
- Human Body Model (HBM) ..... 250 V (Class 1A)

1.4 Thermal characteristics.

Thermal resistance

Case outline	θ_{JA}	θ_{JC}	Unit
Case X 4/	213	143.5 5/	°C/W

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices.
JESD51 – Methodology for the Thermal Measurement of Component Packages (Single Semiconductor Device).

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107).

1/ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2/ See FIGURE 6.
3/ See the Ordering Guide from manufacturer for more information.
4/ Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with nine thermal vias. See JEDEC JESD51.
5/ The device is set to maximum attenuation state.

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, 1.4, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

3.5.3 Terminal function. The terminal function shall be as shown in figure 3.

3.5.4 P4 to P0 Truth table. The truth table shall be as shown in figure 4.

3.5.5 Functional block diagram. The functional block diagram shall be as shown in figure 5.

3.5.6 Maximum Power Dissipation vs Case Temperature (T_{CASE}). The Maximum Power Dissipation vs Case Temperature (T_{CASE}) shall be as shown in figure 6.

3.5.7 RF1 and RF2 Interface Schematic. The RF1 and RF2 Interface Schematic shall be as shown in figure 7.

3.5.8 Parallel Control Voltage Inputs Interface Schematic. The Parallel Control Voltage Inputs Interface Schematic shall be as shown in figure 8.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
FREQUENCY RANGE			0.1		33	GHz
INSERTION LOSS		0.1 GHz to 18 GHz		4.5	5.5	dB
		18 GHz to 26.5 GHz		5.5	7.0	dB
		26.5 GHz to 33 GHz		6	8	dB
ATTENUATION						
Range		Between minimum and maximum attenuation states, 0.1 GHz to 33 GHz		31		dB
Step Size		Between any successive attenuation states, 0.1 GHz to 33 GHz		1		dB
Step Error		Between any successive attenuation states, 0.1 GHz to 33 GHz		0.5		dB
State Error		Referenced to insertion loss state				
		1 dB to 15 dB attenuation states, 0.1 GHz to 33 GHz	−(0.5 + 5% of attenuation state)		+(0.5 + 5% of attenuation state	dB
		16 dB to 31 dB attenuation states, 0.1 GHz to 20 GHz	−(0.5 + 5% of attenuation state)		+(0.5 + 5% of attenuation state)	dB
		16 dB to 31 dB attenuation states, 20 GHz to 33 GHz	−(0.6 + 8% of attenuation state)		+(0.6 + 8% of attenuation state)	dB
RETURN LOSS		RF1 and RF2 pins, all attenuation states, 0.1 GHz to 33 GHz		10		dB
RELATIVE PHASE		Between minimum and maximum attenuation states				
		0.1 GHz to 18 GHz		45		Degrees
		18 GHz to 26.5 GHz		60		Degrees
		26.5 GHz to 33 GHz		80		Degrees

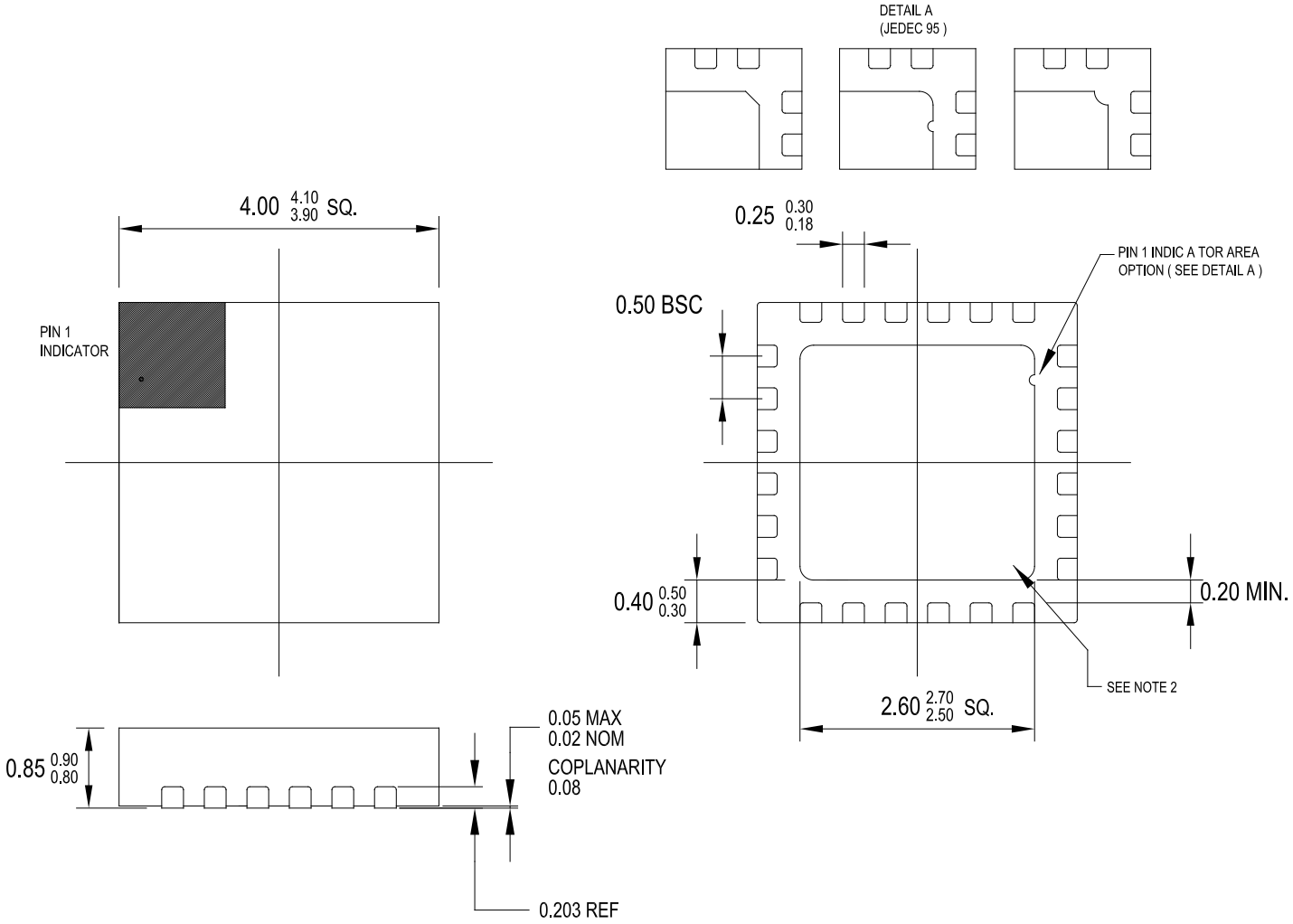
See footnote at end of table.

Test	Symbol	Test conditions 2/	Limits			Unit
			Min	Typ	Max	
SWITCHING CHARACTERISTICS		Between all attenuation states				
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of radio frequency (RF) output		45		ns
On and Off Time	t_{ON}, t_{OFF}	50% digital control input voltage (V_{CTL}) to 90% of RF output		60		ns
INPUT LINEARITY		All attenuation states,				
0.1 dB Compression	P0.1dB	0.1 GHz to 0.5 GHz		20		dBm
		0.5 GHz to 33 GHz		24		dBm
Third-Order Intercept	IP3	8 dBm per tone, 1 MHz spacing				
		0.1 GHz to 0.5 GHz		43		dBm
		0.5 GHz to 33 GHz		40		dBm
SUPPLY CURRENT						
Positive	I_{DD}		2.5	4.5	6.5	mA
Negative	I_{SS}		-7.0	-5.5	-3.0	mA
DIGITAL CONTROL INPUTS		P0 to P4 pins				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		2		5	V
Current						
Low and High	I_{INL}, I_{INH}			<1		µA

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

2/ V_{DD} = 5 V, V_{SS} = −5 V, V_{Px} = 0 V or V_{DD}, T_{CASE} = 25°C, 50 Ω system, unless otherwise noted.

Case X



NOTES:
1. All linear dimensions are in millimeters.
2. Falls within JEDEC MO-220-VGGD-8.

FIGURE 1. Case outline.

DLA LAND AND MARITIME COLUMBUS, OHIO	SIZE A	CODE IDENT NO. 16236	DWG NO. V62/17616
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Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	VSS	24	P0
2	NIC	23	P1
3	NIC	22	P2
4	NIC	21	P3
5	RF1	20	P4
6	NIC	19	NIC
7	NIC	18	VDD
8	NIC	17	NIC
9	NIC	16	NIC
10	NIC	15	NIC
11	NIC	14	RF2
12	NIC	13	NIC

NOTES:
1. NIC = No Internal Connection
2. The exposed PAD must be connected to Ground for proper operation.

FIGURE 2. Terminal connections.

Pin No	Mnemonic	Description
1	VSS	Negative Supply Voltage
2 to 4, 6 to 13, 15 to 17, 19	NIC	Not Internally Connected. These pins are not internally connected; however, all data shown herein was measured with these pins connected to the RF/dc ground of evaluation board.
5, 14	RF1, RF2	RF Inputs or Outputs of Attenuator. This pin is dc-coupled to 0 V and ac matched to 50 Ω. No dc blocking capacitor is necessary when the RF line potential is equal to 0 V dc.
18	VDD	Positive Supply Voltage.
20 to 24	P4 to P0	Parallel Control Voltage Inputs. These pins select the required attenuation. There is no internal pull-up or pull-down resistor on these pins; therefore, they must always be kept at a valid logic level (VINH or VINL) and not be left floating
	EPAD	Exposed Pad. The exposed pad must be connected to ground for proper operation.

FIGURE 3. Terminal function.

Digital Control Input 1/					
P4	**P3**	**P2**	**P1**	**P0**	**Attenuation State (dB)**
H	H	H	H	H	0 dB (reference)
H	H	H	H	L	1 dB
H	H	H	L	H	2 dB
H	H	L	H	H	4 dB
H	L	H	H	H	8 dB
L	H	H	H	H	16 dB
L	L	L	L	L	1+2+4+8+16 = 31 dB

NOTES:
1. Any combination of the control voltage input states shown in this table provides an attenuation equal to the sum of the bits selected.
2. H = High
3. L = Low.

FIGURE 4. P4 to P0 Truth table.

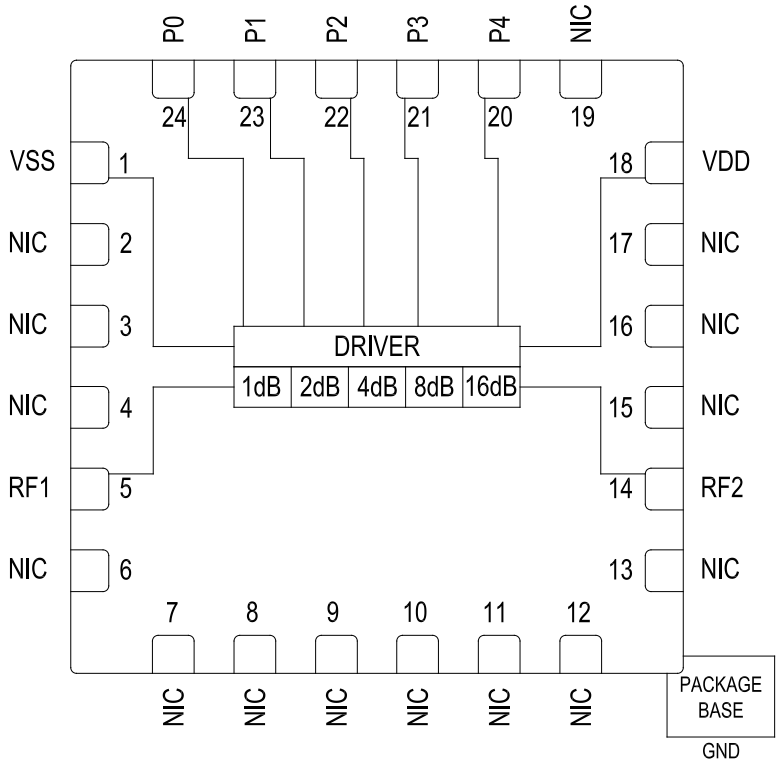

FIGURE 5. Functional block diagram.

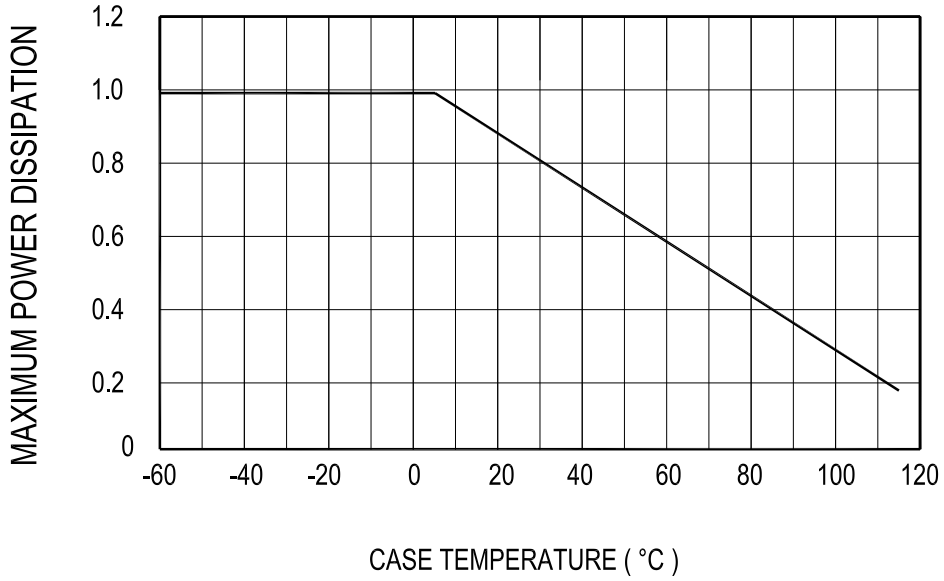

FIGURE 6. Maximum Power Dissipation vs Case Temperature (T_{CASE}).

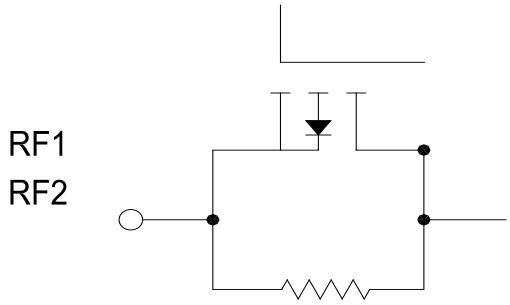

FIGURE 7. RF1 and RF2 Interface Schematic.

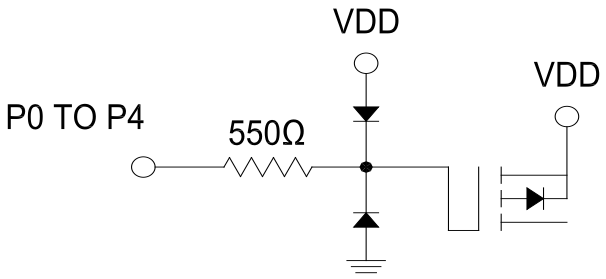

FIGURE 8. Parallel Control Voltage Inputs Interface Schematic.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/programs/smcr/default.aspx

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Order Quantity	Vendor part number
V62/17616-01XE	24355	Tube units = 50	HMC939ATCPZ-EP-PT
		Reel units = 500	HMC939ATCPZ-EP-R7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106