>1.5 W (34 dBm), 24 GHz to 34 GHz, GaAs, pHEMT, MMIC, Power Amplifier

Data Sheet **HMC943APM5E**

FEATURES

- High saturated output power (P_{SAT}): 34 dBm
- High output IP3: 39 dBm
- High gain: 23 dB
- DC supply: 5.5 V at 1300 mA
- No external matching required
- 32-lead, 5 mm × 5 mm LFCSP_CAV package

APPLICATIONS

- Point to point radios
- Point to multipoint radios
- Microwave radios, very small aperture terminals (VSATs), and satellite communications (SATCOM)
- Military and space

FUNCTIONAL BLOCK DIAGRAM

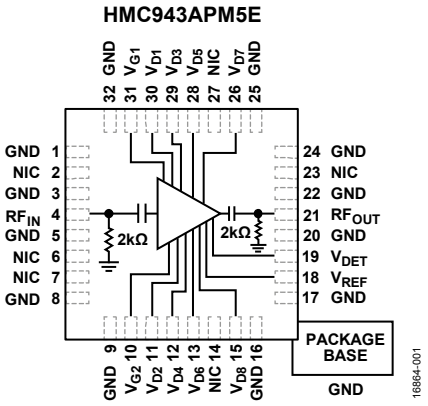

Figure 1.

GENERAL DESCRIPTION

The HMC943APM5E is a four stage, gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC), >1.5 W power amplifier that operates between 24 GHz to 34 GHz. The HMC943APM5E provides 23 dB of gain, 34 dBm of saturated output power (P_{SAT}), and 23% power added efficiency (PAE) from a 5.5 V supply. The high output third-order intercept (IP3) of 39 dBm makes the HMC943APM5E ideal for microwave radio applications. A power detector output is also available. The HMC943APM5E amplifier input/outputs (I/Os) are internally matched to 50 Ω. The device is packaged in a leadless, 5 mm × 5 mm, surface-mount LFCSP_CAV package, and requires no external matching components.

Rev. B

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9/2018—Rev. 0 to Rev. A

Changes to Storage Temperature Range Parameter, Table 3 ... 4

8/2018—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

T_A = 25°C, V_{D1} − V_{D8} = 5.5 V, quiescent supply current (I_{DDQ}) = 1300 mA, and frequency range = 24 GHz to 29 GHz

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		24		29	GHz	
GAIN		20.5	23		dB	
Gain Variation over Temperature			0.04		dB/°C	
RETURN LOSS						
Input			12		dB	
Output			12		dB	
POWER						
Output Power for 1 dB Compression	P1dB	29	33		dBm	
Saturated Output Power	P_{SAT}		34		dBm	
OUTPUT THIRD-ORDER INTERCEPT	IP3		39		dBm	Output power (P_{OUT}) per tone = 22 dBm
SUPPLY VOLTAGE	V_{DD}	4	5.5	6	V	
QUIESCENT SUPPLY CURRENT	I_{DDQ}		1300		mA	Adjust V_{G1} or V_{G2} between −2 V and 0 V to achieve 1300 mA typical, V_{Gx} = −0.85 V typical to achieve I_{DDQ} = 1300 mA

T_A = 25°C, V_{D1} − V_{D8} = 5.5 V, I_{DDQ} = 1300 mA, and frequency range = 29 GHz to 34 GHz

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		29		34	GHz	
GAIN		20.5	23		dB	
Gain Variation over Temperature			0.04		dB/°C	
RETURN LOSS						
Input			10		dB	
Output			13		dB	
POWER						
Output Power for 1 dB Compression	P1dB	30	33		dBm	
Saturated Output Power	P_{SAT}		34		dBm	
OUTPUT THIRD-ORDER INTERCEPT	IP3		37.5		dBm	P_{OUT} per tone = 22 dBm
SUPPLY VOLTAGE	V_{DD}	4	5.5	6	V	
QUIESCENT SUPPLY CURRENT	I_{DDQ}		1300		mA	Adjust V_{G1} or V_{G2} between −2 and 0 V to achieve 1300 mA typical, V_{Gx} = −0.85 V typical to achieve I_{DDQ} = 1300 mA

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter[1]	Rating
Drain Bias Voltage (V_{Dx})	6.5 V
Gate Bias Voltage (V_{Gx})	−2 V to 0 V dc
Radio Frequency (RF) Input Power (RF_{IN})	20 dBm
Output Load Standing Wave Ratio (VSWR)	7:1
Junction Temperature to Maintain 1 Million Hour Mean Time to Failure (MTTF)	175°C
Maximum Peak Reflow Temperature (MSL3)[2]	260°C
Nominal Junction Temperature (T_A = 85°C, V_{Dx} = 5.5 V)	146.5°C
Continuous Power Dissipation, P_{DISS} (T_A = 85°C, Derate 116.3 m W/°C Above 85°C)	10.5 W
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
ESD Sensitivity (Human Body Model)	Class 0B, passed 150 V

[1] When referring to a single function of a multifunction pin in the parameters, only the portion of the pin name that is relevant to the Absolute Maximum Rating is listed. For full pin names of multifunction pins, refer to the Pin Configuration and Function Descriptions section.
[2] See the Ordering Guide for additional information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JC}	Unit
CG-32-2[1]	8.6	°C/W

[1] Thermal resistance (θ_{JC}) is determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel, through the ground pad, to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

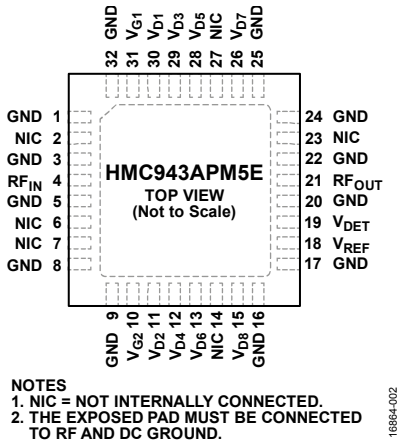


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 5, 8, 9, 16, 17, 20, 22, 24, 25, 32	GND	Ground. These pins are exposed ground pads that must be connected to RF and dc ground.
2, 6, 7, 14, 23, 27	NIC	Not Internally Connected. These pins are not connected internally. However, all data is measured with these pins connected to RF and dc ground externally.
4	RF_{IN}	RF Input. This pin is dc-coupled and matched to 50 Ω. See Figure 4 for the RF_{IN} interface schematic.
10, 31	V_{G2}, V_{G1}	Gate Control for the Amplifier. Adjust V_{Gx} to achieve the recommended bias current. External bypass capacitors of 100 pF, 10 nF, and 4.7 µF are required. See Figure 7 for the V_{Gx} interface schematic. V_{G1} and V_{G2} are internally connected. Therefore, external bias can be applied to either V_{G1} or V_{G2}.
11, 12, 13, 15, 26, 28, 29, 30	V_{D2}, V_{D4}, V_{D6}, V_{D8}, V_{D7}, V_{D5}, V_{D3}, and V_{D1}	Drain Bias for the Amplifier. External bypass capacitors of 100 pF, 0.01 µF, and 4.7 µF are required on each pin. See Figure 5 for the V_{Dx} interface schematic.
18	V_{REF}	Reference Diode Used for Temperature Compensation of V_{DET} RF Output Power Measurements. Used in combination with V_{DET}, this voltage provides temperature compensation to V_{DET} RF output power measurements. See Figure 8 for the V_{REF} interface schematic.
19	V_{DET}	Detector Diode Used for Measurement of the RF Output Power. Detection via this pin requires the application of a dc bias voltage through the external series resistor. Used in combination with V_{REF}, the difference voltage, $V_{REF} - V_{DET}$, is a temperature compensated dc voltage proportional to the RF output power. See Figure 9 for the V_{DET} interface schematic.
21	RF_{OUT}	RF Signal Output. This pad is dc-coupled and matched to 50 Ω over the operating frequency range. See Figure 6 for the RF_{OUT} interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to RF and dc ground.

INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

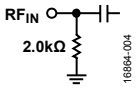


Figure 4. RF_{IN} Interface Schematic

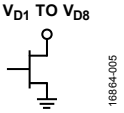


Figure 5. V_{D1} to V_{D8} Interface Schematic

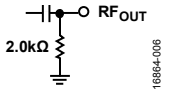
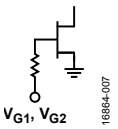


Figure 6. RF_{OUT} Interface Schematic



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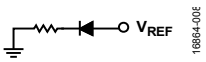


Figure 8. V_{REF} Interface Schematic

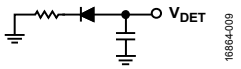


Figure 9. V_{DET} Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

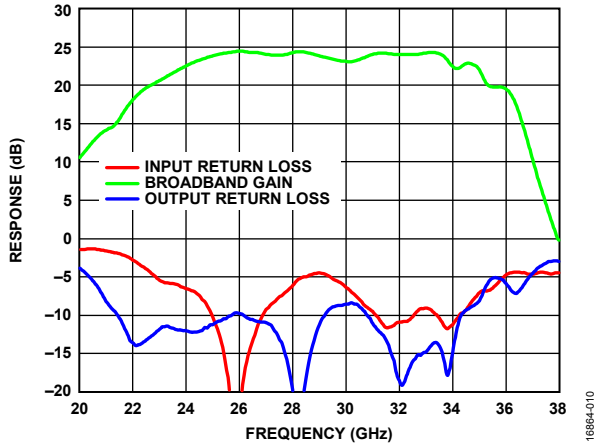
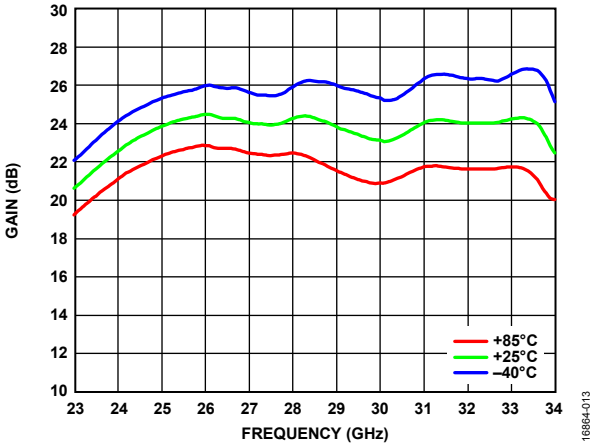


Figure 10. Broadband Gain (S21), Input Return Loss (S11), and Output Return Loss (S22) Response vs. Frequency



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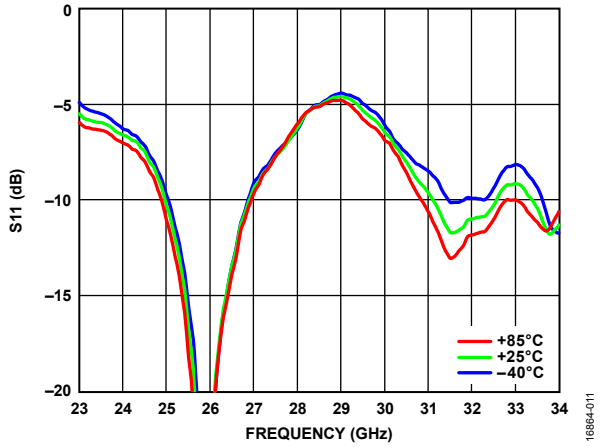
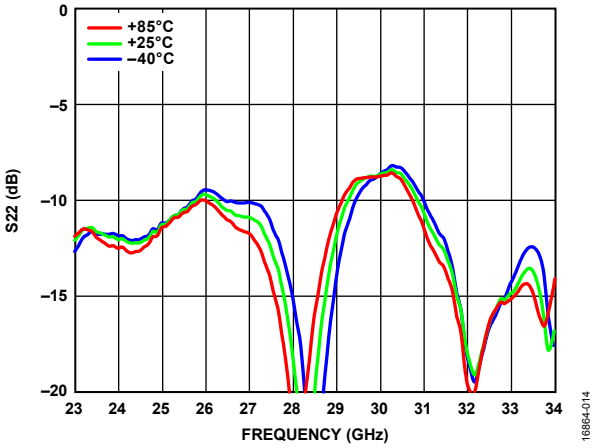


Figure 11. Input Return Loss (S11) vs. Frequency at Various Temperatures



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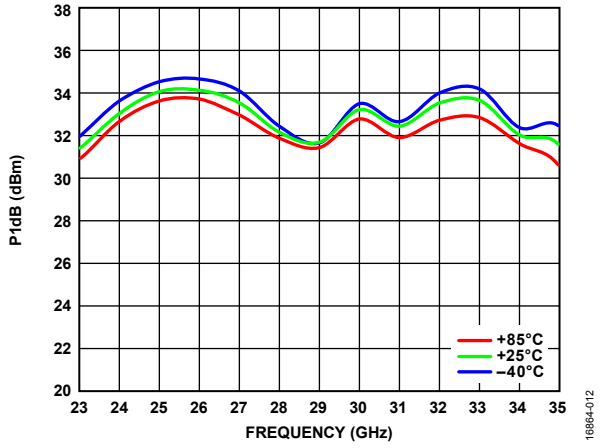

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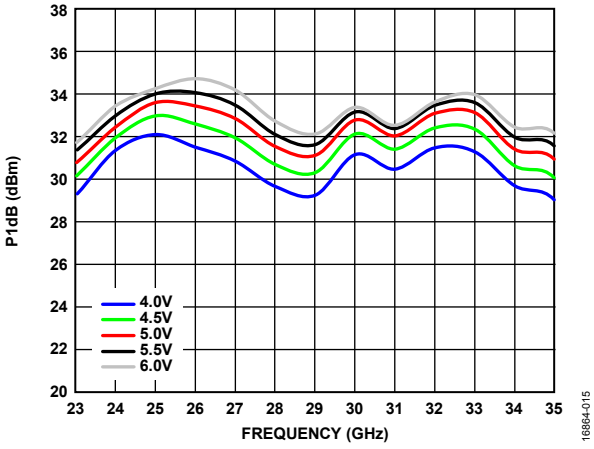
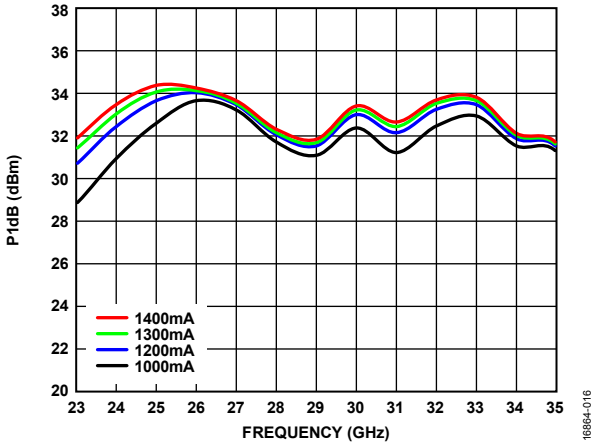


Figure 15. P1dB vs. Frequency at Various Supply Voltages



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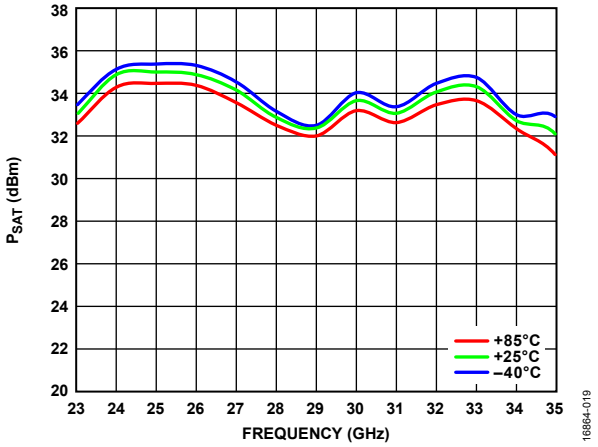

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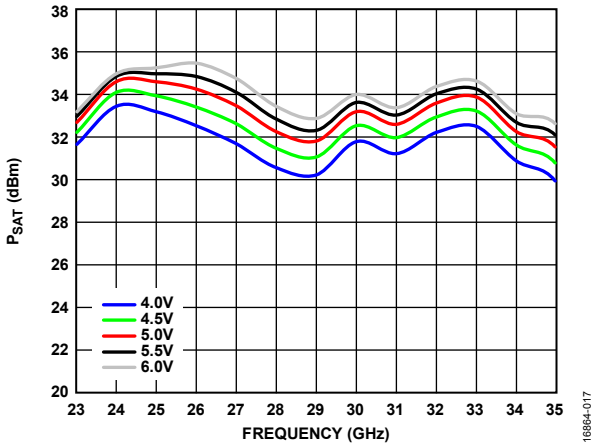


Figure 17. P_{SAT} vs. Frequency at Various Supply Voltages

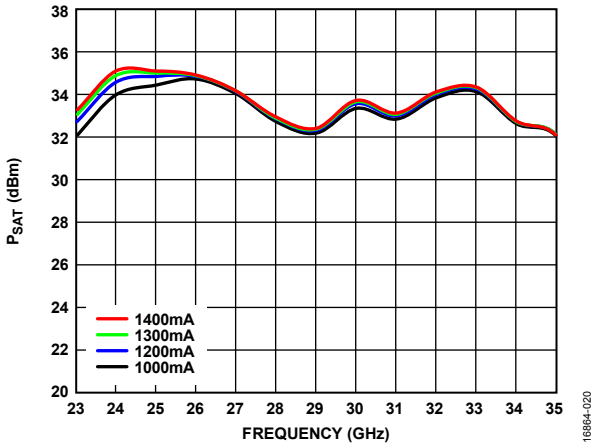


Figure 20. P_{SAT} vs. Frequency at Various Quiescent Currents

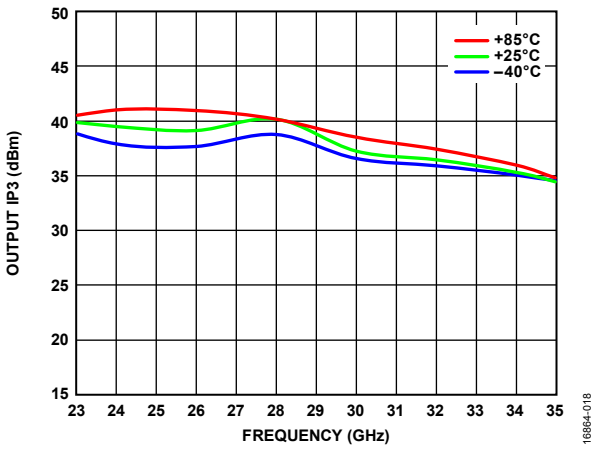
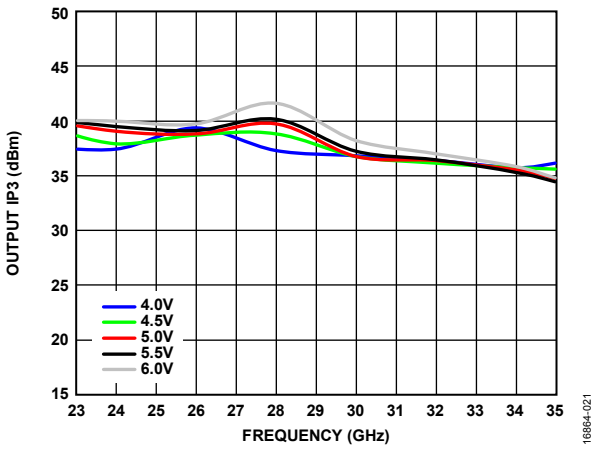


Figure 18. Output IP3 vs. Frequency at Various Temperatures, P_{OUT} per Tone = 22 dBm



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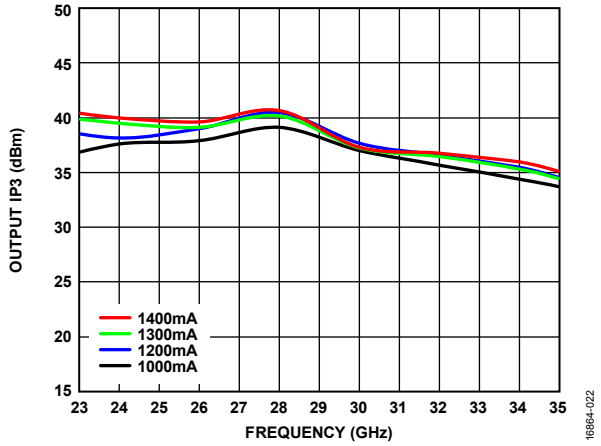

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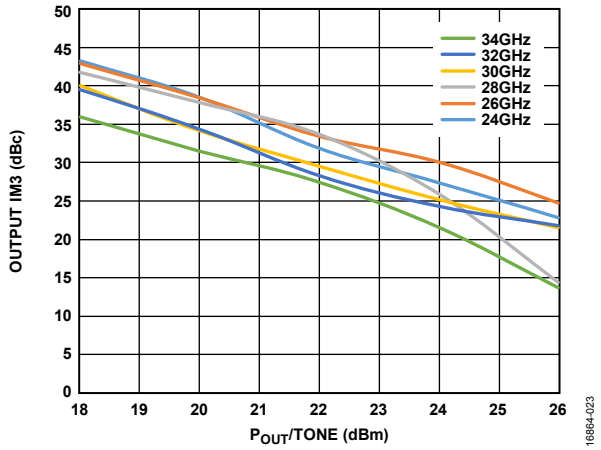

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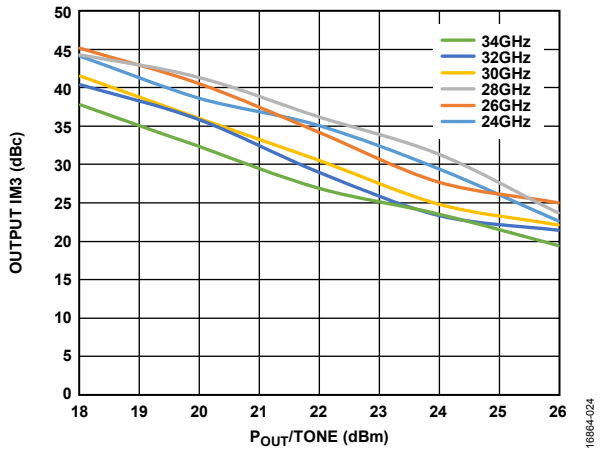

Figure 24. Output IM3 vs. P_{OUT} per Tone, V_{DD} = 5.5 V

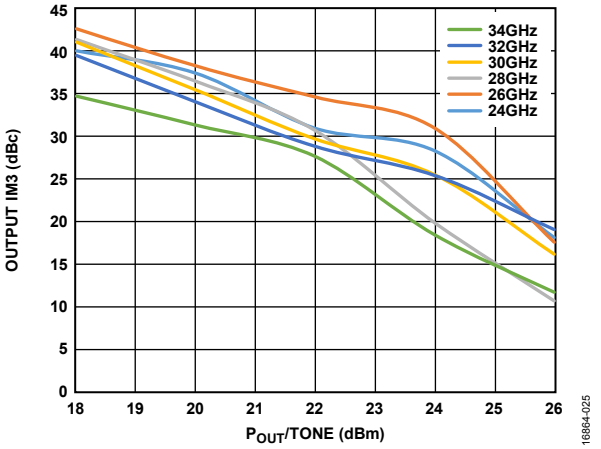

Figure 25. Output IM3 vs. P_{OUT} per Tone, V_{DD} = 4.0 V

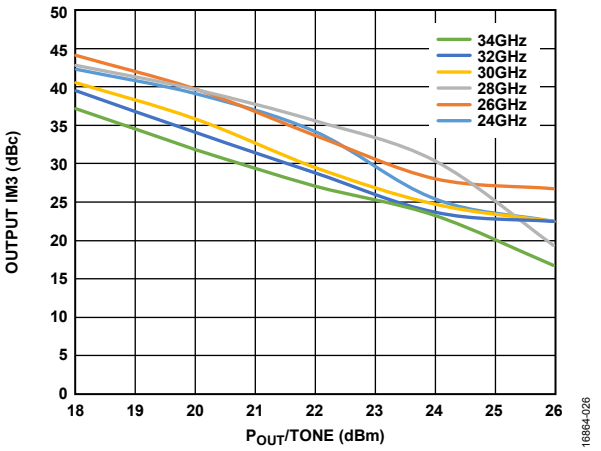

Figure 26. Output IM3 vs. P_{OUT} per Tone, V_{DD} = 5.0 V

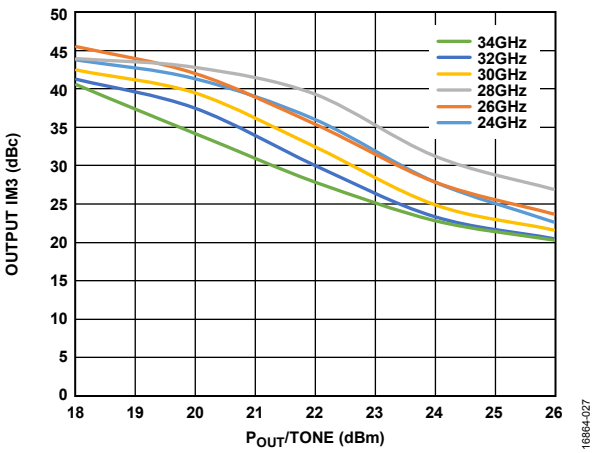

Figure 27. Output IM3 vs. P_{OUT} per Tone, V_{DD} = 6.0 V

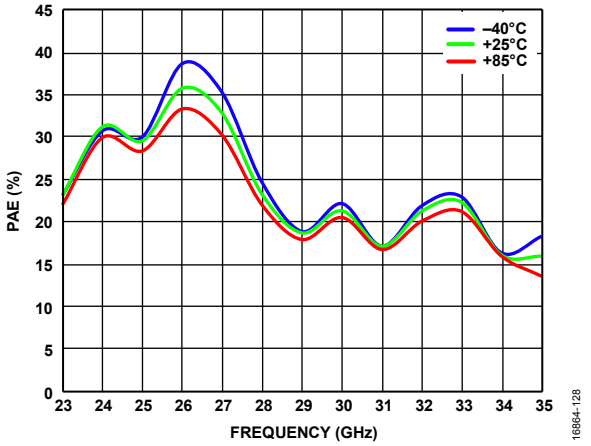

Figure 28. PAE vs. Frequency at Various Temperatures, PAE Measured at P_{SAT}

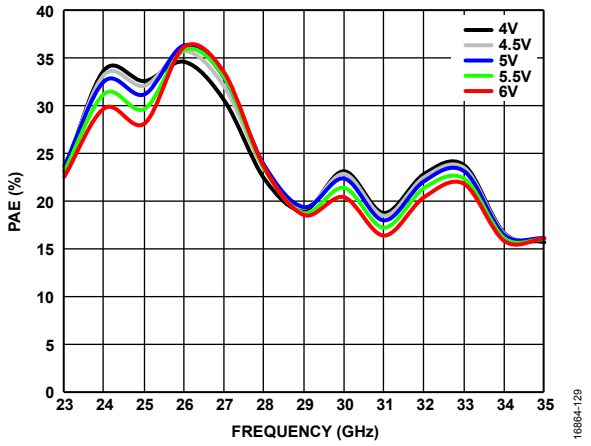

Figure 29. PAE vs. Frequency at Various Supply Voltages, PAE Measured at P_{SAT}

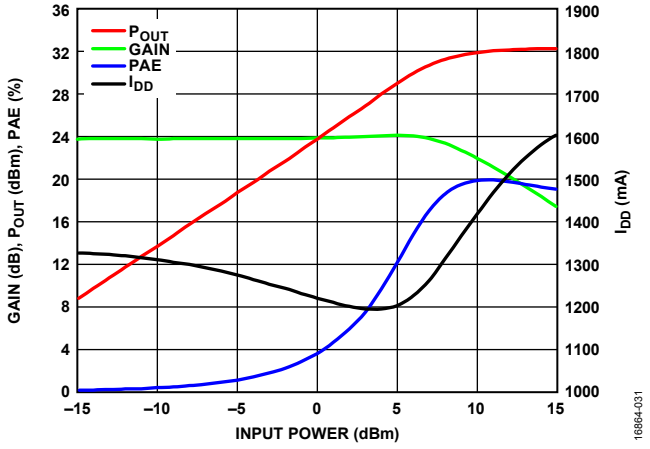

Figure 30. Gain, P_{OUT}, PAE, and Drain Current (I_{DD}) vs. Input Power, Power Compression at 29 GHz

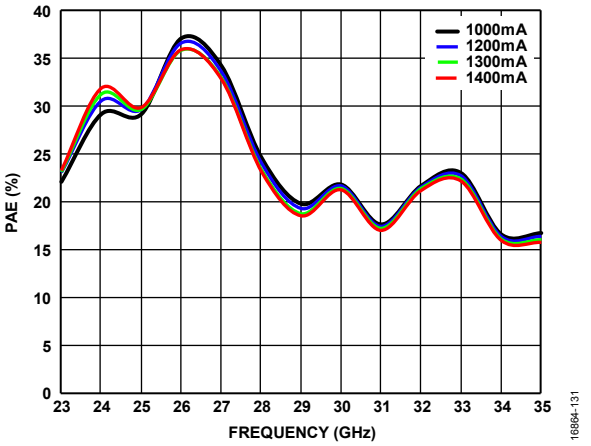

Figure 31. PAE vs. Frequency at Various Quiescent Currents, PAE Measured at P_{SAT}

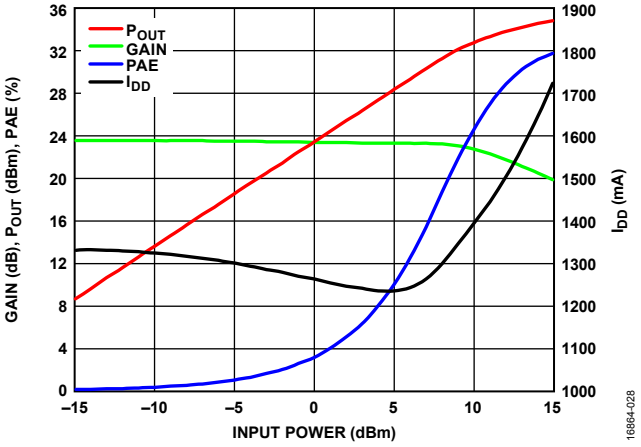

Figure 32. Gain, P_{OUT}, PAE, and I_{DD} vs. Input Power, Power Compression at 24 GHz

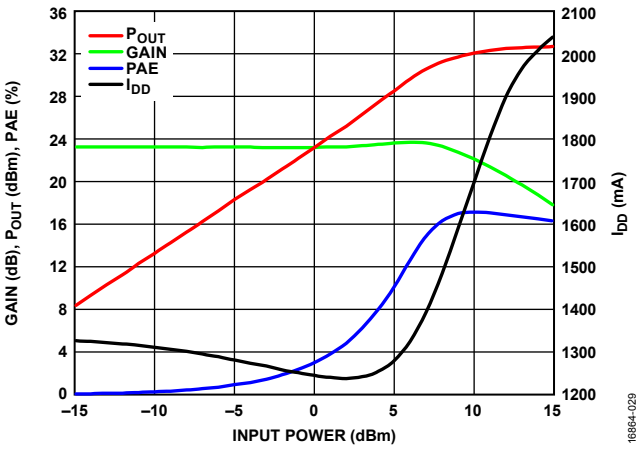

Figure 33. Gain, P_{OUT}, PAE, and I_{DD} vs. Input Power, Power Compression at 34 GHz

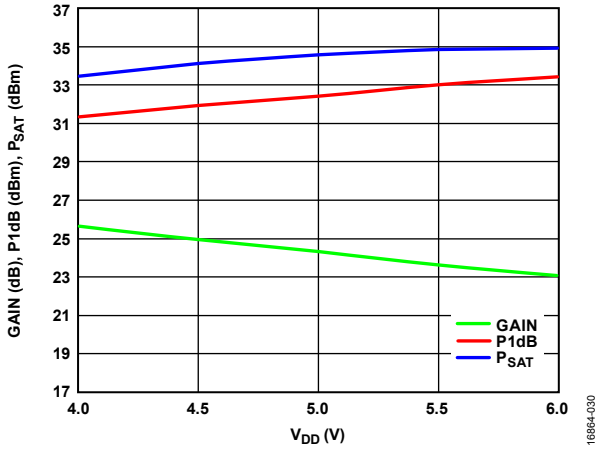

Figure 34. Gain, P1dB, and P_{SAT} vs. V_{DD} at 24 GHz

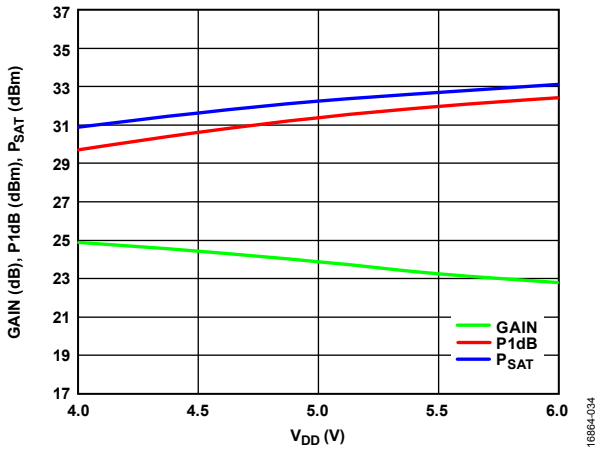

Figure 35. Gain, P1dB, and P_{SAT} vs. V_{DD} at 34 GHz

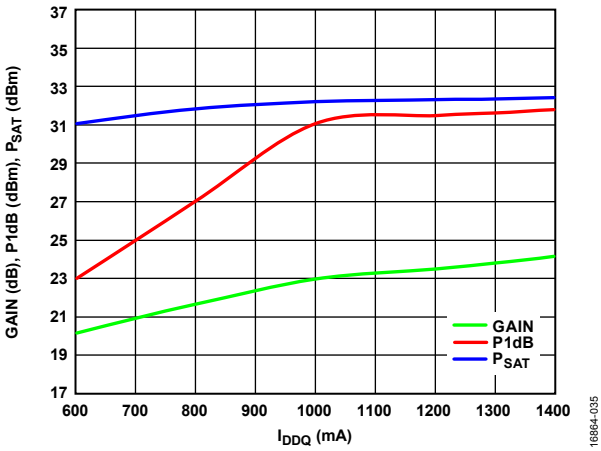

Figure 36. Gain, P1dB, and P_{SAT} vs. I_{DDQ} at 29 GHz

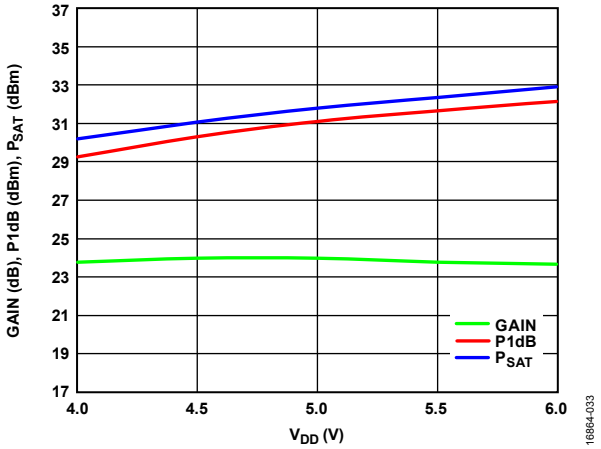

Figure 37. Gain, P1dB, and P_{SAT} vs. V_{DD} at 29 GHz

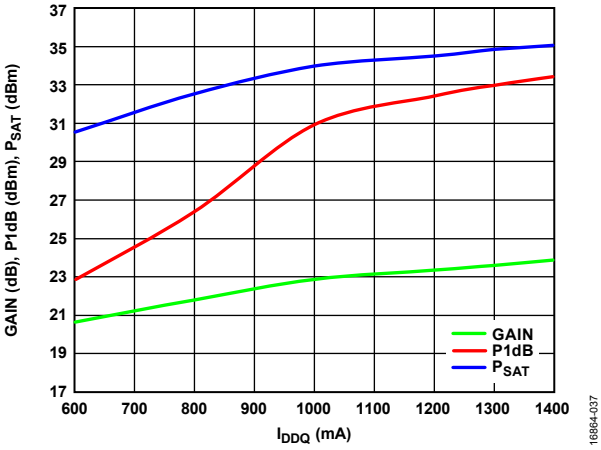

Figure 38. Gain, P1dB, and P_{SAT} vs. I_{DDQ} at 24 GHz

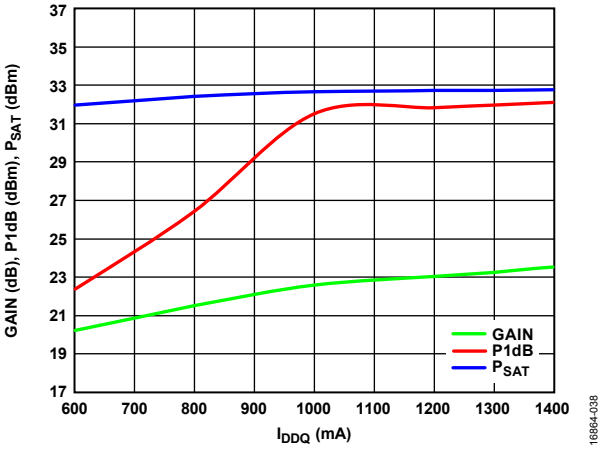

Figure 39. Gain, P1dB, and P_{SAT} vs. I_{DDQ} at 34 GHz

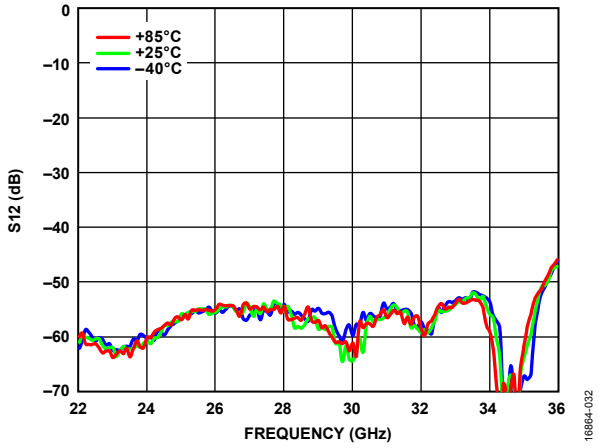

Figure 40. Reverse Isolation (S12) vs. Frequency at Various Temperatures

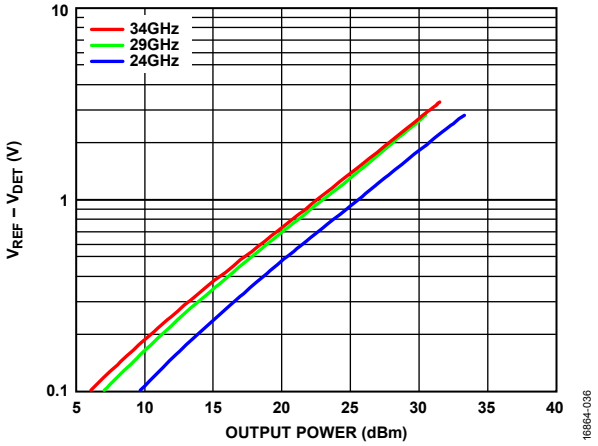

Figure 43. $V_{REF} - V_{DET}$ vs. Output Power at Various Frequencies

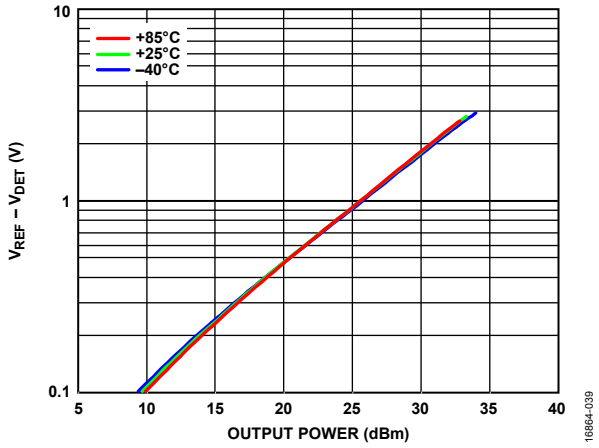

Figure 41. $V_{REF} - V_{DET}$ vs. Output Power at Various Temperatures at 24 GHz

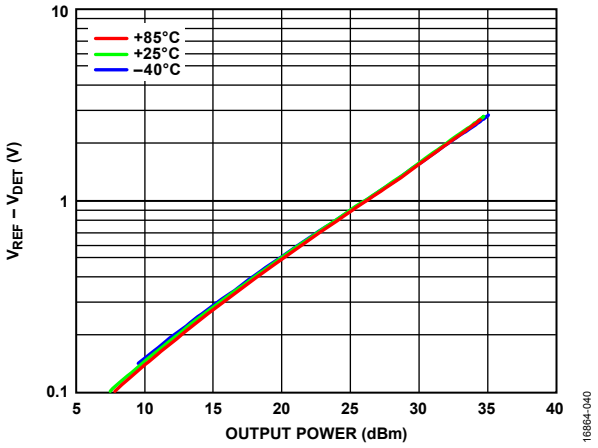

Figure 44. $V_{REF} - V_{DET}$ vs. Output Power at Various Temperatures at 29 GHz

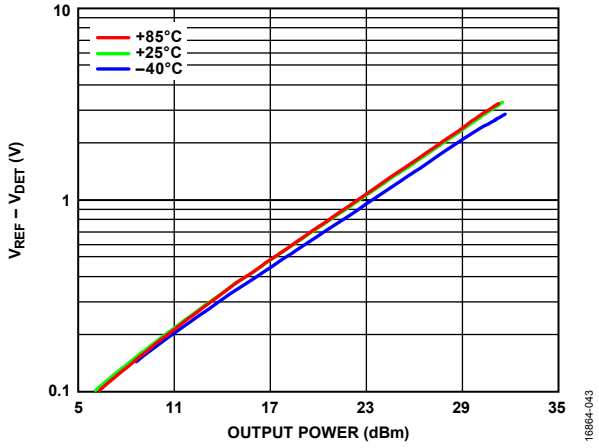

Figure 42. $V_{REF} - V_{DET}$ vs. Output Power at Various Temperatures at 34 GHz

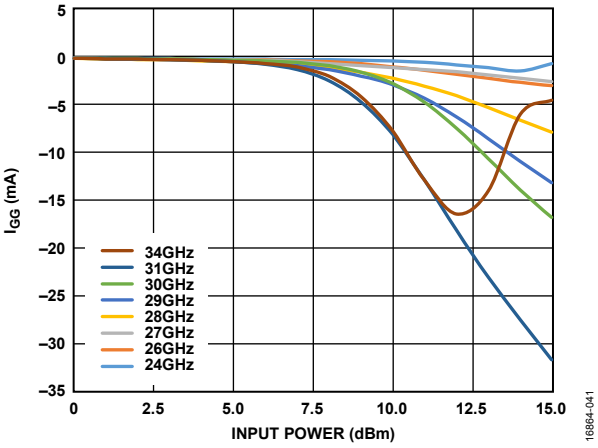

Figure 45. Gate Current (I_{GG}) vs. Input Power at Various Frequencies

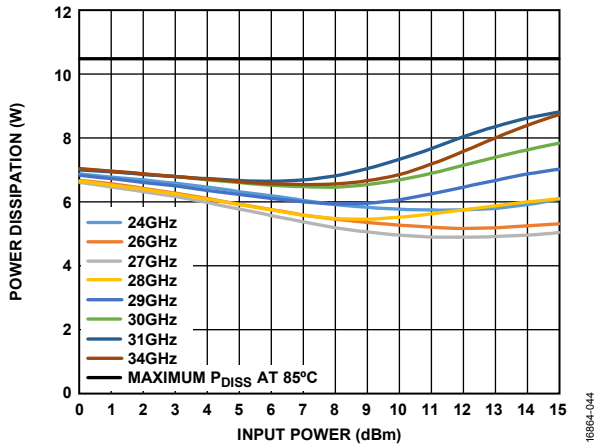

Figure 46. Power Dissipation vs. Input Power at Various Frequencies, T_A = 85°C

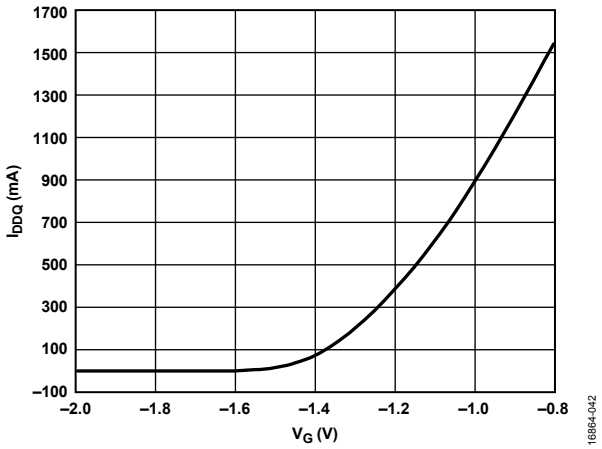

Figure 47. I_{DDQ} vs. Gate Bias Voltage (V_{Gx}), V_{Dx} = 5.5 V, Representative of a Typical Device

THEORY OF OPERATION

The HMC943APM5E is a GaAs, pHEMT, MMIC, >1.5 W power amplifier consisting of four cascaded gain stages. A simplified schematic is shown in Figure 48. The input signal is evenly divided and amplified through four gain stages. These amplified signals are then recombined at the output. Both inputs and outputs are internally matched to 50 Ω for ease of use.

Device drain connections for all stages are available at the package leads. Gate voltage bias can be applied to either V_{G1} or V_{G2} because the bias is internally connected to the gates of devices for all stages.

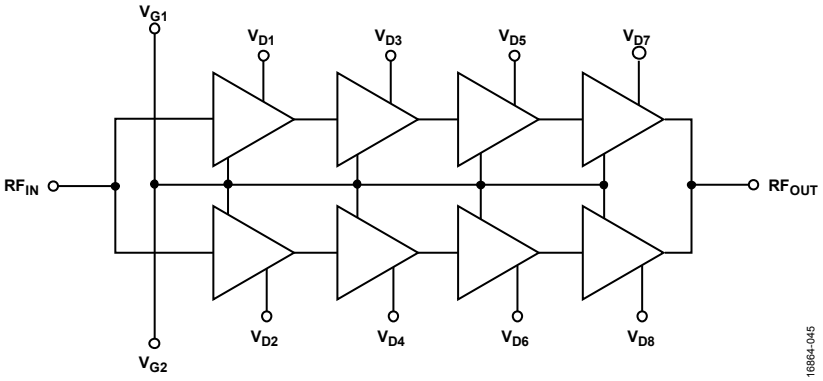

Figure 48. Simplified Schematic Diagram of Amplifier Stages

APPLICATIONS INFORMATION

The HMC943A is a GaAs, pHEMT, MMIC power amplifier. Capacitive bypassing is required for V_{Dx} as well as for V_{Gx} (see Figure 51). Drain bias voltage must be applied to all V_{Dx} pins, and gate bias voltage must be applied to V_{Gx}. Though the RF_{IN} and RF_{OUT} ports ac couple the signal, dc paths to GND are provided to increase the ESD robustness of the device. External dc blocking of both RF_{IN} and RF_{OUT} is desirable when appreciable levels of dc are expected to be present.

All measurements for this device are taken using the evaluation board schematic shown in Figure 51, configured as shown in the evaluation PCB in Figure 50.

The recommended bias sequence during power-up is as follows:

1. Connect the power supply ground to circuit ground (GND).
2. Set V_{G1} or V_{G2} to −2 V.
3. Set V_{Dx} to 5.5 V.
4. Slowly increase V_{G1} or V_{G2} from −2 V until typical I_{DDQ} = 1300 mA is reached.
5. Apply the RF signal.

The recommended bias sequence during power-down is as follows:

1. Turn the RF signal off.
2. Decrease V_{G1} or V_{G2} back to −2 V.
3. Decrease V_{Dx} to 0 V.
4. Decrease V_{G1} or V_{G2} to 0 V.

The bias conditions previously listed (V_{Dx} = 5.5 V, I_{DDQ} = 1300 mA) are the recommended operating points to achieve optimum performance. The data used in this data sheet is taken with the recommended bias conditions. When using the HMC943APM5E with different bias conditions, different performance conclusions may result other than from what is shown in the Typical Performance Characteristics section.

The V_{DET} and V_{REF} pins are the output pins for the internal power detector. The V_{DET} pin is the dc voltage output pin that represents the RF output power rectified by the internal diode and capacitor, which is biased through an external resistor. The V_{REF} pin is the dc voltage output pin that represents the reference diode voltage, which is biased through an external resistor. This voltage is then used to compensate for the temperature variation effects on both diodes. A typical circuit is shown in the Evaluation Board Schematic section that reads out the output voltage and represents the RF output power as shown in Figure 51.

POWER DETECTION

This device has internal output power detection, shown in Figure 49. Power detection is achieved through referencing V_{REF} − V_{DET} to the corresponding output power. The sensing circuit is composed of two diode connected circuit paths, V_{REF} and V_{DET}. V_{DET} changes when the RF output signal couples to the V_{DET} path. The coupled RF signal is then rectified by the detector diode and smoothed out by the shunt capacitor. Because the forward bias voltage for the detector diode is temperature dependent, V_{REF} is used as reference to compensate for temperature in calculation.

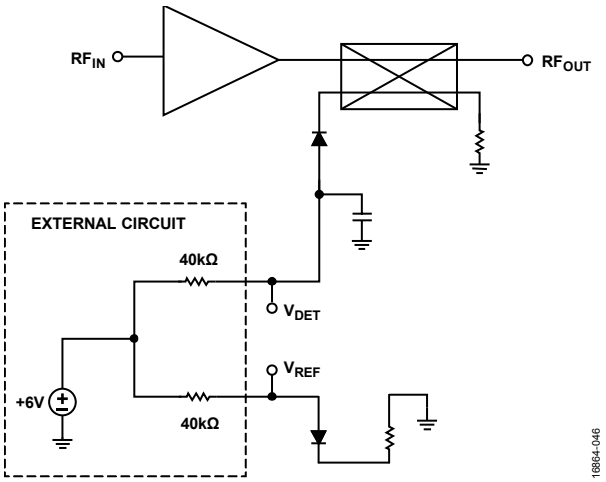

Figure 49. Power Detection Circuit

EVALUATION BOARD

The HMC943APM5E evaluation board is a 2-layer board fabricated using Rogers 4350 material and best practices for high frequency RF design. The RF input and RF output traces have a 50 Ω characteristic impedance. The circuit board is attached to a heat sink using SN96 solder and provides a low thermal resistance path. Components are mounted using SN63 solder, allowing rework of the surface-mount components without compromising the circuit board to heat sink attachment.

The evaluation board and populated components are designed to operate over the ambient temperature range of −40°C to +85°C. During operation, to control the temperature of the HMC943APM5E, attach the evaluation board to a temperature controlled plate. For proper bias sequence, see the Applications Information section.

The evaluation board schematic is shown in Figure 51. A fully populated and tested evaluation board (see Figure 50) is available from Analog Devices, Inc., upon request.

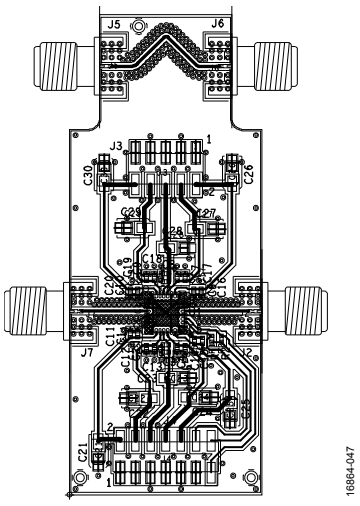

Figure 50. Evaluation PCB

Table 6. Bill of Materials for Evaluation PCB EV1HMC943APM5

Item	Description
J7, J2	Connectors, SRI K connector, SRI 25-146-1000-92
J3, J4	DC pins
C1 to C10	100 pF capacitors, 0402 package
C11 to C20	10,000 pF capacitors, 0402 package
C21 to C30	4.7 µF capacitors, Case A package
R1, R2	40.2 kΩ resistors, 0402 package
U1	HMC943APM5E amplifier
Heat Sink	Used for thermal transfer from the HMC943APM5E amplifier
PCB	EV1HMC943APM5[1]

[1] Circuit board material is Rogers 4350.

EVALUATION BOARD SCHEMATIC

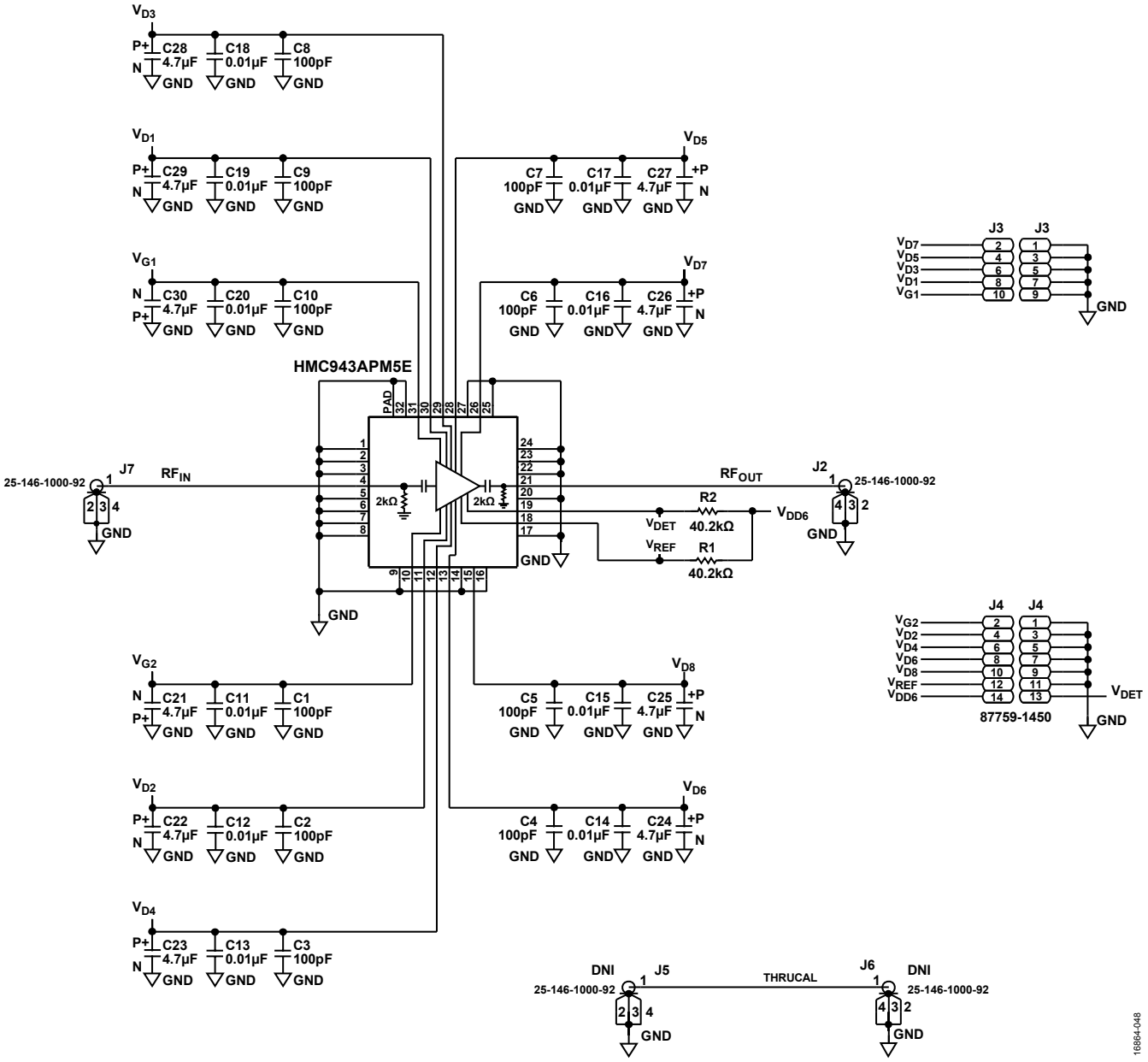

Figure 51. Evaluation Board Schematic

OUTLINE DIMENSIONS

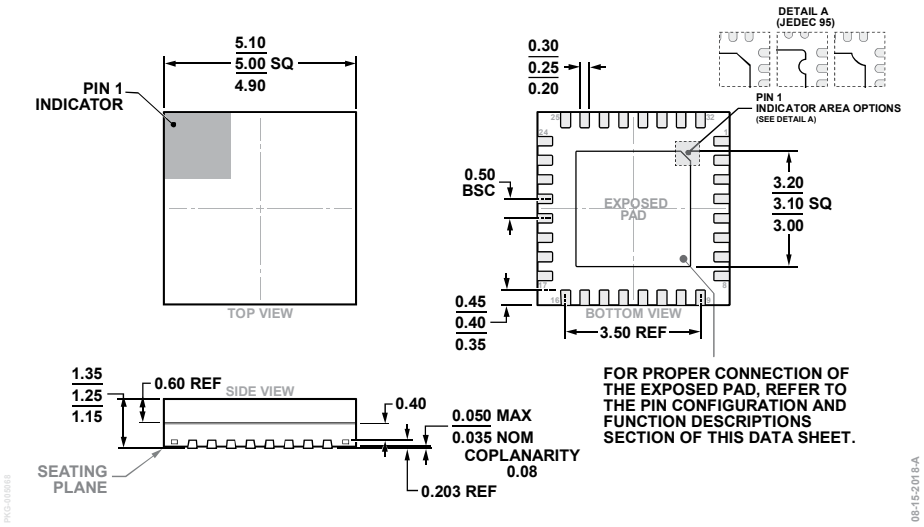

Figure 52. 32-Lead Lead Frame Chip Scale Package [LFCSP_CAV]
5 mm × 5 mm Body and 1.25 mm Package Height
(CG-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Moisture Sensitivity Level (MSL) Rating[3]	Package Description[4]	Package Option
HMC943APM5E	−40°C to +85°C	MSL3	32-Lead LFCSP_CAV	CG-32-2
HMC943APM5ETR	−40°C to +85°C	MSL3	32-Lead LFCSP_CAV	CG-32-2
EV1HMC943APM5			Evaluation Board	

[1] All models are RoHS compliant parts.
[2] When ordering the evaluation board, reference Model Number EV1HMC943APM5.
[3] See the Absolute Maximum Ratings section for additional information.
[4] The lead finish of the HMC943APM5E and the HMC943APM5ETR is nickel palladium gold (NiPdAu).

D16864-0-11/18(B)