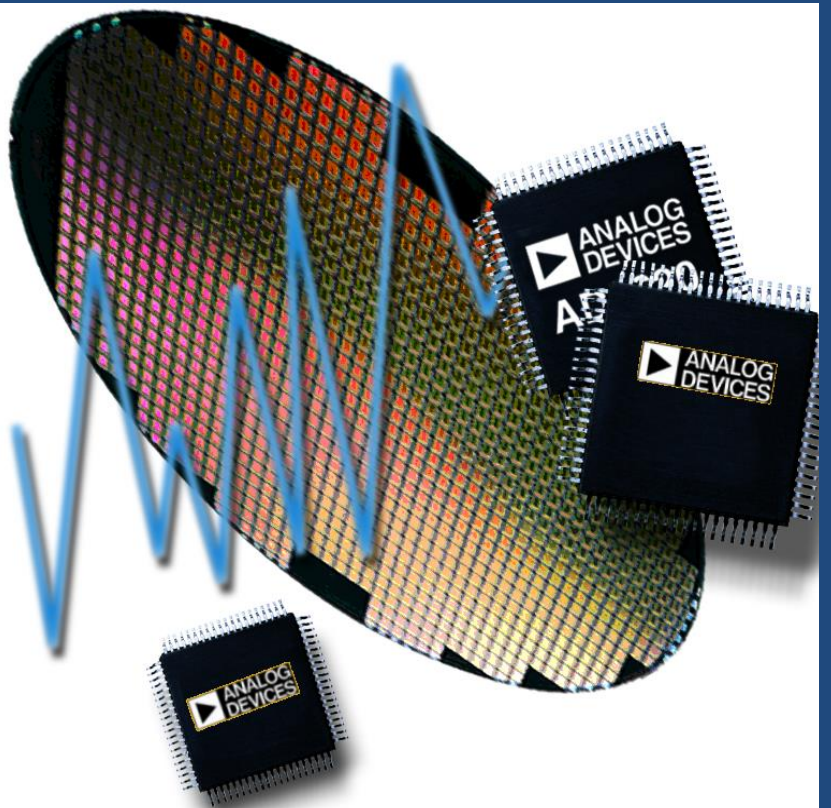


Analog Devices Welcomes Hittite Microwave Corporation

NO CONTENT ON THE ATTACHED DOCUMENT HAS CHANGED





Reliability Report

Report Title:	Qualification Test Report
Report Type:	See Attached
Date:	See Attached

Process FIT Rate Report

QTR: 2013- 00262

Rev: 02

Wafer Process: CMOS-B

HMC920

HMC980

HMC981

Hittite Microwave Corporation is committed to:

- *Supplying products of the highest quality*
- *Advance in state-of-the-art technology that supports our products*
- *Enhance our competitive position with superior product standards*

Hittite's employees recognize the responsibility to:

- *Take the initiative to ensure product quality*
- *Create an environment where the highest standards are maintained*
- *Continue to improve quality practices*

Introduction

The testing performed for this report is designed to accelerate the predominant failure mode, electro-migration (EM), for the devices under test. The devices are stressed at high temperature and DC biased to simulate a lifetime of use at typical operating temperatures. Using the Arrhenius equation, the acceleration factor (AF) is calculated for the stress testing based on the stress temperature and the typical use operating temperature.

This report is intended to summarize all of the High Temperature Operating Life Test (HTOL) data for the CMOS-B process. The FIT/MTTF data contained in this report includes all the stress testing performed on this process to date and will be updated periodically as additional data becomes available. Data sheets for the tested devices can be found at www.hittite.com.

Glossary of Terms & Definitions:

1. **CDM:** Charged Device Model. A specified ESD testing circuit characterizing an event that occurs when a device acquires charge through some triboelectric (frictional) or electrostatic induction processes and then abruptly touches a grounded object or surface. This test was performed in accordance with JEDEC 22-C101.
2. **ESD:** Electro-Static Discharge. A sudden transfer of electrostatic charge between bodies or surfaces at different electrostatic potentials.
3. **HBM:** Human Body Model. A specified ESD testing circuit characterizing an event that occurs when a device is subjected to an electro-static charge stored in the human body and discharged through handling of the electronic device. This test was performed in accordance with JEDEC 22-A114.
4. **HTOL:** High Temperature Operating Life. This test is used to determine the effects of bias conditions and temperature on semiconductor devices over time. It simulates the devices' operating condition in an accelerated way, through high temperature and/or bias voltage, and is primarily for device qualification and reliability monitoring. This test was performed in accordance with JEDEC JESD22-A108.
5. **HTSL:** High Temperature Storage Life. Devices are subjected to 1000 hours at 150°C per JESD22-A103.
6. **Operating Junction Temp (T_{oj}):** Temperature of the die active circuitry during typical operation.
7. **Stress Junction Temp (T_{sj}):** Temperature of the die active circuitry during stress testing.

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Qualification Sample Selection:

All qualification devices used were manufactured and tested on standard production processes and met pre-stress acceptance test requirements.

Summary of Qualification Tests:**HMC920 (QTR11006)**

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial Electrical	40	40	Complete	
HTOL, 1000 hours	40	40	Complete	
Post HTOL Electrical Test	40	40	Pass	

HMC980 (QTR2012-00023)

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial Electrical	193	193	Complete	
HTOL, 1000 hours	77	77	Complete	
Post HTOL Electrical Test	77	77	Pass	
HTOL, 1000 hours	80	80	Complete	
Post HTOL Electrical Test	80	80	Pass	
ESD	36	36	Complete	
Post ESD Electrical Test	36	36	Pass	HBM Class 1A CDM Class III MM 100V

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CMOS-B Failure Rate Estimate

Based on the HTOL test results, a failure rate estimation was determined using the following parameters:

With device ambient case temp, $T_c = 60^\circ\text{C}$

HMC920 (QTR11006)

Operating Junction Temp (T_{oj}) = $62^\circ\text{C}(335^\circ\text{K})$

Stress Junction Temp (T_{sj}) = $127^\circ\text{C}(400^\circ\text{K})$

HMC980 (QTR2012-00023)

Operating Junction Temp (T_{oj}) = $64^\circ\text{C}(337^\circ\text{K})$

Stress Junction Temp (T_{sj}) = $125^\circ\text{C}(398^\circ\text{K})$

Device hours:

HMC920 (QTR11006) = (40 X 1000hrs) = 40,000 hours

HMC980 (QTR2012-00023) = (77 X 1000hrs) = 77,000 hours

For CMOS-B MMIC, Activation Energy = 0.7 eV

Acceleration Factor (AF):

$$AF = \exp\left[\left(\frac{E_A}{k}\right) \cdot \left(\left(\frac{1}{T_{USE}}\right) - \left(\frac{1}{T_{STRESS}}\right)\right)\right]$$

HMC920 (QTR11006) Acceleration Factor = $\exp[0.7/8.6 \text{ e-}5(1/335-1/400)] = 51.8$

HMC980 (QTR2012-00023) Acceleration Factor = $\exp[0.7/8.6 \text{ e-}5(1/337-1/398)] = 40.5$

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Equivalent hours = Device hours x Acceleration Factor

$$\text{Equivalent hours} = (40,000 \times 51.8) + (77,000 \times 40.5) = 5.19 \times 10^6 \text{ hours}$$

Since there were no failures and we used a time terminated test, $F=0$, and $R = 2F+2 = 2$

The failure rate was calculated using Chi Square Statistic:

$$\lambda_{CL} = \frac{\chi^2_{\%CL, 2f+2} \cdot 10^9}{2 \cdot t \cdot SS \cdot AF}$$

at 60% and 90% Confidence Level (CL), with 0 units out of spec and a 60°C package backside temp;

Failure Rate

$$\lambda_{60} = [(\chi^2)_{60,2}] / (2 \times 5.19 \times 10^6) = 1.83 / 1.04 \times 10^7 = 1.76 \times 10^{-7} \text{ failures/hour or } 176 \text{ FIT or MTTF} = 5.68 \times 10^6 \text{ Hours}$$

$$\lambda_{90} = [(\chi^2)_{90,2}] / (2 \times 5.19 \times 10^6) = 4.61 / 1.04 \times 10^7 = 4.44 \times 10^{-7} \text{ failures/hour or } 444 \text{ FIT or MTTF} = 2.25 \times 10^6 \text{ Hours}$$

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