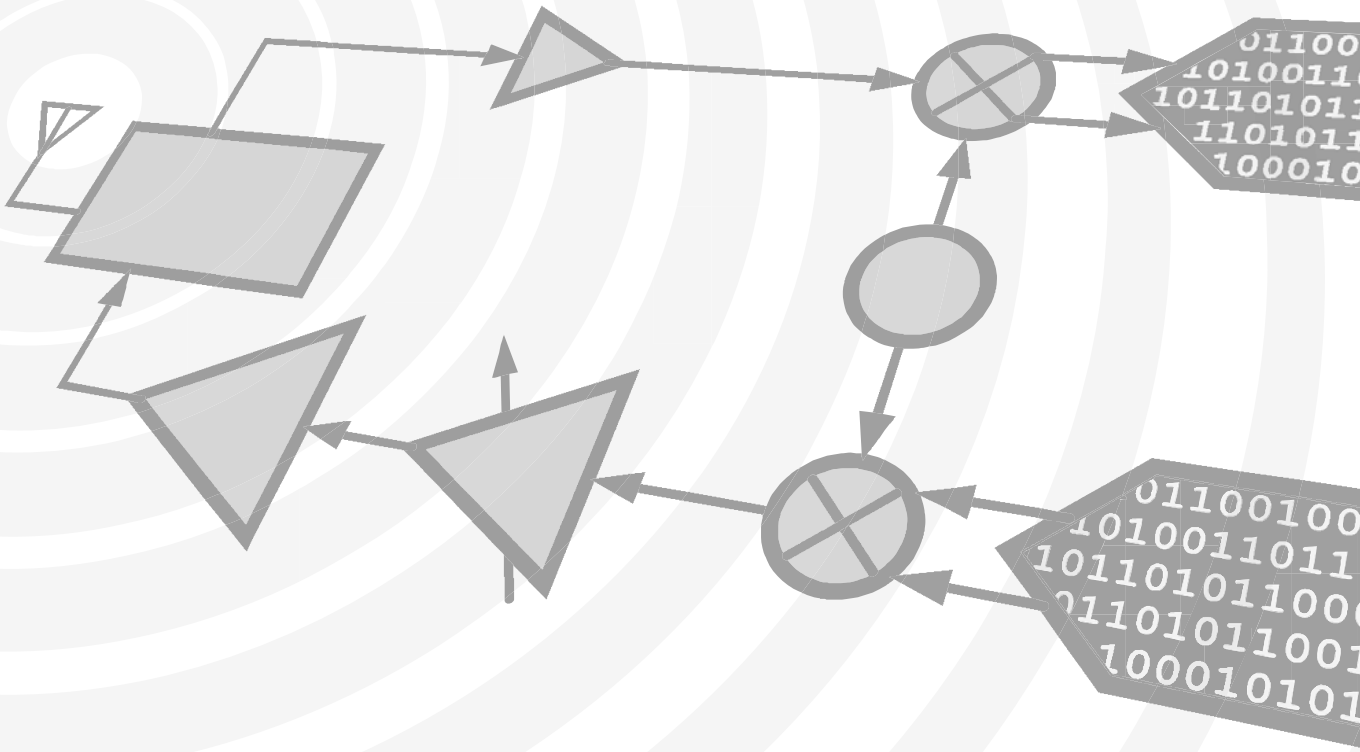
ANALOG DEVICES

Hittite MICROWAVE PRODUCTS FROM ANALOG DEVICES

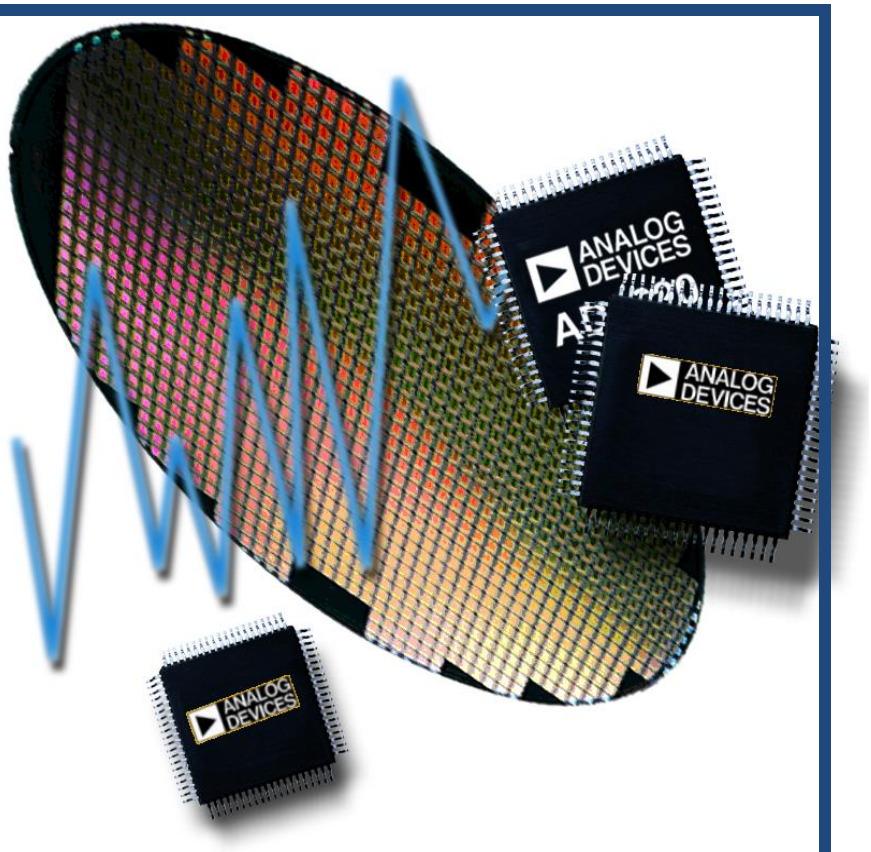
Analog Devices Welcomes Hittite Microwave Corporation

NO CONTENT ON THE ATTACHED DOCUMENT HAS CHANGED



www.analog.com

www.hittite.com



Reliability Report

Report Title: Qualification Test Report

Report Type: See Attached

Date: See Attached

Process FIT Rate Report

QTR: 2013- 00139 **Rev: 02**

Wafer Process: CMOS-C

HMCAD1040-40
HMCAD1040-80
HMCAD1041-40
HMCAD1041-80
HMCAD1050-40
HMCAD1050-80
HMCAD1051-40
HMCAD1051-80
HMCAD1100
HMCAD1101
HMCAD1102
HMCAD1104
HMCAD1510
HMCAD1511
HMCAD1512
HMCAD1513
HMCAD1520

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Process FIT Rate Report

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- *Supplying products of the highest quality*
- *Advance in state-of-the-art technology that supports our products*
- *Enhance our competitive position with superior product standards*

Hittite's employees recognize the responsibility to:

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- *Continue to improve quality practices*

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Introduction

The testing performed for this report is designed to accelerate the predominant failure mode, electro-migration (EM), for the devices under test. The devices are stressed at high temperature and DC biased to simulate a lifetime of use at typical operating temperatures. Using the Arrhenius equation, the acceleration factor (AF) is calculated for the stress testing based on the stress temperature and the typical use operating temperature.

This report is intended to summarize all of the High Temperature Operating Life Test (HTOL) data for the CMOS-C process. The FIT/MTTF data contained in this report includes all the stress testing performed on this process to date and will be updated periodically as additional data becomes available. Data sheets for the tested devices can be found at www.hittite.com.

Glossary of Terms & Definitions:

1. **CDM:** Charged Device Model. A specified ESD testing circuit characterizing an event that occurs when a device acquires charge through some triboelectric (frictional) or electrostatic induction processes and then abruptly touches a grounded object or surface. This test was performed in accordance with JEDEC 22-C101D.
2. **ESD:** Electro-Static Discharge. A sudden transfer of electrostatic charge between bodies or surfaces at different electrostatic potentials.
3. **HBM:** Human Body Model. A specified ESD testing circuit characterizing an event that occurs when a device is subjected to an electro-static charge stored in the human body and discharged through handling of the electronic device. This test was performed in accordance with JEDEC 22-A114E.
4. **HTOL:** High Temperature Operating Life. This test is used to determine the effects of bias conditions and temperature on semiconductor devices over time. It simulates the devices' operating condition in an accelerated way, through high temperature and/or bias voltage, and is primarily for device qualification and reliability monitoring. This test was performed in accordance with JEDEC JESD22-A108D.
5. **Latch-up:** A state in which a low-impedance path, resulting from an overstress that triggers a parasitic thyristor structure, persists after removal or cessation of the triggering condition. The overstress can be a voltage or current surge, an excessive rate of change of current or voltage, or any other abnormal condition that causes the parasitic thyristor structure to become regenerative. This test was performed in accordance with JEDEC JESD78D, Class 1.
6. **Operating Junction Temp (T_{oj}):** Temperature of the die active circuitry during typical operation.
7. **Stress Junction Temp (T_{sj}):** Temperature of the die active circuitry during stress testing.

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Qualification Sample Selection:

All qualification devices used were manufactured and tested on standard production processes and met pre-stress acceptance test requirements.

Summary of Qualification Tests:

HMCAD1050 Qualification (QTR2012-00067)

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial Electrical	80	80	Complete	
HTOL, 168 hours, 125°C T_j	80	80	Complete	
Interim Electrical Test	80	80	Pass	
HTOL, 332 hours, 125°C T_j	80	80	Complete	
Interim Electrical Test	80	80	Pass	
HTOL, 500 hours, 125°C T_j	80	80	Complete	
Interim Electrical Test	80	80	Pass	
HTOL, 1000 hours, 125°C T_j	80	80	Complete	
Post Electrical Test	80	80	Pass	
Pre ESD Electrical Test	9	9	Complete	
ESD, HBM	9	9	Complete	Devices tested from 500-2000V
Post ESD HBM Electrical Test	9	9	Pass	Devices passed 2000V
Pre Latch-up Electrical Test	6	6	Complete	

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TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Latch-up Test	6	6	Complete	
Post Latch-up Electrical Test	6	6	Pass	

HMCAD1100 Qualification (QTR2013-00136)

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial Electrical	80	80	Complete	
HTOL, 168 hours, 125°C T_j	80	80	Complete	
Interim Electrical Test	80	80	Pass	
HTOL, 332 hours, 125°C T_j	80	80	Complete	
Interim Electrical Test	80	80	Pass	
HTOL, 500 hours, 125°C T_j	80	80	Complete	
Interim Electrical Test	80	80	Pass	
HTOL, 1000 hours, 125°C T_j	80	80	Complete	
Post Electrical Test	80	80	Pass	

HMCAD1520 Qualification (QTR2012-00064)

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial Electrical	77	77	Complete	

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Wafer Process: CMOS-C

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
HTOL, 168 hours, 125°C T_j	77	77	Complete	
Interim Electrical Test	77	77	Pass	
HTOL, 500 hours, 125°C T_j	77	77	Complete	
Interim Electrical Test	77	77	Pass	
HTOL, 1000 hours, 125°C T_j	77	77	Complete	
Post Electrical Test	77	77	Pass	
Pre ESD Electrical Test	9	9	Complete	
ESD, HBM	12	12	Complete	Devices tested from 500-2000V
Post ESD HBM Electrical Test	12	12	Pass	Devices passed 2000V (Level 1C)
ESD, CDM	12	12	Complete	Devices tested from 250-1000V
Post ESD CDM Electrical Test	12	12	Pass	Devices passed 1000V (Class III)
Pre Latch-up Electrical Test	6	6	Complete	
Latch-up Test	6	6	Complete	
Post Latch-up Electrical Test	6	6	Pass	

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HMCAD1520 Qualification (QTR2013-00138)

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial Electrical	77	77	Complete	
HTOL, 168 hours, 125°C T_j	77	77	Complete	
Interim Electrical Test	77	77	Pass	
HTOL, 500 hours, 125°C T_j	77	77	Complete	
Interim Electrical Test	77	77	Pass	
HTOL, 1000 hours, 125°C T_j	77	77	Complete	
Post Electrical Test	77	77	Pass	

HMCAD1050 Qualification (QTR2012-00166)

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial Electrical	24	24	Complete	
HTOL, 2000 hours, 125°C T_j	24	24	Complete	
Post Electrical Test	24	24	Pass	

HMCAD1050 Qualification (QTR2012-00166, Additional hours)

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial Electrical	20	20	Complete	

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TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
HTOL, 2000 hours, 125°C T_j	20	20	Complete	
Post Electrical Test	20	20	Pass	

HMCAD1051 Qualification (QTR2012-00166)

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial Electrical	24	24	Complete	
HTOL, 2000 hours, 125°C T_j	24	24	Complete	
Post Electrical Test	24	24	Pass	

HMCAD1051 Qualification (QTR2012-00166, Additional hours)

TEST	QTY IN	QTY OUT	PASS/FAIL	NOTES
Initial Electrical	20	20	Complete	
HTOL, 2000 hours, 125°C T_j	20	20	Complete	
Post Electrical Test	20	20	Pass	

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CMOS-C Failure Rate Estimate

Based on the HTOL test results, a failure rate estimation was determined using the following parameters:

With device ambient case temp, Tc = 65°C

HMCAD1050 (QTR2012-00067)
Operating Junction Temp (T_{oj}) =75°C (348 °K)
Stress Junction Temp (T_{sj}) = 125°C (398 °K)

HMCAD1100 (QTR2013-00136)
Operating Junction Temp (T_{oj}) =75°C (348 °K)
Stress Junction Temp (T_{sj}) = 125°C (398 °K)

HMCAD1520 (QTR2012-00064)
Operating Junction Temp (T_{oj}) =75°C (348 °K)
Stress Junction Temp (T_{sj}) = 125°C (398 °K)

HMCAD1520 (QTR2013-00138)
Operating Junction Temp (T_{oj}) = 75°C (348 °K)
Stress Junction Temp (T_{sj}) = 125°C (398 °K)

HMCAD1050 (QTR2012-00166)
Operating Junction Temp (T_{oj}) =75°C (348 °K)
Stress Junction Temp (T_{sj}) = 125°C (398 °K)

HMCAD1050 (QTR2012-00166, Additional hours)
Operating Junction Temp (T_{oj}) =75°C (348 °K)
Stress Junction Temp (T_{sj}) = 125°C (398 °K)

HMCAD1051 (QTR2012-00166)
Operating Junction Temp (T_{oj}) =75°C (348 °K)
Stress Junction Temp (T_{sj}) = 125°C (398 °K)

HMCAD1051 (QTR2012-00166, Additional hours)
Operating Junction Temp (T_{oj}) =75°C (348 °K)

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Stress Junction Temp (T_{sj}) = 125°C (398 °K)

Device hours:

HMCAD1050 (QTR2012-00067) = (80 X 1000hrs) = 80,000 hours
HMCAD1100 (QTR2013-00136) = (80 X 1000hrs) = 80,000 hours
HMCAD1520 (QTR2012-00064) = (77 X 1000hrs) = 77,000 hours
HMCAD1520 (QTR2013-00138) = (77 X 1000hrs) = 77,000 hours
HMCAD1050 (QTR2012-00166) = (24 X 2000hrs) = 48,000 hours
HMCAD1050 (QTR2012-00166, Additional hours) = (20 X 2000hrs) = 40,000 hours
HMCAD1051 (QTR2012-00166) = (24 X 2000hrs) = 48,000 hours
HMCAD1051 (QTR2012-00166, Additional hours) = (20 X 2000hrs) = 40,000 hours

For CMOS-C MMIC, Activation Energy = 0.7 eV

Acceleration Factor (AF):

$$AF = \exp\left[\left(\frac{E_A}{k}\right)\cdot\left(\left(\frac{1}{T_{USE}}\right)-\left(\frac{1}{T_{STRESS}}\right)\right)\right]$$

HMCAD1050 (QTR2012-00067) Acceleration Factor = exp[0.7/8.6 e^{-5}(1/348-1/398)] = 18.9
HMCAD1100 (QTR2013-00136) Acceleration Factor = exp[0.7/8.6 e^{-5}(1/348-1/398)] = 18.9
HMCAD1520 (QTR2012-00064) Acceleration Factor = exp[0.7/8.6 e^{-5}(1/348-1/398)] = 18.9
HMCAD1520 (QTR2013-00138) Acceleration Factor = exp[0.7/8.6 e^{-5}(1/348-1/398)] = 18.9
HMCAD1050 (QTR2012-00166) Acceleration Factor = exp[0.7/8.6 e^{-5}(1/348-1/398)] = 18.9
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HMCAD1051 (QTR2012-00166) Acceleration Factor = exp[0.7/8.6 e^{-5}(1/348-1/398)] = 18.9
HMCAD1051 (QTR2012-00166) Acceleration Factor = exp[0.7/8.6 e^{-5}(1/348-1/398)] = 18.9

Equivalent hours = Device hours x Acceleration Factor

Equivalent hours =
(80,000x18.9)+(80,000x18.9)+(77,000x18.9)+(77,000x18.9)+(48,000x18.9)+(40,000x18.9)
+(48,000x18.9)+(40,000x18.9)= 9.25×10^6 hours

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Since there were no failures and we used a time terminated test, F=0, and R = 2F+2 = 2

The failure rate was calculated using Chi Square Statistic:

$$\lambda_{CL} = \frac{\chi^2_{\%CL,2f+2} \cdot 10^9}{2 \cdot t \cdot ss \cdot AF}$$ at 60% and 90% Confidence Level (CL), with 0 units out of spec and a 65°C package backside temp;

Failure Rate

$\lambda_{60} = [(\chi^2)_{60,2}]/(2X \quad 9.25x10^6 \ )] = 1.83/\ 1.85x10^7 = \ 9.89x10^{-8}$ failures/hour or 99 FIT, or MTTF = $1.01x10^7$ hours

$\lambda_{90} = [(\chi^2)_{90,2}]/(2X \quad 9.25x10^6 \ )] = 4.61/\ 1.85x10^7 = \ 2.49x10^{-7}$ failures/hour or 249 FIT, or MTTF = $4.01x10^6$ hours

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