HMCAD1513

v00.0414

8-BIT A-TO-D CONVERTER (ADC) DUAL 500 MSPS / QUAD 250 MSPS

Features

- 8-bit High Speed Dual / Quad ADC
  Dual Channel Mode: F_{Smax} = 500 MSPS
  Quad Channel Mode: F_{Smax} = 250 MSPS
- Integrated Cross Point Switches (Mux Array)
- 1X to 50X Digital Gain –
  No Missing Codes up to 32X
- 2X Gain: 49.8 dB SNR. 10X Gain: 48 dB SNR
- Internal Low Jitter Programmable Clock Divider
- Ultra Low Power Dissipation
  710 mW including I/O at 500 MSPS
- 0.5 µs Start-up Time from Sleep,
  15 µs from Power Down
- Internal Reference Circuitry with no
  External Components Required
- Coarse and Fine Gain Control
- Digital Fine Gain Adjustment for each ADC
- Internal Offset Correction
- 1.8 V Supply Voltage
- 1.7 - 3.6 V CMOS Logic on Control Interface Pins
- Serial LVDS/RSDS Output
- 7x7 mm QFN 48 (LP7D) Package

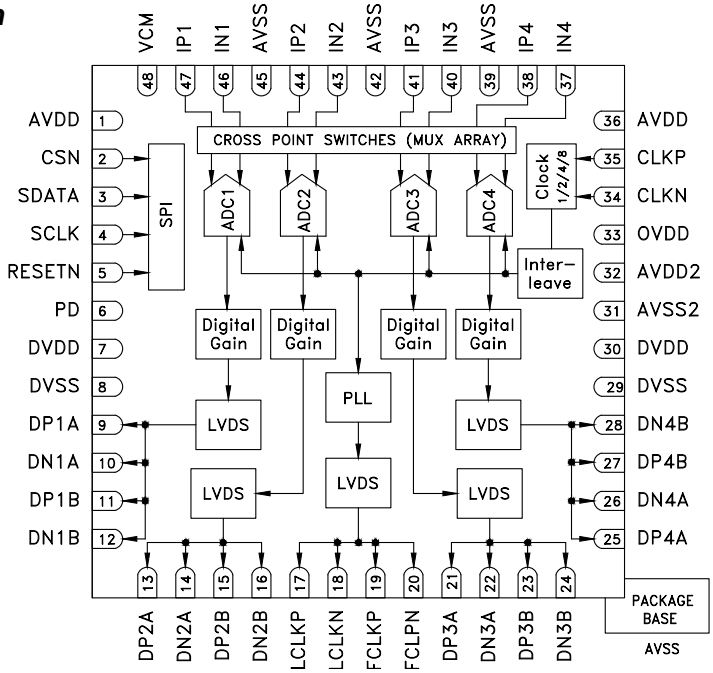
Typical Applications

- Microwave backhaul
- Satellite Receivers

Pin Compatible Parts

Device	Channels	Resolution (bits)	Sample Rate (MSPS)	ECCN
HMCAD1062	4	14	80/105/125	3A991.c.3
HMCAD1068	2	14	80/105/125	3A991.c.3
HMCAD1052	4	12	160	3A001.a.5.a.3
HMCAD1054	2	12	320	3A001.a.5.a.3
HMCAD1056	1	12	640	3A001.a.5.a.3
HMCAD1510	4 / 2 / 1	8	125/250/500	3A991.c.1
HMCAD1511	4 / 2 / 1	8	250/500/1000	3A001.a.5.a.1
HMCAD1512	2 / 1	8	450 / 900	3A001.a.5.a.1
HMCAD1513	4 / 2	8	250 / 500	3A991.c.1
HMCAD1520	4 4 / 2 / 1	14 12	80/105 160/320/640	3A001.a.5.a.4

Functional Diagram



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ANALOG DEVICES

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8-BIT A-TO-D CONVERTER (ADC) DUAL 500 MSPS / QUAD 250 MSPS

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8-BIT A-TO-D CONVERTER (ADC) DUAL 500 MSPS / QUAD 250 MSPS

General Description

The HMCAD1513 is a versatile high performance low power analog-to-digital converter (ADC), utilizing time-interleaving to increase sampling rate. Integrated Cross Point Switches activate the input selected by the user.

In dual channel mode, any two of the four inputs can be selected to each ADC channel. In quad channel mode, any input can be assigned to any ADC channel.

An internal, low jitter and programmable clock divider makes it possible to use a single clock source for all operational modes.

The HMCAD1513 is based on a proprietary structure, and employs internal reference circuitry, a serial control interface and serial LVDS/RSDS output data. Data and frame synchronization clocks are supplied for data capture at the receiver. Internal 1 to 50X digital coarse gain with ENOB > 7.5 up to 16X gain, allows digital implementation of oscilloscope gain settings. Internal digital fine gain can be set separately for each ADC to calibrate for gain errors.

Various modes and configuration settings can be applied to the ADC through the serial control interface (SPI). Each channel can be powered down independently and data format can be selected through this interface. A full chip idle mode can be set by a single external pin. Register settings determine the exact function of this pin.

HMCAD1513 is designed to easily interface with Field Programmable Gate Arrays (FPGAs) from several vendors.

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Electrical Specifications

Operating Conditions

Parameter	Description	Min	Typ	Max	Unit
V_{AVDD}	Analog supply voltage range	1.7	1.8	2.0	V
V_{DVDD}	Digital and output driver voltage range	1.7	1.8	2.0	V
V_{OVDD}	Digital CMOS Inputs supply voltage range	1.7	1.8	3.6	V
T_A	Ambient temperature	-40		+85	°C

Note: The conditions listed in this table must be observed for the device to be functional as specified in this document. These conditions do not guarantee specific performance levels – which are listed in the DC Electrical Specifications, AC Specifications, and Digital and Switching Specifications, and apply under the test conditions specified therein.

Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Unit
T_j	Junction temperature			+110	°C
$T_{storage}$	Storage temperature	-65		+150	°C
AVDD	Analog supply voltage in reference to AVSS	-0.3		+2.3	V
DVDD	Digital supply voltage in reference to DVSS	-0.3		+2.3	V
OVDD	Digital CMOS Inputs supply voltage in reference to AVSS	-0.3		+3.9	V
|AVSS-DVSS|	Supply difference – AVSS and DVSS are connected internally			0.0	V
V_{analog}	Analog inputs and outputs in reference to AVSS	-0.3		AVDD+0.3 or +2.3	V
V_{clock}	Clock input pins voltage in reference to AVSS	-0.3		OVDD+0.3 or 3.9	V
VLVDS	LVDS output pins voltage in reference to DVSS	-0.3		DVDD+0.2 or +2.3	V
$V_{digital-in}$	Digital input pins voltage in reference to DVSS	-0.3		OVDD+0.3 or 3.9	V
ESD Rating	Human body model	2000			V
	Charged device model	1000			V
–	Soldering profile characteristics	J-STD-020			

Note: Operating the device beyond the limits specified in this table may cause immediate damage to the device. Functional operation of the device is further limited by the Operating Conditions. Device functionality is not implied by the Absolute Maximum Ratings.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Thermal Information

Parameter	Description	Min	Typ	Max	Unit
θ_{JA}	Thermal resistance – junction-to-ambient			21	°C/W
θ_{JCb}	Thermal resistance – junction-to-case bottom pad			3.2	°C/W

Note: The thermal pad at the bottom of the device package must be attached to the PCB ground plane. It is also recommended that the thermal pad should be connected to a metal pad on the underside of the PCB through multiple vias for heat conduction purposes as this is the most optimal path for heat dissipation of this device.

DC Electrical Specifications

AVDD = 1.8 V, DVDD = 1.8 V, OVDD = 1.8 V, FS = 125 MSPS, Quad Channel Mode, 50% clock duty cycle, -1 dBFS 70 MHz input signal, 1x/0 dB digital gain (fine and coarse), unless otherwise noted.

Parameter	Description	Min	Typ	Max	Unit
DC accuracy					
No missing codes			Guaranteed		
Offset	Offset error after internal digital offset correction		0.05		LSB
G_{abs}	Gain error			±6	%FS
G_{rel}	Gain matching between channels. ±3 σ value at worst case conditions		±0.5		%FS
Gain flatness	DC to 300 MHz DC to 425 MHz		±0.5 ±1.0		dB
INL	Integral non linearity		±0.5		LSB
DNL	Differential non linearity		±0.5		LSB
$V_{CM,out}$	Common mode voltage output		$V_{AVDD}/2$		
Analog Input					
$V_{CM,in}$	Analog input common mode voltage	V_{CM} – 0.1		V_{CM} +0.2	V
FSR	Differential input voltage full scale range		2		Vpp-diff
FSR2X	Differential input voltage full scale range, gain = 2X		1		Vpp-diff
C_{in}	Differential Input capacitance Dual/Quad channel mode		7/5		pF
R_{in}	Differential input resistance 250/500 MSPS		1.8/0.9		kΩ

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AC Specifications

AVDD = 1.8 V, DVDD = 1.8 V, OVDD = 1.8 V, 50% clock duty cycle, -1 dBFS 71 MHz input signal, Gain = 1X, RSDS output data levels, unless otherwise noted. Minimum/maximum specifications are valid for full condition range.

Parameter	Description		Min	Typ	Max	Unit
Performance						
SNR	Signal to Noise Ratio					
	Dual Ch Mode, F_S = 500 MSPS	Gain=2X (FSR = 1 Vpp-diff)		49.8		dBFS
		Gain=1X (FSR = 2 Vpp-diff)	48.5	49.8		dBFS
	Quad Ch Mode, F_S = 250 MSPS	Gain=2X (FSR = 1 Vpp-diff)		49.9		dBFS
		Gain=1X (FSR = 2 Vpp-diff)	48.5	49.9		dBFS
SNDR	Signal to Noise and Distortion Ratio					
	Dual Ch Mode, F_S = 500 MSPS	Gain=2X (FSR = 1 Vpp-diff)		48.5		dBFS
		Gain=1X (FSR = 2 Vpp-diff)	43	48.5		dBFS
	Quad Ch Mode, F_S = 250 MSPS	Gain=2X (FSR = 1 Vpp-diff)		49.5		dBFS
		Gain=1X (FSR = 2 Vpp-diff)	47	49.6		dBFS
SFDR	Spurious Free Dynamic Range					
	Dual Ch Mode, F_S = 500 MSPS	Gain=2X (FSR = 1 Vpp-diff)		56		dBc
		Gain=1X (FSR = 2 Vpp-diff)	43.5	56		dBc
	Quad Ch Mode, F_S = 250 MSPS	Gain=2X (FSR = 1 Vpp-diff)		59		dBc
		Gain=1X (FSR = 2 Vpp-diff)	49	59		dBc
HD2/3	Worst of HD2/HD3					
	Dual Ch Mode, F_S = 500 MSPS	Gain=2X (FSR = 1 Vpp-diff)		72		dBc
		Gain=1X (FSR = 2 Vpp-diff)	60	69		dBc
	Quad Ch Mode, F_S = 250 MSPS	Gain=2X (FSR = 1 Vpp-diff)		82		dBc
		Gain=1X (FSR = 2 Vpp-diff)	55	75		dBc
ENOB	Effective number of Bits					
	Dual Ch Mode, F_S = 500 MSPS	Gain=2X (FSR = 1 Vpp-diff)		7.8		bits
		Gain=1X (FSR = 2 Vpp-diff)	6.9	7.8		bits
	Quad Ch Mode, F_S = 250 MSPS	Gain=2X (FSR = 1 Vpp-diff)		7.9		bits
		Gain=1X (FSR = 2 Vpp-diff)	7.5	7.9		bits
$X_{tlk,2}$	CrossTalk Dual Ch Mode. –1 dBFS 70 MHz signal applied to input 1 or 4, –1 dBFS 71 MHz signal applied to alternate input. Valid for input 1 and 4.			–90		dBc
$X_{tlk,4}$	CrossTalk Quad Ch Mode. –1 dBFS 70 MHz signal applied to input 1, 2, 3 or 4, –1 dBFS 71 MHz signal applied to alternate input. Valid for all input combinations.			–73		dBc
Power Supply	Dual Ch: F_S = 500 MSPS, Quad Ch: F_S = 250 MSPS.					
I_{AVDD}	Analog supply current			270		mA
I_{DVDD}	Digital and output driver supply current			125		mA
P_{AVDD}	Analog Power			486		mW
P_{DVDD}	Digital Power			224		mW
P_{TOT}	Total Power Dissipation			710	850	mW
P_{PD}	Power Down Mode dissipation			15		µW
P_{SLP}	Deep Sleep Mode power dissipation			72		mW
P_{SLPCH}	Power dissipation with all channels in sleep channel mode (Light sleep)			153		mW
P_{SLPCH_SAV}	Power dissipation savings per channel off (Quad Channel mode)			139		mW
Analog Input						
FPBW	Full Power Bandwidth			650		MHz
Clock Inputs						
F_{Smax}	Max. conversion rate in modes: Dual Ch / Quad Ch		500 / 250			MSPS
F_{Smin}	Min. conversion rate in modes: Dual Ch / Quad Ch				60 / 30	MSPS

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Digital and Switching Specifications

AVDD = 1.8V, DVDD = 1.8V, OVDD = 1.8V, RSDS output data levels, unless otherwise noted.

Parameter	Description	Min	Typ	Max	Unit
Clock Inputs					
DC	Duty Cycle	45		55	% high
Compliance	LVDS supported up to 700 MHz		LVPECL, Sine wave, CMOS, LVDS		
$V_{CK,diff}$	Differential input voltage swing, LVDS, LVPECL	450			mVpp
$V_{CK,sine}$	Differential input voltage swing, sine wave clock input	1500			mVpp
$V_{CK,CMOS}$	Voltage input range CMOS (CLKN connected to ground)		V_{OVDD}		
$V_{CM,CK}$	Input common mode voltage. Keep voltages within ground and voltage of OVDD	0.3		V_{OVDD} – 0.3	V
C_{CK}	Differential Input capacitance		3		pF
F_{CKmax}	Maximum input frequency on CLK pins		1000		MHz
Logic inputs (CMOS)					
V_{HI}	High Level Input Voltage. V_{OVDD} ≥ 3.0 V	2			V
V_{HI}	High Level Input Voltage. V_{OVDD} = 1.7 V – 3.0 V	0.8 ·V_{OVDD}			V
V_{LI}	Low Level Input Voltage. V_{OVDD} ≥ 3.0 V	0		0.8	V
V_{LI}	Low Level Input Voltage. V_{OVDD} = 1.7 V – 3.0 V	0		0.2 · V_{OVDD}	V
I_{HI}	High Level Input leakage Current			±10	µA
I_{LI}	Low Level Input leakage Current			±10	µA
C_I	Input Capacitance		3		pF
Data Outputs					
Compliance			LVDS / RSDS		
V_{OUT}	Differential output voltage, LVDS		350		mV
V_{OUT}	Differential output voltage, RSDS		150		mV
V_{CM}	Output common mode voltage		1.2		V
Output coding	Default/optional		Offset Binary/ 2's complement		
Timing Characteristics					
t_A	Aperture delay		1.5		ns
t_{jrms}	Aperture jitter, One bit set to '1' in jitter_ctrl<7:0>		300		fsrms
T_{skew}	Timing skew between ADC channels		2.5		psrms
T_{SU}	Start up time from Power Down Mode and Deep Sleep Mode to Active Mode. See section "Clock Frequency" for details.		15		µs
T_{SLPCH}	Start up time from Sleep Channel Mode to Active Mode		0.5		µs
T_{OVR}	Out of range recovery time		1		clock cycles
T_{LATQ}	Pipeline delay, Quad Channel Mode		32		clock cycles
T_{LATD}	Pipeline delay, Dual Channel Mode		64		clock cycles
LVDS Output Timing Characteristics					
t_{SK}	Data skew with respect to LCLK		±100	±200	ps
T_{PROP}	Clock propagation delay	6·T_{LVDS} +2.2	7·T_{LVDS} +3.5	7·T_{LVDS} +5.0	ns
	LVDS bit-clock duty-cycle	45		55	% LCLK cycle
	Frame clock cycle-to-cycle jitter			2.5	% LCLK cycle
T_{EDGE}	Data rise- and fall time 20% to 80%		0.28	0.35	ns
$T_{CLKEDGE}$	Clock rise- and fall time 20% to 80%		0.28	0.35	ns

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Pins and Interfaces

Pin Configuration and Description

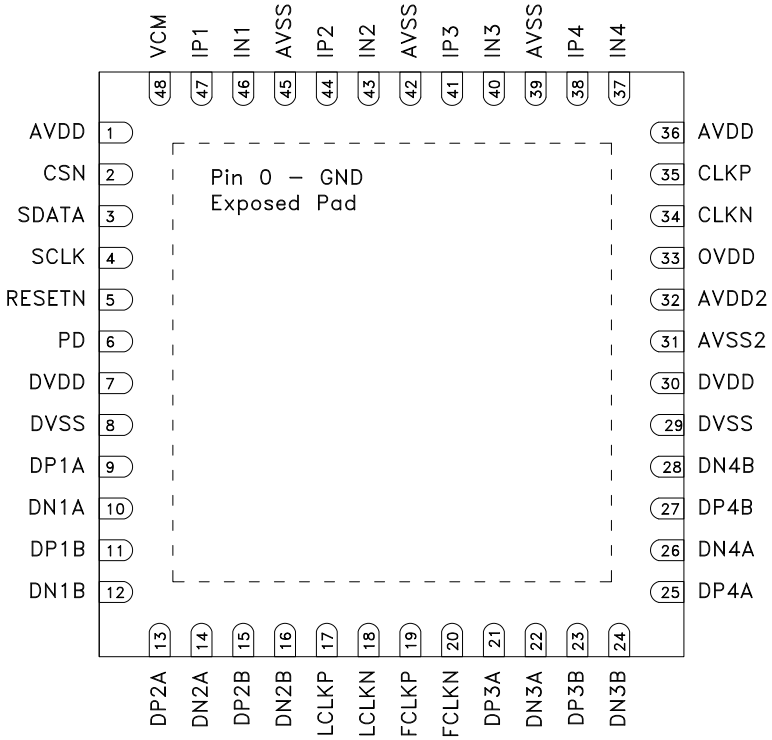
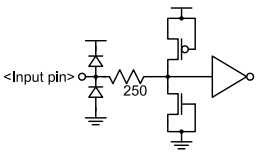


Figure 1. Package Diagram (Top View)

Table 1. Pin Descriptions

Pin Name	Description	Pin Number	# Of Pins	Interface Schematics
GND	Thermal pad and main ground connection	0	1	–
AVDD	Analog power supply, 1.8 V	1, 36	2	
AVDD2	Analog power supply domain 2, 1.8 V	32	1	
DVDD	Digital and I/O power supply, 1.8V	7, 30	2	
DVSS	Digital ground	8, 29	2	
OVDD	Digital CMOS Inputs supply voltage	33	1	
AVSS	Analog ground	39, 42, 45	3	
AVSS2	Analog ground domain 2	31	1	
CSN	Chip select enable. Active low	2	1	
SDATA	Serial data input	3	1	
SCLK	Serial clock input	4	1	
RESETN	Reset SPI interface. Active low	5	1	
PD	Power-down input. Activate after applying power in order to initialize the ADC correctly. Alternatively use the SPI power down feature	6	1	

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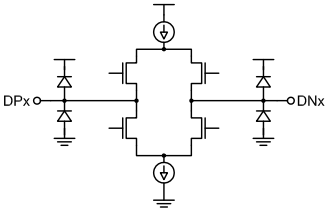
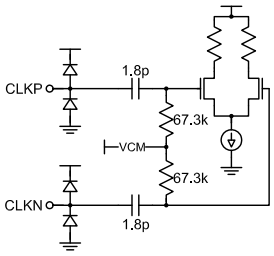
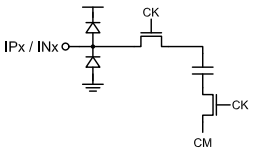
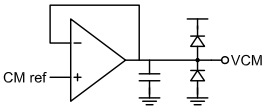
Pin Name	Description	Pin Number	# Of Pins	Interface Schematics
DP1A	LVDS channel 1A, positive output	9	1	
DN1A	LVDS channel 1A, negative output	10	1	
DP1B	LVDS channel 1B, positive output	11	1	
DN1B	LVDS channel 1B, negative output	12	1	
DP2A	LVDS channel 2A, positive output	13	1	
DN2A	LVDS channel 2A, negative output	14	1	
DP2B	LVDS channel 2B, positive output	15	1	
DN2B	LVDS channel 2B, negative output	16	1	
LCLKP	LVDS bit clock, positive output	17	1	
LCLKN	LVDS bit clock, negative output	18	1	
FCLKP	LVDS frame clock (1X), positive output	19	1	
FCLKN	LVDS frame clock (1X), negative output	20	1	
DP3A	LVDS channel 3A, positive output	21	1	
DN3A	LVDS channel 3A, negative output	22	1	
DP3B	LVDS channel 3B, positive output	23	1	
DN3B	LVDS channel 3B, negative output	24	1	
DP4A	LVDS channel 4A, positive output	25	1	
DN4A	LVDS channel 4A, negative output	26	1	
DP4B	LVDS channel 4B, positive output	27	1	
DN4B	LVDS channel 4B, negative output	28	1	
CLKN	Negative differential input clock.	34	1	
CLKP	Positive differential input clock	35	1	
IN4	Negative differential input signal, channel 4	37	1	
IP4	Positive differential input signal, channel 4	38	1	
IN3	Negative differential input signal, channel 3	40	1	
IP3	Positive differential input signal, channel 3	41	1	
IN2	Negative differential input signal, channel 2	43	1	
IP2	Positive differential input signal, channel 2	44	1	
IN1	Negative differential input signal, channel 1	46	1	
IP1	Positive differential input signal, channel 1	47	1	
VCM	Common mode output pin, 0.5 · AVDD	48	1	

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Serial Interface

The HMCAD1513 configuration registers can be accessed through a serial interface formed by the pins SDATA (serial interface data), SCLK (serial interface clock) and CSN (chip select, active low). The following occurs when CSN is set low:

- Serial data are shifted into the chip
- At every rising edge of SCLK, the value present at SDATA is latched
- SDATA is loaded into the register every 24th rising edge of SCLK

Multiples of 24-bit words data can be loaded within a single active CSN pulse. If more than 24 bits are loaded into SDATA during one active CSN pulse, only the first 24 bits are kept. The excess bits are ignored. Every 24-bit word is divided into two parts:

- The first eight bits form the register address
- The remaining 16 bits form the register data

Acceptable SCLK frequencies are from 20 MHz down to a few Hertz. Duty-cycle does not have to be tightly controlled.

SPI Timing Diagram

Figure 2 shows the timing of the serial port interface. Table 2 explains the timing variables used in Figure 2.

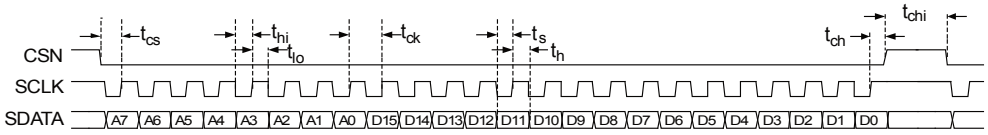

Figure 2. Serial Port Interface Timing

Table 2. Serial Port Interface Timing Definitions

Parameter	Description	Minimum value	Unit
t_{cs}	Setup time between CSN and SCLK	8	ns
t_{ch}	Hold time between SCLK and CSN	8	ns
t_{hi}	SCLK high time	20	ns
t_{lo}	SCLK low time	20	ns
t_{ck}	SCLK period	50	ns
t_s	Data setup time	5	ns
t_h	Data hold time	5	ns

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Digital Output Interface

By default, the HMCAD1513 digital outputs conform to the ANSI-644 LVDS (Low-voltage differential signaling) standard, i.e. the *ilvds** register fields in register 0x11 are set to '000'. In this mode the LVDS driver current is set to 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a 350 mV swing at the receiver. The LVDS driver current level is recommended in the cases where the LVDS receiver does not accept a reduced signal swing

The generally recommended LVDS driving current is the RSDS (Reduced strength differential signaling) which is used by setting the *ilvds** registers to '010'. In this mode the LVDS driver current is set to 1.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a 150 mV swing at the receiver. The reduced driver current gives a power consumption advantage over the LVDS driver current level, while preserving full robustness with most LVDS receivers.

To achieve full robustness for the HMCAD1513 LVDS outputs it is highly recommended to utilize a single point-to-point topology terminated with 100 Ω as close to the LVDS receiver as possible. The routing traces should be fully differential traces with impedance matched to the load and matched on length.

When these guidelines are followed, a PCB trace length up to 12 inches can be recommended. Figure 3 and Figure 4 show the LVDS Eye diagrams for LVDS and RSDS driving currents respectively, measured over the termination resistor, at a distance of 12 inches from the ADC.

The LVDS output signals are differential outputs with 1.2 V common mode voltage. When a '1' is set the DPxx will be 350/150mV higher than DNxx for LVDS/RSDS respectively. When a '0' is set the DPxx will be 350/150 mV lower than DNxx for LVDS/RSDS respectively. This means that the total differential output signal is 700/300 mVp-p for LVDS/RSDS respectively.

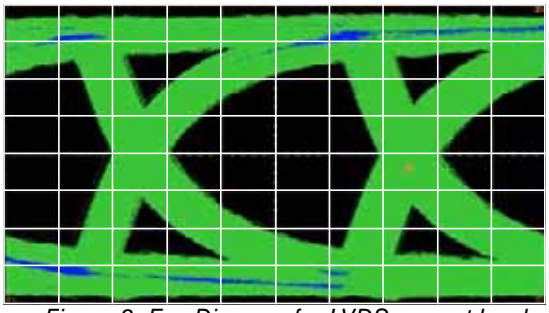

*Figure 3. Eye Diagram for LVDS current level (*ilvds = *'1'), acquired 10" from ADC. Dual Channel Mode at 500 MSPS. Scale: 110 mV/ over 200 ps/*

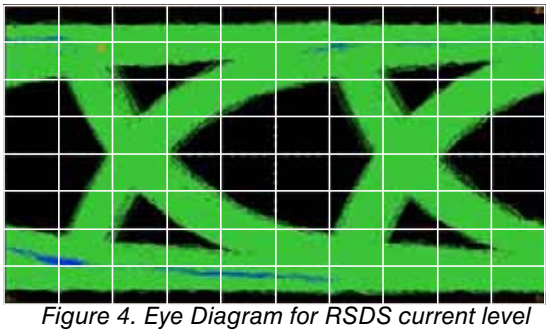

*Figure 4. Eye Diagram for RSDS current level (*ilvds = *'0'), acquired 10" from ADC. Dual Channel Mode at 500 MSPS. Scale: 54 mV/ over 200 ps/*

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Timing Diagrams

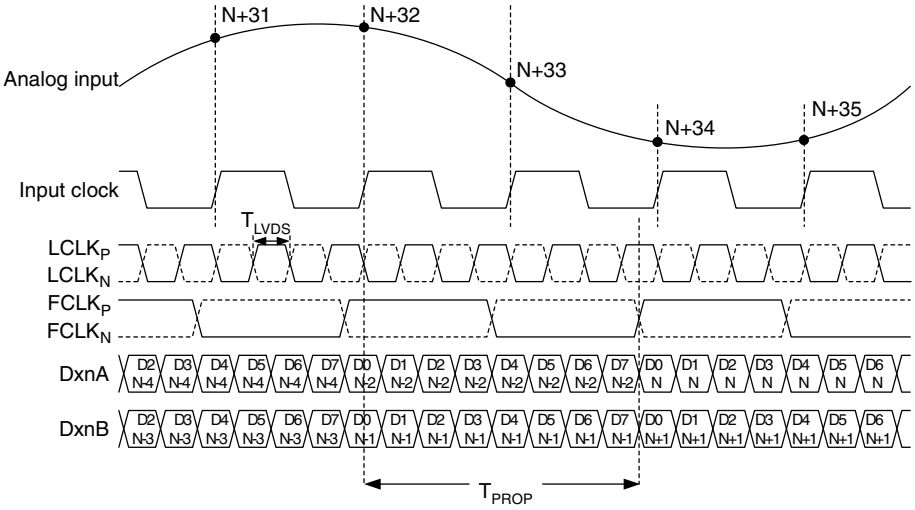

Figure 5. Quad channel – LVDS timing 8-bit output

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Timing Diagrams, continued

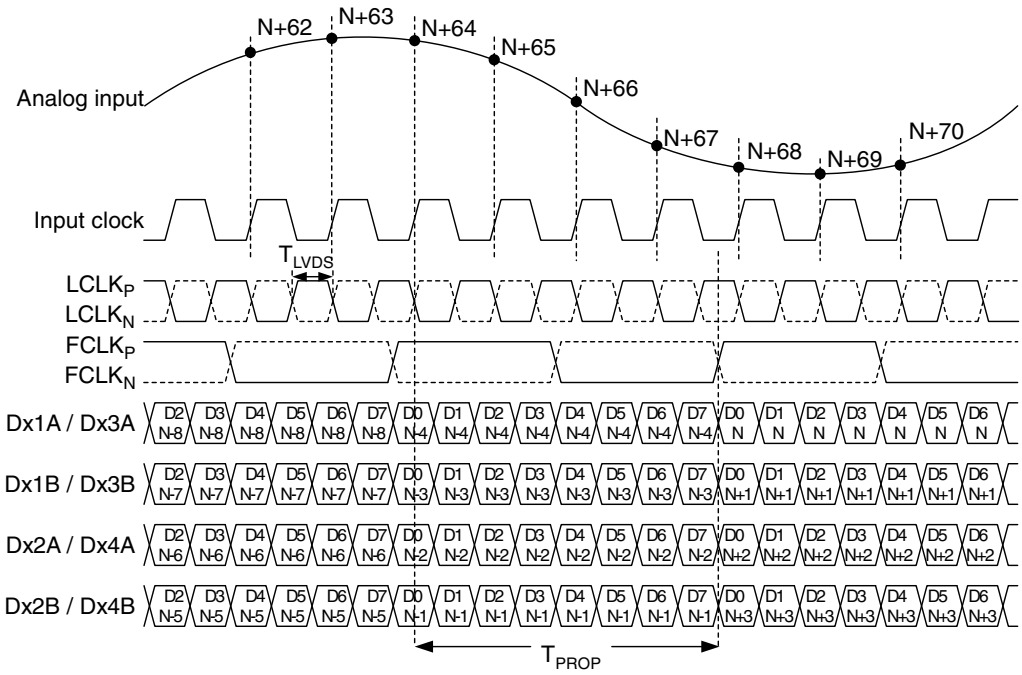

Figure 6. Dual channel – LVDS timing 8-bit output

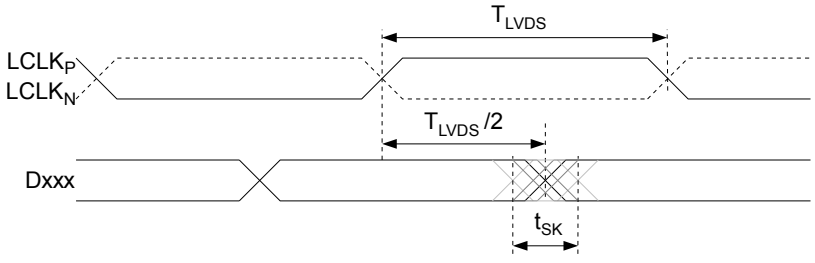

Figure 7. LVDS data timing

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Typical Performance Plots

Figure 1. Performance vs. Input Frequency

Dual Mode, 500 MSPS, Ain = -1 dBFS, Gain 1x

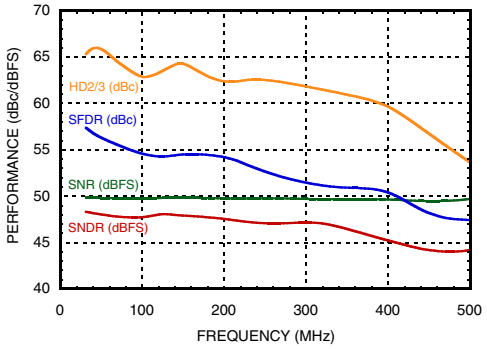

Figure 2. Performance vs. Input Frequency

Dual Mode, 500 MSPS, Ain = -1 dBFS, Gain 2x

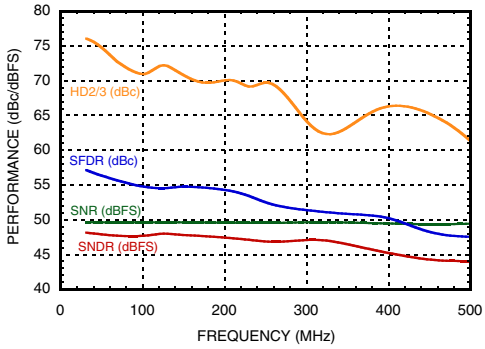

Figure 3. Performance vs. Input Frequency

Quad Mode, 250 MSPS, Ain = -1 dBFS, Gain 1x

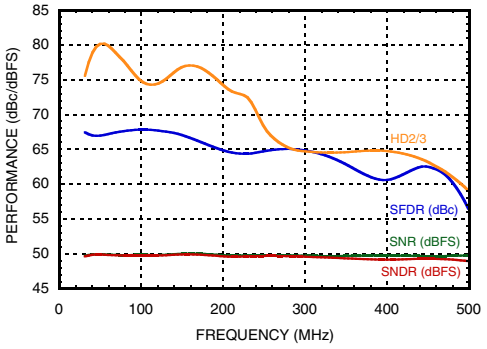

Figure 4. Performance vs. Input Frequency

Quad Mode, 250 MSPS, Ain = -1 dBFS, Gain 2x

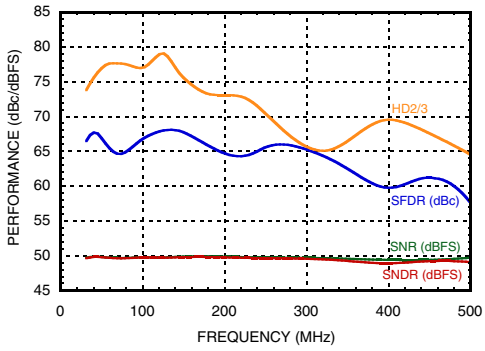

Figure 5. Performance vs. Temperature

Dual Mode, 500 MSPS, Fin = 70 MHz, Ain = -1 dBFS, Gain 1x

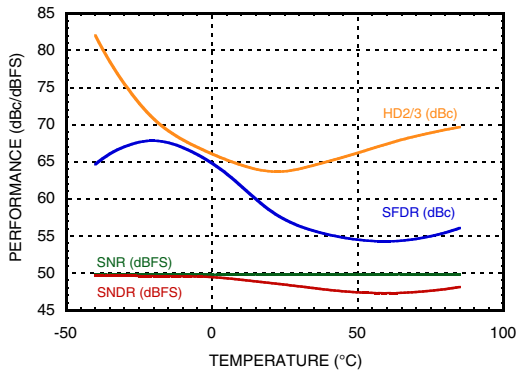

Figure 6. Performance vs. Temperature

Quad Mode, 250 MSPS, Fin = 70 MHz, Ain = -1 dBFS, Gain 1x

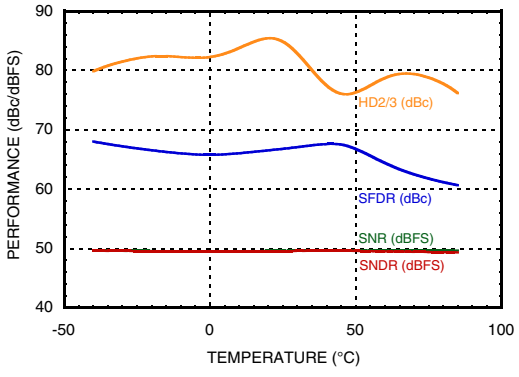

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Figure 7. Performance vs. Supply Voltage

Dual Mode, 500 MSPS, Fin = 70 MHz, Ain = -1 dBFS, Gain 1x

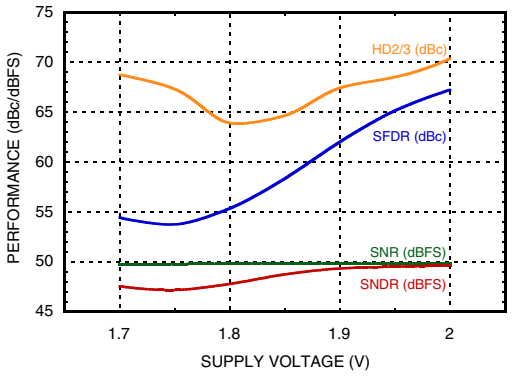

Figure 8. Performance vs. Supply Voltage

Quad Mode, 250 MSPS, Fin = 70 MHz, Ain = -1 dBFS, Gain 1x

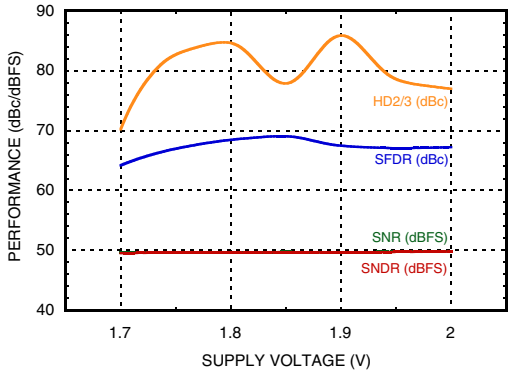

Figure 9. Performance vs. Input Amplitude

Dual Mode, 500 MSPS, Fin = 70 MHz, Gain 1x

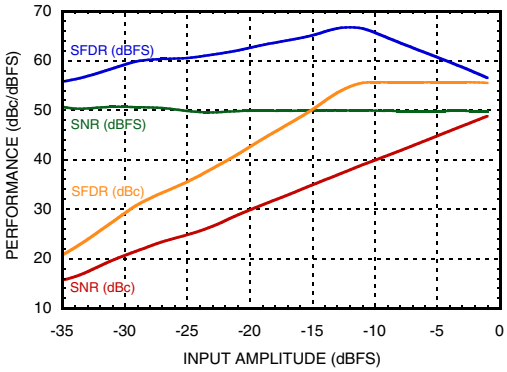

Figure 10. Performance vs. Input Amplitude

Quad Mode, 250 MSPS, Fin = 70 MHz, Gain 1x

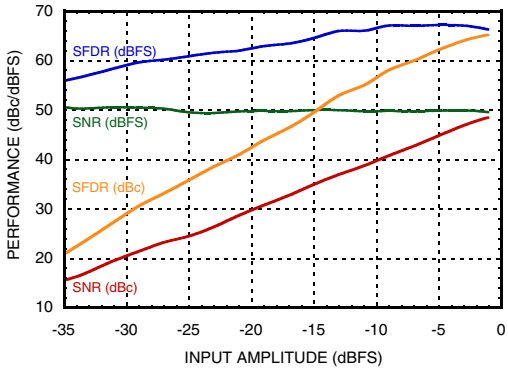

Figure 11. Performance vs. Full Scale Range

Dual Mode, 500 MSPS, Fin = 70 MHz, Ain = -1 dBFS, Gain 1x

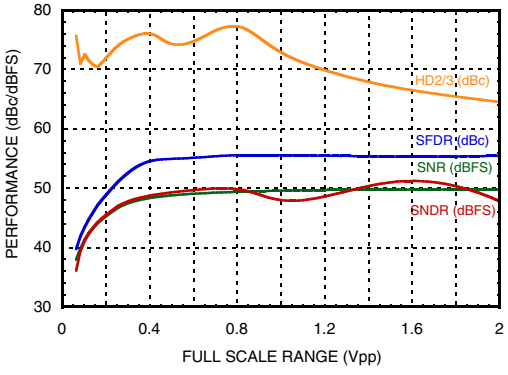

Figure 12. Performance vs. Full Scale Range

Quad Mode, 250 MSPS, Fin = 70 MHz, Ain = -1 dBFS, Gain 1x

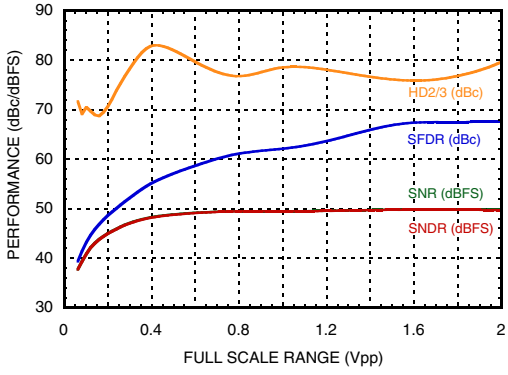

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Figure 13. Differential Nonlinearity – DNL

Dual Mode, 500 MSPS, Fin = 71 MHz, Ain = –1 dBFS, Gain 1x

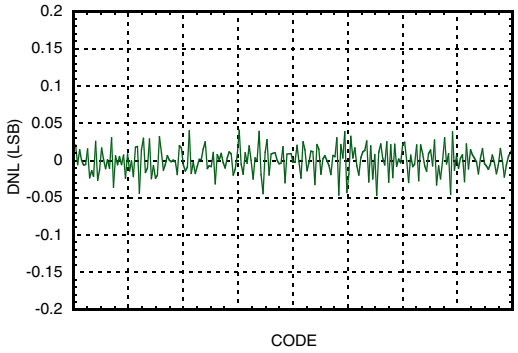

Figure 14. Differential Nonlinearity – DNL

Quad Mode, 250 MSPS, Fin = 71 MHz, Ain = –1 dBFS, Gain 1x

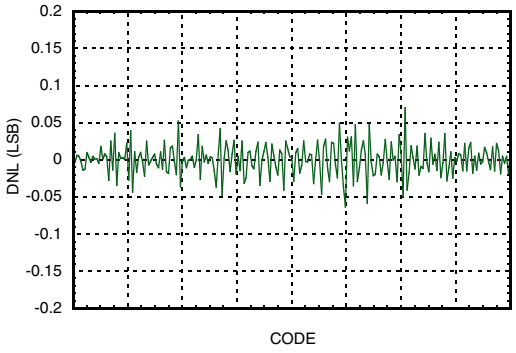

Figure 15. Integral Nonlinearity – INL

Dual Mode, 500 MSPS, Fin = 71 MHz, Ain = –1 dBFS, Gain 1x

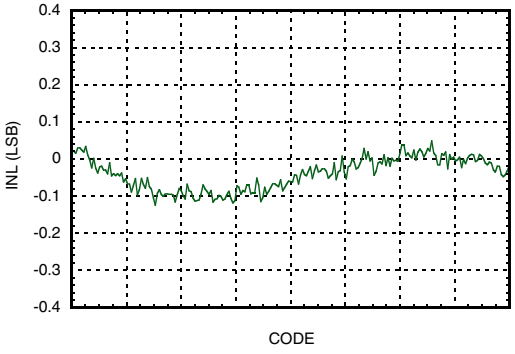

Figure 16. Integral Nonlinearity – INL

Quad Mode, 250 MSPS, Fin = 71 MHz, Ain = –1 dBFS, Gain 1x

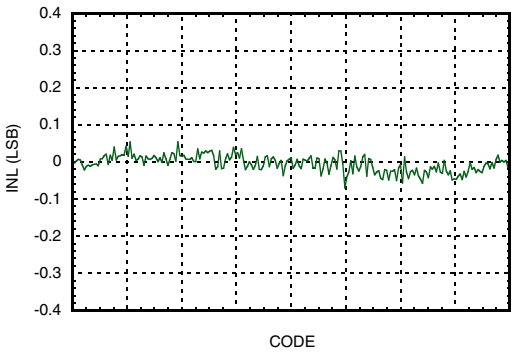

Figure 17. Fourier Transform – FFT

Dual Mode, 500 MSPS, Fin = 71 MHz, Ain = –1 dBFS, Gain 1x

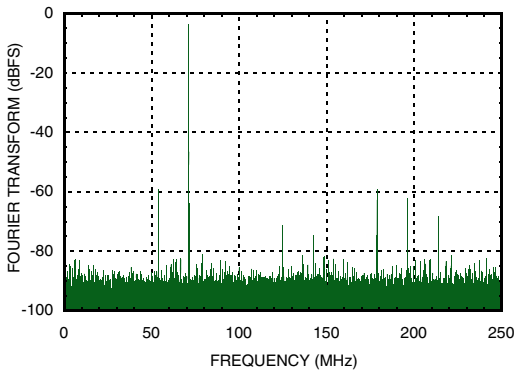

Figure 18. Fourier Transform – FFT

Quad Mode, 250 MSPS, Fin = 71 MHz, Ain = –1 dBFS, Gain 1x

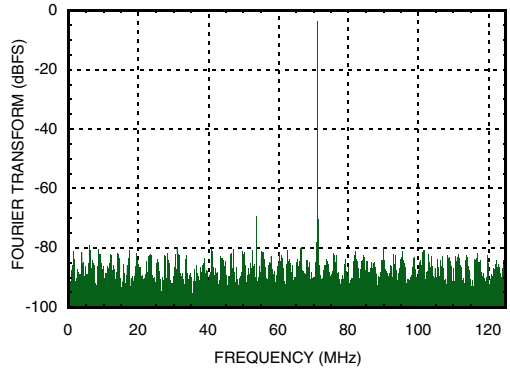

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Figure 19. Performance vs. Sampling Rate

Dual Mode, Fin = 71 MHz, Ain = –1 dBFS, Gain 1x

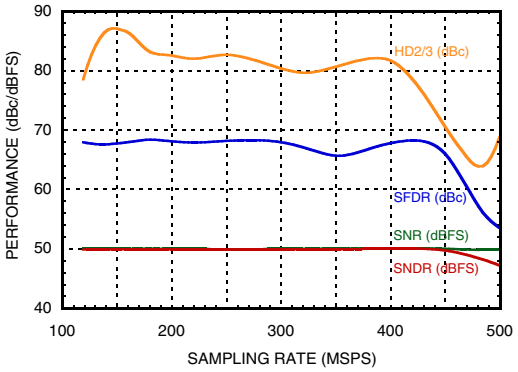


Figure 20. Performance vs. Sampling Rate

Quad Mode, Fin = 71 MHz, Ain = –1 dBFS, Gain 1x

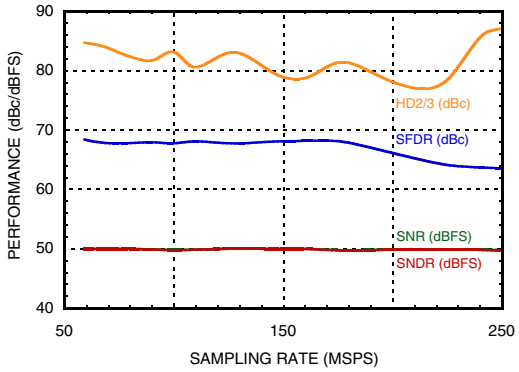
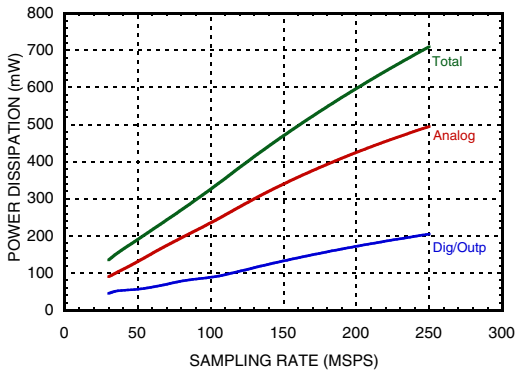


Figure 21. Power Dissipation vs. Sampling Rate

Quad Mode, Fin = 70 MHz, Ain = -1 dBFS, Gain 1x



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Register Map Summary

Table 3. Register Map

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
rst *	Self-clearing software reset*	'0' – Inactive																X	0x00
sleep4_ch<3:0>	Channel-specific sleep mode for a Quad Channel setup	'0000' Inactive													X	X	X	X	0x0F
sleep2_ch<1:0>	Channel-specific sleep mode for a Dual Channel setup	'00' Inactive											X	X					
sleep	Go to sleep-mode	'0' – Inactive								X									
pd	Go to power-down	'0' – Inactive							X										
pd_pin_cfg <1:0>	Configures the PD pin function	'00' PD pin invokes power-down mode					X	X											
ilvds_lclk<2:0>	LVDS current drive programmability for LCLKP and LCLKN pins	'000' 3.5 mA drive														X	X	X	0x11
ilvds_fclk<2:0>	LVDS current drive programmability for FCLKP and FCLKN pins	'000' 3.5 mA drive										X	X	X					
ilvds_dat<2:0>	LVDS current drive programmability for output data pins	'000' 3.5 mA drive						X	X	X									
en_lvds_term	Enables internal termination for LVDS buffers	'0' Termination disabled		X															0x12
term_lclk<2:0>	Programmable termination for LCLKN and LCLKP buffers	'000' Termination disabled		1												X	X	X	
term_fclk<2:0>	Programmable termination for FCLKN and FCLKP buffers	'000' Termination disabled		1								X	X	X					
term_dat<2:0>	Programmable termination for output data buffers	'000' – Termination disabled		1				X	X	X									
invert4_ch<3:0>	Channel specific swapping of the analog input signal for a Quad Channel setup	'0000' IPx is positive input													X	X	X	X	0x24
invert2_ch<1:0>	Channel specific swapping of the analog input signal for a Dual Channel setup	'00' IPx is positive input											X	X					
en_ramp	Enables a repeating full-scale ramp pattern on the outputs	'000' Inactive										X	0	0					0x25
dual_custom_ pat	Enable the mode wherein the output toggles between two defined codes	'000' Inactive										0	X	0					
single_custom_ pat	Enables the mode wherein the output is a constant specified code	'000' Inactive										0	0	X					
bits_custom1 <7:0>	Bits for the single custom pattern and for the first code of the dual custom pattern	0x00	X	X	X	X	X	X	X	X									0x26
bits_custom2 <7:0>	Bits for the second code of the dual custom pattern	0x00	X	X	X	X	X	X	X	X									0x27
cgain4_ch1 <3:0>	Programmable coarse gain channel 1 in a Quad Channel setup	'0000' 1x gain													X	X	X	X	0x2A
cgain4_ch2 <3:0>	Programmable coarse gain channel 2 in a Quad Channel setup	'0000' 1x gain									X	X	X	X					
cgain4_ch3 <3:0>	Programmable coarse gain channel 3 in a Quad Channel setup	'0000' 1x gain					X	X	X	X									
cgain4_ch4 <3:0>	Programmable coarse gain channel 4 in a Quad Channel setup	'0000' 1x gain	X	X	X	X													
cgain2_ch1 <3:0>	Programmable coarse gain channel 1 in a Dual Channel setup	'0000' 1x gain													X	X	X	X	0x2B
cgain2_ch2 <3:0>	Programmable coarse gain channel 2 in a Dual Channel setup	'0000' 1x gain									X	X	X	X					
jitter_ctrl<7:0>	Clock jitter adjustment	0x01 (one bit set) minimal power									X	X	X	X	X	X	X	X	0x30
channel_num <1:0>*	Set number of channels: Dual or Quad Channel Mode*	'01' Dual Channel Mode														X	X		0x31
clk_divide <1:0>*	Define clock divider factor: 1, 2, 4 or 8*	'00' Divide by 1							X	X									

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Table 3: Register Map, continued

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
cgain_cfg	Configures the coarse gain setting	'1' – x-gain selected																X	0x33
fine_gain_en	Enable use of fine gain	'0' – disabled															X		
fgain_branch1 <6:0>	Programmable fine gain for branch 1	'000 0000' 0dB gain										X	X	X	X	X	X	X	0x34
fgain_branch2 <6:0>	Programmable fine gain for branch 2	'000 0000' 0dB gain		X	X	X	X	X	X	X									
fgain_branch3 <6:0>	Programmable fine gain for branch 3	'000 0000' 0dB gain										X	X	X	X	X	X	X	0x35
fgain_branch4 <6:0>	Programmable fine gain for branch 4	'000 0000' 0dB gain		X	X	X	X	X	X	X									
fgain_branch5 <6:0>	Programmable fine gain for branch 5	'000 0000' 0dB gain										X	X	X	X	X	X	X	0x36
fgain_branch6 <6:0>	Programmable fine gain for branch 6	'000 0000' 0dB gain		X	X	X	X	X	X	X									
fgain_branch7 <6:0>	Programmable fine gain for branch 7	'000 0000' 0dB gain										X	X	X	X	X	X	X	0x37
fgain_branch8 <6:0>	Programmable fine gain for branch 8	'000 0000' 0dB gain		X	X	X	X	X	X	X									
inp_sel_adc1 <4:0>	Input select for ADC 1	'00010' Signal input: IP1/IN1												X	X	X	X	0	0x3A
inp_sel_adc2 <4:0>	Input select for ADC 2	'00100' Signal input: IP2/IN2				X	X	X	X	0									
inp_sel_adc3 <4:0>	Input select for ADC 3	'01000' Signal input: IP3/IN3												X	X	X	X	0	0x3B
inp_sel_adc4 <4:0>	Input select for ADC 4	'10000' Signal input: IP4/IN4				X	X	X	X	0									
phase_ddr<1:0>	Controls the phase of the LCLK output relative to data	'10' – 90 degrees										X	X						0x42
pat_deskew	Enable deskew pattern mode	'00' – Inactive															0	X	0x45
pat_sync	Enable sync pattern mode	'00' – Inactive															X	0	
btc_mode	Binary two's complement format for ADC output data	'0' – Straight offset binary														X			0x46
msb_first	Serialized ADC output data comes out with MSB first	'0' – LSB first													X				
adc_curr<2:0>	ADC current scaling	'000' – Nominal														X	X	X	0x50
ext_vcm_bc <1:0>	VCM buffer driving strength control	'01' – ±20 µA											X	X					
lvds_pd_mode	Controls LVDS power down mode	'0' – High z-mode																X	0x52
low_clk_freq *	Low clock frequency used*	'0' – Inactive													X	0	0	0	0x53
lvds_advance	Advance LVDS data bits and frame clock by one clock cycle	'00' – Inactive											0	X		0	0	0	
lvds_delay	Delay LVDS data bits and frame clock by one clock cycle	'00' – Inactive											X	0		0	0	0	
fs_cntrl<5:0>	Fine adjust ADC full scale range	'10 0000' 0% change											X	X	X	X	X	X	0x55
startup_ctrl <2:0> *	Controls start-up time *	'000'														X	X	X	0x56

Undefined register addresses must not be written to; incorrect behaviour may be the result.

Unused register bits (blank table cells) must be set to '0' when programming the registers.

All registers can be written to while the chip is in power down mode.

* These registers require a Power Down Mode Cycle when written to (See Start up Initialization on next page).

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Start Up Initialization

For proper operation and performance of the HMCAD1513, the following procedure must be followed:

Step #	Address	Data	Description
1. Apply power	–	–	Ensure supply voltages are settled properly before proceeding.
2. Reset ADC	0x00	0x0001	A reset can be invoked by one of two ways: a) By applying a low-going pulse (minimum 20 ns) on the RESETN pin (asynchronous). b) By using the SPI to set the *rst* bit high. When this bit is set, internal registers are reset to default values, the *rst* bit is self-reset to zero. When using this method, do not apply any low-going pulse on the RESETN pin.
3. If desired: Select clock divider and/or change to Quad Channel Mode	0x31		See also "0x31 – Modes of Operation and Clock Divide Factor" on page 21
4. If desired: Adjust *jitter_ctrl* for high performance at high FCK (above 800 MHz)	0x30	0x00FF	See also "Clock Jitter Performance" on page 25
5. If desired: Reduce LVDS driving current	0x11	0x0222	The recommended setting is 0x0222, giving RSDS (1.5 mA) driving currents. The default (0x0000) LVDS driving currents (3.5 mA) should be used for LVDS receivers not supporting RSDS.
6. If desired: Increase driving current on VCM pin	0x50	0x0030	The recommended setting is 0x0030 (max. driving current). When full strength is not required, the driving strength can be decreased to save power consumption. If the VCM pin is not in use, the buffer can be switched off, 0x0000.
7. If desired: Write additional register settings			Any changes to any other registers/bits marked with an asterisk (*) in Table 3 must be written now.
8. Set ADC in Power Down Mode	0x0F	0x0200	Power down can be set by one of two ways: a) By setting the PD pin high (asynchronous). b) By writing the *pd* bit in register 0x0F to '1'.
9. Wake ADC from Power Down Mode	0x0F	0x0000	Depending on the method chosen in step 8: a) Set PD pin low again b) Set register bit *pd* in register 0x0F to '0'
10. Wait for Start-Up	–	–	See "Table 10. Start-Up Time Control Settings" on page 25

During normal operation, the register values marked with an asterisk (*) in Table 3 are set by first writing the desired register value and then performing a Power Down Cycle, i.e. by executing steps 7 to 10.

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Register Description

0x00 – Software Reset

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
rst*	Self-clearing software reset	'0' – Inactive																X	0x00

Setting the *rst* register bit to '1' restores the default value of all the internal registers including the *rst* register bit itself.

0x31 – Modes of Operation and Clock Divide Factor

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
channel_num<1:0>*	Set number of channels: Dual or Quad Channel Mode	'01' 2 channels														X	X		0x31
clk_divide<1:0>*	Define clock divider factor: 1, 2, 4 or 8	'00' Divide by 1							X	X									

The HMCAD1513 has two main operating modes controlled by the register bits *channel_num<1:0>* as defined in Table 4. Power down mode, as described in section 'Startup Initialization', must be activated after or during a change of operating mode to ensure correct operation. All active operating modes utilize interleaving of eight internal ADC branches (two per ADC channel) to achieve high sampling speed. Quad Channel Mode interleaves two ADC branches per channel, while Dual Channel Mode interleaves four ADC branches per channel.

Table 4. Modes of Operation

channel_num <1:0>	Mode of operation	Description
01 (default)	Dual Channel	Dual channel where channel 1 is made by interleaving ADC1 and ADC2, channel 2 by interleaving ADC3 and ADC4
10	Quad Channel	Quad channel where channel 1 corresponds to ADC1, channel 2 to ADC2, channel 3 to ADC3 and channel 4 to ADC4

Only one of the two bits should be activated at the same time.

clk_divide<1:0> allows the user to apply an input clock frequency Fck higher than the sampling rate Fs. The clock divider will divide the input clock frequency by a factor of 1, 2, 4, or 8, defined by the *clk_divide<1:0>* register. By setting the *clk_divide<1:0>* value relative to the *channel_num<1:0>* value, the same input clock frequency can be used for all settings on number of channels. E.g: When increasing the number of channels from 2 to 4, the maximum sampling rate is reduced by a factor of two. By letting *clk_divide<1:0>* follow the *channel_num<1:0>* value, and change it from 1 to 2, the internal clock divider will provide the reduction of the sampling rate without changing the input clock frequency.

Table 5. Clock Divider Factor

clk_divide<1:0>	Clock Divider Factor	Sampling rate (FS)
00 (default)	1	Input clock frequency Fck / 1
01	2	Input clock frequency Fck / 2
10	4	Input clock frequency Fck / 4
11	8	Input clock frequency Fck / 8

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0x3A, 0x3B – Input Select

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
inp_sel_adc1 <4:0>	Input select for ADC 1	'00010' Signal input: IP1/IN1												X	X	X	X	0	0x3A
inp_sel_adc2 <4:0>	Input select for ADC 2	'00100' Signal input: IP2/IN2				X	X	X	X	0									
inp_sel_adc3 <4:0>	Input select for ADC 3	'01000' Signal input: IP3/IN3												X	X	X	X	0	0x3B
inp_sel_adc4 <4:0>	Input select for ADC 4	'10000' Signal input: IP4/IN4				X	X	X	X	0									

Each ADC is connected to the four input signals via a fully flexible cross point switch, set up by *inp_sel_adcx*.

In Dual Channel mode, a channel consists of two ADC cores which are interleaved according to Table 4 on page 21. The two cores per channel require identical inputs. Any two of the four inputs can be selected to each ADC channel. However, Input 1 and 4 should be used to for full CrossTalk performance. If input 2 or 3 is utilized in Dual Channel Mode, please refer to Quad Channel CrossTalk.

In Quad Channel mode any input can be assigned to any ADC channel. The switching of inputs can be done during normal operation, and no additional actions are needed. The switching will occur instantaneously at the end of each SPI command.

Table 6. Input Select

inp_sel_adcx<4:0>	Selected Input
0 0010	IP1/IN1
0 0100	IP2/IN2
0 1000	IP3/IN3
1 0000	IP4/IN4
other	Do not use

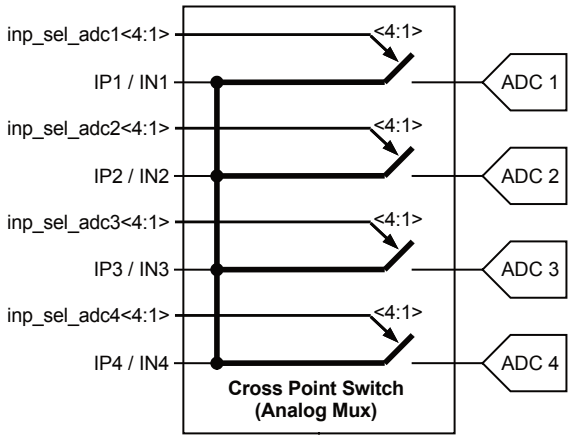

Figure 8. ADC input signals through Cross Point Switch

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0x55 – Full-Scale Control

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
fs_cntrl <5:0>	Fine adjust ADC full scale range	'10 0000' 0% change											X	X	X	X	X	X	0x55

The full-scale voltage range of HMCAD1513 can be adjusted using an internal 6-bit DAC controlled by the *fs_cntrl* register. Changing the value in the register by one step, adjusts the full-scale range by approximately 0.3%. This leads to a maximum range of ±10% adjustment. Table 9 shows how the register settings correspond to the full-scale range. Note that the values for full-scale range adjustment are approximate. The DAC is, however, guaranteed to be monotonous.

The full-scale control and the programmable gain features differ in two major ways:

1. The full-scale control feature controls the full-scale voltage range in an analog fashion, whereas the programmable gain is a digital feature.
2. The programmable gain feature has much coarser gain steps and larger range than the full-scale control.

Table 7. Register Values with Corresponding Change in Full-Scale Range

fs_cntrl<5:0>	Full-Scale Range Adjustment
111111	9.70%
111110	9.40%
…	…
100001	0.30%
100000	0%
011111	-0.3%
…	…
000001	-9.7%
000000	-10%

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0x50 – Current Control

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
adc_curr<2:0>	ADC current scaling.	'000' – Nominal														X	X	X	0x50
ext_vcm_bc<1:0>	VCM buffer driving strength control	'01' – ±20 µA											X	X					

There are two registers that impact performance and power dissipation.

The *adc_curr* register scales the current consumption in the ADC core. The performance is guaranteed at the nominal setting. Lower power consumption can be achieved by reducing the *adc_curr* value, see Table 8. The impact on performance is low for settings down to minimum, but will depend on the ADC sampling rate.

Table 8. ADC Current Control Settings

adc_curr<2:0>	ADC Core Current
100	-40%
101	-30%
110	-20%
111	-10%
000 (default)	Nominal
001	Do not use
010	Do not use
011	Do not use

Table 9. External Common Mode Voltage Buffer Driving Strength

ext_vcm_bc<1:0>	VCM buffer driving strength (µA) Max current sinked/sourced from VCM pin with < 20 mV voltage change.
00	Off (VCM floating)
01 (default)	±20
10	±400
11 (recommended)	±700

The *ext_vcm_bc* register controls the driving strength in the buffer supplying the voltage on the VCM pin. If this pin is not in use, the buffer can be switched off (*ext_vcm_bc* = '00'). The VCM pin driving strength can be decreased to save power consumption when full strength is not required.

The maximum driving strength (ext_vcm_bc = '11') is recommended if power dissipation is not extremely im*portant as* it results in the most accurate VCM output voltage.

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0x30, 0x56 – Start-up and Clock Jitter Control

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
startup_ctrl<2:0>	Controls start-up time	'000'														X	X	X	0x56
jitter_ctrl<7:0>	Clock jitter adjustment	'0000 0001' one bit set									X	X	X	X	X	X	X	X	0x30

To optimize start up time, register *startup_ctrl* is provided where the start-up time in number of clock cycles can be set. Some internal circuitry have start up times that are clock frequency independent. Default counter values are set to accommodate these start up times at the maximum clock frequency (sampling rate). This will lead to increased start up times at low clock frequencies. Setting the value of this register to the nearest higher clock frequency will reduce the count values of the internal counters, to better fit the actual start up time, such that the start up time will be reduced. The start up times from power down and sleep modes are changed by this register setting. If the clock divider is used (set to other than 1), the input clock frequency must be divided by the divider factor to find the correct clock frequency range (see Table 5).

Table 10. Start-Up Time Control Settings

Quad Channel Mode			
startup_ctrl <2:0>	Sampling Rate Range (MSPS)	Startup Delay (clock cycles)	Startup Delay (µs)
100	160 - 250	3072	12.3 - 19.2
000	100 - 160	1984	12.4 - 19.8
001	65 - 100	1280	12.8 - 19.7
010	40 - 65	840	12.9 - 21
011	30 - 40	520	13 - 17.3
other	Do not use	-	-

Dual Channel Mode			
startup_ctrl <2:0>	Sampling Rate Range (MSPS)	Startup Delay (clock cycles)	Startup Delay (µs)
100	320 - 500	6144	12.3 - 19.2
000	200 - 320	3968	12.4 - 19.8
001	130 – 200	2560	12.8 - 19.7
010	80 - 130	1680	12.9 - 21
011	60 – 80	1040	13 - 17.3
other	Do not use	-	-

When the clock division factor is 2 or higher, Clock Input Frequencies $F_{CK} \leq 1000$ MHz are applicable. To maintain high performance for high Clock Input Frequencies $F_{CK} \geq 800$ MHz it is recommended to set two or more bits in *jitter_ctrl*.

jitter_ctrl<7:0> allows the user to set a trade-off between power consumption and clock jitter. If all bits in the register are set low, the clock signal is stopped. The clock jitter depends on the number of bits set to '1' in the *jitter_ctrl<7:0>* register. Which bits are set high does not affect the result.

Table 11. Clock Jitter Performance

Number of bits to '1' in jitter_ctrl<7:0>	Clock jitter performance [fsrms]	Module current consumption [mA]
0	Clock stopped	
1 (default)	lowest power	1
2 (recommended for F_{CK} > 800 MHz)	:	2
3	:	3
4	:	4
5	:	5
6	:	6
7	:	7
8	lowest jitter	8

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0x42, 0x46, 0x53 – LVDS Output Configuration and Control

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
low_clk_freq	Low clock frequency used	'0' – Inactive													X				0x53
lvds_advance	Advance LVDS data bits and frame clock by one clock cycle	'00' – Inactive											0	X					
lvds_delay	Delay LVDS data bits and frame clock by one clock cycle	'00' – Inactive											X	0					
phase_ddr<1:0>	Controls the phase of the LCLK output relative to data	'10' – 90 degrees										X	X						0x42
btc_mode	Binary two's complement format for ADC output data	'0' Straight offset binary														X			0x46
msb_first	Serialized ADC output data comes out with MSB first	'0' – LSB first													X				

The HMCAD1513 uses an 8-bit serial LVDS output interface as shown in the Timing Diagrams section. The different selection of number of channels (*channel_num*<1:0> in register 0x31) uses the LVDS outputs as defined by Table 12.

Table 12. Use of LVDS Outputs

channel_num<1:0> in register 0x31	Channel Number	LVDS Outputs Used
'01' - Dual channel mode	Channel 1	D1A, D1B, D2A, D2B
	Channel 2	D3A, D3B, D4A, D4B
'10' - Quad channel mode	Channel 1	D1A, D1B
	Channel 2	D2A, D2B
	Channel 3	D3A, D3B
	Channel 4	D4A, D4B

Maximum data output bit-rate for HMCAD1513 is 1 Gb/s. The maximum sampling rate for the different configurations is given by Table 13. The sampling rate F_S is set by the frequency of the input clock F_{CK} and the clock divider, $F_S = F_{CK}$ / clk_div. The frame-rate, i.e. the frequency of the FCLK signal on the LVDS outputs, depends on the selected mode and the sampling frequency (F_S) as defined in Table 13.

If the HMCAD1513 device is used at a low sampling rate the register bit *low_clk_freq* has to be set to '1'. See Table 13 for when to use this register bit for the different modes of operation.

Table 13. Sampling and Frame Rate Properties in Dual and Quad Channel Mode

Mode of Operation	Maximum Sampling Rate F_{Smax} (MSPS)	Frame Rate (FCLK Frequency)	Limit When *low_clk_freq* Should Be Activated
Dual Channel	500	F_S / 4	F_S < 120 MHz
Quad Channel	250	F_S / 2	F_S < 60 MHz

To ease timing in the receiver when using multiple HMCAD1513, the device has the option to adjust the timing of the output data and the frame clock. The propagation delay with respect to the ADC input clock can be moved one LVDS clock cycle forward or backward, by using *lvds_delay* and *lvds_advance*, respectively. See Figure 9 for details. Note that LCLK is not affected by *lvds_delay* or *lvds_advance* settings.

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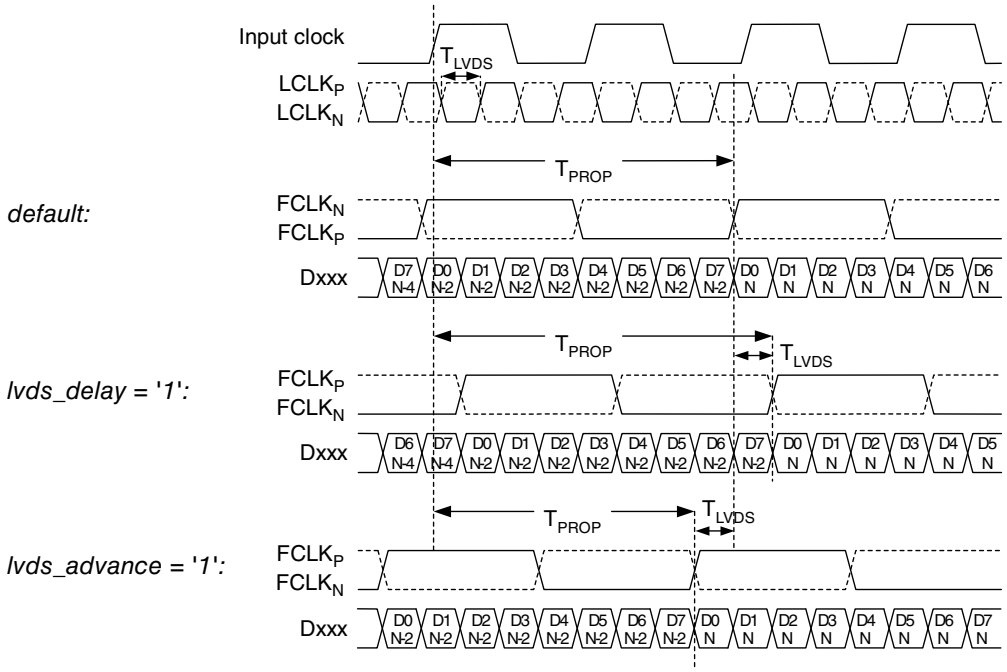

Figure 9.LVDS output timing adjustment

The LVDS output interface of HMCAD1513 is a DDR interface. The default setting is with the LCLK rising and falling edge transitions in the middle of alternate data windows. The phase for LCLK can be programmed relative to the output frame clock and data bits using *phase_ddr<1:0>*. The LCLK phase modes are shown in Figure 10. The default timing is identical to setting *phase_ddr<1:0>*='10'.

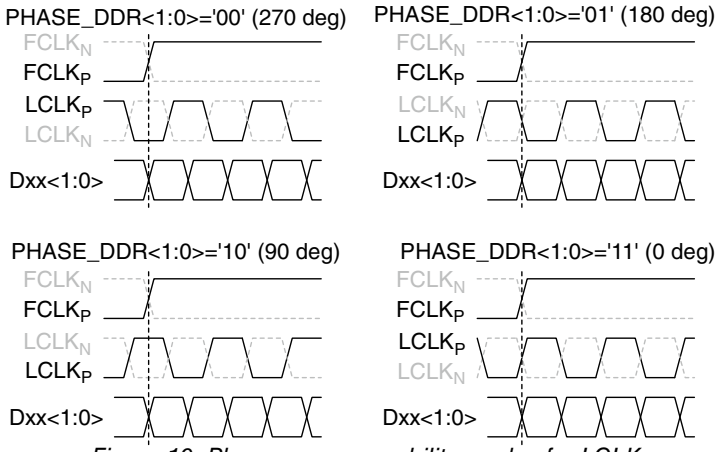

Figure 10. Phase programmability modes for LCLK

The default data output format is offset binary. Two's complement mode can be selected by setting the *btc_mode* bit to '1' which inverts the MSB.

The first bit of the frame (following the rising edge of FCLKP) is the LSB of the ADC output for default settings. Programming the *msb_first* mode results in reverse bit order, and the MSB is output as the first bit following the FCLKP rising edge.

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0x11 – LVDS Drive Strength Programmability

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
ilvds_lclk <2:0>	LVDS current drive programmability for LCLKP and LCLKN pins.	'000' 3.5 mA drive														X	X	X	0x11
ilvds_fclk <2:0>	LVDS current drive programmability for FCLKP and FCLKN pins.	'000' 3.5 mA drive										X	X	X					
ilvds_dat <2:0>	LVDS current drive programmability for output data pins.	'000' 3.5 mA drive						X	X	X									

The current delivered by the LVDS output drivers can be configured as shown in Table 14. The default current is 3.5 mA, according to the LVDS standard.

To reduce power consumption in the HMCAD1513, Reduced Swing Data Signaling (RSDS), is recommended. The output current drive setting should then be 1.5 mA.

Setting the *ilvds_lclk<2:0>* register controls the current drive strength of the LVDS clock output on the LCLKP and LCLKN pins.

Setting the *ilvds_fclk<2:0>* register controls the current drive strength of the frame clock output on the FCLKP and FCLKN pins.

Setting the *ilvds_dat<2:0>* register controls the current drive strength of the data outputs on the D[8:1]P and D[8:1]N pins.

Table 14. LVDS Output Drive Strength for LCLK, FCLK & Data

ilvds_*<2:0>	LVDS Drive Strength
000	3.5 mA (default)
001	2.5 mA
010	1.5 mA (RSDS)
011	0.5 mA
100	7.5 mA
101	6.5 mA
110	5.5 mA
111	4.5 mA

Table 15. LVDS Output Internal Termination for LCLK, FCLK and Data

term_*<2:0>	LVDS Internal Termination
000	Termination disabled
001	260Ω
010	150Ω
011	94Ω
100	125Ω
101	80Ω
110	66Ω
111	55Ω

0x12 – LVDS Internal Termination Programmability

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
en_lvds_term	Enables internal termination for LVDS buffers	'0' Termination disabled		X															0x12
term_lclk <2:0>	Programmable termination for LCLKN and LCLKP buffers	'000' Termination disabled		1												X	X	X	
term_fclk<2:0>	Programmable termination for FCLKN and FCLKP buffers	'000' Termination disabled		1								X	X	X					
term_dat <2:0>	Programmable termination for output data buffers	'000' Termination disabled		1				X	X	X									

The off-chip load on the LVDS buffers may represent a characteristic impedance that is not perfectly matched with the PCB traces. This may result in reflections back to the LVDS outputs and loss of signal integrity. This effect can be mitigated by enabling an internal termination between the positive and negative outputs of each LVDS buffer. Internal termination mode can be selected by setting the *en_lvds_term* bit to '1'. Once this bit is set, the internal termination values for the bit clock, frame clock, and data buffers can be independently programmed using sets of three bits. Table 15 shows how the internal termination of the LVDS buffers are programmed. The values are typical values and can vary by up to ±20% from device to device and across temperature.

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0x0F, 0x52 – Power Mode Control

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
sleep4_ch<4:1>	Channel-specific sleep mode for a Quad Channel setup	'0000' Inactive													X	X	X	X	0x0F
sleep2_ch<2:1>	Channel-specific sleep mode for a Dual Channel setup	'00' Inactive											X	X					
sleep	Go to sleep-mode	'0' – Inactive								X									
pd	Go to power-down	'0' – Inactive							X										
pd_pin_cfg <1:0>	Configures the PD pin function	'00' – PD pin invokes power-down mode					X	X											
lvds_pd_mode	Controls LVDS power down mode	'0' – High z-mode																X	0x52

The HMCAD1513 device has several modes for power management, from sleep modes with short start up time to full power down with extremely low power dissipation. There are two sleep modes, both with the LVDS clocks (FCLK, LCLK) running, such that the synchronization with the receiver is maintained. The first is a light sleep mode (*sleep*_ch*) with short start up time, and the second a deep sleep mode (sleep) with the same start up time as full power down.

Setting *sleep4_ch<n>* = '1' sets channel *<n>* in a Quad Channel setup in sleep mode. Setting *sleep2_ch<n>* = '1' sets channel *<n>* in a Dual Channel setup in sleep mode. This is a light sleep mode with short start up time.

Setting *sleep* = '1', puts all channels to sleep, but keeps FCLK and LCLK running to maintain LVDS synchronization. The start up time is the same as for complete power down. Power consumption is significantly lower than for setting all channels to sleep by using the *sleep*_ch* register.

Setting *pd* = '1' completely powers down the chip, including the band-gap reference circuit. Start-up time from this mode is significantly longer than from the *sleep*_ch* mode. The synchronization with the LVDS receiver is lost since LCLK and FCLK outputs are put in high-Z mode.

Setting *pdn_pin_cfg<1:0>* = 'x1' configures the circuit to enter sleep channel mode (all channels off) when the PD pin is set high. This is equal to setting all channels to sleep by using *sleep*_ch*. The channels can not be powered down separately using the PD pin. Setting *pdn_pin_cfg<1:0>* = '10' configures the circuit to enter (deep) sleep mode when the PD pin is set high (equal to setting *sleep* = '1'). When *pdn_pin_cfg <1:0>* = '00', which is the default, the circuit enters the power down mode when the PD pin is set high.

Table 16. PD Pin Function

pdn_pin_cfg<1:0>	Effect when setting PD pin high
00 (default)	invoke power down
01 or 11	invoke light sleep mode, like *sleepx_ch* = '1111'
10	invoke sleep mode, like *sleep* = '1'

The *lvds_pd_mode* register configures whether the LVDS data output drivers are powered down or kept alive in sleep and sleep channel modes. LCLK and FCLK drivers are not affected by this register, and are always on in sleep and sleep channel modes. If *lvds_pd_mode* is set low (default), the LVDS output is put in high Z mode, and the driver is completely powered down. If *lvds_pd_mode* is set high, the LVDS output is set to constant 0, and the driver is still on during sleep and sleep channel modes.

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0x33, 0x2A, 0x2B, 0x34-0x37 – Programmable Gain

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
cgain_cfg	Configures the coarse gain setting	'1' – x-gain enabled																X	0x33
fine_gain_en	Enable use of fine gain	'0' – Disabled															X		
cgain4_ch1 <3:0>	Programmable coarse gain channel 1 in a Quad Channel setup	'0000' 1x gain													X	X	X	X	0x2A
cgain4_ch2 <3:0>	Programmable coarse gain channel 2 in a Quad Channel setup	'0000' 1x gain									X	X	X	X					
cgain4_ch3 <3:0>	Programmable coarse gain channel 3 in a Quad Channel setup	'0000' 1x gain					X	X	X	X									
cgain4_ch4 <3:0>	Programmable coarse gain channel 4 in a Quad Channel setup	'0000' 1x gain	X	X	X	X													
cgain2_ch1 <3:0>	Programmable coarse gain channel 1 in a Dual Channel setup	'0000' 1x gain													X	X	X	X	0x2B
cgain2_ch2 <3:0>	Programmable coarse gain channel 2 in a Dual Channel setup.	'0000' 1x gain									X	X	X	X					
fgain_branch1<6:0>	Programmable fine gain for branch1	'000 0000' 0dB gain										X	X	X	X	X	X	X	0x34
fgain_branch2<6:0>	Programmable fine gain for branch 2	'000 0000' 0dB gain		X	X	X	X	X	X	X									
fgain_branch3<6:0>	Programmable fine gain for branch 3	'000 0000' 0dB gain										X	X	X	X	X	X	X	0x35
fgain_branch4<6:0>	Programmable fine gain for branch 4	'000 0000' 0dB gain		X	X	X	X	X	X	X									
fgain_branch5<6:0>	Programmable fine gain for branch 5	'000 0000' 0dB gain										X	X	X	X	X	X	X	0x36
fgain_branch6<6:0>	Programmable fine gain for branch 6	'000 0000' 0dB gain		X	X	X	X	X	X	X									
fgain_branch7<6:0>	Programmable fine gain for branch 7	'000 0000' 0dB gain										X	X	X	X	X	X	X	0x37
fgain_branch8<6:0>	Programmable fine gain for branch 8	'000 0000' 0dB gain		X	X	X	X	X	X	X									

The device includes a digital programmable gain in addition to the Full-scale control. The programmable gain of each channel can be individually set using a four bit code, indicated as *cgain*<3:0>*. The gain is configured by the register *cgain_cfg*: when *cgain_cfg* equals '0' a gain in dB steps is enabled as defined in Table 17, otherwise if *cgain_cfg* equals '1' the gain is defined by Table 18. There will be no missing codes for gain settings of 32x (30dB) or lower, due to higher than 8 bit resolution internally.

Table 17. Gain setting – dB Step

cgain_cfg	cgain*<3:0>	Implemented Gain (dB)
0	0000	0
0	0001	1
0	0010	2
0	0011	3
0	0100	4
0	0101	5
0	0110	6
0	0111	7
0	1000	8
0	1001	9
0	1010	10
0	1011	11
0	1100	12
0	1101	Not used
0	1110	Not used
0	1111	Not used

Table 18. Gain Setting – x Step

cgain_cfg	cgain*<3:0>	Implemented Gain Factor (x)
1	0000	1
1	0001	1.25
1	0010	2
1	0011	2.5
1	0100	4
1	0101	5
1	0110	8
1	0111	10
1	1000	12.5
1	1001	16
1	1010	20
1	1011	25
1	1100	32
1	1101	50
1	1110	Not used
1	1111	Not used

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There is a digital fine gain implemented for each ADC to adjust the fine gain errors between the ADCs. The gain is controlled by *fgain_branch** as defined in Table 19. There will be no missing codes when using digital fine gain, due to higher resolution internally.

To enable the fine gain function the register bit *fine_gain_en* has to be activated, set to '1'.

See also section "Interleaving Effects and Sampling Order" on page 33.

Table 19. Fine Gain Setting

fgain_branchx<6:0>							Arithmetic Function	Implemented Gain (x)	Gain (dB)
0	1	1	1	1	1	1	OUT = (1 + 2^{-8} + 2^{-9} + 2^{-10} + 2^{-11} + 2^{-12} + 2^{-13}) * IN	1.0077	0.0665
0	1	1	1	1	1	0	OUT = (1 + 2^{-8} + 2^{-9} + 2^{-10} + 2^{-11} + 2^{-12}) * IN	1.0076	0.0655
0	1	1	1	1	0	1	OUT = (1 + 2^{-8} + 2^{-9} + 2^{-10} + 2^{-11} + 2^{-13}) * IN	1.0074	0.0644
0	1	1	1	1	0	0	OUT = (1 + 2^{-8} + 2^{-9} + 2^{-10} + 2^{-11}) * IN	1.0073	0.0634
0	0	0	0	0	1	1	OUT = (1 + 2^{-12} + 2^{-13}) * IN	1.0004	0.0031
0	0	0	0	0	1	0	OUT = (1 + 2^{-12}) * IN	1.0002	0.0021
0	0	0	0	0	0	1	OUT = (1 + 2^{-13}) * IN	1.0001	0.001
0	0	0	0	0	0	0	OUT = IN	1.0000	0.0000
1	1	1	1	1	1	1	OUT = IN	1.0000	0.0000
1	1	1	1	1	1	0	OUT = (1 - 2^{-13}) * IN	0.9999	-0.0011
1	1	1	1	1	0	1	OUT = (1 - 2^{-12}) * IN	0.9998	-0.0021
1	1	1	1	1	0	0	OUT = (1 - 2^{-12} - 2^{-13}) * IN	0.9996	-0.0032
1	0	0	0	0	1	1	OUT = (1 - 2^{-8} - 2^{-9} - 2^{-10} - 2^{-11}) * IN	0.9927	-0.0639
1	0	0	0	0	1	0	OUT = (1 - 2^{-8} - 2^{-9} - 2^{-10} - 2^{-11} - 2^{-13}) * IN	0.9926	-0.0649
1	0	0	0	0	0	1	OUT = (1 - 2^{-8} - 2^{-9} - 2^{-10} - 2^{-11} - 2^{-12}) * IN	0.9924	-0.0660
1	0	0	0	0	0	0	OUT = (1 - 2^{-8} - 2^{-9} - 2^{-10} - 2^{-11} - 2^{-12} - 2^{-13}) * IN	0.9923	-0.0670

0x24 – Analog Input Invert

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
invert4_ch <3:0>	Channel specific swapping of the analog input signal for a Quad Channel setup	'0000' – IPx is positive input													X	X	X	X	0x24
invert2_ch <1:0>	Channel specific swapping of the analog input signal for a Dual Channel setup	'00' – IPx is positive input											X	X					

The IPx pin represents the positive analog input pin, and INx represents the negative (complementary) input. Setting the bits marked *invertx_ch<n>* (individual control for each channel) causes the inputs to be swapped. INx would then represent the positive input, and IPx the negative input.

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0x25 to 0x27, 0x45 – LVDS Test Patterns

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
en_ramp	Enables a repeating full-scale ramp pattern on the outputs	'000' Inactive										X	0	0					0x25
dual_custom_pat	Enable the mode wherein the output toggles between two defined codes	'000' Inactive										0	X	0					
single_custom_pat	Enables the mode wherein the output is a constant specified code	'000' Inactive										0	0	X					
bits_custom1 <7:0>	Bits for the single custom pattern and for the first code of the dual custom pattern. <0> is the LSB	0x00	X	X	X	X	X	X	X	X									0x26
bits_custom2 <7:0>	Bits for the second code of the dual custom pattern	0x00	X	X	X	X	X	X	X	X									0x27
pat_deskew	Enable deskew pattern mode	'00' – Inactive															0	X	0x45
pat_sync	Enable sync pattern mode	'00' – Inactive															X	0	

To ease the LVDS synchronization setup of HMCAD1513, several test patterns can be set up on the outputs. Normal ADC data are replaced by the test pattern in these modes:

Setting *en_ramp* to '1' sets up a repeating full-scale **ramp pattern** on all data outputs. The ramp starts at code zero and is increased 1 LSB every clock cycle, see Figure 12. It returns to zero code and starts the ramp again after reaching the full-scale code.

A **constant value** can be set up on the outputs by setting *single_custom_pat* to '1', and programming the desired value in *bits_custom1<7:0>.* In this mode, *bits_custom1<7:0>* replaces the ADC data at the output, and is controlled by LSB-first and MSB-first modes (*msb_first* in register 0x46) in the same way as normal ADC data are.

The device may also be set up to **alternate between two codes** by programming *dual_custom_pat* to '1'. The two codes are the contents of *bits_custom1<7:0>* and *bits_custom2<7:0>*, see Figure 13.

Two preset patterns can also be selected:

Deskew pattern: Set using *pat_deskew*, this mode replaces the ADC output with a pattern consisting of alternating zeros and ones - MSB will be a zero.

Sync pattern: Set using *pat_sync*, the normal ADC word is in this mode replaced by a fixed synchronization pattern where the output word is split in two and the upper part of the word is ones and the lower part is zeros.

Note: Only one of the above patterns should be selected at the same time.

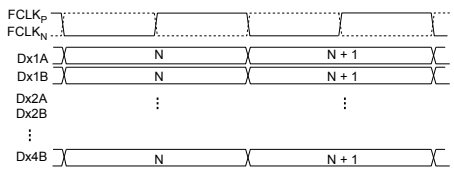

Figure 12. LVDS test pattern en_ramp (two subsequent FCLK frames)

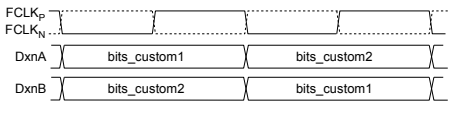

Figure 13. LVDS test pattern dual_custom_pat (two subsequent FCLK frames)

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Theory of Operation

HMCAD1513 is a multi Mode high-speed, CMOS ADC, consisting of eight ADC branches, configured in different channel modes, using interleaving to achieve high speed sampling. For all practical purposes, the device can be considered to contain four ADCs. Fine gain is adjusted for each of the eight branches separately.

HMCAD1513 utilizes a LVDS output, described in 'Register Description – LVDS Output Configuration and Control'. The clocks needed (FCLK, LCLK) for the LVDS interface are generated by an internal PLL.

The HMCAD1513 operates from one clock input, which can be differential or single ended. The sampling clocks for each of the four channels are generated from the clock input using a carefully matched clock buffer tree. Internal clock dividers are utilized to control the clock for each ADC during interleaving. The clock tree is controlled by the Mode of operations.

HMCAD1513 uses internally generated references. The differential reference value is 1.0 V. This results in a differential input of –1.0 V to correspond to the zero code of the ADC, and a differential input of +1.0 V to correspond to the full-scale code (code 255).

The ADC employs a Pipeline converter architecture. Each Pipeline Stage feeds its output data into the digital error correction logic, ensuring excellent differential linearity and no missing codes.

HMCAD1513 operates from two sets of supplies and grounds. The analog supply and ground set is identified as AVDD and AVSS, while the digital set is identified by DVDD and DVSS. AVSS and DVSS are electrically connected on-chip. AVSS and DVSS are internally connected.

Interleaving Effects and Sampling Order

Interleaving ADCs will generate interleaving artifacts caused by gain, offset and timing mismatch between the ADC branches. The design of HMCAD1513 has been optimized to minimize these effects. It is not possible, though, to eliminate mismatch completely, such that additional compensation may be needed, especially when using high digital gain settings. The internal digital fine gain control may be used to compensate for gain errors between the ADC branches. Due to the optimization of HMCAD1513 there is not a one-to-one correspondence between the sampling order, LVDS output order and the branch number. Table 20 and 24 give an overview of the corresponding branches, LVDS outputs and sampling order for the different high speed modes.

Table 20. Quad Channel Mode

Channel #	Sampling Order	LVDS Output	Fine Gain Branch
1	1	D1A	1
	2	D1B	2
2	1	D2A	3
	2	D2B	4
3	1	D3A	5
	2	D3B	6
4	1	D4A	7
	2	D4B	8

Table 21. Dual Channel Mode

Channel #	Sampling Order	LVDS Output	Fine Gain Branch
1	1	D1A	1
	2	D1B	3
	3	D2A	2
	4	D2B	4
2	1	D3A	5
	2	D3B	7
	3	D4A	6
	4	D4B	8

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Recommended Usage

Analog Input

The analog input to HMCAD1513 ADC is a switched capacitor sample-and-hold amplifier optimized for differential operation.

Operation at common mode voltages at mid supply is recommended even if performance will be good for the ranges specified. The VCM pin provides a voltage suitable as common mode voltage reference. The internal buffer for the VCM voltage can be switched off, and driving capabilities can be changed programming the *ext_vcm_bc<1:0>* register.

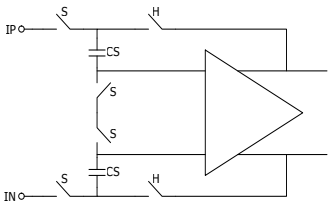

Figure 14. Input configuration

Figure 14 shows a simplified drawing of the input network. The signal source must have sufficiently low output impedance to charge the sampling capacitors within one clock cycle.

In Dual channel mode, Input 1 and 4 should be used for full CrossTalk performance. If input 2 or 3 is utilized in Dual channel mode, please refer to Quad Channel CrossTalk.

DC-Coupling

For DC coupling the common mode input voltage from the ADC driver must match the $V_{CM,IN}$ specification given in the Electrical Specifications on page 4. Preferably, the ADC common mode output voltage (VCM pin) should be used as reference to set the common mode input voltage. The input amplifier (e.g. HMC1023LP5E) could be inside a companion chip or it could be a dedicated amplifier.

For ADC drivers not optimized to drive the 0.9 V VCM in the ADC from a common ground, VCM alignment with ADC can be achieved by using a negative voltage for VSS in the ADC driver.

Figure 15 shows a recommended configuration for DC-coupling. Note that the common mode input voltage must be controlled according to specified values. Preferably, the VCM output should be used as reference to set the common mode voltage.

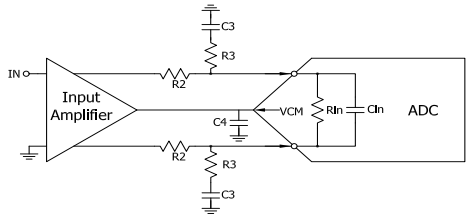

Figure 15. DC coupled input

An RC shunt to ground (R3 and C3) is inserted to optimize the direct sampling input of the ADC. For wide band applications the recommended values are 20 Ω for R3 and 10 pF for C3. For applications optimized for frequencies lower than 150 MHz, C3 can be increased to reduce the ADC driver noise bandwidth.

A series resistor, R2 is inserted to ensure the pass band flatness for the ADC input. The recommended value for R2 is 10 Ω. The value for R2 depends on the distance between ADC driver and ADC. For wide band applications it is highly recommended to minimize the distance between the ADC driver and the ADC input pins, and to keep the value of R2 low.

The ADC VCM output voltage is decoupled to ground through C4. The recommended value for C4 is 10 nF per channel.

AC-Coupling

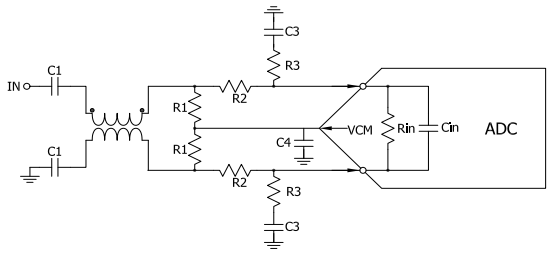

Figure 16. Transformer coupled input

A balun configuration is recommended for high performance AC-coupled input networks. Figure 16 shows a recommended configuration utilizing this configuration. The balun termination resistors (R1) define the impedance of the input network. The recommendations for R2, R3, C3 and C4 are as for DC coupling.

Make sure that a transformer with sufficient linearity is selected, and that the bandwidth of the transformer is appropriate. It is important to minimize second order

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distortion. This type of transformer coupled input is the preferred configuration to optimize Signal to Noise Ratio. A differential amplifier or differential Variable Gain Amplifier may result in higher linearity since they most often are less dependent on a pure resistive load. Magnetic coupling between the transformers and PCB traces may impact channel crosstalk, and must hence be taken into account during PCB layout.

Due to the switched nature of the ADC input stage, there will be some kick-back going from the ADC input and back into the driver. If these kick-backs are not terminated properly at the source side, they are reflected and will add to the input signal at the ADC input. This could reduce the ADC performance. To avoid this effect, the source must effectively terminate the ADC kick-backs, or the traveling distance should be very short.

Differential amplifiers are often suited to terminate the kick-back efficiently. It is of utmost importance that the amplifier is placed close to the ADC input to minimize any transmission line effects on the trace from the amplifier to the ADC input. The bandwidth in this node should also be maximized to allow the kick-back to settle within the available time.

In Figure 16 the ADC common mode setup for AC-Coupling is shown. By connecting the termination resistors (R1) to the ADC VCM output, the ADC Common mode voltage will be set up correctly given an AC-coupling capacitor (C1) to control the lower pass-band frequency.

The value of C1 must be defined based on the requirement to the high-pass cut-off frequency.

Note that Start Up Time from Sleep Mode and Power Down Mode will be affected by this filter as the time required to charge the series capacitors is dependent on the filter cut-off frequency.

Clock Input and Jitter Considerations

Typically high-speed ADCs use both clock edges to generate internal timing signals. In HMCAD1513 only the rising edge of the clock is used.

The input clock can be supplied in a variety of formats. The clock pins are AC-coupled internally, hence a wide common mode voltage range is accepted. Differential clock sources such as LVDS, LVPECL or differential sine wave can be utilized. LVDS/LVPECL clock signals must be appropriately terminated as close to the ADC clock pins as possible. For CMOS inputs, the CLKN pin should be connected to ground, and the CMOS clock signal should be connected to CLKP. CMOS input clock is not recommended above 200 MHz clock frequency. For differential sine wave clock input the amplitude must be at least ±0.8 Vpp. No additional configuration is needed to set up the clock source format.

The quality of the input clock is important for high-speed ADCs. The contribution to SNR from clock jitter with a full scale signal at a given frequency is shown in equation 1.

$$SNR_{jitter} = -20 \cdot \log (2 \cdot \pi \cdot f_{IN} \cdot T_{jrms}) \quad (1)$$

where f_{IN} is the signal frequency, and T_{jrms} is the root-mean-square (rms) ADC aperture jitter measured in seconds. The rms jitter is the total of all jitter sources including the clock generation circuitry, clock distribution and internal ADC circuitry.

For applications where jitter may limit the obtainable performance, it is of utmost importance to limit the clock jitter. This can be obtained by using precise and stable clock references (e.g. Hittite PLL/VCO solutions, such as HMC1035LP6GE) and make sure the clock distribution is well controlled. It might be advantageous to use analog power and ground planes to ensure low noise on the supplies to all circuitry in the clock distribution. It is of utmost importance to avoid crosstalk between the ADC output bits and the clock and between the analog input signal and the clock since such crosstalk often results in harmonic distortion.

The jitter performance is improved with reduced rise and fall times of the input clock. Hence, optimum jitter performance is obtained with LVDS or LVPECL clock with fast edges. CMOS and sine wave clock inputs will result in slightly degraded jitter performance.

If the clock is generated by other circuitry, it should be re-timed with a low jitter master clock as the last operation before it is applied to the ADC clock input.

Using PLL/VCO as Clock Source

When the direct ADC clock generation is not available, a high performance PLL/VCO should be utilized to generate a low jitter master clock. This should be applied to the ADC either directly or through a fan out buffer.

The recommended PLL/VCO for HMCAD1513 is HMC1035LP6GE. The recommended fan out buffer is HMC987LP5E.

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Definition of Terms

Aperture delay (t_{AD}) The delay difference between Analog and Clock inputs to sampling.

$t_{AD} = T_{sd} - T_{id}$, where

T_{sd} delay from Clock input to sampling, and
T_{id} delay from Analog input to sampling.

Aperture jitter (t_{jrms}) The sample-to-sample variation in Aperture delay.

Cross Talk (X_{tlk}) Crosstalk is the signal coupling between the ADC channels, and is measured by applying full scale signals to both an adjacent channel and to the channel of interest. The crosstalk is the ratio of power in between the signal applied to the adjacent channel and the signal power at the channel of interest that origin from the adjacent channel.

Decibel – carrier (dBc) A unit where the parameter is measured by comparing to the applied fundamental (or carrier) power in the given test.

Decibel – Full Scale (dBFS) A unit where the parameter is measured by comparing to the theoretical maximum fundamental power based on Full Scale Range.

Differential Non-Linearity (DNL) The DNL is the deviation from the ideal voltage that causes a change of one single code (1 LSB). The DNL plot is a diagram showing this deviation for all the codes in the ADC. The DNL parameter is the worst case value on this diagram.

Effective Number of Bits (ENOB) Measures the converter performance in terms of number of bit resolution, based on a perfect ADC with quantization noise.

ENOB = (SNDR – 1.76)/6.02.

Full Power Bandwidth (FPBW) The analog input frequency where the power of the fundamental is reduced by 3 dB compared to the low-frequency value.

Full Scale Range (FSR) The voltage difference at the analog input of the ADC between the voltage that will *generate the maximum digital output code*, and the voltage that will *generate the minimum digital output code*.
When referring to deviation in Full Scale Range this means that the analog voltages giving max/min output code are different from the theoretical values. A Full Scale Range fundamental is a sine wave where the lowest value gives minimum output code and the highest value gives maximum output code.

Noise Power Bandwidth (NoiseBW) The analog input frequency where the power of the fundamental is reduced by 3 dB compared to the low-frequency value.

Gain error (G_{abs}) The deviation from ideal Full Scale Range. This parameter is independent from G_{rel}.

Gain flatness The input frequency range where the Gain variation is within the specified number of dB.

Gain matching (G_{rel}) The mismatch in Full Scale Range between the ADC channels. This parameter is independent from G_{abs}.

Integral Non-Linearity (INL) The INL is the deviation of the ADC transfer function from an ideal straight line. The INL plot is this deviation generated with the best fit method for the ADC Full Scale range. The INL parameter is the worst case value on this line.

Signal to Noise Ratio (SNR) The ratio of the power of the fundamental to the power of the noise measured in dB. SNR excludes DC, harmonics and interleaving spurs.

Signal to Noise and Distortion Ratio (SNDR) The ratio of the power of the fundamental to the power of the noise and distortion measured in dB. SNDR excludes DC.

Spurious Free Dynamic Range (SFDR) The ratio of the power of the fundamental to the power of the highest harmonic or spurious component.

Document Changes

Version	Comment
v00.0414	Initial release

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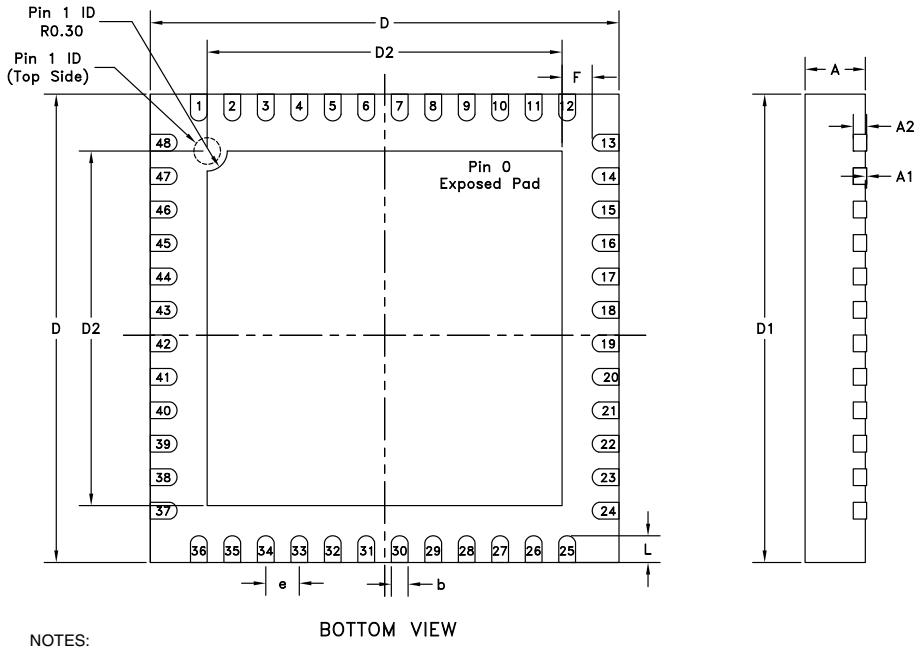
Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Table 22. 7x7 mm QFN 48 Pin (LP7) Dimensions

Symbol	Millimeter			Inch		
	Min	Typ	Max	Min	Typ	Max
A	0.8	0.9	1	0.031	0.035	0.039
A1	0	0.02	0.05	0	0.001	0.002
A2		0.2			0.008	
b	0.19	0.25	0.31	0.007	0.01	0.012
D, D1	6.9	7	7.1	0.272	0.276	0.280
D2	5.15	5.3	5.41	0.203	0.209	0.213
L		0.4			0.016	
e	0.44	0.50	0.46	0.017	0.020	0.022
F	0.20			0.008		

Package Information

Part Number	Package Body Material	Lead Finish	MSL [1]	Package Marking [2]
HMCAD1513	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	Level 2A	HAD1513 XXXXX

[1] MSL, Peak Temp: The moisture sensitivity level rating classified according to the JEDEC industry standard and to peak solder temperature.
[2] Lot number XXXXX

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