LINEAR TECHNOLOGY

DESIGN NOTES

Achieving Microamp Quiescent Current in Switching Regulators

Design Note 11

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Many battery powered applications require very wide ranges of power supply output current. Normal conditions require currents in the ampere range, while standby or "sleep" modes draw only microamperes. A typical lap top computer may draw 1 to 2 amperes running while needing only a few hundred microamps for memory when turned off. In theory, any switching regulator designed for loop stability under no-load conditions will work. In practice, a regulator's relatively large quiescent current may cause unacceptable battery drain during low output current intervals.

Figure 1 shows a typical flyback regulator. In this case the 6V battery is converted to a 12V output by the inductive flyback voltage produced each time the LT®1070's V_{SW} pin is internally switched to ground. An internal 40kHz clock produces a flyback event every 25µs. The energy in this event is controlled by the IC's internal error amplifier, which acts to force the feedback (FB) pin to a 1.23V reference. The error amplifiers high impedance output (the V_C pin) uses an RC damper for stable loop compensation.

This circuit works well but pulls 9mA of quiescent current. If battery capacity is limited by size or weight this may be too high. How can this figure be reduced while retaining high current performance?

A solution is suggested by considering an auxiliary V_C pin function. If the V_C pin is pulled within 150mV of ground the IC shuts down, pulling only 50 microamperes. Figure 2's special loop exploits this feature, reducing quiescent current to only 150 microamperes. Here, circuitry is placed between the feedback divider and the V_C pin. The LT1070's internal feedback amplifier and reference are not used. Figure 3 shows operating waveforms under no-load conditions. The 12V output (trace A) ramps down over a period of seconds. During this time comparator A1's output (trace B) is low, as are the paralleled inverters. This pulls the V_C pin (trace C) low, putting the IC in its 50µA shutdown mode. The V_{SW} pin (trace D) is high, and no inductor current flows.

When the 12V output drops about 20mV, A1 triggers and the inverters (74C04) go high, pulling the V_C pin up and turning on the regulator. The V_{SW} pin pulses the inductor at the 40kHz clock rate, causing the output to abruptly rise. This action trips A1 low, forcing the V_C pin back to shutdown. This "bang-bang" control loop keeps the 12V output within the 20mV ramp hysteresis window set by R3-R4. Diode clamps prevent V_C pin overdrive. Note that the loop oscillation period of 4-5 seconds means the R6-C2 time constant at V_C is not a significant term. Because the LT1070 spends almost all of the time in shutdown, very little quiescent current (150µA) is drawn.

Figure 4 shows the same waveforms with the load increased to 3mA. Loop oscillation frequency increases to keep up with the loads sink current demand. Now, the V_C pin waveform (trace C) begins to take on a filtered appearance. This is due to R6-C2's 10ms time constant. If the load continues to increase, loop oscillation frequency will also increase. The R6-C2 time constant, however, is fixed. Beyond some frequency, R6-C2 must average loop oscillations to DC.

Figure 5 plots what occurs, with a pleasant surprise. As output current rises, loop oscillation frequency also rises until about 500Hz. At this point the R6-C2 time constant filters the V_C pin to DC and the LT1070 transitions into "normal" operation. With the V_C pin at DC it is convenient to think of A1 and the inverters as a linear error amplifier with a closed loop gain set by the R1-R2 feedback divider. In fact, A1 is still duty cycle modulating, but at a rate far above R6-C2's break frequency. The phase error contributed by C1 (which was selected for low loop frequency at low output currents) is dominated by the R6-C2 roll off and the R7-C3 lead into A1. The loop is stable and responds linearly for all loads beyond 80mA. In this high current region the LT1070 behaves like Figure 1's circuit.

The loop described provides a controlled, conditional instability to lower regulator quiescent current by a factor of 60 without sacrificing high power performance. Although demonstrated in a boost converter, it is readily exportable to other configurations, (e.g., multi-output flyback, buck, etc.) allowing LT1070 use in low quiescent power applications.

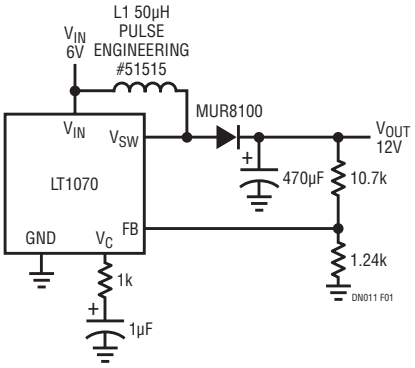

Figure 1. Typical LT1070 Flyback Regulator

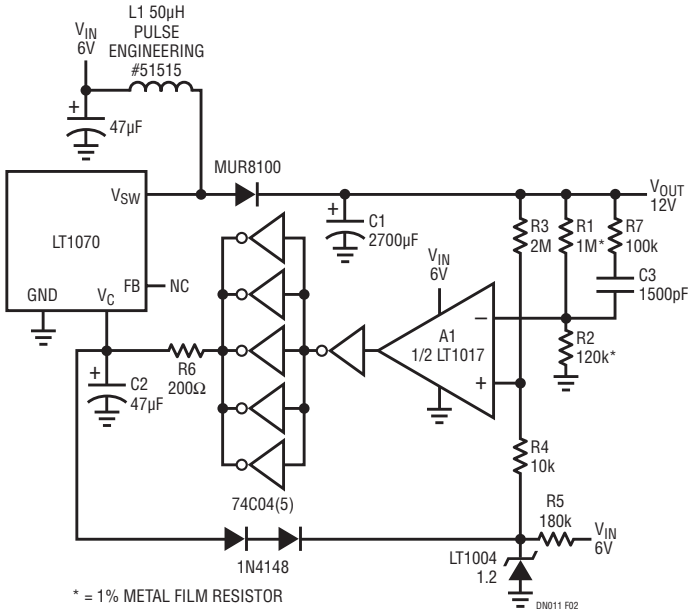

Figure 2. Low Quiescent Current Flyback Regulator

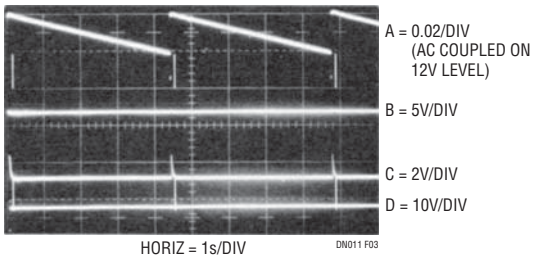

Figure 3. Waveforms at No Load for Figure 2 (Traces B and D Retouched for Clarity)

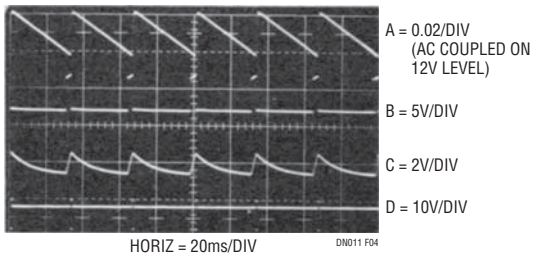

Figure 4. Waveforms at 3mA Load for Figure 2

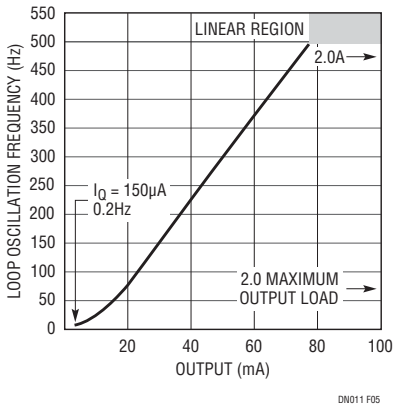

Figure 5. Output Current vs Loop Oscillation Frequency for Figure 2

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