Using the LTC Op Amp Macromodels

Getting the Most from SPICE and the LTC Library

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INTRODUCTION

This application note is an overview discussion of the Linear Technology SPICE macromodel library. It assumes little if any prior knowledge of this software library or its history. However, it does assume familiarity with both the analog simulation program SPICE (or one of its many derivatives), and modern day op amps, including bipolar, JFET, and MOSFET amplifier technologies.

Some Preliminary SPICE Facts of Life

In the past few years, SPICE simulations have really begun to capture a high level of attention on the part of analog circuit designers. Perhaps this is due to more affordable high performance computers, or perhaps the time for simulation is now upon us. In any event, the bottom line is that IC vendors are now making macromodels for op amps available to their customers.

For the analog circuit designer, there can be no better fate for simulations, viewing this situation in terms of which model to use. Designers no longer need worry about whether the third party supplier's model can really cut it. Speaking in terms of the ultimate potential, no one can know an actual part better than the people who designed and produced it, that is the original source IC vendor. The only possible caveat to this scenario is that the vendor supplying an op amp model needs to fully understand not only the real part, *but they must also understand SPICE and modeling issues.* Without both types of understanding firmly in place, the user can end up with a real part that works well and a model which doesn't. For such a case, simulation will be of little value; simulation runs to verify circuit performance won't match the actual part's bench performance.

Fortunately, this type of problem seems to be diminishing. If this were not so, the rapid increase in attention to models would not be taking place. However, all is not necessarily peaceful bliss for analog designs, and yes, we still need to actually build breadboards to check out circuit designs in the lab. The go-go project managers may say "Simulate it, we don't have time to fool with the breadboard and hand-built prototypes." Rarely will this ramrod approach be a truly wise move, now or in the future, except in specialized circumstances.

While it is certainly true that we are in the age of computers, and that they really do aid our tasks in many ways, that is simply not enough for all cases. SPICE (or any simulation tool) can only act upon the information fed into it to analyze a circuit. Model quality issues set aside for the moment, can you honestly say that you have fully sufficient characterization data for every single relevant connection point/load that your circuit will ever see? Do you understand *all* of the parasitic issues it will face? If you can say yes to all of these, then maybe all that you need is just a good op amp model, and SPICE. More likely, there will always be some uncertainties, so breadboarding will remain the only advisable choice for relatively complex circuits, particularly those never built before.

This then leaves a question of model quality and degree of functionality to be answered. Are the presently available models enough? Just how far can they be trusted for the types of simulations that are to be performed? Hopefully, most of these answers will be more apparent by the end of this note, as it contains many different examples. Nevertheless, no IC vendor (or other model supplier) is likely to ever stand up and say, "We guarantee this model when used with simulator ABC, and the simulated performance will be within X% of the actual part connected within a corresponding circuit."

Forget it, SPICE simply doesn't work that way, and likely never will. What SPICE *is* good for is predictive analysis, worst case limit testing, design feasibilities, etc. But even then it will always have limitations; it will never be any better than the information fed to it, and obviously this impacts macromodels as well as all other circuit elements. This may sound at first like a questionable reward, but bear in mind just how you can do a worst case design performance limit for a board with several dozen components. Traditionally, this has been not only difficult, it very often didn't get done at all (except by production line "hot patches"). Logically then, IC manufacturers offering macromodels place caveats and performance limitations on them, which should be understood by the user. These caveats don't make the models at all useless, but they do define the nature and extent of what they can achieve. The following model disclaimer is typical, and is excerpted from the LTC model library:

"This library of macromodels is being supplied to LTC users as an aid to circuit designs. While the models reflect reasonably close similarity to corresponding devices in performance terms, their use is not suggested as a replacement for breadboarding. Simulation should be used as a forerunner or a supplement to traditional lab testing.

Users should very carefully note the following factors regarding these models: Model performance in general will reflect typical baseline specs for a given device, and certain aspects of performance may not be modeled fully. While reasonable care has been taken in their preparation, we cannot be responsible for correct application on any and all computer systems. Model users are hereby notified that these models are supplied as is, with no direct or implied responsibility on the part of LTC for their operation within a customer circuit or system. Further, Linear Technology Corporation reserves the right to change these models without prior notice.

In all cases, the current data sheet information for a given real device is your final design guideline, and is the only actual performance guarantee. For further technical information, refer to individual device data sheets. Your feedback and suggestions on these (and future) models will be appreciated!"...

So, perhaps the first thing to understand about SPICE op amp macromodels is that they invariably come with caveats. Such are the op amp macromodel facts of life.

But, like many other things in design engineering, an op amp macromodel can be good or bad, dependent upon what you need to do with it. Indeed, circuit requirements differ, and either DC or AC considerations can drive a given application. At LTC, we feel that the *overall* performance of a macromodel is what can make or break it. Therefore, the op amp modeling has been directed towards getting maximum real world performance in the models, that is performance which in many ways is like the actual op amp device. But, it also means models which do not sacrifice general utility to maximize one single aspect of performance, AC, DC, or whatever.

A Background of SPICE Op Amp Macromodels

Circuit designers generally like to work quickly and efficiently with SPICE simulations, so the macromodel approach is fundamentally very attractive, for good reason. Rather than using a full set of transistors, macromodels use the various controlled sources supported within SPICE, and they also minimize/simplify P-N junctions as much as possible. This approach can increase simulation speed several fold over a full circuit using 30-40 actual transistor models. It can also work well (within its limitations) given a well designed macromodel.

Op amp macromodeling got its start about 15 years ago, in what is now a classic topological approach by Boyle, Cohn, Pederson, and Solomon.[1] The model topology described in this seminal work has now become known generically as the Boyle macromodel. With recent advances in computing hardware, modeling as a linear circuit design aid has taken off in the last few years. This of course has re-focused attention on modeling techniques in general, but the Boyle architecture in particular. Now, armed with better macromodels for their designs, analog circuit architects are able in many cases to move more quickly toward better designs.

Note 1: Boyle, G.R., Cohn, B.M., Pederson, D.O., Solomon, J.E., "Macromodeling of Integrated Circuit Operational Amplifiers," IEEE Journal of Solid-State Circuits, Vol. SC-9, # 6, December 1974.

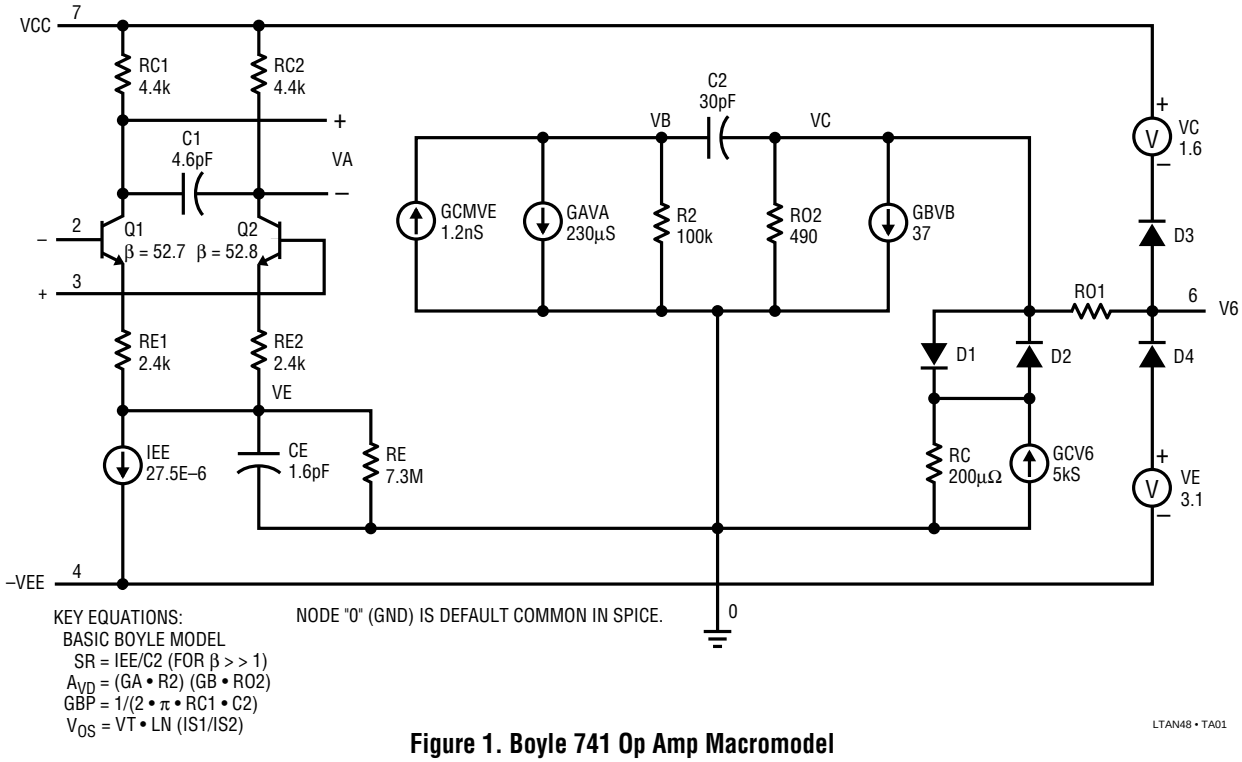

Figure 1. Boyle 741 Op Amp Macromodel

A Short Course on the Boyle Macromodel

While the Boyle model topology has become a default macromodel standard, it also has received criticism for op amp performance aspects it doesn't handle. Unfortunately, not all of this criticism has been well focused, or couched in a meaningful perspective. For example, many critics of the Boyle model often fault it *for what it doesn't do in its original or most basic form*, and simply ignore more recent enhancements (which, ironically, aren't so hard to find). One such case of Boyle based macromodels with many useful enhancements are those produced by the MicroSim Parts[2] program. And, as the following discussions show, the basic Boyle model has been usefully enhanced and expanded in other regards.

The Boyle macromodel is shown in Figure 1, essentially just as it was originally described in the 1974 paper. This example model is for a 741 op amp, which has a bipolar NPN input stage. The model parameters are noted in the figure, and when run, this macromodel duplicates the characteristics of the device quite well. Comparison of the actual parameters for the 741 as modeled can be done by a detailed contrast of the paper's appendix parameters, and those of this figure. Note that the typical op amp pin numbers have been added to tie this model more closely to a real device. As will later be apparent, this nodal convention is used throughout in the LTC amplifiers.

Listing 1 (see listings at end of application note) is a sample macromodel for an 8741 op amp. This model was produced by the LTC macromodel program for NPN op amps, with input data taken from the Boyle paper appendix (Note: there is no *actual* LTC "8741"; this particular model was done as an exercise). Comparison of the first portions of this model with the values of Figure 1 shows good correlation.[3]

Some of the key equations for the basic Boyle macromodel are noted in Figure 1, and they all can be found within the text of the paper itself. The key op amp parameters modeled are gain bandwidth product (GBP), slew rate (SR), phase margin, DC gain (A_{VD}), CMRR, input offset voltage (V_{OS}), input bias current (I_B), input offset current

Note 2: MicroSim, vendor of PSpice™, Probe™, and Parts™. 20 Fairbanks, Irvine, CA, 92718, (714) 770-3022.

Note 3: This comparison of the Listing 1 8741 macromodel with the Boyle original is valid only for the code within sections "INPUT" and portions of "INTERMEDIATE." As will be noticed, there are only slight differences here (due to rounding). Because of the different type of voltage/current limiting used in the LTC macromodel, there are major differences in gb, RO2, and those portions following, which show up as new code after "OUTPUT."

(I_{OS}), output current limiting (I_{SC}), output voltage limits (V_{SAT} ±), output resistance (R_{OUT}), and power supply quiescent current (I_Q). *(Note: The diode/VCCS and diode/voltage source elements of this figure around RO1 are associated with the voltage and current limiting of the original Boyle model. Inasmuch as these networks are not heavily used in the LTC macromodels, they are not discussed in any detail. The new LTC functional replacements for current and voltage limiting will be discussed in the following section).*

Gain-Normalized Input Stage Operation

There is a very important design distinction of the Boyle model topology which allows it to be extremely flexible with regard to adaptations to other input transistor types. Referring to Figure 2, a simplified schematic-form Boyle type model, this feature lies in the fact that the input differential transistor pair Q1/Q2 are, in fact, set by the macromodel design parameters to operate at a differential gain of unity. In the case of the bipolar types shown, the original Boyle design equations establish this by the presumption that the gain from the amplifier's ± inputs to the differential output VA is by definition unity.

In the original model, this unity gain, or gain-normalized operating condition for Q1/Q2 was provided by the inclusion of emitter resistances, RE1/RE2. These resistors force the differential topology to this gain (once given a current for IEE). This gain normalization step adds great usefulness to the model, in simplifying the design expressions for slew rate and gain bandwidth product. As a result, it leads to the substitution of other input devices within this architecture with relative ease.

Speaking more broadly, the input stage gain-normalization step provides specifically for implementing variants of the structure, without major topology changes. As noted, the original paper allowed for NPN or PNP bipolar pairs in the basic design equations. However, if the model topology is viewed more generally, a fundamental fact about it is that *virtually any differentially operated transconductance pair* can be used in the front end. From the signal point VA (the differential outputs of Q1/Q2), the

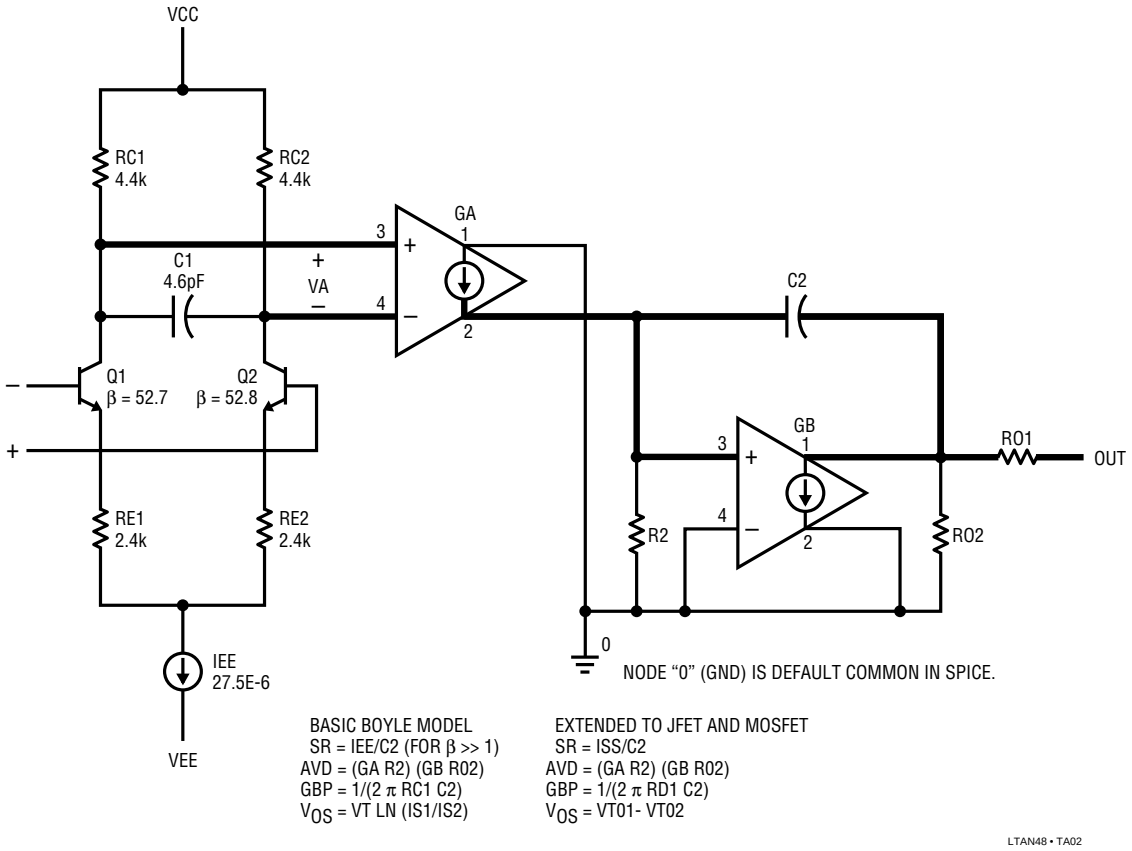

Figure 2. Input Gain-Normalized Op Amp Macromodel

remaining path of the model can be essentially the same, with the basic design equations holding. For example, in the case of a PFET type amplifier, Q1/Q2 are replaced by P-channel FETs J1/J2; or for PMOS types, they become MOS devices M1/M2, and so on.

With other variations of this type of macromodel topology, provisions are made for transconductance adjustments to the stage, such that the differential pair used operates at unity gain. This can be either through the transconductance parameters of the transistors themselves, or via the associated degeneration resistances (RS1/RS2 for FET devices would correspond to the RE1/RE2 for bipolars). Of course, for whatever type of transconductance devices used, suitable biasing steps must be made.

Note that this general concept allows many variations of the original Boyle model to exist. The basic Boyle model design equations of Figure 1 then can be viewed to dictate the model's performance. This can easily be extended to include the various types mentioned. For example, as shown in the extended equations, the PFET and PMOS expression for SR will follow the same form, with I_{SS} replacing IEE. The corresponding expression for GBP in these amplifiers is similar, with RD1 substituting for RC1.

In creating a different input stage op amp, the different input transistor types are accommodated via the SPICE transistor model parameters of J1/J2, M1/M2, etc. The specific transistor model parameters of these devices then determine the amplifier input V_{OS}, I_B, and I_{OS}.

While this input stage gain normalization step makes the input flexible, it does have a basic trade-off. Because the input transistors are operated at current/gain levels generally unlike those used in the actual op amp, the noise properties are generally uncorrelated (note that a low noise op amp will have a very high voltage gain in the first stage, distinctly unlike this model). As a result of this, the input noise performance of a gain-normalized model will usually not track the real IC accurately. Please note however that this factor is *not* unique to Boyle type models, it is just as true for other models with input stage gain normalization.

THE LTC APPROACH TO SPICE OP AMP MACROMODELS

The LTC approach to op amp macromodels has been one aimed towards achieving design improvements within the models, but with a balanced array of simulation enhancements. Attention has been directed towards practical, useful op amp macromodels which emulate the LTC catalog devices in both their specifications as well as general functionality. This approach has been rooted in building on the Boyle macromodel topology, enhancing it where appropriate. To one degree or another, this has been done for each case of the family of the four amplifier macromodel topologies supported.

LTC macromodels are produced in original form by an appropriate member from a family of macromodel programs. These programs implement the algorithms and otherwise support features of the customized op amp macromodels. For a given program, the output consists of a SPICE compatible ASCII file, in the form of an op amp specific macromodel. With this approach, op amp macromodels can be produced virtually as fast as spec sheet definition data can be keyed in.

As noted, the program produces an ASCII macromodel, and Figure 3 is a header portion of a sample macromodel produced by one of the programs. Note that the header includes information in the form of SPICE comment lines (those lines* prefixed), in addition to the actual code of the macromodel itself. In this case the header is for the LT1022 (top line). On line two, the date/time stamp and the general model type are listed. In the next four lines all key specs as used within the model are recorded. This information comprises the macromodel specifications, and the format is generally consistent across the four families of

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*
* Linear Technology LT1022 op amp model
* Written: 05-10-1990 15:08:03 Type: PFET input, internal comp.
* Typical specs:
* Vos=1.0E–04, Ib=1.0E–11, Ios=2.0E–12, GBP=8.0E+06Hz, Phase mar.= 45 deg,
* SR (low)=2.5E+01V/us, SR (high)=5.0E+01V/us, Av=112.0dB, CMRR= 92.0dB,
* Vsat(+)=1.8V, Vsat(–)=1.8V, Isc=+/–30mA, Rout= 50ohms, Iq= 5mA.
* (input cm clamp *optional*)
*
* Connections: + – V+V–O                                    LTAN48 • TA20
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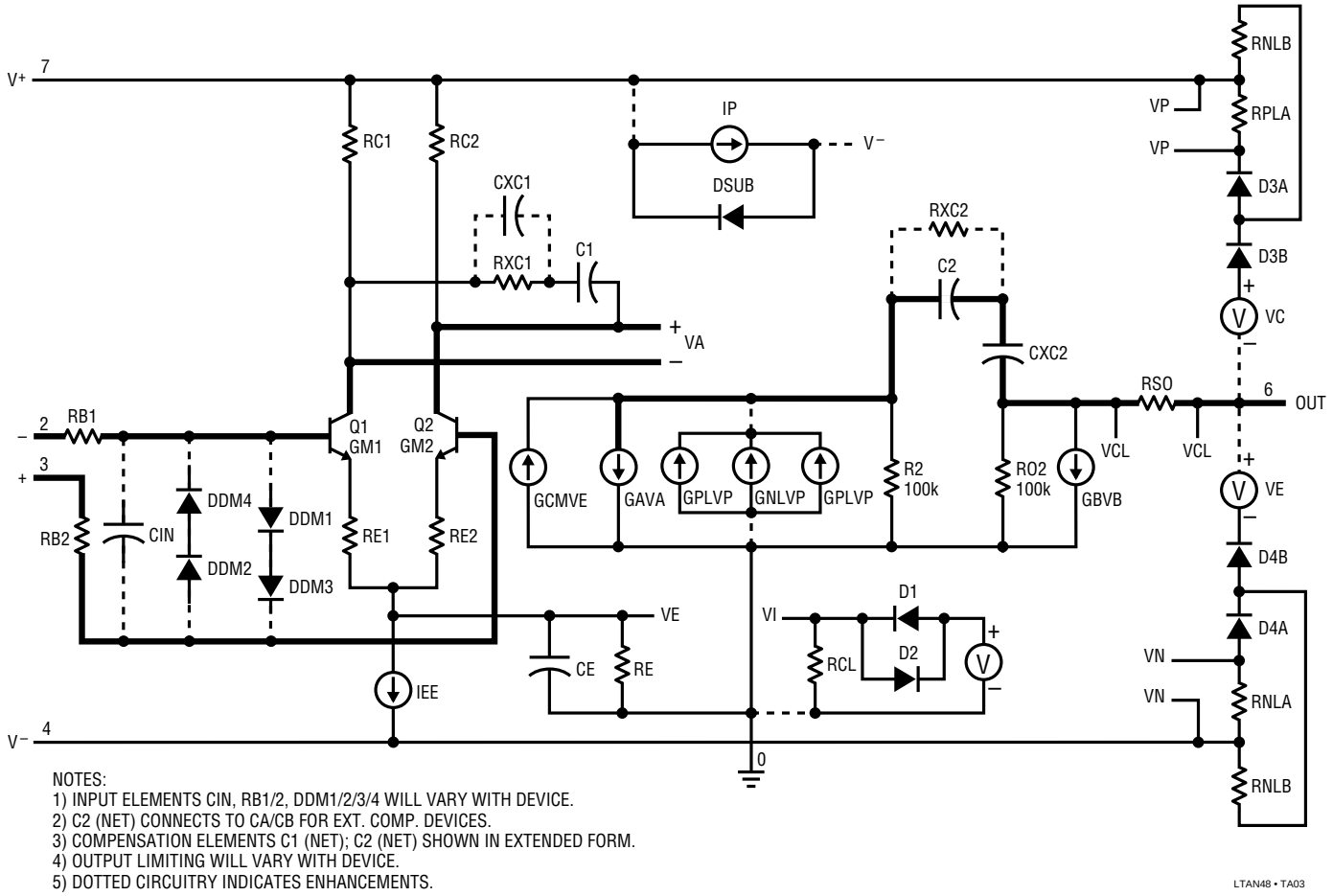
Figure 3. Header Portion Sample



NOTES:
1) INPUT ELEMENTS CIN, RB1/2, DDM1/2/3/4 WILL VARY WITH DEVICE.
2) C2 (NET) CONNECTS TO CA/CB FOR EXT. COMP. DEVICES.
3) COMPENSATION ELEMENTS C1 (NET); C2 (NET) SHOWN IN EXTENDED FORM.
4) OUTPUT LIMITING WILL VARY WITH DEVICE.
5) DOTTED CIRCUITRY INDICATES ENHANCEMENTS.

LTAN48 • TA03

Figure 4A. Bipolar NPN Input Op Amp Macromodel (Simple)

macromodel types. An optional comment line completes the main part of the header. The macromodel header conveniently documents actual working parameters of the model.

Obviously, the programmed approach is an efficient method for generating new or revised macromodels for release to the public. It also has the important additional feature that it allows LTC application engineers to quickly respond to field requests for custom macromodel values for any parameter modeled.

THE LTC MACROMODEL FAMILY

As previously noted, the LTC macromodel families are comprised of four types of models. There are models for NPN and PNP bipolar input devices, for P-channel JFET input devices, and for PMOS FET input devices. While there are similarities across these four macromodel types, there are also unique distinctions within each. The following sections detail each of these macromodel types, illustrating the common overall features as well as those unique to each type of device.

The LTC Bipolar NPN Input Macromodels

Listing 2 (see listing at end of application note) is a macromodel of the LT1007 NPN bipolar op amp, which generally corresponds directly to the complete NPN macromodel schematic of Figure 4.[4] For clarity, the schematic is shown in two forms; the “simple” form in Figure 4A uses symbolic connections, while the “detailed” form in Figure 4B follows the actual listing.

This schematic appears busy, because of the fact that it shows all possible options of this NPN topology. While all

Note 4: This generic schematic has no values for this NPN case, nor will those for the other amplifiers. Instead, actual values for the device under discussion are noted in the model listing.

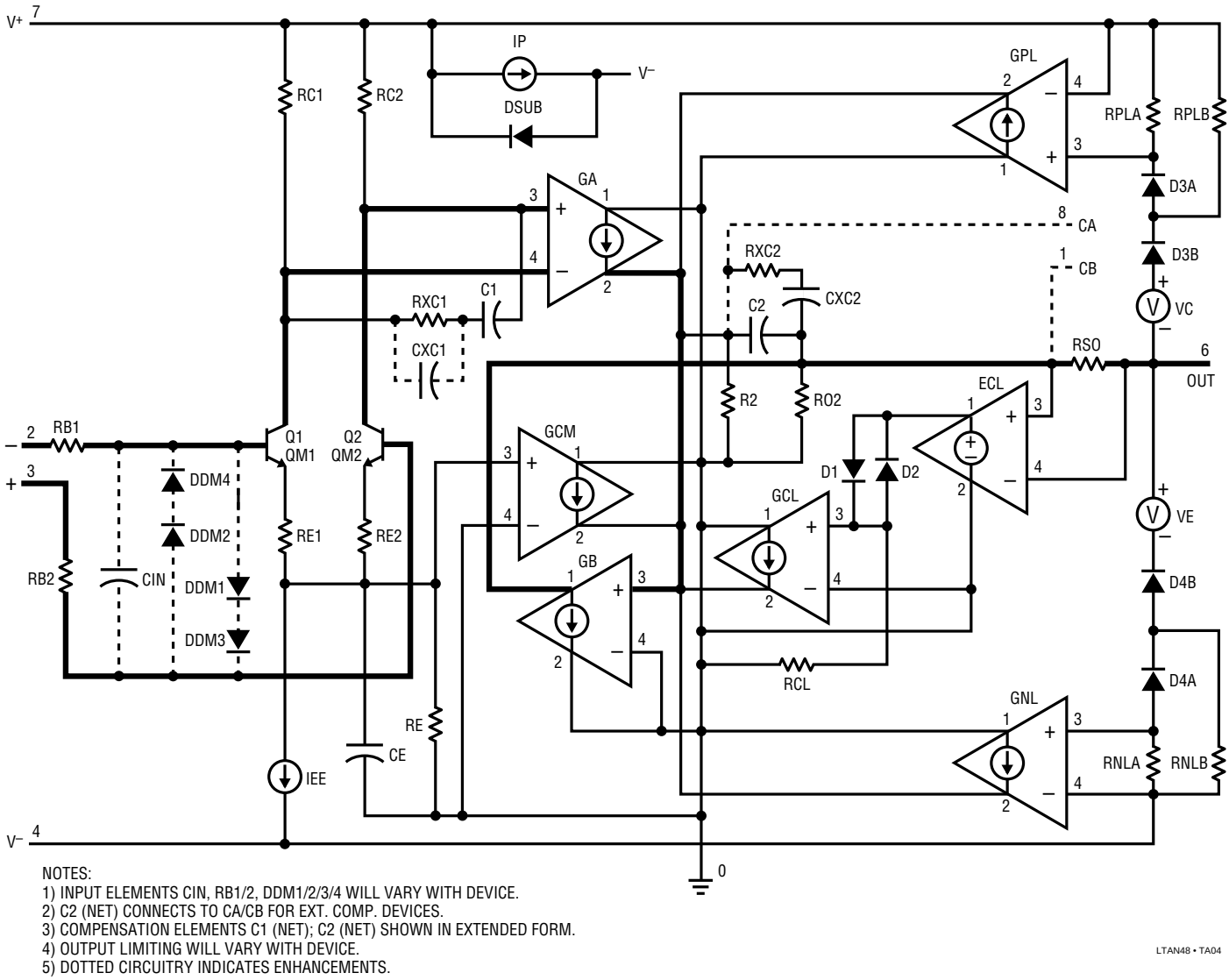


Figure 4B. Bipolar NPN Input Op Amp Macromodel (Detailed)

of the possible options need not be present within a given device, most of them are in fact used in the case of the LT1007. With regard to the schematic as shown, the many device specific conditional details which this NPN macromodel can handle will be discussed in this context.

At the very front end of the model, there is optional use of differential input clamp diodes, with or without series resistance, etc., and similar comments apply to CIN. These model enhancements are employed specifically to closely mimic device characteristics. For example, with the (real) LT1007 and OP-27 type of device shown, a pair of two-diode differential clamps are used, DDM1-DDM4, but without a series resistance (RB1 = RB2 = 0). These options (and others) are shown dotted in Figure 4, to suggest the multiple possibilities, and will vary from one device type to another. Other DC enhancements used are a power consumption current source IP, to mimic DC current drain, and a reverse substrate diode, DSUB (which also can be given a breakdown voltage to simulate maximum supply voltage). Overall, the general intent is to make the macromodels behave more as their real IC counterparts, in these and other functional details.

Throughout this macromodel the main DC signal flow path is shown by the heavy lines, for clarity. Controlled sources GA and GB function as they do in Figure 1, as do passive components R2, RO2, C2, and C1. As is noted, both C1 and

C2 can be expanded from the original Boyle single capacitor, to more complex optional network(s). The LT1007 uses both of these networks, to simulate the multiple pole-zero roll-off characteristic of the actual device. This is covered in more detail in the following section, with performance examples.

The output stage of this model is entirely new vis-a-vis the Boyle model, and is discussed in the following section in terms of the new current/voltage limiters. Because of the reduced 1Ω value used for RSO (or RS), the net small signal output resistance of this model will usually be dominated by the value for RO2. This in turn makes the RO2 value higher, compared to a basic Boyle model, and it also makes GB larger (for the same DC gain).

Improved Voltage and Current Limiting

In the original Boyle model of Figure 1, bias voltages VE and VC along with diodes D3 and D4 were used to a provide brute-force type output voltage limiting. While workable, this scheme produces large internal limit currents within the model. It also can give rise to gain errors in very high gain precision amplifiers, due to parasitic diode leakages below the limiter threshold.

For maximum output current simulation, diodes D1 and D2 of Figure 1 provide current limiting by indirectly sensing the voltage drop across RO1 (the controlled source GC produces a replica of the output voltage across RC, which effectively places D1/D2 in parallel with RO1). When D1 or D2 conduct to start limiting, this also produces very large currents in limit, as well as some gain degradation below threshold.

In many macromodels, LTC has implemented new forms of voltage and current limiting. These schemes use buffered biased diodes, which allow both full amplifier gain below the limit thresholds, as well as accurate limit thresholds for output voltage and current. They are described now, and are used not only within many of the NPN macromodels, but throughout the family of models.

Voltage limiting in the new model of Figure 4B can be described for either the negative or positive swing, as they are similar. The positive swing limiter, which is composed of D3A, D3B, VC, RPLA, RPLB and GPL, will be described. This setup would appear at first as a modified brute-force limiter with two series diodes and a similar offset voltage source for the threshold. It is not however; it is in fact a local closed loop system, which depletes the total current available from source GA when the output voltage limit threshold is reached. This allows clean limiting, with no large internal currents.

The buffered biased diode D3A and resistance RPLB are used to control the leakage of D3B, which would otherwise cause gain errors for an amplifier of the LT1007/OP-27 family. This voltage limit technique was found to be justified for most op amps with DC gains of 120dB or more. With it active, the LT1007's 150dB gain is reached within a fraction of a dB.

Current limiting in this model is symmetrical, that is it has the same current limit level for both source and sink currents. This is typical of amplifiers which use bipolar output stages. CMOS output stages are often asymmetrical, and a modified form of this current limiter will be shown under the discussion of the PMOS input amplifier types.

To minimize loading effects of the current limiter, it uses a dedicated floating differential input buffer amplifier, ECL. This VCVS senses the voltage drop across RSO (or RS), which is directly proportional to output current. The current limit threshold is defined by the gain of ECL, and the characteristics of D1, D2, RCL, and GCL. In this instance, the local loop is closed when the amplified output of ECL drives RCL, through either D1 or D2. As was true in the case of the voltage limiter, when the limit threshold is reached the controlled source (in this case GCL) depletes all available current from GA. Again, this allows clean current limiting, with no large internal currents being produced.

Because of the buffering by ECL, this type of current limiter has very low errors when below its threshold. Not only are the errors low with regard to gain degradation, but the current limit is very accurate.

There is also a much more subtle advantage common to these two limiters, and that is the fact that they are achieved via a parallel feedback path. As such, they will by definition be transparent below threshold, a point already made above. However, a useful side advantage of this is that this macromodel can get along quite well in truth

without either limiter (for special cases). In fact, they can be disabled for signal purposes very simply, by commenting out the controlled source driving GA, be it either GPL, GNL, or GCL. This can come in handy, if it should ever be necessary to troubleshoot a circuit and/or model for errors.

Caution!

Those who may be tempted to try this should of course know what they are about! Do bear in mind that a macromodel without any limiters is capable of very high voltages and/or currents! Perhaps a more significant bonus of this limiter design scheme is that special "turbo" forms of a given model can be saved, such as an LT1007 model sans limiters. This will greatly speed up analyses, *as long as the external circuit provides for a proper DC loop closure*.

Macromodel Embedded Models

At the bottom of each macromodel listing is a section titled MODELS, which does in fact define those transistor, diode, or any other models used local to the macromodel. In the case of the NPN LT1007 op amp, the NPN models for Q1/Q2 are, as noted, different in terms of IS and BF (current gain), for the following reasons.

V_{OS}, the input offset voltage of the amplifier input pair, is modeled by using two slightly different NPN transistor models, QM1 and QM2. The ratio of their two saturation currents will produce an offset voltage, V_{OS}, which is:

$$V_{OS} = kT/q^* \ln(IS1/IS2)$$

With the ratios as shown in Listing 2, this produces the typical 20μV offset of the LT1007C.

Bias and offset currents are modeled by using a different BF for the two input pair halves, as:

$$BF1 = IC1/(I_B + (I_{OS}/2)) \text{ and } BF2 = IC2/(I_B - (I_{OS}/2))$$

The BF values shown for QM1 and QM2 are those which correspond to currents of I_B = 15nA and I_{OS} = 12nA (again for the LT1007C). The gains listed appear high, however this is a by-product of the fact that the actual LT1007 device uses bias current compensation, and the model accounts for this simply with a higher BF.

The remaining models used in the LT1007 are diodes used in various locations, with IS scaled as to the specific use.

Phase/Frequency Response Extensions

One performance area where op amp modeling has recently received strong attention is in regard to frequency response. The original Boyle model of Figure 1 has a dominant pole set by C2 and a secondary pole set by C1. Many op amps now popular have a much more complex phase/frequency response. As a result, using a basic Boyle model AC topology to simulate their transient response can be inaccurate for some applications.

Solutions to modeling additional poles and zeros can range from simple to complex, depending upon what overall trade-off the model designer chooses. For example, a number of sequential pole/zero stages can be added to a model for very fine emulation of small signal transients. In practice, this approach needs to be weighed carefully on an overall basis.

It is not under question here that it is possible to greatly improve upon a simple Boyle type models' phase/frequency response. However, what the macromodel user needs to know is not just how the AC response is improved, but also what is the price to be paid for it. The end results may or may not be worth the possible drawbacks, specifically potential penalties in terms of additional memory required, longer simulation times, and possible convergence issues. Of course these considerations are basic, and are applicable to any model, LTC types included. Nevertheless, it should be noted that these types of problems exaggerate very quickly with multiple amplifier simulations (such as in active filters). It is entirely possible to create more complex models which will not even run in larger multi-amp circuits, when used in standard PC environments with modest memory (~500K).

Alternately, an intermediate approach to modeling some additional poles and zeros can be taken, simply by extending the above mentioned two compensation caps of the basic Boyle model with additional network elements. It is

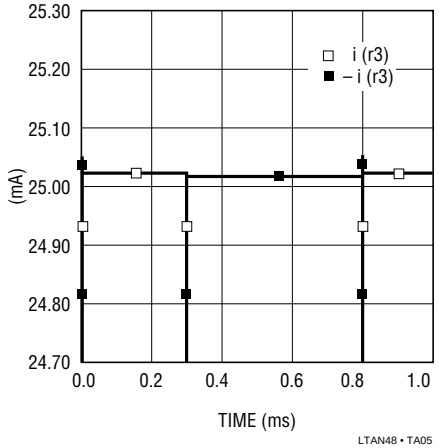


Figure 5A. LT1007 Test F6: I_{SC} (Open Loop, $V_S = \pm 15V$)

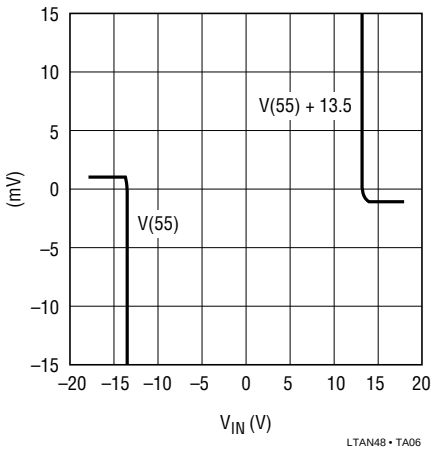


Figure 5B. LT1007 Test F7: V_{SAT} ($V_S = \pm 15V$)

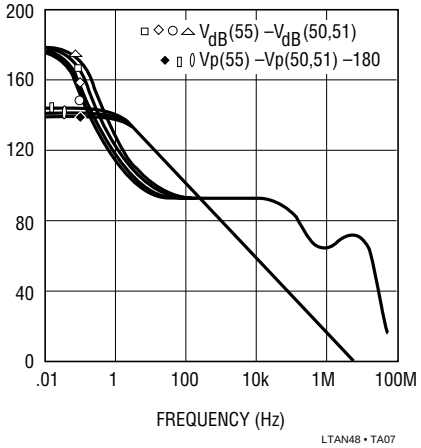


Figure 5C. LT1007 Test F8: Gain/Phase

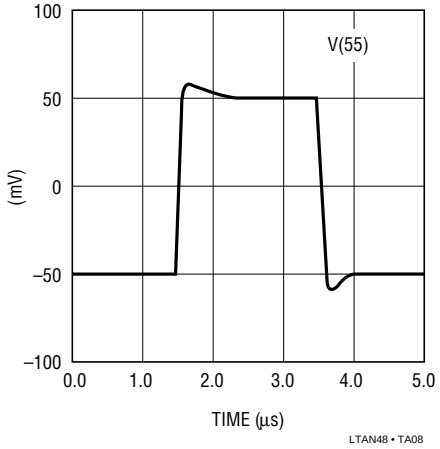


Figure 5D. LT1007 Test F5: Transient Response

Figure 5. Composite Performance Points

this approach that LTC has used in Figure 4. For C1, RXC1/CXC1 can be added as one extension, while for C2, RXC2/CXC2 can be added. Speaking generally, these are part-specific options, with defaults (i.e., no extensions used) of only C1 and C2. Of course for the LT1007 under discussion a full set is used, as noted by Listing 2.

In contrast to arbitrary additional pole/zero stages, this method can be viewed as relatively limited, which in truth it is. However, it has the advantage of minimal added complexity, as no active stages are added to the model. It also has the fundamental virtue of working well within the overall Boyle topology, since it is an extension of it. Together, these controls allow more complex frequency responses to be simulated without additional active stages, with a net result of minimal simulation overhead increases. NPN model examples which use it are the LT1007/LT1037 families, the LT1028 and LT1115, and the OP-27/OP-37 families, but it is an option available with all device families.

NPN Macromodel Performance

At this point, some sample macromodel performance will be shown to illustrate key points. For these and the following SPICE displays, the macromodels used were taken directly from the current released LTC diskette. For the purposes of this application note, the models were edited into the form of the listings as shown herein (by editing out only the header and copyright notice sections for brevity). These files were then used in the various simulations. Unless specified otherwise, the test circuits use ±15V power supplies, and the op amp model tested has a (+) input node of (50), a (–) input node of (51), an

output of (55), and the signal source is applied to node (2). Unless otherwise specified, no SPICE option default changes were made in the CIR files used for the tests. A 16MHz IBM PC compatible computer was used under DOS 4.01, along with MicroSim's PSpice version 4.03 (DOS version). A ramdisk was used as the work disk in all simulations.

The picture series of Figure 5 in composite form illustrates various performance points of the LT1007 macromodel.

In terms of the new limiting schemes employed, they are shown by Figure 5, in tests LT1007 F6 and F7. For display of short circuit current, test F6 operates the amplifier as a comparator (open loop) on ±15V supplies, with the output driving a low value resistor (10Ω). The display is a dual trace of the load current I(R3) and its mirror –I(R3). This allows both the ± current limits to be shown here, on an expanded ±1% scale. As can be noted, both the limits are well within 1% of the design current limit of 25mA.

For display of output voltage saturation, the amplifier is connected in a unity gain inverter on ±15V supplies, and driven with a –18V to +18V ramp. This overdrives the amplifier at input/output of more than ±13.5V, so the extremes of the input sweep can be used to evaluate output saturation. Both extremes of display are offset by the nominal limiting voltage of ±13.5V, so the error can be shown expanded around zero, with a range of ±1%. Both limits are well less than 1% in terms of error.

Gain and phase response of this particular model is interesting, as it clearly shows the effects of the C1/RXC1/CXC1 and C2/RXC2/CXC2 extensions to frequency response. Shown in Figure 5, test F8, is a composite plot of inverting mode gain/phase operating with ±15V supplies. The load resistance is varied as a parameter, in steps of 100k, 10k, 2k, and 1k. As shown, the gain varies slightly around the nominal 146dB for the various loads, as would be expected for a 70Ω output resistance. The phase response shows a multiple pole/zero characteristic just before unity gain crossover point, as does the real LT1007. While the macromodel display is not as dramatic in terms of phase change as the data sheet, it is still effective for its purpose.

Figure 5, test F5 is a small signal transient test with the LT1007 connected as a follower, emulating a corresponding data sheet photo. The test is a deceptively simple one, as most would think a voltage follower is a fairly straightforward circuit. Actually, it is a real stress test for an op amp macromodel, in terms of potential problems with convergence, memory usage, required simulation time, and so on. This particular simulation runs without any mishap whatsoever, in about 20s on a 16MHz 386 PC clone, using PSpice 4.03, with no tweaking of SPICE defaults. It also runs with no apparent problems , as one of the LTC demo simulations distributed on the SPICE macromodel diskette (using a demo PSpice version 3.06).[5]

These performance tests summarize those aspects of the LT1007 NPN macromodel previously discussed as new design features. It should be kept in mind that many of them can also appear in other models as well, but they will not necessarily be repeated with subsequent examples.

The LTC Bipolar PNP Input Macromodels

With bipolar PNP input stage op amps, a distinct application and functional difference is that they often are designed for single supply operation, often with supplies of 5V or less. In addition, they may also be designed for micropower applications, with current drains of 100μA per amplifier, or even less. LTC has a large number of such amplifiers, with the macromodels supporting them using either of two PNP model topologies.

The LTC PNP macromodels are, in some senses, similar to those using the NPN model topology. While it is true that there are similarities, since both are based on a Boyle model, there are also many practical differences. Speaking of those beyond the obvious polarity differences, the unique distinctions are largely due to functional characteristics of the various amplifiers modeled. And, they are in turn brought about by the single supply and/or micropower operational features previously mentioned. These differences are the thrust of the LTC modeling enhancements.

The LT1013 Family of Macromodels

In terms of historical accuracy, the family of LTC SPICE macromodels for op amps had its beginnings in 1988,

Note 5: The "DEMO1007.CIR" file on the LTC SPICE diskette invites users to try this "simple" transient test with other models, to compare relative performance. It can be revealing for such a seemingly innocent test.

with the release of macromodels for the PNP input op amps LT1013 and LT1014.[6] These models actually had their roots in the MicroSim Parts program, and Listing 3, the macromodel for the LT1013/LT1014, is the version available today. Close akin are derivative models for the LT1013A and the LT1013D. Also related to this model are those of the LT1006 family, including the LT1006, the LT1006A, and the LT1006S8.

The enhancements that these models offer over the original Parts version are three-fold:

- One is the input common mode clamping circuitry (DCM1/DCM2 and VCMC);
- Two is the use of different models for input transistors Q1/Q2 (which allows input bias and offset currents, as well as offset voltage to be simulated);
- Three is the use of a controlled output saturation characteristic when operating near the negative supply rail.

Further discussion and performance examples of this specific model type are found in LTC Design Note 13.

The LT1078/LT1178 Families of Macromodels

More recent examples of LTC bipolar PNP input amplifiers are the two micropower families, the 45µA quiescent current/amplifier LT1078, LT1079, LT1077; and the lower power (15µA quiescent) LT1178 and LT1179. Figure 6 is a dual schematic of the macromodel topology used for these types of PNP op amps. It simulates all those features previously noted, and is discussed below. For the purpose of minimum repetition, only features which differ from models previously discussed are addressed here. Figure 6A is the simple version, while Figure 6B shows all detail, like the actual macromodel listing.

LTC single supply op amps have had a distinction of input phase reversal protection since the introduction of the LT1013/LT1014. This also includes more recent devices such as the LT1078 and LT1178 families. For simulation of this in the macromodel, diodes DCM1 and DCM2 provide

Note 6: Jung, W. G., "An LT1013 Op Amp Macromodel," Linear Technology Design Note # 13, July, 1988.

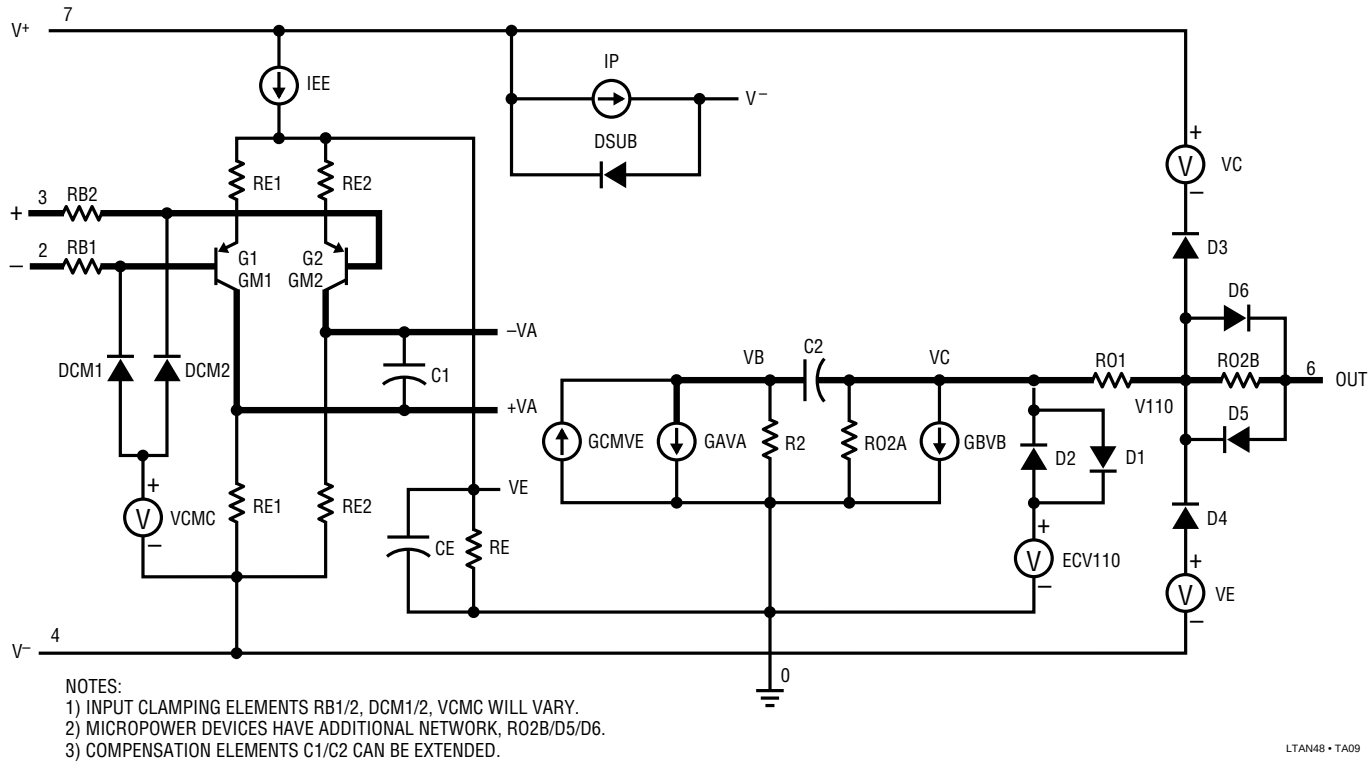


Figure 6A. Bipolar PNP Input Op Amp Macromodel (Simple)

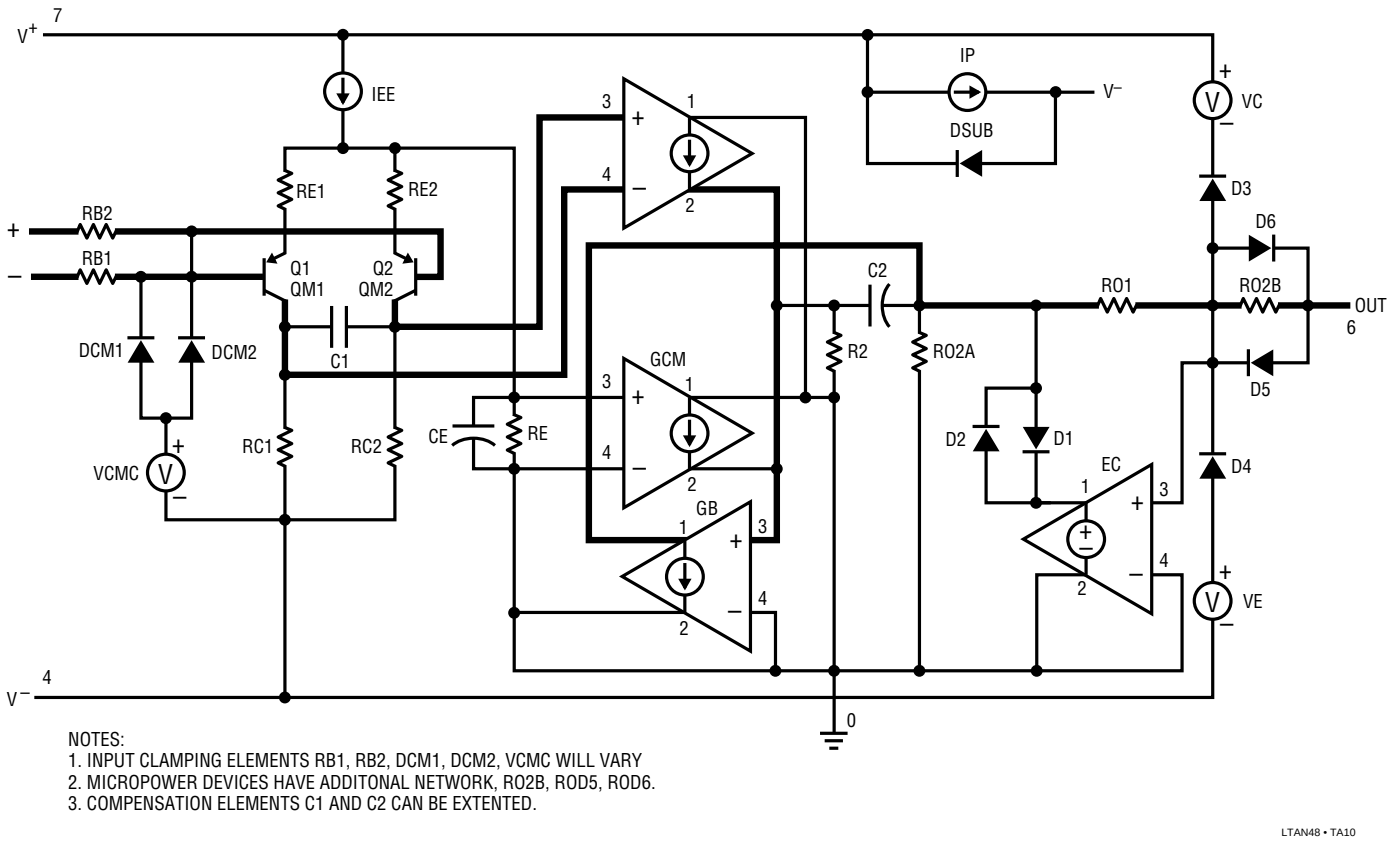


Figure 6B. Bipolar PNP Input Op Amp Macromodel (Detailed)

a negative range input common clamp, for voltages applied to the Q1-Q2 inputs. With the two diodes referenced to a slightly positive common mode clamp voltage, VCMC, they are reverse biased for normal CM voltages. Note that the perspective here is with regard to the negative supply rail, which is also the negative CM limit for single-supply use.

In customizing a macromodel, the inclusion or exclusion of the clamp diodes is an option, as is the RB1/RB2 current limit resistor value, and VCMC. For these single supply devices, VCMC is typically 0.4V, which allows linear common mode response a few hundred mV below ground, just like the actual devices. Without this network, an LT1078 macromodel will (mis)behave just like typical 324/358 amplifiers, with input stage saturation when the inputs are taken below GND. This will be evident by an uncontrolled sign reversal at the output, or hard positive rail saturation.

A key feature added to this model specifically for micropower devices is the extra output network, RO2B and D5/D6. For ordinary dual supply applications, or even single supply uses where close simulation of output voltage saturation is not highly critical, this network isn't needed. However, for single supply op amps such as the LTC PNP input devices which feature active pulldown and linear negative swing operation, simulation to within a few mV of the negative rail is entirely possible. To properly simulate this, a model which displays characteristics similar to the real device when sinking current is needed, which is the function of this network.

LT1078 Macromodel Performance

The LT1078 is a device which illustrates all of the previously mentioned performance points. Its model, shown in Listing 4, can be compared to the schematic of Figure 6 for actual values. The composite pictures of Figure 7 illustrate various performance points.

In terms of CM protection, the model input diode clamp works effectively, as shown by Figure 7, test F3, an overdriven input, +5V single rail follower. Here, the DC input V(2) is swept from –5V to 6V. The displayed output

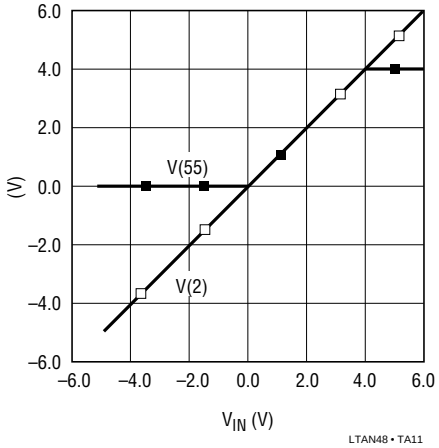


Figure 7A. LT1078 Test F3: +5V Supply, Overdriven Follower

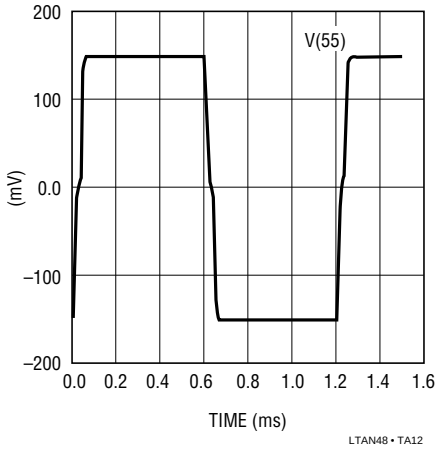


Figure 7B. LT1078 Test F6: I_{SC} (Open Loop, V_S = ±15V)

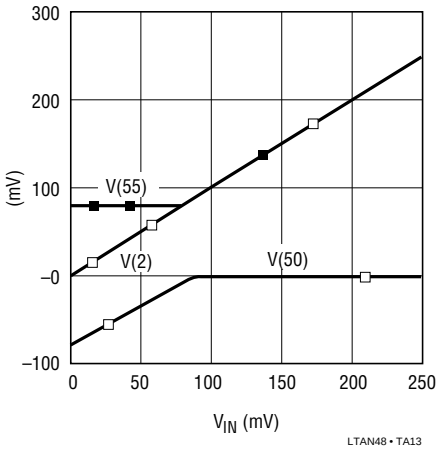


Figure 7C. LT1078 Test F7: Negative Saturation Characteristics

Figure 7. Composite Performance Points

is V(55), and as noted, it is clamped at 0V/4V limits, and there is no phase reversal when the input is taken well below GND (maximum input sink current is 5V/100k).

Figure 7, test F6 shows output voltage V(55) into a 10Ω load, as a test of output current limit. The ± limit levels are 150mV, which corresponds to ±15mA, as is specified for the model. This display also shows the effects of the RO2B/D5/D6 Class B output stage used in the model, as is evident by the multiple slope rise/fall.

For a single supply micropower op amp, one of the more difficult aspects of model performance lies in simulating the supply rail saturation, while retaining the micropower performance and a relatively high maximum current output. For the LT1078 typical supply current is only 45μA, and the output resistance is a few kΩ. Yet, the device can also deliver ±15mA (just demonstrated). For the macromodel, the output Class B network allows concurrent micropower small signal characteristics, as well as this relatively high maximum current. The importance of the small signal characteristics come to play for single supply applications, where the output stage is called upon to sink current at output voltages near GND (or the V– rail).

The finer details of the output current sinking near the negative rail are shown in Figure 7, test F7. This test is for a voltage follower, with a DC input V(2) swept from 0V to 5V. The output stage of the model is required to sink 100μA, when the output voltage V(55) is close to GND. As can be noted, the model is linear with voltages above 100mV. For lower voltages, it saturates at about 80mV while sinking 100μA, as does the real LT1078.

The LTC P-Channel JFET (PFET) Macromodels

Historically speaking, the use of both junction and MOSFET transistor types within a Boyle type macromodel topology was described by Krajewska and Holmes, in an early enhancement to the Boyle model.[7] The Krajewska topology is a modified Boyle type model with either type of FET replacing the bipolars of the original model. This enhancement took advantage of the gain-normalization referred to previously.

Note 7: Krajewska, G., Holmes, F.E., "Macromodeling of FET/Bipolar Operational Amplifiers," IEEE Journal of Solid-State Circuits, Vol. SC-14, # 6, December 1979.

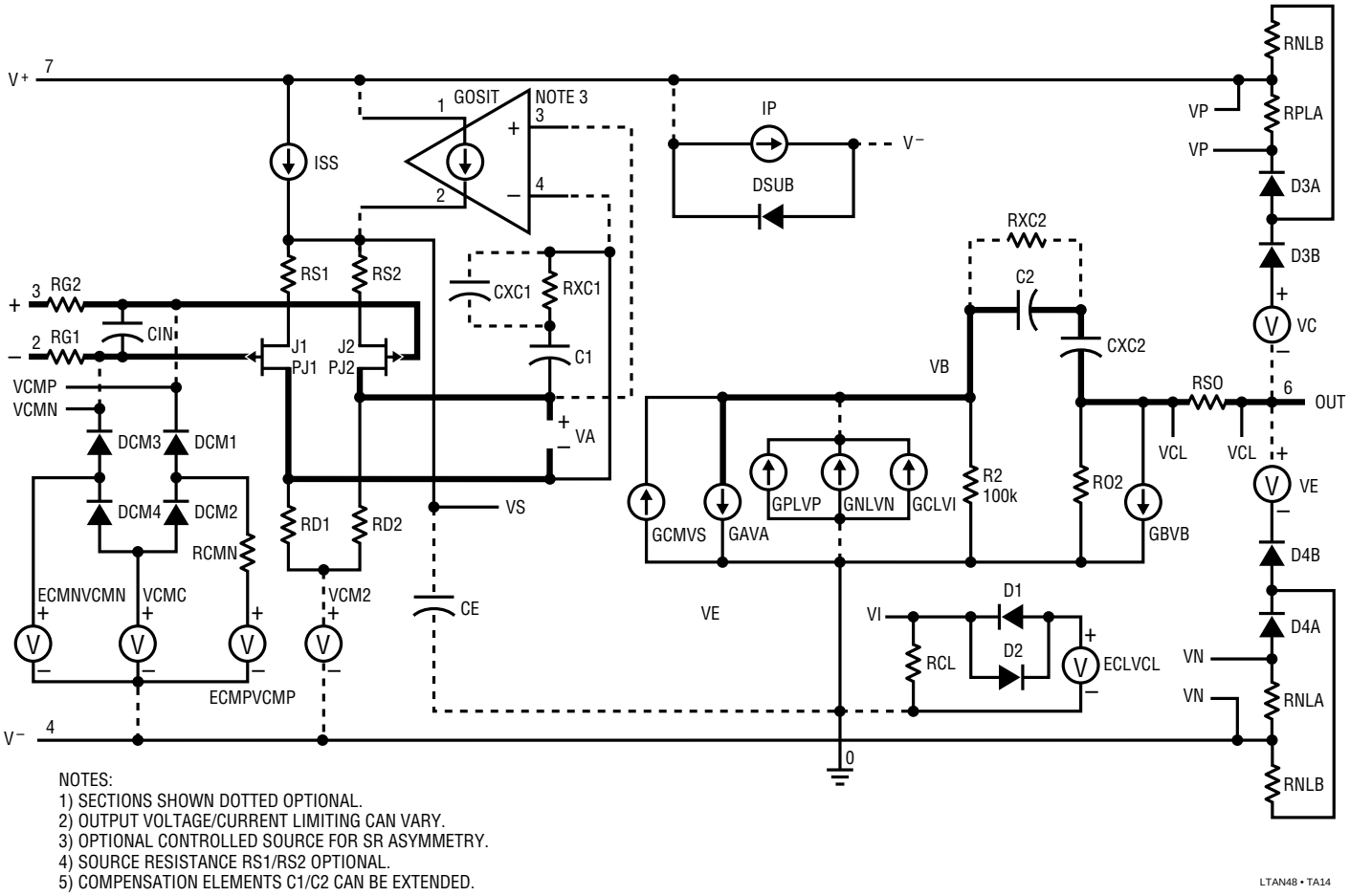
Junction FET input op amps make up an important part of the overall field of op amps, as they are capable of both medium to higher speed performance and have low DC errors. For modeling factors, LTC has chosen to realize a JFET amplifier type, specifically P-channel (PFET) input stage types, with part specific enhancements for the PFET macromodels.

The LTC PFET op amp macromodel is shown in schematic form in Figures 8A and 8B, (simple and detailed respectively). On an overall basis this model is fundamentally similar to that of Krajewska, but it has several adaptations added. It can in fact become one of the more complex models in the LTC library, when all features are used. The following discussions highlight the various enhancements beyond the basic Krajewska form of the Boyle model. Those model improvement areas previously discussed will not be covered in detail. The actual macromodel of an LT1056 (a representative LTC PFET op amp) is shown in Listing 5.

PFET Macromodel Features

At the input side of the PFET macromodel is the J1/J2 front end, which has a number of options possible within this stage. Input capacitance is simulated by C_{IN}, and series gate resistances RG1/RG2 are optionally added.

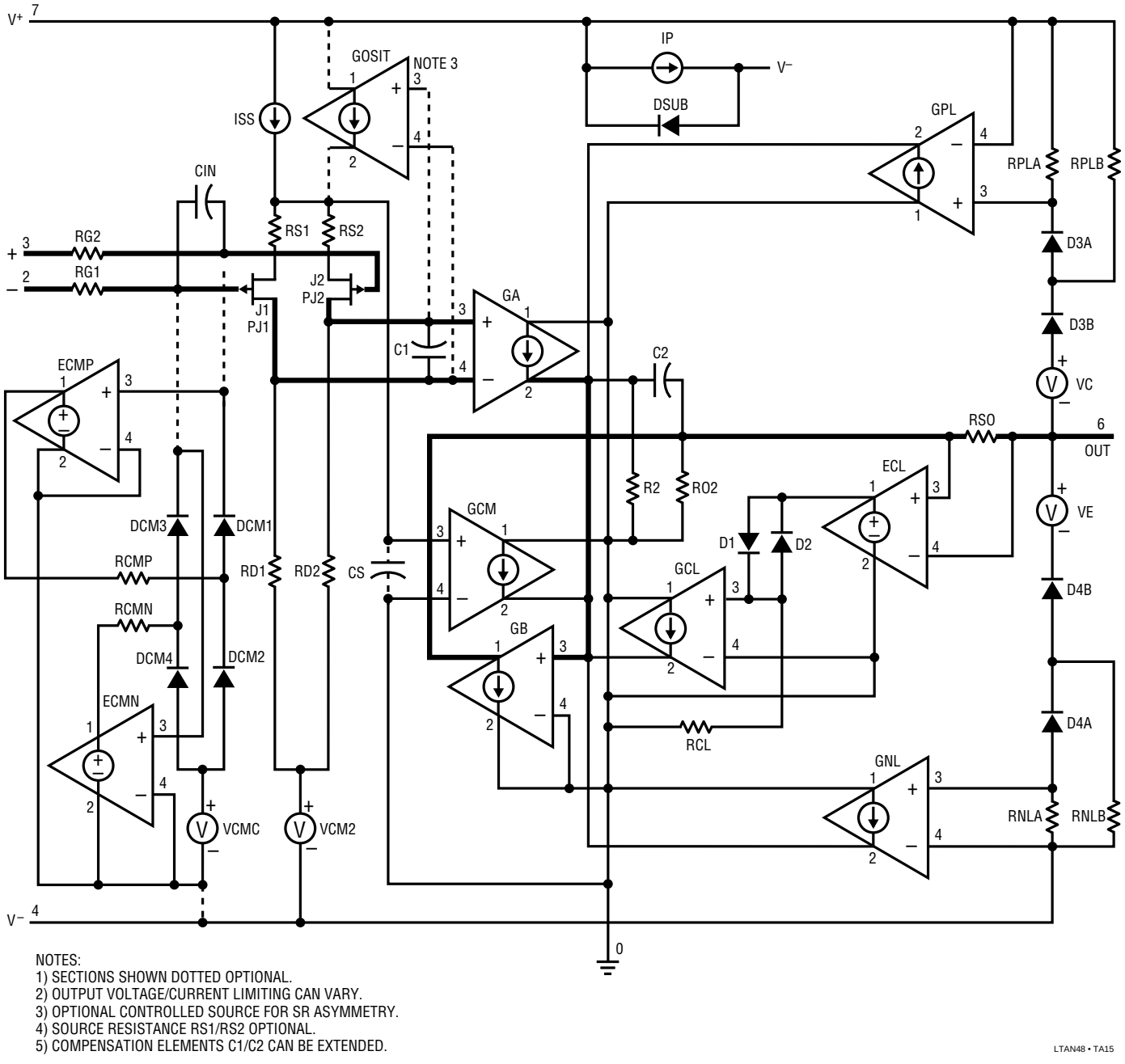
The optional buffered clamping network around DCM1-DCM4 is quite complex, and warrants some discussion. This circuit simulates the anti-phase reversal common mode clamping present in most (but not all) LTC PFET input amplifiers. In the actual parts which use it, this clamp becomes active whenever the input voltage approaches within 4V (or less) of the negative supply rail. This prevents the sign inversion typically seen in most PFET input op amps, when the negative CM range is exceeded.



NOTES:
1) SECTIONS SHOWN DOTTED OPTIONAL.
2) OUTPUT VOLTAGE/CURRENT LIMITING CAN VARY.
3) OPTIONAL CONTROLLED SOURCE FOR SR ASYMMETRY.
4) SOURCE RESISTANCE RS1/RS2 OPTIONAL.
5) COMPENSATION ELEMENTS C1/C2 CAN BE EXTENDED.

LTAN48 • TA14

Figure 8A. P-Channel JFET Op Amp Macromodel (Simple)



NOTES:
1) SECTIONS SHOWN DOTTED OPTIONAL.
2) OUTPUT VOLTAGE/CURRENT LIMITING CAN VARY.
3) OPTIONAL CONTROLLED SOURCE FOR SR ASYMMETRY.
4) SOURCE RESISTANCE RS1/RS2 OPTIONAL.
5) COMPENSATION ELEMENTS C1/C2 CAN BE EXTENDED.

LTAN48 • TA15

Figure 8B. P-Channel JFET Op Amp Macromodel (Detailed)

The circuit appears moderately complex, but is so out of necessity. For high performance in this macromodel, clamping diodes DCM1 and DCM3 are bootstrapped, for lowest leakage. VCVS followers ECMP and ECMN, through resistances RCMP and RCMN, reduce the voltage seen by these two diodes to a zero potential for inputs where the clamp is *not* active. This is necessary to preserve the low pA bias currents of J1/J2, for normal operating range CM voltages (when the clamp is back biased). In other words, the clamp must clamp effectively below its voltage threshold, yet it must not introduce leakage errors which would ruin the bias current characteristics seen at the op amp input(s). Actually the bootstrapping is quite effective, with DCM1 and DCM3 introducing a pA or less of error.

As noted, this circuit is an option with all LTC PFET input amplifiers which employ a 356 type topology, which includes the LT1056, LT1057, LT1058, LT1022, and older

industry standard parts such as the LF156-LF356 series, the OP-15/OP-16 series, and the related duals. Since the clamp circuit is only needed for simulations which need to explore overvoltage CM inputs, it comes commented out within the respective model files.

P-channel JFETs J1/J2 have individual model characteristics calculated to yield an input stage unity gain, gate currents consistent with the I_B/I_{OS} of the amplifier modeled, and the V_{OS} characteristics of the op amp. All of these are as defined by models JM1 and JM2, respectively. For the gain-normalization of the input stage, the JFET transconductance parameter BETA is adjusted for J1/J2, to provide unity gain. Alternatively, source resistances RS1/ RS2 can be used for gain normalization. This option is one that can be exercised at the time the model is created (in the interest of simplicity however, no present models use these resistances). V_{OS} is modeled simply as the difference in the V_{TO} for the two models.

A subtle detail which may not be obvious is the (optional) use of voltage source VCM2, which appears within the LT1056 model (and similar topologies). This bias voltage simulates negative input range change of V_{OS}, characteristic of these amplifiers.

In the inner stages of the model, overall gain and frequency response capability characteristics are similar to the NPN prototype discussed previously, and extensions to both C1 and C2 can optionally be used. These extensions are not used with the LT1056.

As noted in the discussion of gain-normalization, the basic equations which govern this model are quite close to the original Boyle expressions, with the adaptations for different circuit references. These are summarized in Figure 2. The SR of the Figure 8 model is set by the tail current of J1/ J2 and C2 for the most simple JFET amplifier cases. However, many P-channel JFET op amps are *not* just simple cases, in the sense that they don't slew symmetrically. For asymmetric slewing JFET amplifiers, the optional circuitry used is described in detail in the Appendix, and it employs the VCCS GOSIT, connected as shown. JFET amplifiers which have symmetric SR characteristics use a more straightforward signal path, where the SR is simply ISS/C2.

The remainder of this model (the output stage with enhanced voltage/current limiters) is similar to the NPN macromodel.

PFET Macromodel Performance

The performance of the LT1056 device, illustrated in the composite pictures of Figure 9, shows many of the key behavior points of this model type.

One of the rather unique aspects of the 355/356 and other family relation PFET op amps is the asymmetrical slewing. With the LT1056, this pattern of behavior is shown in Figure 9, test F1. This test, for a voltage follower on ±15V supplies, slews twice as fast for negative going swings as for positive. The measured rates are +14V/µs, –28V/µs, and the SPICE result here compares well with the data sheet. This transient test runs in around 25s, with minor PSpice power supply ramping to find a bias point.[8] (A .IC command for node 55 minimized the bias iterations, but was not essential).

The demonstration of the voltage clamping circuit and its effect on input currents is shown in Figure 9, test F3. In this test the LT1056 is overdriven as a voltage follower, with a DC sweep input of –15V to +15V. The three part display shows input/output linearity (left), amplifier bias current (middle), and clamping current in the circuit's 10k input resistor (right). For this specific test, the LT1056 model was edited to uncomment the "CMCLAMP" section and activate the limiter.

In the left plot of Figure 9, test F3, the LT1056 shows only low errors due to gain and CM, until the limits are reached. Note that the positive limit is due to the LT1056 output swing limit at positive 13.2V (the negative output limit is –13.2). However, the negative range limit of this follower is due to the *input clamp*, and occurs nearly 2V sooner, just under –11V. This is the clamp threshold of 4V (relative to –15V). In the middle plot, the bias current of J1 is stable

Note 8: The PSpice simulator used in these tests has an internal bias point seek algorithm to aid in convergence. This routine lowers/raises the supplies to find a suitable biasing condition for the circuit. The necessity for this will vary circuit by circuit, but in general amplifier circuits with initial input conditions which start at some extreme (such as –10V, in this case) can be slower in biasing. A ".IC" command can be used to minimize this, if desired.

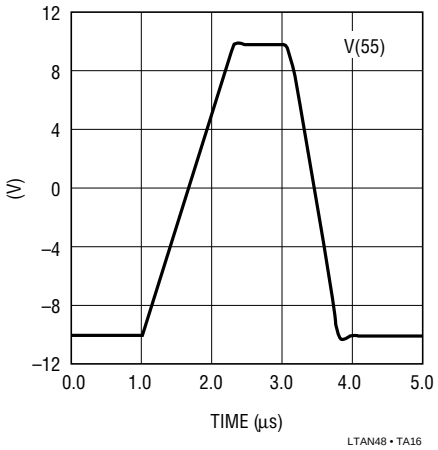


Figure 9A. LT1056 Test F1: Asymmetric Slew Rate

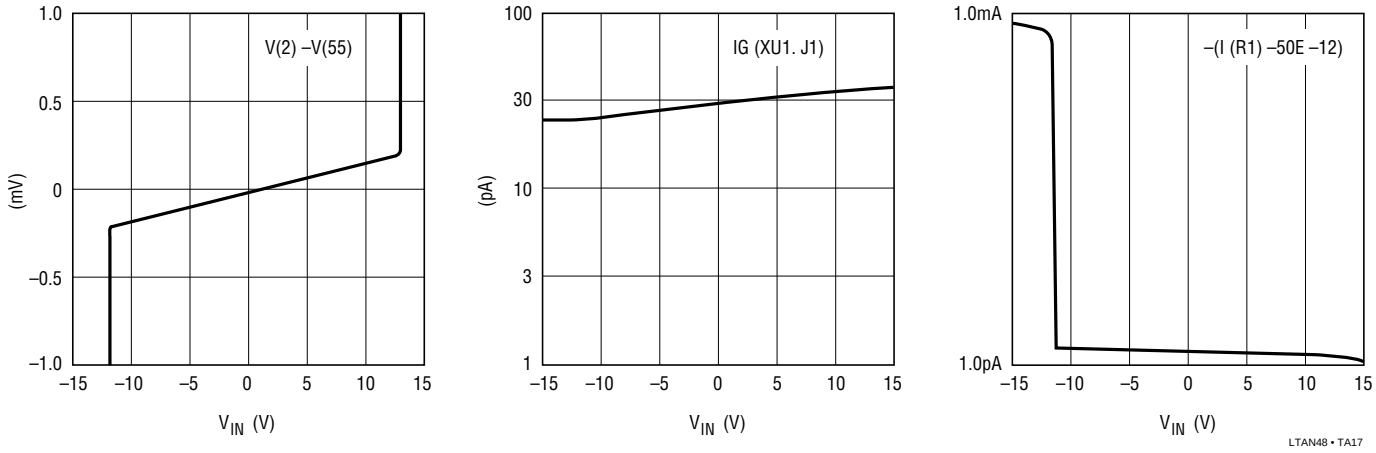


Figure 9B. LT1056 Test F3: Input Clamp, ±15V, Overdriven Follower

Figure 9. Composite Performance Points

over this range, indicating that the overall follower loop is active. In the right plot, the current in the 10k input resistor is displayed for the entire input dynamic range. It is only a few pA within the range where the amplifier is operating linearly, but then rises rapidly to about 400µA, as the clamp takes over.

The LTC P-Type MOSFET (PMOS) Macromodel Family

The LTC PMOS input op amp macromodel is shown in schematic form in Figures 10A and 10B, and a representative model for the LTC1050 is shown in Listing 6. Like the close-cousin PFET amplifier model of Figure 8, this PMOS model resembles the corresponding model of Krajewska,[9] with regards to some aspects of the input stage.

What has been said for the model of Figure 8 is generally true when PMOS transistors are used (M1/M2 in Figure 10 replace J1/J2 of Figure 8). With this PMOS FET adaptation, diodes DG1 and DG2 simulate the bias currents of the device (as opposed to the fixed current sources of the Krajewska model). As was true for the JFET transistor models, the model parameters of these diodes provide for I_B/I_{OS} characteristics. As previously, CIN simulates amplifier input capacitance.

In this PMOS input macromodel much of the remainder of the overall model is similar, and little changes in the

Note 9: Krajewska, G., Holmes, F.E., "Macromodeling of FET/Bipolar Operational Amplifiers," IEEE Journal of Solid-State Circuits, Vol. SC-14, # 6, December 1979.

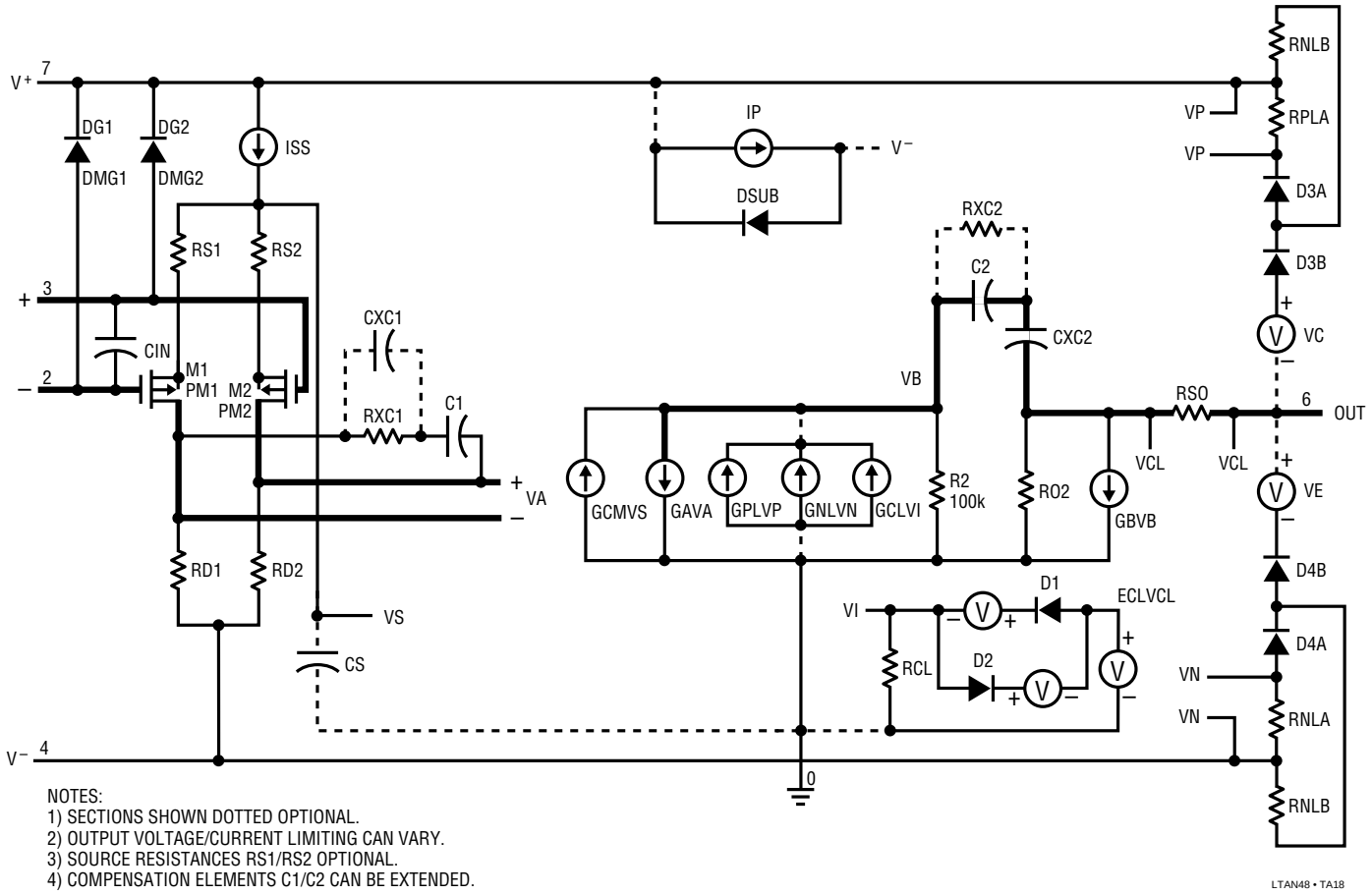


Figure 10A. PMOS FET Op Amp Macromodel (Simple)

equations (refer to Figure 2 again). Practically speaking, the variation of a PMOS input stage model allows such useful device categories as the low I_B and very low V_{OS} chopper-stabilized units.[10] Accurate rail-rail output limit characteristics also allow features of single supply CMOS technologies to be realistically modeled.

PMOS Macromodel Features

One area where the emphasis on fidelity to the actual devices influences a model is found in this PMOS macromodel. While it is in fact more complex, it is so for the reason of better match to the real parts. But, IC vendors haven't all taken such steps in modeling op amps with PMOS inputs and CMOS outputs. For example, inspection of some models released show such obvious deficiencies as input transistors unlike what is in the part actually modeled, and/or a lack of close attention to output limiting levels. Obviously, such models can't simulate input or output CM ranges with a high degree of fidelity, even though these factors can be critical to single supply use.

The output current/voltage limiters used with the LTC PMOS model are of the more complex form shown because of several important performance issues. For example, amplifiers emulated by these PMOS models have rail-rail outputs, with mV level saturation voltages typical of CMOS outputs. The amplifiers also have the 160dB gains, 140dB CMRRs, and sub-microvolt V_{OS} levels, as is typical of chopper stabilized amps. Many of these performance characteristics are made possible by some model

Note 10: These models emulate actual LTC chopper amplifiers in terms of the ultra low offset, the high gain, and also in terms of single (low voltage) supply operation, input/output ranges, etc. However, there is no actual commutation function, and therefore the effects of clocking parasitics of the actual device aren't modeled.

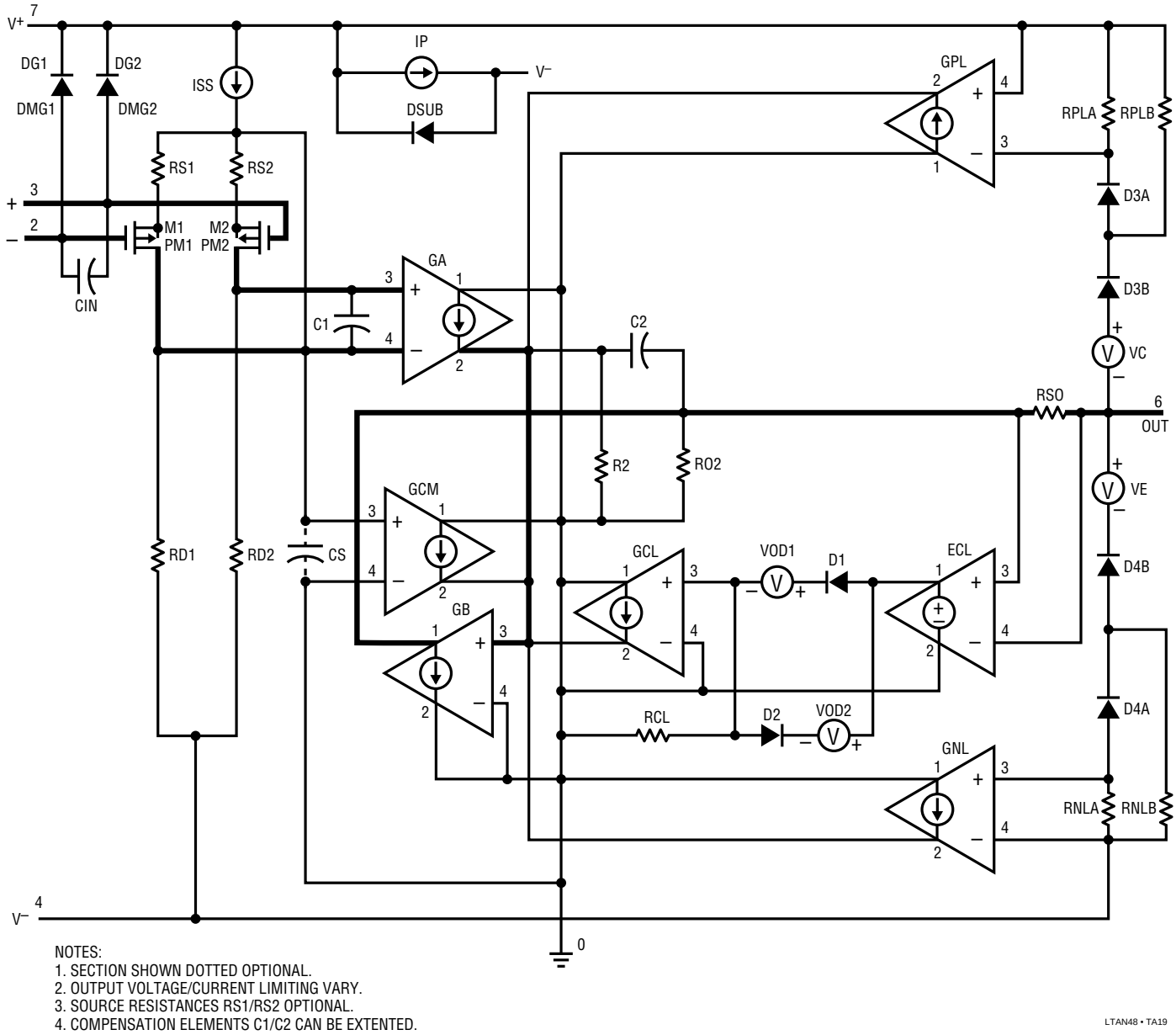


Figure 10B. PMOS FET Op Amp Macromodel (Detailed)

features shown in Figure 10, such as the already discussed improved voltage limiters, for very low saturation voltages with minimal gain error.

The current limiting in this model also has some unique performance issues. Most current limit schemes used within op amp macromodels are symmetrical regarding sinking/sourcing output current, as previously described for the NPN macromodel limiter. For the most part this is not a problem, since most op amps also have symmetric limits.

However, some amplifier types do not limit symmetrically at all, and may have a skew of 3-5 times between the sinking/sourcing current levels. A case in point are those amplifiers which have CMOS common drain outputs, where the upper P device can source less current than the lower N device can sink. For example the LTC1050 under discussion can source 5mA of current, while it can sink 20mA.

The LTC improved modeling method for current limiting allows different degrees of asymmetry to be incorporated.

In the circuits of Figure 10 the output current is sampled by a low value series resistor, RSO, typically 1Ω. The current proportional voltage drop across RSO is scaled by VCVS ECL, which of course eliminates any possible loading effects on the output. As noted with the NPN model, this technique was in fact developed to remove loading effects of brute-force limiting, which can cause gain errors in a very high gain amplifier such as the LTC1050. While any op amp being modeled with gain of more than 120dB can be subject to limiter-related loading errors, in chopper-type amplifiers where gains are typically 160dB or more, it can become critical.

Along with the value of RSO, the gain of ECL plus the diodes D1/D2 and voltage sources VOD1/VOD2 are selected to provide separate ±current limit thresholds. The gain of ECL is common for both current limits, and the two voltage sources are adjusted to reflect the desired threshold for sinking/sourcing of current. In the LTC1050 model, the source and sink currents are 5mA and 20mA, respectively. Should there be a model case of equal currents, then the diodes are the same and the voltage sources are dropped.

PMOS Macromodel Performance

The performance of the LTC1050 op amp is illustrated in the composite pictures of Figure 11.

A test which demonstrates the rail-rail response characteristics is shown in Figure 11, test F7. The conditions of this test are a unity gain inverter with a single supply of +5V, driven with an input DC sweep of –6V to +1V. This deliberately overdrives the amplifier at both dynamic range extremes. The two plots show the input/output error highly magnified, a relatively sensitive test of saturation near the ± rails. The upper trace shows the general behavior, while the bottom trace shows the error on a ±10mV scale. Even on the expanded scale the input/output error is hard to see, but it is about 12mV with the output at 100mV from either rail, 500µV at 200mV, 12µV at 300mV, and essentially at the V_{OS} level for lower voltages.

As noted previously, a unique feature of the PMOS macromodel type is the ability to have different ±output current limits. With the LTC1050 model tested, this asymmetrical limiting is shown in Figure 11, test F6. For this test the conditions are an open loop comparator with ±5V

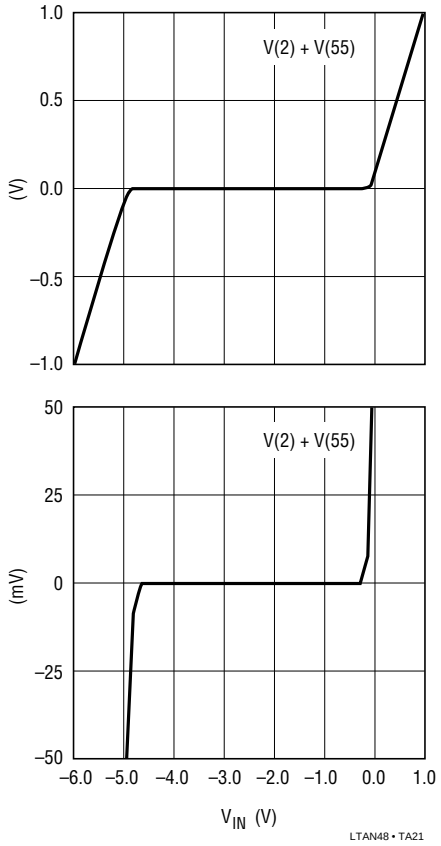


Figure 11A. LTC1050 Test F7: Input/Output Linearity, SS (–) Mode

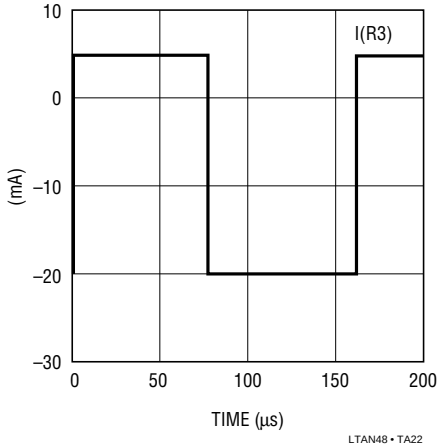


Figure 11B. LTC1050 Test F6: I_{SC} (V_S = ±5V)

Figure 11. Composite Performance Points

supplies and a 10Ω load. As can be noted, the current in load resistor R3 is +5mA/–20mA.

Examples of LTC op amps using this PMOS model are the LTC1050 series, and related parts in the chopper stabilized family.

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SPICE documents available from: EECS/ERL Industrial Support Office, 497 Cory Hall, University of California at Berkeley, Berkeley, CA 94720

APPENDIX

Improved JFET Op Amp Model Slews Asymmetrically

SPICE macromodels for op amps have been available for some time, for both bipolar[1, 2] and JFET[3] input stage device types. Interestingly however, not much attention has been given in the models available to controlled slewing asymmetry. Dependent upon a given amplifier design topology, the large signal characteristics can have various degrees of slew rate (SR) asymmetry. It therefore makes good sense to have models which emulate real IC parts in this regard.

A case in point is that of the available P-channel JFET input op amps, many which have a characteristic SR response which is asymmetrical. In fact, popular op amps with topologies like the original 355/356 types are intrinsically faster for negative going output swings than they are for positive. Similar comments apply to such related devices as the OP-15, OP-16, etc. Since this type of JFET device topology was introduced, the SR specified on the data sheet has typically been the *lower* of two dissimilar rates, i.e., the slower, *positive* edge SR. Thus, given an op amp with a typical SR spec of 14V/μs for positive going edges, the same amp will have a corresponding negative SR of about 28V/μs.

Ironically, this quite common JFET amplifier slewing characteristic has not been well modeled thus far. Most macromodels currently available simply do not address the asymmetric SR issue at all. Others have means of modeling it, but it is seldom found used.

A means of SR control was built into the original Boyle[1] model, and it addresses SR asymmetry for common mode

(CM) signals by means of a common emitter (source) capacitor, CE (CS, for JFET amps). However, using this capacitor alone for a general SR symmetry control mechanism leaves something to be desired, as the resulting slopes are not consistent. LTC has implemented a new means of modeling SR asymmetry, shown in Figure A1.

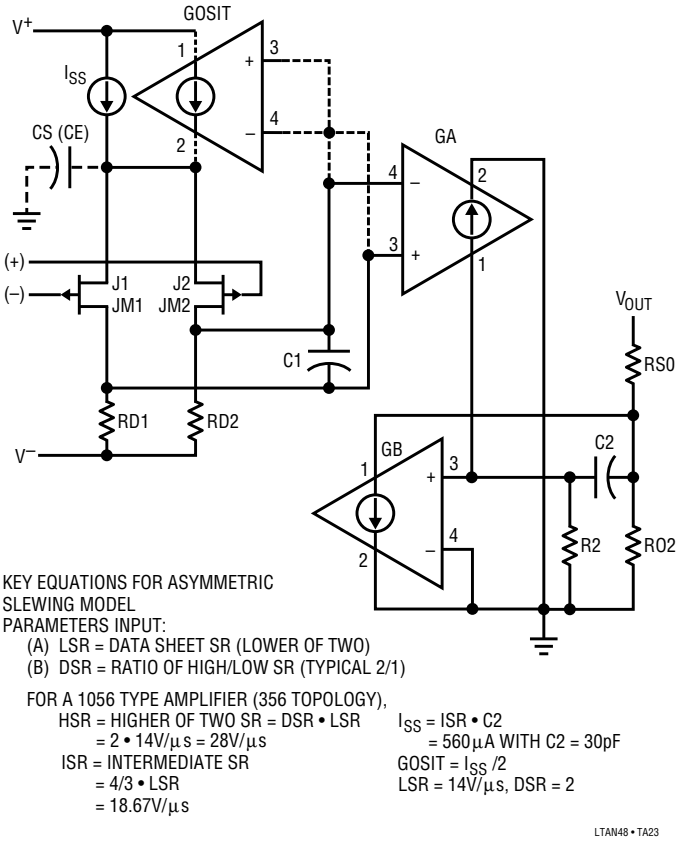

Figure A1. The LTC Asymmetric Slewing JFET Macromodel Has Little Additional Complexity, But Offers Controlled Slewing Response

The circuit as shown here is a simplified Boyle type model with P-channel JFET input devices, J1 and J2. As this type (or similar input structure) of model is typically used, the SR is simply ISS/C2, which is symmetrical when CS is zero. When the common source capacitor CS is added, the SR for CM signals can be adapted (corresponds to CE in the Boyle paper). Unfortunately, this strategy works best for CM amplifier inputs, and not as well for inverting inputs.

The LTC method of modeling asymmetrical SR employs an added VCCS (shown dotted), which dynamically modifies the total tail current available to J1/J2. This controlled source, "GOSIT," is driven by the differential output of J1/J2 and produces a current which adds/subtracts to/from the fixed current, ISS. The resulting current available to charge/discharge compensation capacitor C2 is thus higher for one slewing slope than it is for the opposite. This is true regardless of whether the amplifier is operating in an inverting or non-inverting input mode. As an option, CS can still be used for further control of slewing for CM inputs (shown dotted).

In generating a new macromodel with asymmetrical SR, the *lower* of the two slew rates is input from the data sheet. Also input is the *ratio* of the high-to-low SR. Algorithms in the program used by LTC then calculate an appropriate static value or ISS and the gain of VCCS GOSIT, so that the proper slewing characteristic will be produced by the model.

A representative example op amp with these characteristics is the LT1056, a high performance op amp topologically much like the LF156-LF356 and OP-16 types (also produced by LTC, with corresponding macromodels available). Some sample lines of code taken directly from the released LT1056 model are shown below. These are shown for both the asymmetric form as released, and for an (edited) symmetric case.

Actually, only one SPICE model element is added to produce the asymmetric SR as opposed to symmetric, and that is the VCCS, GOSIT. The LT1056 example just below, taken from the released library, produces SRs of +14V/µs and –28V/µs, respectively.

```
** END CM CLAMP
C1 80 90 1.5000E-11
ISS 7 12 5.6000E-04
GOSIT 7 12 90 80 2.8000E-04
* INTERMEDIATE
```

When the controlled source GOSIT is omitted, the model reverts to simple symmetric slewing, where the SR will be ±(ISS)/C2. This is shown below, with ISS adjusted for a (symmetric) SR of 14V/µs. Those lines of code edited are shown below in **bold**.

```
** END CM CLAMP
C1  80 90 1.5000E-11
* for a (symmetric) SR of 14V/µs,
```

*** ISS = (1.4e7)*(3e –11) = 420μA**
ISS 7 12 4.2000E-04
*** comment out GOSIT with first column "*"**
*** GOSIT 7 12 90 80 2.8000E-04**
* INTERMEDIATE

*** Also, if a similar GBP is desired, adjust the**
*** BETA (only) parameter of models JM1/JM2**
*** BETA should be adjusted by the**
*** inverse proportion of the ISS change, or,**
*** in this case 1/(420/560) = 560/420 = 1.33 times,**
*** as:**
.MODEL JM1 PJF (IS = 1.1000E –11
+ BETA = 1.267E-03 VTO = –1.000000E +00)

Note again that this adjustment to BETA applies to *both* JM1 and JM2, and that *no other* inline .MODEL parameters should be changed. (There is no harm if BETA is not changed, except for a low GBP).

The non-inverting mode waveforms of a typical SPICE run using the LT1056 macromodel and parallel lab results with an actual LT1056 device are shown in Figure 2.

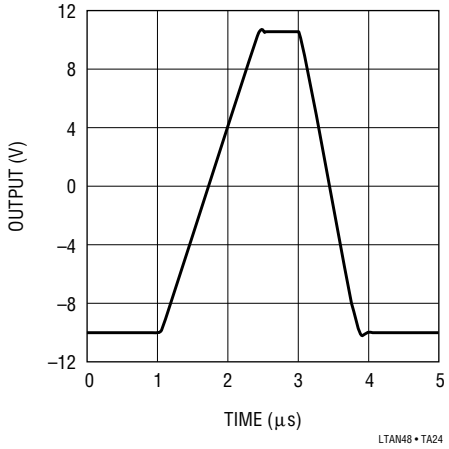

Figure 2A. LT1056 SR (+) Mode, Macromodel

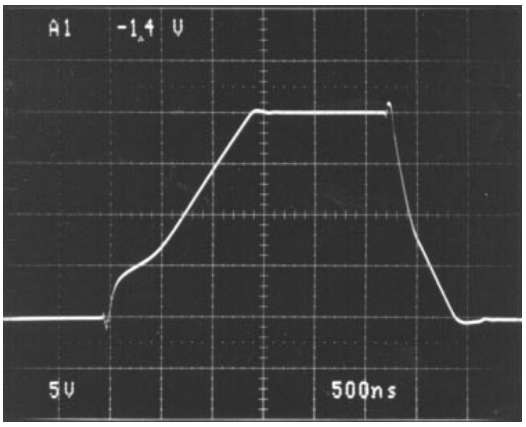

Figure 2B. LT1056 SR (+) Mode, Lab Photo

Listing 1

```
*
* Linear Technology 8741 op amp model
* Written: 10-29-1990 12:55:37 Type: Bipolar NPN input, internal comp.
* Typical specs:
* Vos=3.0E-04, Ib=2.6E-07, Ios=7.0E-10, GBP=1.2E+06Hz, Phase mar.= 73.2
deg,
* SR(-)=9.0E-01V/us, SR(+)=7.2E-01V/us, Av=112.4dB, CMRR=106.0dB,
* Vsat(+)=0.800V, Vsat(-)=2.300V, Isc=+26/-26mA, Rout= 566ohms,
Iq=1.98mA.
* (As per Boyle Appendix)
*
* Connections: + - V+V-O
.SUBCKT 8741 3 2 7 4 6
* INPUT
RC1 7 80 4.3521E+03
RC2 7 90 4.3521E+03
Q1 80 2 10 QM1
Q2 90 3 11 QM2
CIN 2 3 2.0000E-12
C1 80 90 4.5288E-12
RE1 10 12 +2.3917E+03
RE2 11 12 +2.3917E+03
IEE 12 4 2.7512E-05
RE 12 0 7.2696E+06
CE 12 0 7.5000E-12
* INTERMEDIATE
GCM 0 8 12 0 1.1516E-09
GA 8 0 80 90 2.2978E-04
R2 8 0 1.0000E+05
C2 1 8 3.0000E-11
GB 1 0 8 0 3.2110E+01
RO2 1 0 5.6500E+02
* OUTPUT
RSO 1 6 1.0000E+00
ECL 18 0 1 6 3.2808E+01
GCL 0 8 20 0 1.0000E+00
RCL 20 0 1.0000E+01
D1 18 19 DM1
VOD1 19 20 0.0000E+00
D2 20 21 DM1
VOD2 21 18 0.0000E+00
*
D3A 131 70 DM3
D3B 13 131 DM3
GPL 0 8 70 7 1.0000E+00
VC 13 6 2.1831E+00
RPLA 7 70 1.0000E+01
RPLB 7 131 1.0000E+03
D4A 60 141 DM3
D4B 141 14 DM3
GNL 0 8 60 4 1.0000E+00
VE 6 14 3.6831E+00
RNLA 60 4 1.0000E+01
RNLB 141 4 1.0000E+03
*
IP 7 4 1.9525E-03
DSUB 4 7 DM2
* MODELS
.MODEL QM1 NPN (IS=8.0000E-16 BF=5.2662E+01)
.MODEL QM2 NPN (IS=8.0928E-16 BF=5.2807E+01)
.MODEL DM1 D (IS=1.0000E-20)
.MODEL DM2 D (IS=8.0000E-16 BV=4.8000E+01)
.MODEL DM3 D (IS=1.0000E-16)
.ENDS 8741
*
* - - - - - * FINI 8741 * - - - - - * [OAMM VN02 10/29/90]
```

Listing 2

```
.SUBCKT LT1007 3 2 7 4 6
RC1 7 80 6.6315E+02
RC2 7 90 6.6315E+02
Q1 80 2 10 QM1
Q2 90 3 11 QM2
*
C1 80 91 200E-12
RXC1 91 90 50
CXC1 91 90 500E-12
C2 8 98 4.000E-12
RXC2 8 98 4.00K
CXC2 1 98 27.000E-12
*
CIN 3 2 5E-12
DDM1 2 104 DM2
DDM3 104 3 DM2
DDM2 3 105 DM2
DDM4 105 2 DM2
RE1 10 12 -2.6233E+01
RE2 11 12 -2.6233E+01
IEE 12 4 7.5030E-05
RE 12 0 2.666E+06
CE 12 0 1.579E-12
GCM 0 8 12 0 7.558E-10
GA 8 0 80 90 1.5080E-03
R2 8 0 1.000E+05
GB 1 0 8 0 1.9176E+03
RO2 1 0 6.900E+01
*
RS 1 6 1
ECL 18 0 1 6 2.828E+01
GCL 0 8 20 0 1
RCL 20 0 1E3
D1 18 20 DM1
D2 20 18 DM1
*
D3A 131 70 DM3
D3B 13 131 DM3
GPL 0 8 70 7 1
VC 13 6 3.0909
```

```
RPLA 7 70 1E4
RPLB 7 131 1E5
D4A 60 141 DM3
D4B 141 14 DM3
GNL 0 8 60 4 1
VE 6 14 3.0909
RNLA 60 4 1E4
RNLB 141 4 1E5
*
IP 7 4 2.625E-03
DSUB 4 7 DM2
* MODELS
.MODEL QM1 NPN (IS=8.0000E-16 BF=1.7857E+03)
.MODEL QM2 NPN (IS=8.0062E-16 BF=4.1667E+03)
.MODEL DM1 D (IS=1.000E-19)
.MODEL DM2 D (IS=8.000E-16)
.MODEL DM3 D (IS=1.000E-20)
.ENDS LT1007
*
.SUBCKT LT1007CS 3 2 7 4 6
X_LT1007CS 3 2 7 4 6 LT1007
.ENDS LT1007CS
* - - - - - * FINI LT1007 FAMILY * - - - - - *
```

Listing 3

```
.SUBCKT LT1013 1 2 3 4 5
*
C1 11 12 8.661E-12
C2 6 7 30.00E-12
DC 8 53 DX
DE 54 8 DX
DLP 90 91 DX
DLN 92 90 DX
DP 4 3 DX
EGND 99 0 POLY(2) (3,0) (4,0) 0 .5 .5
FB 7 99 POLY(5) VB VC VE VLP VLN 0 2.475E9 -2E9 2E9 2E9 -2E9
GA 6 0 11 12 113.1E-6
GCM 0 6 10 99 225.7E-12
IEE 3 10 DC 12.03E-6
HLIM 90 0 VLIM 1K
Q1 11 102 13 QM1
Q2 12 101 14 QM2
RB1 2 102 400
RB2 1 101 400
DCM1 105 102 DX
DCM2 105 101 DX
VCMC 105 4 DC 0.4
R2 6 9 100.0E3
RC1 4 11 8.841E3
RC2 4 12 8.841E3
RE1 13 10 4.519E3
RE2 14 10 4.519E3
REE 10 99 16.63E6
RO1 8 5 80
RO2 7 99 25
IP 3 4 328E-6
VB 9 0 DC 0
VC 3 53 DC 1.610
VE 54 4 DC .61
VLIM 7 8 DC 0
VLP 91 0 DC 25
VLN 0 92 DC 25
.MODEL DX D(IS=800.0E-18)
.MODEL QM1 PNP (IS=8.000E-16 BF=3.974E+02)
.MODEL QM2 PNP (IS=8.019E-16 BF=4.027E+02)
.ENDS
```

Listing 4

```
.SUBCKT LT1078 3 2 7 4 6
* INPUT
RC1 4 80 2.653E+04
RC2 4 90 2.653E+04
Q1 80 102 10 QM1
Q2 90 103 11 QM2
RB1 2 102 6.000E+02
RB2 3 103 6.000E+02
DCM1 105 102 DM2
DCM2 105 103 DM2
VCMC 105 4 4.000E-01
C1 80 90 8.660E-12
RE1 10 12 4.958E+03
RE2 11 12 4.958E+03
IEE 7 12 2.412E-06
RE 12 0 8.292E+07
CE 12 0 1.579E-12
* INTERMEDIATE
GCM 0 8 12 0 1.501E-10
GA 8 0 80 90 3.770E-05
R2 8 0 1.000E+05
C2 1 8 3.000E-11
GB 1 0 8 0 2.449E+02
* OUTPUT
RO1 1 110 1.000E+02
RO2A 1 0 1.083E+03
RO2B 6 110 8.170E+02
EC 17 0 110 0 1
D1 1 17 DM1
D2 17 1 DM1
D3 110 13 DM2
D4 14 110 DM2
D5 6 110 DM2
D6 110 6 DM2
VC 7 13 1.490E+00
VE 14 4 7.911E-01
IP 7 4 4.259E-05
DSUB 4 7 DM2
* MODELS
.MODEL QM1 PNP (IS=8.000E-16 BF=1.992E+02)
```

```
.MODEL QM2 PNP (IS=8.012E-16 BF=2.008E+02)
.MODEL DM1 D (IS=3.718E-24)
.MODEL DM2 D (IS=8.000E-16)
.ENDS LT1078
*
.SUBCKT LT1079 3 2 7 4 6
X_LT1079 3 2 7 4 6 LT1078
.ENDS LT1079
*
.SUBCKT LT1077 3 2 7 4 6
X_LT1077 3 2 7 4 6 LT1078
.ENDS LT1077
*
* - - - - - * FINI LT1078 FAMILY * - - - - - * [OAMM VP02 5/11/90]
```

Listing 5

```
.SUBCKT LT1056 3 2 7 4 6
* INPUT
VCM2 40 4 2.0000E+00
RD1 40 80 9.6458E+02
RD2 40 90 9.6458E+02
J1 80 102 12 JM1
J2 90 103 12 JM2
CIN 2 3 4.0000E-12
RG1 2 102 2.0000E+00
RG2 3 103 2.0000E+00
** CM CLAMP
* DCM1 107 103 DM4
* DCM2 105 107 DM4
* VCMC 105 4 4.0E+00
* ECMP 106 4 103 4 1
* RCMP 107 106 1E+04
* DCM3 109 102 DM4
* DCM4 105 109 DM4
* ECMN 108 4 102 4 1
* RCMN 109 108 1E+04
** END CM CLAMP
C1 80 90 1.5000E-11
ISS 7 12 5.6000E-04
GOSIT 7 12 90 80 2.8000E-04
* INTERMEDIATE
GCM 0 8 12 0 1.3052E-08
GA 8 0 80 90 1.0367E-03
R2 8 0 1.0000E+05
C2 1 8 3.0000E-11
GB 1 0 8 0 7.8368E+01
RO2 1 0 4.9000E+01
* OUTPUT
RSO 1 6 1.0000E+00
ECL 18 0 1 6 1.7377E+01
GCL 0 8 20 0 1.0000E+00
RCL 20 0 1.0000E+03
D1 18 20 DM1
D2 20 18 DM1
*
D3A 131 70 DM3
D3B 13 131 DM3
GPL 0 8 70 7 1.0000E+00
VC 13 6 2.9595E+00
RPLA 7 70 1.0000E+04
RPLB 7 131 1.0000E+05
D4A 60 141 DM3
D4B 141 14 DM3
GNL 0 8 60 4 1.0000E+00
VE 6 14 2.9595E+00
RNLA 60 4 1.0000E+04
RNLB 141 4 1.0000E+05
*
IP 7 4 4.4400E-03
DSUB 4 7 DM2
* MODELS
.MODEL JM1 PJF (IS=1.1000E-11 BETA=9.5964E-04 VTO=-1.000000E+00)
.MODEL JM2 PJF (IS=9.0000E-12 BETA=9.5964E-04 VTO=-9.998600E-01)
.MODEL DM1 D (IS=1.0000E-15)
.MODEL DM2 D (IS=8.0000E-16 BV=4.8000E+01)
.MODEL DM3 D (IS=1.0000E-16)
.MODEL DM4 D (IS=1.0000E-09)
.ENDS LT1056
*
* - - - - - * FINI LT1056 * - - - - - * [OAMM VJ02 05/08/90]
```

Listing 6

```
.SUBCKT LTC1050 3 2 7 4 6
* INPUT
RD1 4 80 2.1221E+03
RD2 4 90 2.1221E+03
M1 80 2 12 12 PM1
M2 90 3 12 12 PM2
CIN 2 3 5.0000E-12
DG1 2 7 DMG1
DG2 3 7 DMG2
C1 80 90 1.5000E-11
ISS 7 12 1.2000E-04
CS 12 0 1.2857E-11
* INTERMEDIATE
GCM 0 8 12 0 1.4902E-10
GA 8 0 80 90 4.7124E-04
R2 8 0 1.0000E+05
C2 1 8 3.0000E-11
GB 1 0 8 0 1.0664E+04
RO2 1 0 1.9900E+02
* OUTPUT
RSO 1 6 1.0000E+00
ECL 18 0 1 6 1.7955E+02
GCL 0 8 20 0 1.0000E+00
RCL 20 0 1.0000E+01
D1 18 19 DM1
VOD1 19 20 0.0000E+00
```

```
D2 20 21 DM1
VOD2 21 18 2.6932E+00
*
D3A 131 70 DM3
D3B 13 131 DM3
GPL 0 8 70 7 1.0000E+00
VC 13 6 1.4332E+00
RPLA 7 70 1.0000E+01
RPLB 7 131 1.0000E+03
D4A 60 141 DM3
D4B 141 14 DM3
GNL 0 8 60 4 1.0000E+00
VE 6 14 1.4332E+00
RNLA 60 4 1.0000E+01
RNLB 141 4 1.0000E+03
*
IP 7 4 8.8000E-04
DSUB 4 7 DM2
* MODELS
.MODEL PM1 PMOS (KP=1.8506E-03 VTO=-1.1000000E+00)
.MODEL PM2 PMOS (KP=1.8506E-03 VTO=-1.1000005E+00)
.MODEL DM1 D (IS=1.0000E-20)
.MODEL DM2 D (IS=8.0000E-16 BV=1.9800E+01)
.MODEL DM3 D (IS=1.0000E-16)
.MODEL DMG1 D (IS=2.0010E-11)
.MODEL DMG2 D (IS=9.9998E-15)
.ENDS LTC1050
*
* - - - - - * FINI LTC1050 * - - - - - * [OAMM VM02 5/11/90]
```


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