# Measurement and Control Circuit Collection
Diapers and Designs on the Night Shift

Jim Williams

Introduction

During my wife's pregnancy I wondered what it would *really* be like when the baby was finally born. Before that time, there just wasn't much mothering and fathering to do. As a consolation, we busied ourselves watching the baby's heartbeat (Figure 1) on a thrown-together fetal heart monitor (see References).
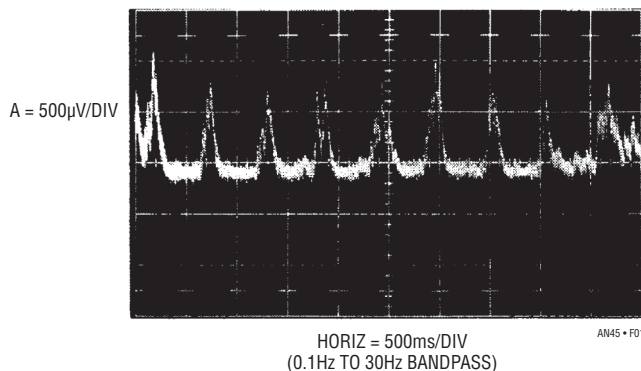
Figure 1. Michael's Fetal Heartbeat 4 1/2 Months into Pregnancy

When Michael was born things got noticeably busier in a hurry. My wife and I split up the evening duties. I got the night shift, 2 am to 7 am. After a few weeks, Michael and I got the hang of it and things began to go (relatively) smoothly. The two of us had mastered feedings, naps, crying jags, bottles, diapers and such and we began looking around for something to do. I decided to introduce Michael to the glories of late night circuit hacking. I first learned about wee hours circuit design at MIT in the 1970s. There was a subculture there that loaded up on pizza, soft drinks, and junk food, took it all into the lab, and closed the door until long after daylight. I was an enthusiastic convert.

Michael and I changed the rules just a bit. We loaded up on formula, diapers, and bottles and went into the lab.

The circuits in this collection represent our efforts, which stopped when he (more or less) began sleeping through the night. Most of the breadboarding occurred between feedings, with design reviews and discussions during feedings. As such, the circuits are annotated with the number of feedings required for their completion; e.g., a "3-bottle circuit" took three feedings. The circuit's degree of difficulty, and Michael's degree of cooperation, combined to determine the bottle rating, which is duly recorded in each figure.
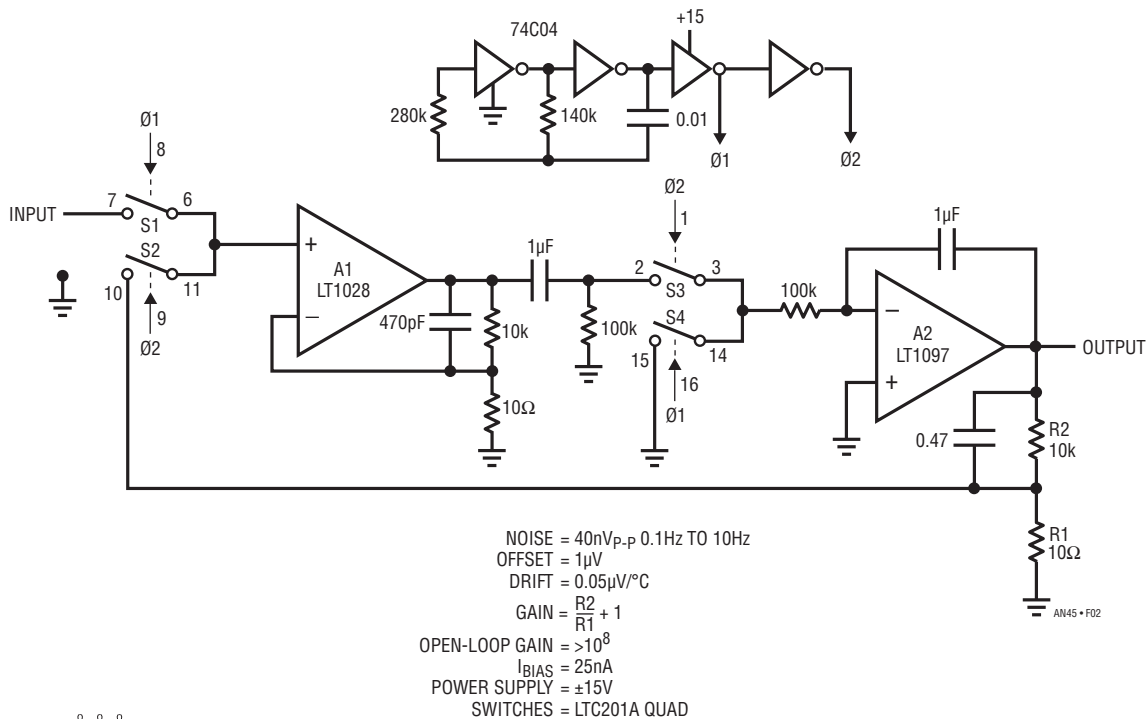
Low Noise and Drift Chopped Bipolar Amplifier

Figure 2's circuit combines the low noise of an LT®1028 with a chopper based carrier modulation scheme to achieve an extraordinarily low noise, low drift DC amplifier. DC drift and noise performance exceed any currently available monolithic amplifier. Offset is inside 1µV, with drift less than 0.05µV/°C. Noise in a 10Hz bandwidth is less than 40nV, far below monolithic chopper-stabilized amplifiers.

Bias current, set by the bipolar LT1028 input, is about 25nA. These specifications suit demanding transducer signal conditioning situations such as high resolution scales and magnetic search coils.

The 74C04 inverters form a simple 2-phase square wave clock running at about 350Hz. The oscillator provides complementary drive to S1 and S2, causing A1 to see a chopped version of the input voltage. A1 amplifies this AC signal. A1's square wave output is synchronously demodulated by S3 and S4. Because these switches are synchronously driven with the input chopper, proper amplitude and polarity information is presented to A2, the DC output amplifier. This stage integrates the square wave into a DC voltage, providing the output. The output is divided down (R2 and R1) and fed back to the input chopper where it serves as a zero signal reference. Gain, in this case 1000, is set by the R1-R2 ratio. Because A1 is AC-coupled, its DC offset and drift do not affect overall circuit offset, resulting in the extremely low offset and drift noted.

Figure 2. The Chopped Bipolar Amplifier. Noise Is Inside 40nV with 0.05µV/°C Drift

Figure 3, a noise plot of the amplifier in a 0.1Hz to 10Hz bandwidth, shows less than 40nV of peak-to-peak noise. A1 and the 60Ω resistance of S1-S2 contribute about equally to form this noise. When using this amplifier it is important to realize that A1's bias current flowing through the input source impedance causes additional noise. In general, to maintain low noise performance, source resistance should be kept below 500Ω. Fortunately, transducers such as strain gauge bridges, RTDs, and magnetic detectors are well below this figure.
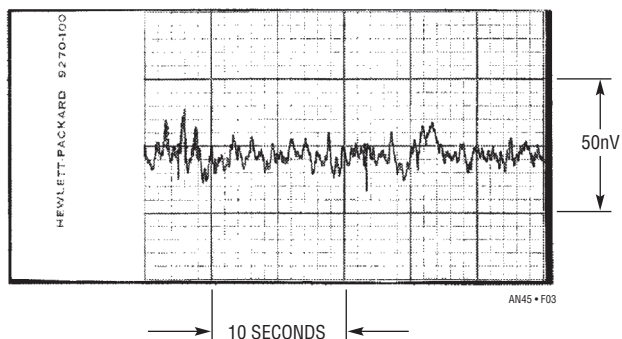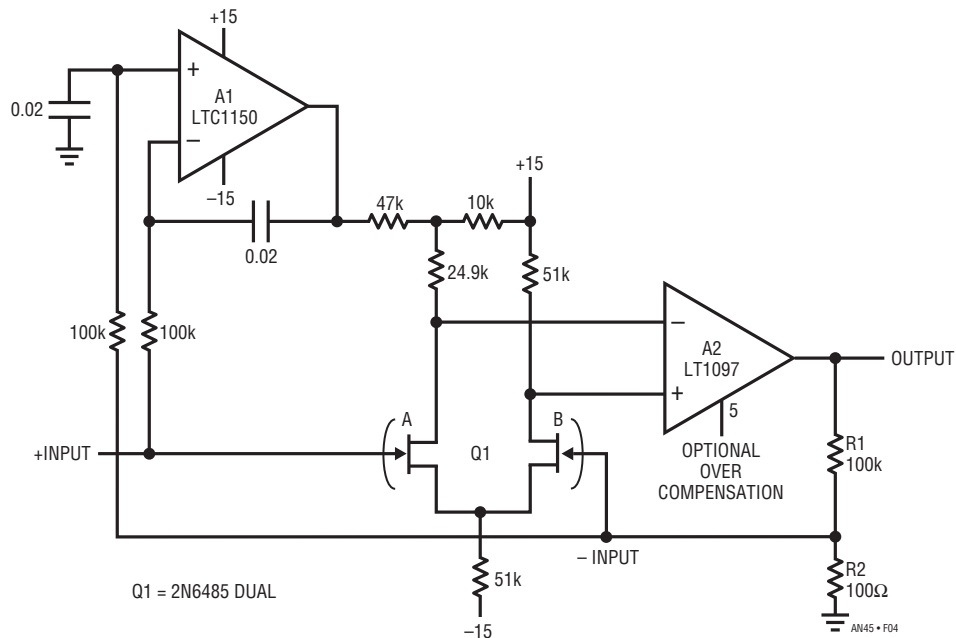

Figure 3. Noise in a 0.1Hz to 10Hz Bandwidth in Less Than 40nV with 0.05µV/°C Drift

Low Noise and Drift-Chopped FET Amplifier

Figure 4's circuit combines the low drift of a chopper-stabilized amplifier with a pair of low noise FETs. The result is an amplifier with 0.05µV/°C drift, offset within 5µV, 50pA bias current, and 200nV noise in a 0.1Hz to 10Hz bandwidth. The noise performance is especially noteworthy; it is almost eight times better than monolithic chopper-stabilized amplifiers.

FET pair Q1 differentially feeds A2 to form a simple low noise op amp. Feedback, provided by R1 and R2, sets closed-loop gain (in this case 1000) in the usual fashion. Although Q1 has extraordinarily low noise characteristics, its 15mV offset and 25µV/°C drift are poor. A1, a chopper-stabilized amplifier, corrects these deficiencies. It does this by measuring the difference between the amplifier's inputs and adjusting Q1A's channel current to minimize the difference. Q1's skewed drain values ensure that A1 will be able to capture the offset. A1 supplies whatever current is required into Q1A's channel to force offset within 5µV. Additionally, A1's low bias current does not appreciably add to the overall 50pA amplifier bias current. As shown, the amplifier is set up for a noninverting gain of 1000, although other gains and inverting operation are possible.

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Figure 4. Chopper-Stabilized FET Pair Combines Low Bias, Offset and Drift with 200nV Noise

Figure 5 is a plot of noise measured in a 0.1Hz to 10Hz bandwidth. The performance obtained is almost an order of magnitude better than any monolithic chopper-stabilized amplifier, while retaining low offset and drift.
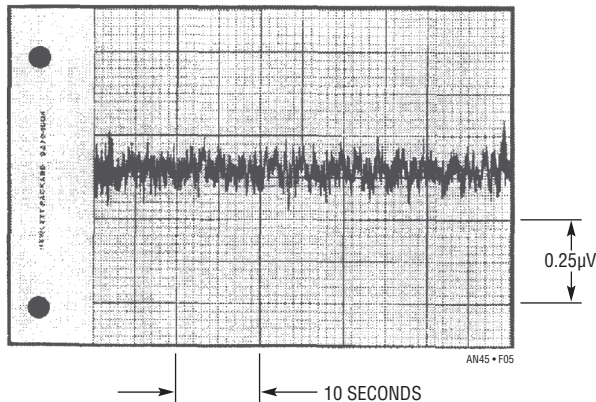
Figure 5. Noise Performance for Figure 4. A1's Low Offset and Drift are Retained, but Noise Is Almost Ten Times Better

A2's optional overcompensation can be used (capacitor to ground) to optimize damping for low closed-loop gains.

Stabilized, Wideband Cable Driving Amplifier with Low Input Capacitance

Figure 6's amplifier has over 20MHz of small-signal bandwidth driving 100mA loads, capacitance or cable.

Input capacitance is below 1.5pF and bias current about 100pA. The output is fully protected. These features make this amplifier ideal as an ATE pin amplifier, video A/D input buffer, or cable driver. The amplifier also permits wideband probing when oscilloscope probe loading is not tolerable. The overall amplifier is composed of a low input capacitance FET, two LT1010 buffers, and a discrete gain stage. A3 acts as a DC restoration loop. The 33Ω resistors sense A1's operating current, biasing Q3 and Q4. These devices furnish complementary voltage gain to A2, which provides the circuit's output. Feedback is from A2's output to A1's output, which is a low impedance point. This "current mode" feedback permits fixed bandwidth over a wide range of closed-loop gains. This contrasts with normal feedback schemes where bandwidth degrades as closed-loop gain increases.

A3's stabilizing loop compensates large offsets in the signal path, which are dominated by mismatch in Q3 and Q4. A3 measures the DC difference between the amplifier's input and output and biases the signal path to correct for offset. Correction is implemented by controlling Q1's channel current via Q2. The channel current sets Q1's V_{GS}, allowing A3 to control overall circuit offset. The 9k to 1k feedback divider feeding A3 is selected to equal the gain ratio of the circuit, in this case 10.
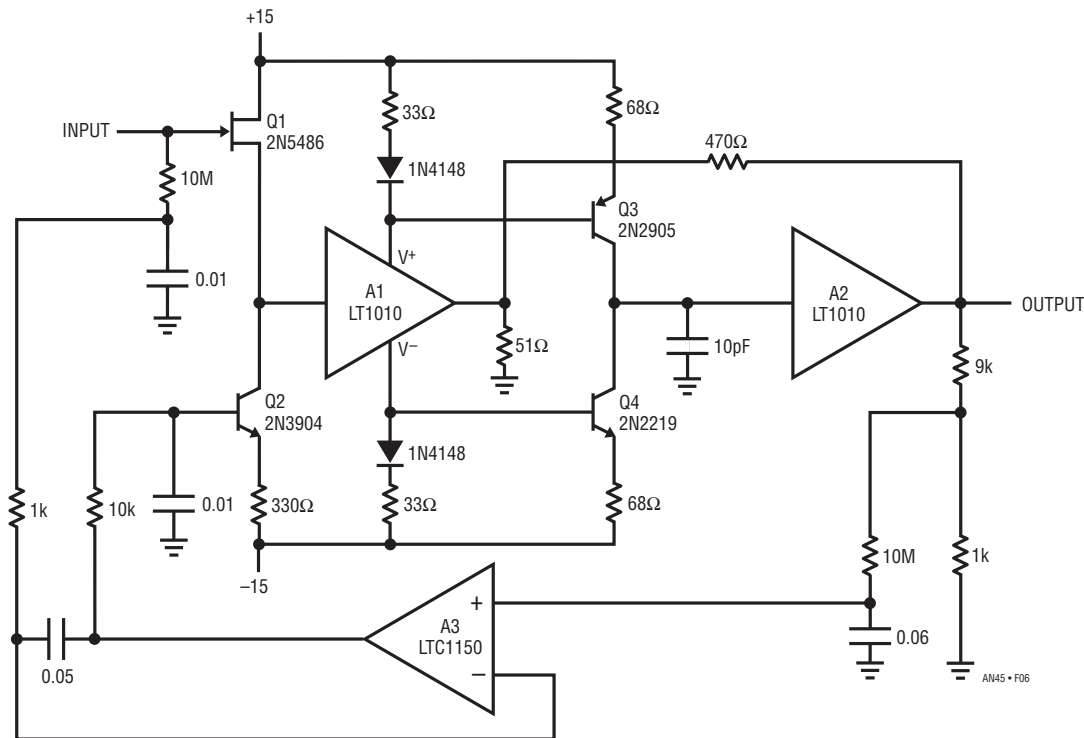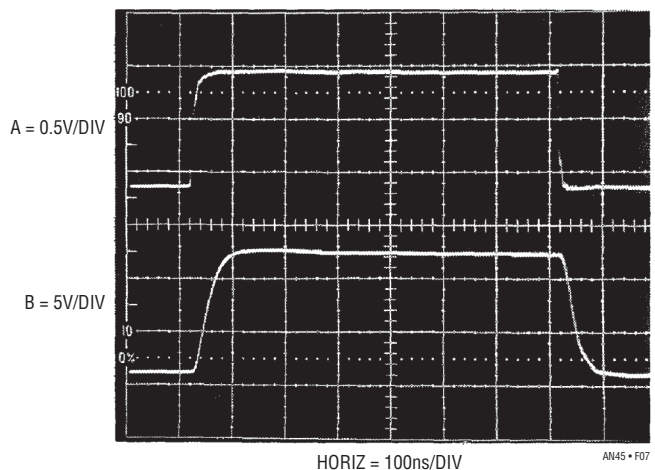
Figure 6. Stabilized, Wideband Cable Driving Amplifier with Low Input Capacitance

The feedback scheme makes A1's output look like the negative input of the amplifier, with closed-loop gain set by the ratio of the 470Ω and 51Ω resistors. The outstanding feature of this connection is that the bandwidth becomes relatively independent of closed-loop gain over a reasonable range. For this circuit, small-signal bandwidth exceeds 20MHz over gains of 1 to 20. The loop is quite stable, and the 10pF value at A2's input provides good damping over a wide range of gains.

Figure 7 shows large-signal performance at a gain of 10 driving 10 feet of cable. A fast input pulse (trace A) produces the output shown (trace B). Response is quick and clean with no slew residue or poor dynamics.

Voltage Programmable, Ground Referred Current Source

Precise, voltage programmable, ground referred current sources are usually complex and require trimming. Figure 8's simple, powerful configuration produces output current in strict accordance with the sign and magnitude of the control voltage. Dynamic response is well controlled,

Figure 7. Wideband Amplifier's Response Driving A 10 Foot Cable

and no trimming is required. The circuit's accuracy and stability are almost entirely dependent upon resistor R.

A1, biased by V_{IN}, drives current through R (in this case 10Ω) and the load. Instrumentation amplifier A2, operating at a gain of 100, senses across R. A2's output closes a loop back to A1. Because A1's loop forces a fixed voltage

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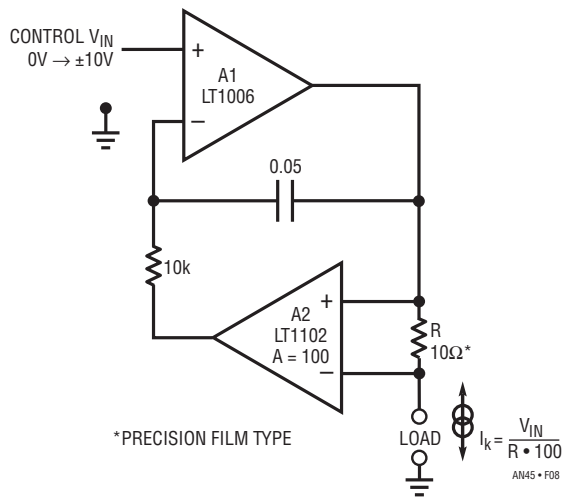
Figure 8. Voltage Programmable Current Source Is Simple and Precise

HORIZ = 20μs/DIV

AN45 • F09

Figure 9. Current Source Dynamics Are Clean, with No Slew Residue or Aberrations

across R, the current through the load is constant. The 10k-0.05μF combination sets A1's roll-off, and the circuit is stable.
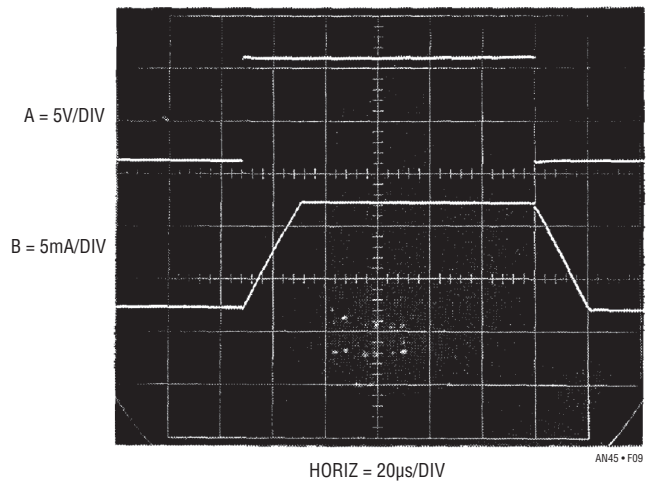
Assuming an errorless component for R, the circuit's initial error is dominated by A2's 0.05% gain specification and its 5ppm/°C temperature coefficient. High grade film or wirewound resistors will maintain this level of performance.

Figure 9 shows dynamic response for a full-scale input step. Trace A is the voltage control input while trace B shows the output current. Response is clean, with no slew residue or aberrations.

5V Powered, Fully Floating 4mA to 20mA Current Loop Transmitter

4mA to 20mA current-loop transmitters are frequently required in industrial process control. Often, because of uncertain or dangerous common mode voltages, it is desirable that the generated 4mA to 20mA current be completely galvanically isolated from the transmitter's input. Figure 10's circuit does this while operating from a single 5V supply.

A2's positive input assumes a bias dependent upon the input and the 4mA trim setting. Under these conditions A2's output heads positive, turning on Q1 and Q2. Q2's collector drives T1's primary, which is chopped by Q3 and Q4. Complementary chopper drive comes from the 74C74 flip-flop outputs, with oscillator I_1 setting a 25kHz clock rate. T1's output, producing voltage step-up, is rectified,

filtered, and applied to the load. A3 senses load current across the 16Ω shunt and drives T2's center tap. Q9 and Q10, receiving complementary drive picked off from T1's secondary, modulate T2's DC center-tap voltage. T2's secondary receives this information, with flip-flop driven Q6-Q7 demodulating it back to DC at T2's center tap. T2's center tap voltage is fed A2, completing an isolated control loop. Changes in the circuit's input voltage cause this loop to adjust the load current accordingly. Conversely, load resistance changes have no effect, because the loop forces whatever voltage is necessary to maintain a constant 16Ω shunt voltage. Because T1 can supply up to 50V, load current remains fixed over load resistance swings from 0Ω to 2500Ω. Power supply shifts are similarly rejected by the loop, and the transformer modulation-demodulation scheme permits 0.05% accuracy and stability over temperature and a 250V common mode range. Greater common mode voltages are possible with increased transformer breakdown ratings.

Several subtleties aid circuit performance. I_2-I_3 and I_4-I_5 provide drive delays to Q6 and Q7. These delays approximate the delay through T1 to modulator pair Q9/Q10. This helps the four transistors switch simultaneously, aiding modulator-demodulator accuracy. Zener connected Q5 ensures that T1 produces enough voltage to power A3 and Q9/Q10, even when the load is 0Ω. Q8, similarly Zener connected, clamps gate drive to Q9 and Q10, improving modulator linearity by preventing excessive gate drive variations over operating conditions. The diodes in A3's output
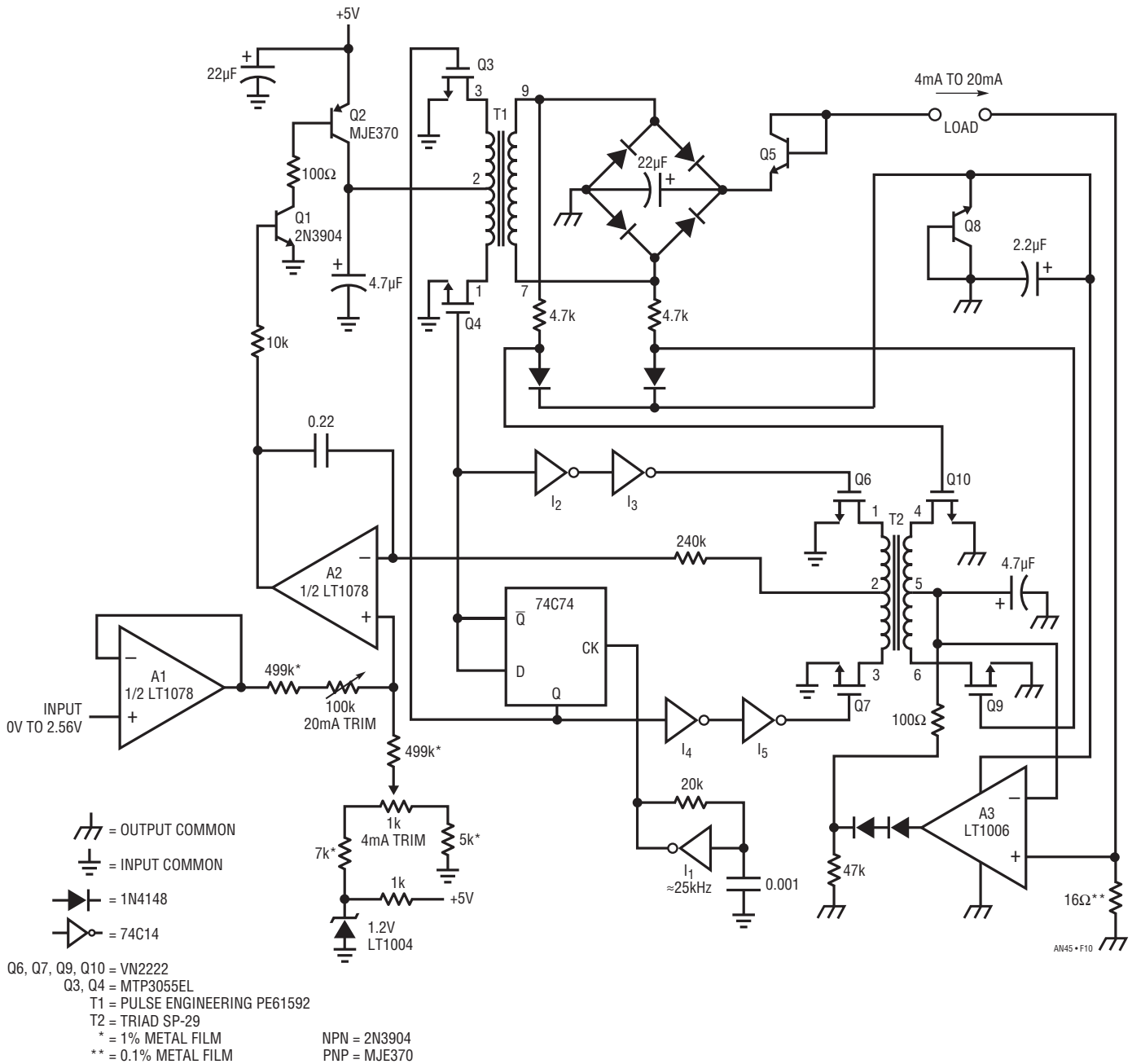
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Figure 10. 5V Powered, Fully Floating 4mA to 20mA Current Loop Transmitter

ensure proper loop start-up. They prevent T2's center tap from receiving any bias until A3 has enough power supply voltage to function normally. To calibrate this circuit apply 0V input and adjust the 4mA trim for 4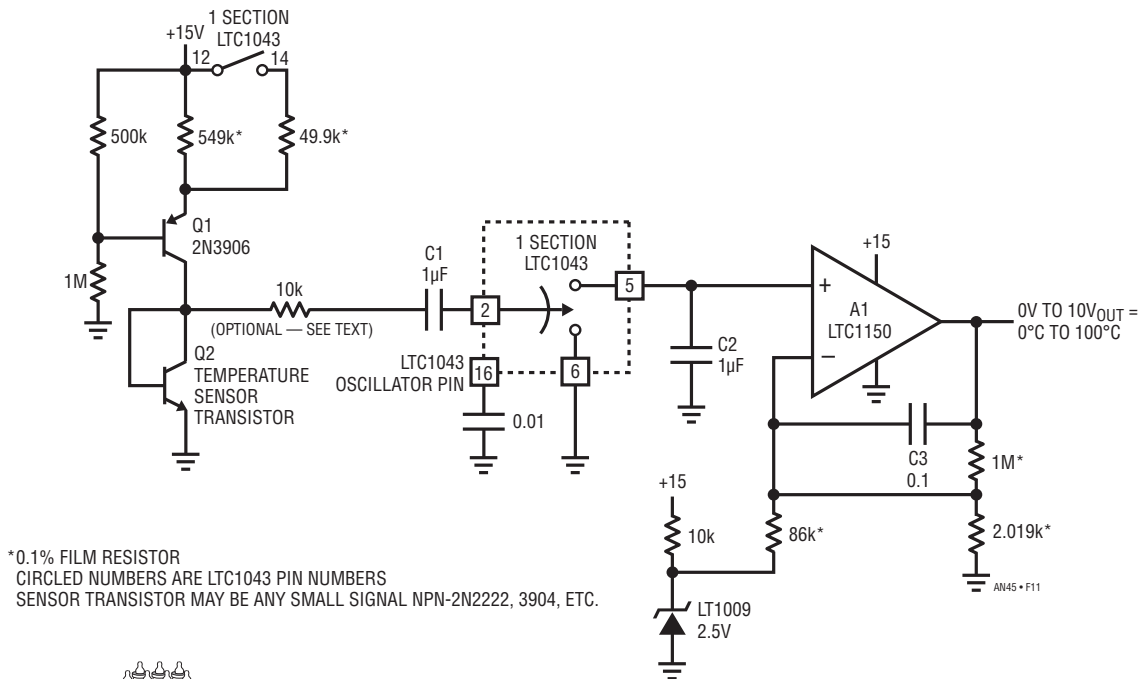.00mA output (0.064V across the 16Ω shunt). Next, apply 2.56V input and set the 20mA trimmer for 20.00mA output (0.3200V across the 16Ω shunt). Repeat this procedure until both points are fixed. Note that the 2.56V input range is directly compatible with D/A converter outputs, permitting digital control.

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Transistor ΔV_BE Based Thermometer

Low cost makes transistors potentially attractive as temperature sensors. Almost all transistor-sensed thermometer circuits utilize the base-emitter diode voltage shift with temperature as the sensing mechanism. Unfortunately, the absolute diode voltage is unpredictable, necessitating circuit calibration. Additionally, if the transistor sensor ever requires replacement, the calibration must be repeated. This constraint often negates the transistor sensor's cost and convenience advantages.
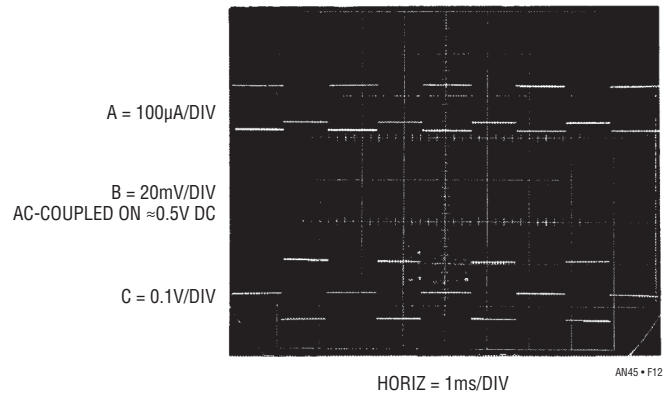
Figure 11's transistor sensor thermometer overcomes this difficulty. The circuit provides a 0V to 10V output corresponding to a 0°C to 100°C temperature excursion at the sensor transistor. Accuracy is ±1°C. No calibration is required, and any common small-signal NPN transistor can serve as the sensor. The circuit is based on the predictable relationship between current and voltage in a transistor V_{BE} junction.[1] At room temperature, the V_{BE} junction diode shifts 59.16mV per decade of current. The temperature dependence of this constant is 0.33%/°C, or 198µV/°C. This ΔV_{BE} versus current relationship holds, regardless of the V_{BE} diode's absolute value.

Note 1: See References 1 through 4.

The LTC®1043 contains switches whose state is controlled by an on-chip oscillator. The 0.01µF capacitor at Pin 16 sets oscillator frequency at about 500Hz. Q1 operates as a switched-value current source, alternating between about 10µA and 100µA (trace A, Figure 12) as the LTC1043 commutates switch Pin 12 and Pin 14. The two currents' exact value is unimportant, so long as their *ratio* remains constant. Because of this, Q1 requires no reference, although its emitter resistor's ratio is precise. The alternating 10µA to 100µA stepped current to the sensor transistor (Q2)

A = 100µA/DIV

B = 20mV/DIV
AC-COUPLED ON ≈0.5V DC

C = 0.1V/DIV

HORIZ = 1ms/DIV

AN45 • F12

Figure 12. Waveforms for the ΔV_BE Based Thermometer

*0.1% FILM RESISTOR
 CIRCLED NUMBERS ARE LTC1043 PIN NUMBERS
 SENSOR TRANSISTOR MAY BE ANY SMALL SIGNAL NPN-2N2222, 3904, ETC.

Figure 11. ΔV_BE Based Thermometer Does Not Require Calibration

causes the theoretical 59.16mV (25°C) excursion (trace B) to appear across the V_{BE} junction. This signal is coupled to a switched demodulator via C1, which strips off Q2's DC bias. LTC1043 switch Pin 2 (trace C) sees only the 59mV waveform, which is referenced to ground via demodulator action at Pin 5 and Pin 6. Pin 5, connected to capacitor C2, sits at Pin 2's DC peak value. A1 amplifies this DC signal, with the LT1004 providing offset so 0°C equals 0V. The optional 10k resistor protects against ESD events, which may occur if Q2 is located at the end of a cable.

Using the components shown, the circuit achieves ±1°C accuracy over a sensed 0°C to 100°C range. Substituting randomly selected 2N3904s and 2N2222s for Q2 showed less than 0.4°C spread over 25 devices from various manufacturers.

Micropower, Cold Junction Compensated Thermocouple-to-Frequency Converter

Figure 13 is a complete, digital output, thermocouple signal conditioner. The circuit produces a 0kHz to 1kHz output in response to a sensed 0°C to 100°C temperature excursion.

Cold junction compensation is included, and accuracy is within 1°C with stable 0.1°C resolution. Additionally, the circuit functions from a single supply, which may range from 4.75V to 10V. Maximum current consumption is 360µA.

The LT1025 provides an appropriately scaled cold junction compensation voltage to the type K thermocouple. As a result, the voltage at schematic point "A" varies from 0mV to 4.06mV over a sensed 0°C to 100°C range (type K slope is 40.6µV/°C). The remaining components form a voltage-to-frequency converter that directly converts this millivolt level signal without the usual DC gain stage. A1's negative input is biased by the thermocouple. A1's output drives a crude V-F converter, comprised of Q2, the 74C14 inverters, and associated components. Each V-F output pulse causes a fixed quantity of charge to be dispensed into C3 from C2 via the LTC201 based charge pump. C3 integrates the charge packets, producing a voltage at A1's positive input. A1's output forces the V-F converter to run at whatever frequency is required to balance the amplifier's inputs. This feedback action eliminates drift and nonlinearities in the V-F converter as an error term and the output frequency
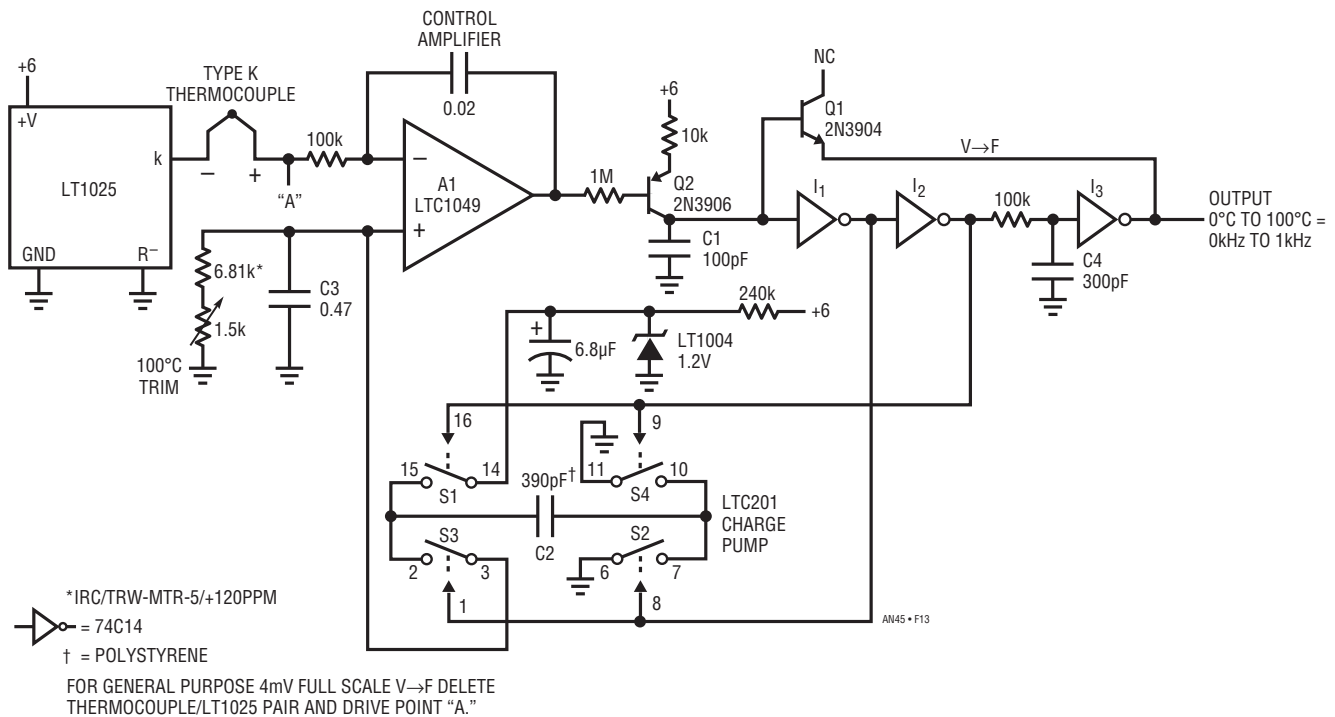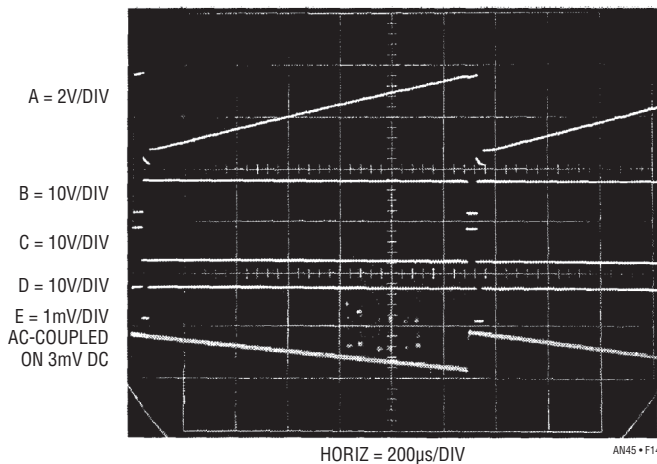

Figure 13. Thermocouple Sensed Temperature-to-Frequency Converter

is solely a function of the DC conditions at A1's inputs. The 0.02µF capacitor forms a dominant response pole at A1, stabilizing the loop. Chopper stabilized A1's low V_{OS} offset and drift eliminate offset error in the circuit, despite an output LSB value of only 4.06µV (0.1°C).

Figure 14 details circuit operation. A1's output biases current source Q2, producing a ramp (trace A, Figure 14) across C1. When the ramp crosses I_1's threshold, the cascaded inverter chain switches, producing complementary outputs at I_1 (trace B) and I_2 (trace C). I_3's RC delayed response (trace D) turns on diode connected Q1, discharging C1 and resetting the ramp. The ramp aberrations before the reset are due to transient I_1 input currents during switching (near top of ramp). Q1's V_{BE} diode rounding and reverse charge transfer (bottom of ramp) account for the discontinuities during the ramp's low point.

A = 2V/DIV
B = 10V/DIV
C = 10V/DIV
D = 10V/DIV
E = 1mV/DIV
AC-COUPLED
ON 3mV DC

HORIZ = 200µs/DIV   AN45 • F14

Figure 14. Waveforms for the Thermocouple-to-Frequency Converter

The complementary I_1-I_2 outputs clock the LTC201 switch based charge pump. C2 is alternately charged to the LT1004's reference voltage via S1 and S4 and discharged into C3 through S2 and S3. Each time this cycle occurs, C3's voltage is forced up (trace E). C3's average voltage is set by the 6.81k to 1.5k trimmer resistance across it. A1 servo controls the repetition rate of the V-F to bring its inputs to the same value, closing a control loop. The 0.02µF capacitor smooths A1's response to DC.

To calibrate this circuit, disconnect the thermocouple and drive point "A" with 4.06mV. Next, set the 1.5k trimmer for exactly 1000Hz output. Connect the thermocouple and

the circuit is ready for use. Recalibration is not required if the thermocouple is replaced.

It is worth noting that this circuit can directly digitize any millivolt level signal by deleting the LT1025 thermocouple pair and directly driving point "A."

Relative Humidity Signal Conditioner

Relative humidity is a difficult physical parameter to transduce, and most transducers require fairly complex signal conditioning circuitry. Figure 15 combines simple circuitry with a capacitively based transducer to achieve good results. This circuit, which runs from a 9V battery, is accurate within 2% in the 5% to 90% relative humidity range.

The sensor specified has a nominal 500pF capacitance at RH = 76%, with a slope of 1.7pF/% RH. The average voltage across the device must be zero. This prevents deleterious electrochemical migration in the sensor. LTC1043 section "A," driven by an internal oscillator, alternately charges the sensor from a resistively scaled portion of the LT1004 reference and discharges it into A1's summing point. Note that the switching is arranged so that sensor related current flows out of A1's summing point. The 0.1µF series capacitor ensures the sensor sees the required zero average voltage, with the 22MΩ resistor preventing charge accumulation, which would stop current flow. The average current out of A1's summing point is balanced by packets of charge delivered by the LTC1043 switched capacitor section "C" in A1's feedback loop. The 0.1µF feedback capacitor gives A1 an integrator-like response, and its output is DC. As such, changes in sensor capacitance are seen as DC shifts in A1's output. A1 responds by raising its output positive to whatever DC potential is required to maintain its summing point at zero.

To allow 0% RH to equal 0V, offsetting is required. The signal and feedback terms biasing A1's summing point are expressed in charge form. Because of this, the offset must also be delivered to the summing point as charge, instead of a simple DC current. If this is not done, the circuit will be affected by drift in the LTC1043's internal oscillator. LTC1043 section "B" serves this function, delivering LT1004 referenced offsetting charge to A1.

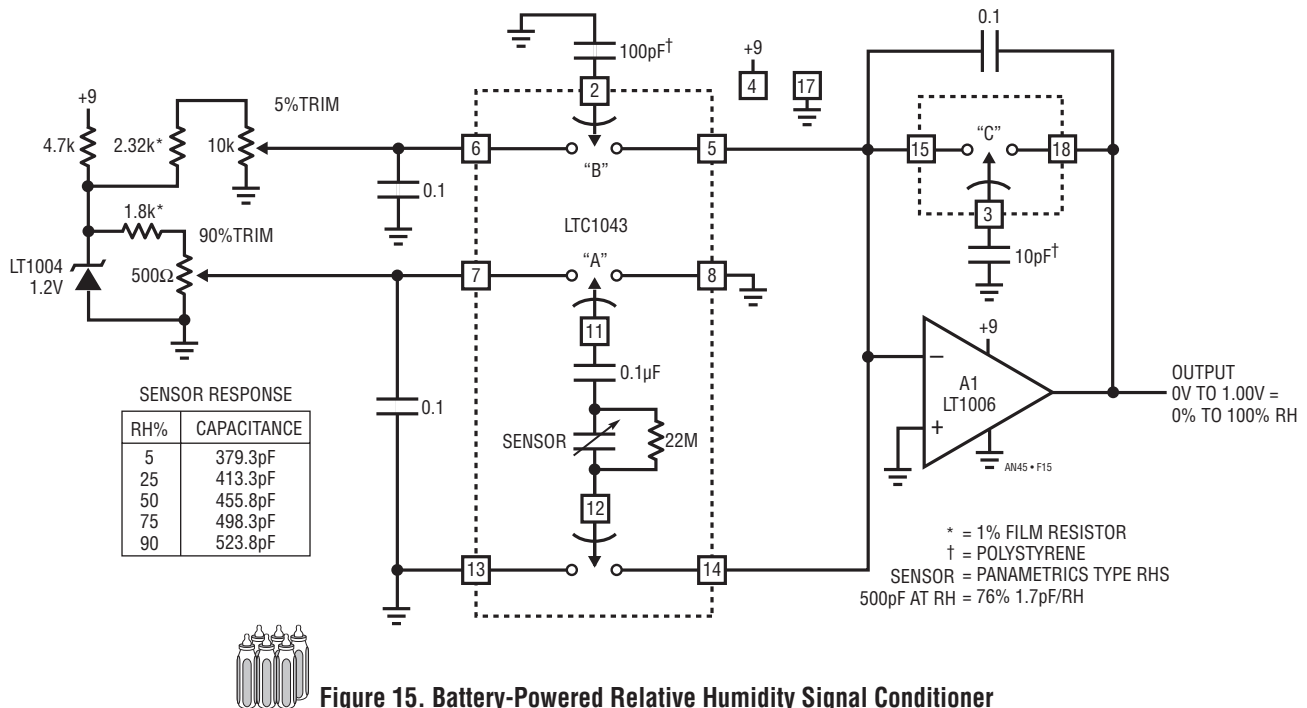**Figure 15. Battery-Powered Relative Humidity Signal Conditioner**

SENSOR RESPONSE

RH%	CAPACITANCE
5	379.3pF
25	413.3pF
50	455.8pF
75	498.3pF
90	523.8pF

* = 1% FILM RESISTOR
† = POLYSTYRENE
SENSOR = PANAMETRICS TYPE RHS
500pF AT RH = 76% 1.7pF/RH

Drift terms in this circuit include the LT1004 and the ratio stability of the sensor and the polystyrene capacitors. These terms are well within the sensor's 2% accuracy specification, and temperature compensation is not required. To calibrate this circuit, place the sensor in a 5% RH environment and set the "5% RH trim" for 50mV output. Next, place the sensor in a 90% RH environment and set the "90% trim" for 900mV output. Repeat this procedure until both points are fixed. If known RH environments are unavailable, the capacitance versus RH table in Figure 15 may be utilized, although it applies for an ideal sensor. The capacitor values may be built-up or directly dialed out on a precision variable air capacitor (General Radio #722D).

Inexpensive Precision Electronic Barometer

Until recently, precision electronically based pressure measurements required expensive transducers. Capacitive and bonded strain gauge based approaches provide unmatched results, but costs are often prohibitive. Additionally, if low power operation is desired, signal conditioning for these devices can become complex.

Semiconductor based pressure transducers becoming available offer significant improvement over earlier devices. Figure 16's circuit utilizes such a device to form a low cost barometer. The LT1027 reference and A1 form a

current source to put precisely 1.5mA through transducer T1, in accordance with the manufacturer's specifications. Instrumentation amplifier A3 takes a differential gain of 10 from T1's bridge output. A2 provides additional gain to yield a calibrated output directly in inches of mercury.

T1's manufacturer specifies a nominal 115mV at full scale, although each device is supplied with precise calibration data. This information considerably simplifies calibration. To calibrate the circuit, simply adjust the potentiometer at A1 until the output corresponds to the scale factor supplied with the unit.

This circuit, compared to a long column mercury barometer, tracked ambient pressure variations from 29.75" to 30.32" over three months with only two counts of uncertainty. Additionally, over 50 turn-on/turn-off cycles had no measurable effect. Changes in pressure, particularly rapid ones, correlated quite nicely to changing weather conditions.

1.5V Powered Radiation Detector

Figure 17's circuit provides an audible "tick" signal each time radiation or a cosmic ray passes through the detector. The LT1073 switching regulator pulses T1. T1 takes gain via its turns ratio and drives a voltage tripler, providing 500V bias to the detector. R1 and R2 provide scaled feedback to
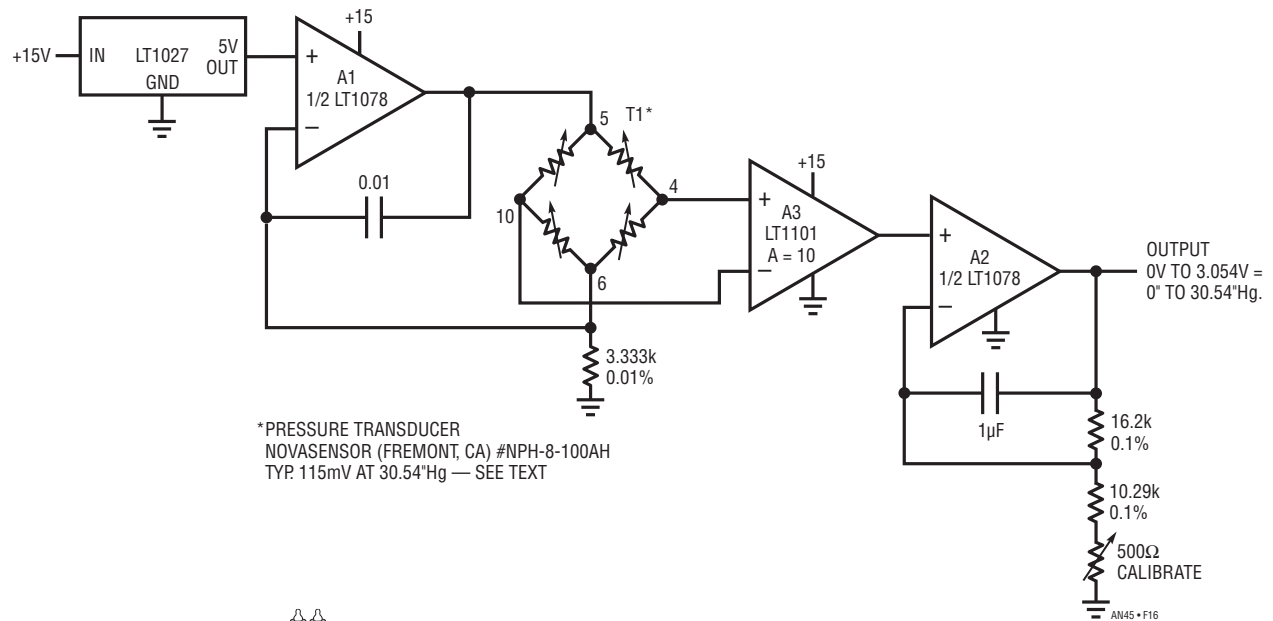
*PRESSURE TRANSDUCER
NOVASENSOR (FREMONT, CA) #NPH-8-100AH
TYP. 115mV AT 30.54"Hg — SEE TEXT

OUTPUT
0V TO 3.054V =
0" TO 30.54"Hg.

AN45 • F16

Figure 16. A Simple, Inexpensive Precision Barometer

T1 = COILTRONICS CTX10052-1
X1 = PROJECTS UNLIMITED AT11K
D1, D2, D3 = MUR1100
C1 = 0.1µF, 200V
C2 = 0.1µF, 400V
C3 = 0.1µF, 600V
R1 = VICTOREEN SLIM-MOX-108
DETECTOR = LND-712 LND CORP, OCEANSIDE, N.Y.

AN45 • TA17

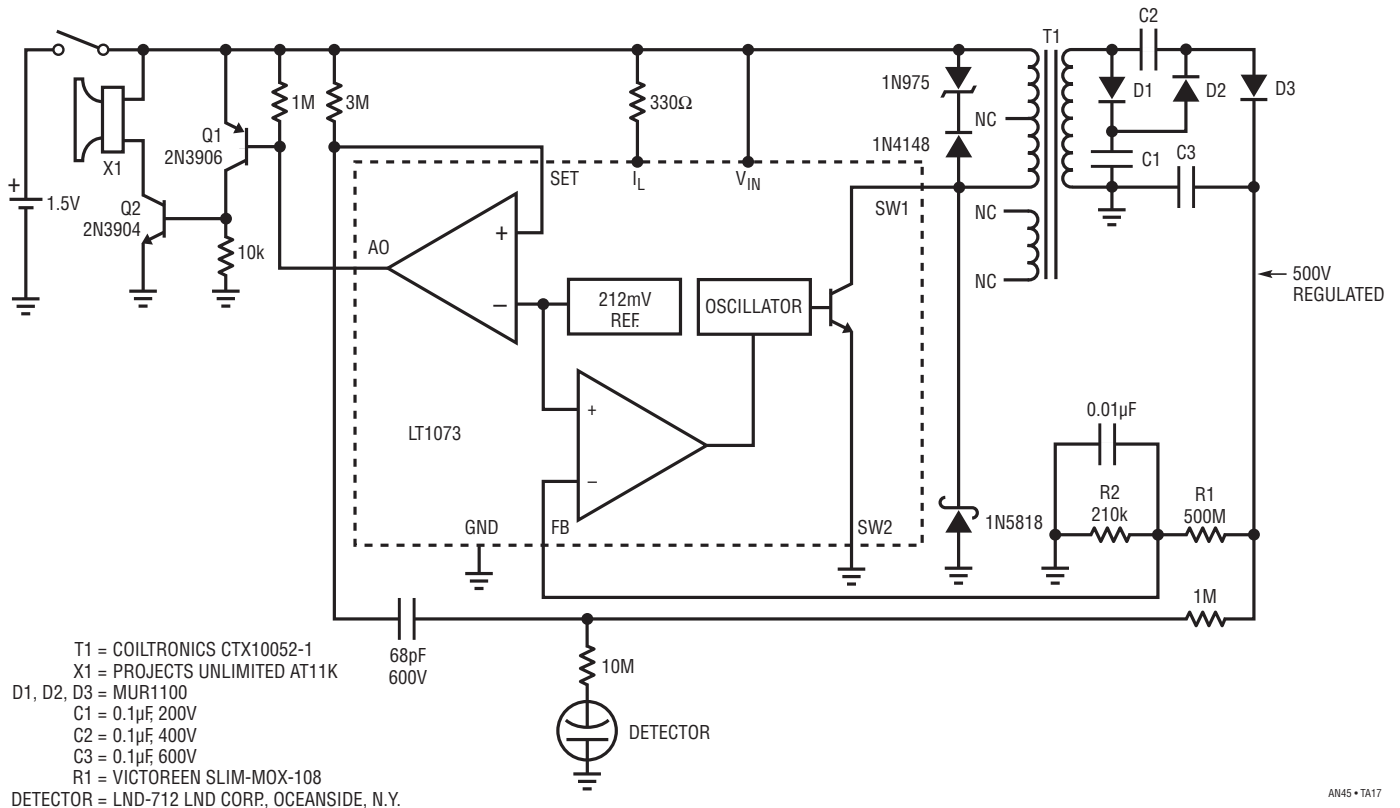**Figure 17. 1.5V Powered Radiation Detector**

the LT1073, closing a control loop. The 0.01µF lag adds AC hysteresis and the Schottky diode clamps negative going T1 excursions. When radiation or a cosmic ray strikes the detector, impedance drops briefly, transferring a quick negative going spike through the 68pF capacitor. This spike triggers the LT1073's auxiliary gain block, configured here as a comparator. Q1 and Q2 provide additional gain to drive the audible beeper. About 10 to 15 cosmic rays per minute are recorded in a normal environment.

9ppm Distortion, Quartz Stabilized Oscillator

A spectrally pure sine wave oscillator is required for data converter, filter and audio testing. Figure 18 provides a stable frequency output with extremely low distortion.

This quartz stabilized 4kHz oscillator has less than 9ppm (0.0009%) distortion in its 10V$_{P-P}$ output.

To understand circuit operation, temporarily assume A2's output is grounded. With the crystal removed, A1 and the A3 power buffer form a noninverting amplifier with a grounded input. The gain is set by the ratio of the 47k resistor to the 50k potentiometer—opto-isolator pair. Inserting the crystal closes a positive feedback path at the crystal's resonant frequency, and oscillations occur. A4 compares A3's positive peaks with the LT1004 2.5V negative reference. The diode in series with the LT1004 provides temperature compensation for A3's rectifier diode. A4 biases the LED portion of the opto-isolator, controlling
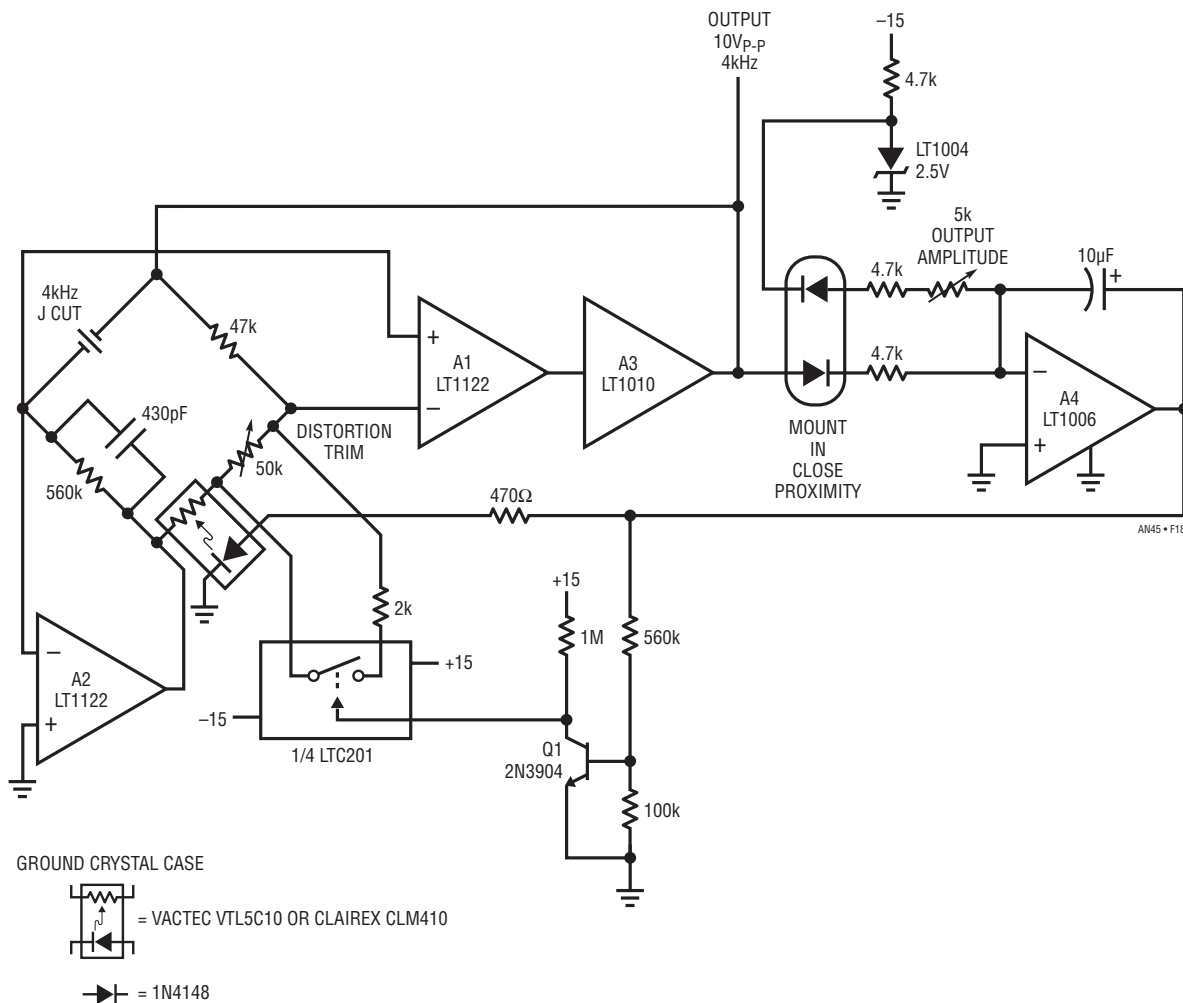

Figure 18. Quartz Stabilized 4kHz Oscillator with 9ppm Distortion

the photoresistor's resistance. This sets loop gain to a value permitting stable amplitude oscillations. The 10µF capacitor stabilizes this amplitude control loop.

A2's function is to eliminate the common mode swing seen by A1. This dramatically reduces distortion due to A1's common mode rejection limitations. A2 does this by servo controlling the 560kΩ-photocell junction to maintain its negative input at 0V. This action eliminates common mode swing at A1, leaving only the desired differential signal.

Q1 and the LTC201 switch form a start-up loop. When power is first applied oscillations may build very slowly. Under these conditions A4's output saturates positive, turning on Q1. The LTC201 switch turns on, shunting the 2kΩ resistor across the 50kΩ potentiometer. This raises A1's loop gain, forcing a rapid build-up of oscillations. When oscillations rise high enough A4 comes out of saturation, Q1 and the switch go off and the loop functions normally.

The circuit is adjusted for minimum distortion by adjusting the 50kΩ potentiometer while monitoring A3's output with a distortion analyzer. This trim sets the voltage across the photocell to the optimum value for lowest distortion. The circuit's power supply should be well regulated and bypassed to ensure the distortion figures quoted.

After trimming, A3's output (trace A, Figure 19) contains less than 9ppm (0.0009%) distortion. Residual distortion components (trace B) include noise and second harmonic residue. Oscillation frequency, set by crystal tolerance, is typically within 50ppm with less than 2.5ppm/°C drift.

A = 5V/DIV

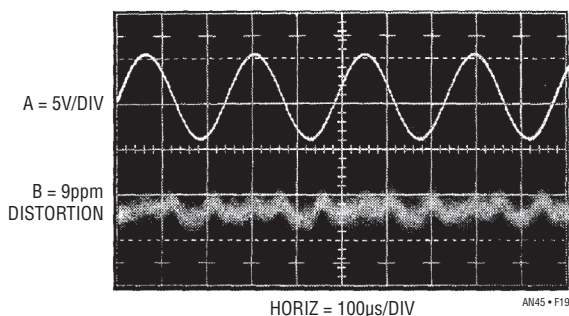B = 9ppm DISTORTION

HORIZ = 100µs/DIV

AN45 • F19

Figure 19. Oscillator Output and its 9ppm Distortion Residue

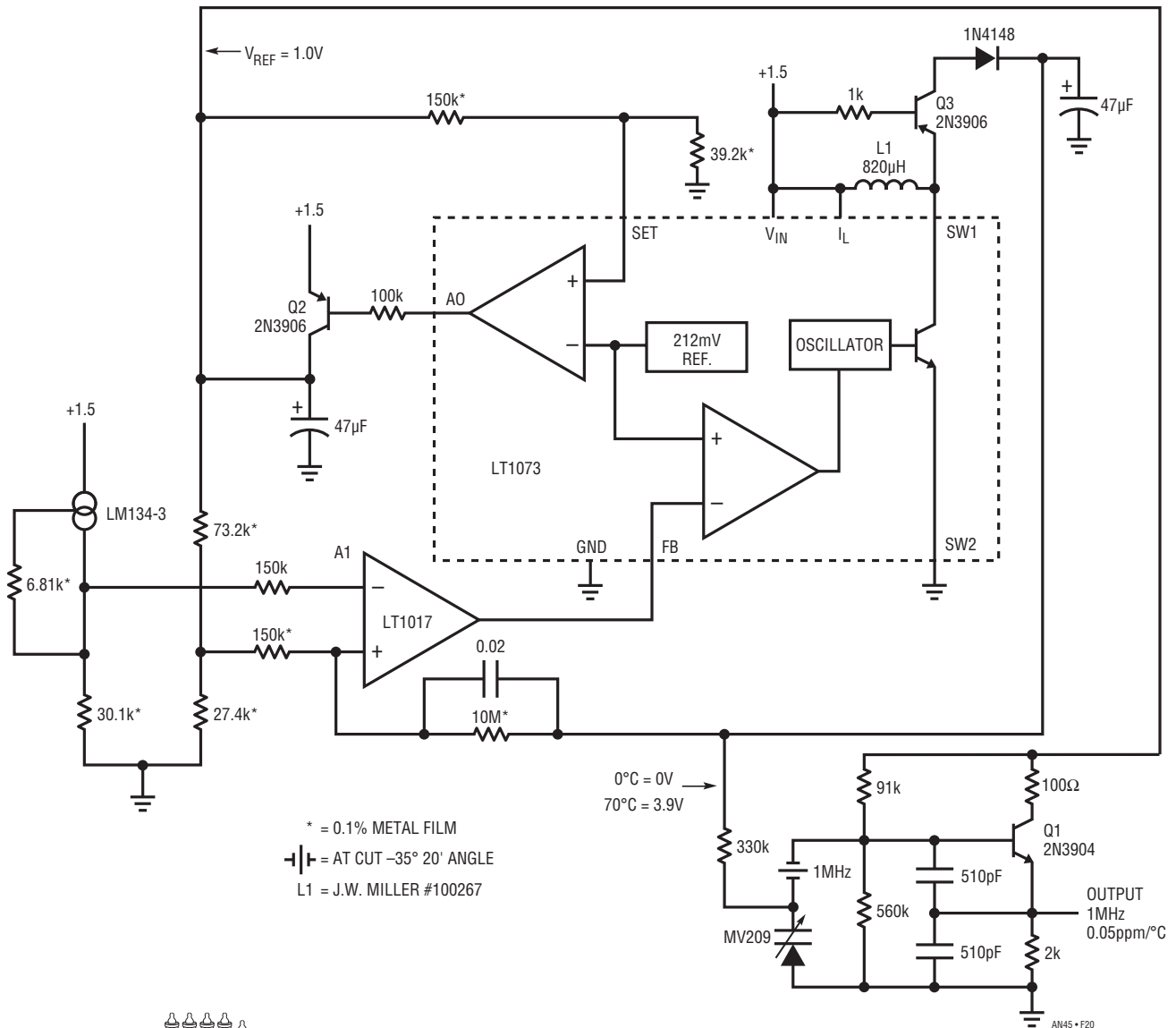## 1.5V Powered Temperature Compensated Crystal Oscillator

Many single cell systems require a stable clock source. Crystal oscillators which run from 1.5V are relatively easy to construct. However, if good stability over temperature is required, things become more difficult. Ovenizing the crystal is one approach, but power consumption is excessive. An alternate method provides open loop, frequency correcting bias to the oscillator. The bias value is determined by absolute temperature. In this fashion, the oscillator's thermal drift, which is repeatable, is corrected. The simplest way to do this is by slightly varying the crystal's resonance point with a variable shunt or series impedance. Varactor diodes, the capacitance of which varies with reverse voltage, are commonly employed for this purpose. Unfortunately, these diodes require volts of reverse bias to generate significant capacitance shift, making direct 1.5V powered operation impossible.

Figure 20 improves the temperature stability of a 1.5V powered crystal oscillator by a factor of 20. It does this by slightly tuning the crystal's resonance as ambient temperature varies. Q1 and associated components form a 1MHz Colpitts oscillator which normally has a temperature coefficient of about 1ppm/°C. The remainder of the circuit implements the temperature correction. The LM134 senses ambient temperature, converting it to a current which flows through the 30.1k resistor. This resistor's voltage is subtracted from a reference potential by A1. The stable subtraction voltage is derived from the LT1073's 212mV reference via Q2 and the 73.2k to 27.4k resistors. Feedback from Q2's collector to the LT1073's auxiliary amplifier closes the reference loop, which also powers the Colpitts oscillator. The 47µF capacitor frequency compensates the loop.

A1's output controls the remaining portion of the LT1073, which is configured as a voltage step-up switching regulator. L1's high voltage inductive events are rectified and stored in the 47µF output capacitor, resulting in a stepped-up DC potential. This potential is fed back to A1, closing a control loop. Because A1 is biased by the temperature sensitive LM134, the loop's output varies with ambient temperature in a controlled manner. Q3's drop forces the step-up converter to always run, regardless of the loop's required output voltage. This permits smooth and continuous varactor bias from 0V to 3.9V over a 0°C to 70°C

Figure 20. 1.5V Powered Temperature Compensated Crystal Oscillator

ambient operating environment. This output is applied to the varactor diode in the oscillator circuit. The varactor's capacitance, a function of its DC bias, thus varies with ambient temperature. This change in capacitance shifts the crystal's resonant frequency, opposing temperature induced crystal drift. For the values given in the circuit and the crystal cut specified, residual oscillator drift is only 0.05ppm/°C. This compares favorably with 1ppm/°C drift with no compensation used. The circuit functions from 1.7V down to 1.1V with no specification degradation. Current drain is only 230µA. Applications include portable high accuracy clocks, survival radios, and secure communications.

90µA Precision Voltage-to-Frequency Converter

Figure 21 is a micropower voltage-to-frequency converter. A 0V to 5V input produces a 0kHz to 10kHz output with a linearity of 0.05%. Gain drift is 80ppm/°C. Maximum current consumption is only 90µA, almost 30 times lower than currently available V-F converters. To understand circuit operation, assume C1's positive input is slightly below its negative input (C2's output is low). The input voltage causes a positive going ramp at C1's positive input (trace A, Figure 22). C1's output is low, biasing the CMOS inverter output high. This allows current to flow from Q1's emitter, through the inverter supply pin to the 100pF capacitor. The
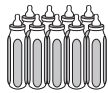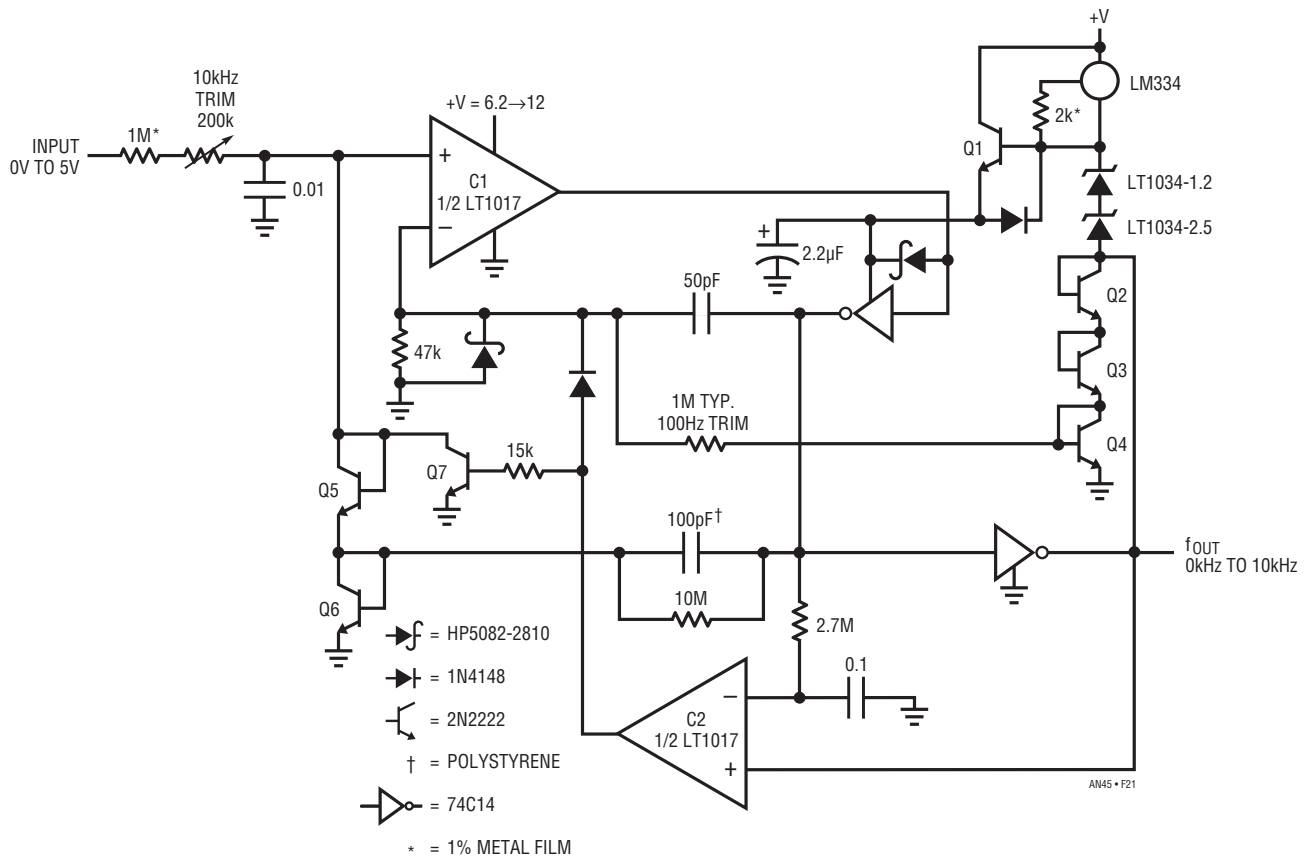
Figure 21. V-to-F Converter Achieves 0.05% Linearity While Requiring Only 90µA Supply Current

2.2µF capacitor provides high frequency bypass, maintaining low impedance at Q1's emitter. Diode connected Q6 provides a path to ground. The 100pF unit charges to a voltage that is a function of Q1's emitter potential and Q6's drop. When the ramp at C1's positive input goes high enough, C1's output goes high (trace B) and the inverter switches low (trace C). The Schottky clamp prevents CMOS inverter input overdrive. This action pulls current from C1's positive input capacitor via the Q5-100pF route (trace D). This current removal resets C1's positive input ramp to a potential slightly below ground, forcing C1's output to go low. The 50pF capacitor furnishes AC positive feedback, ensuring that C1's output remains positive long enough for a complete discharge of the 100pF capacitor. The Schottky diode prevents C1's input from being driven outside its negative common mode limit. When the 50pF unit's feedback decays, C1 again switches low and the entire cycle repeats. The oscillation frequency depends directly on the input voltage derived current.
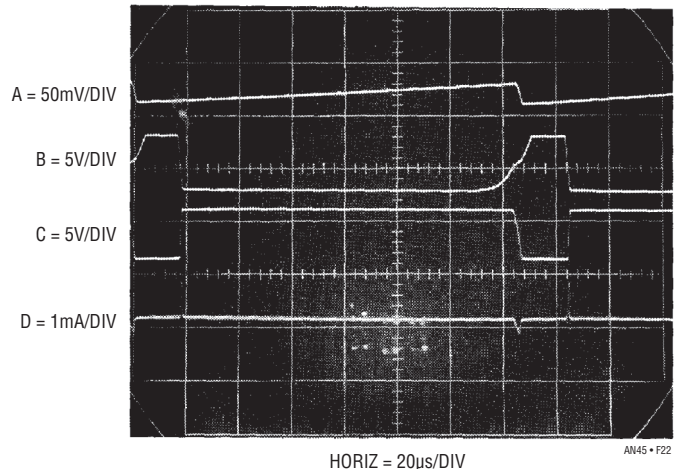

Figure 22. Micropower V-to-F Converter's Waveforms

Q1's emitter voltage must be carefully controlled to get low drive. Q3 and Q4 temperature compensate Q5 and Q6 while Q2 compensates Q1's V_{BE}. The two LT1034s are the actual voltage reference and the LM334 current source provides 35μA bias to the stack. The current drive provides excellent supply immunity (better than 40ppm/V) and also aids circuit temperature coefficient. It does this by utilizing the LM334's 0.3%/°C temperature coefficient to slightly temperature modulate the voltage drop in the Q2-Q4 trio. This correction's sign and magnitude directly oppose that of the –120ppm/°C, 100pF polystyrene capacitor, aiding overall circuit stability.

The Q1 emitter-follower efficiently delivers charge to the 100pF capacitor. Both base and collector current end up in the capacitor. The CMOS inverter provides low loss SPDT reference switching without significant drive losses. The 100pF capacitor draws only small transient currents during its charge and discharge cycles. The 50pF-47k positive feedback combination draws insignificantly small switching currents. Figure 23, a plot of supply current versus operating frequency, reflects the low power design. At zero frequency, the LT1017's quiescent current and the 35μA reference stack bias account for all current drain. There are no other paths for loss. As frequency scales up, the charge/discharge cycle of the 100pF capacitor introduces the 1.5μA/kHz increase shown.
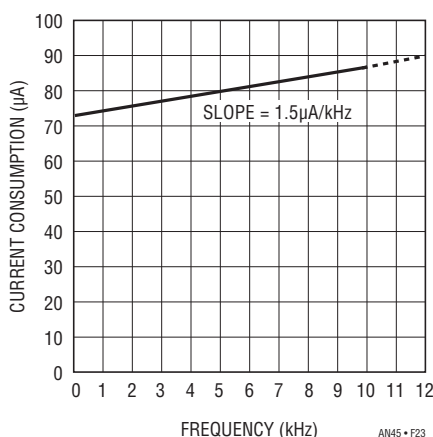
Figure 23. Current Consumption vs Frequency for the V-to-F Converter

Circuit start-up or overdrive can cause the circuit's AC-coupled feedback to latch. If this occurs, C1's output goes high. C2, detecting this via the inverter and the 2.7M-0.1μF lag, also goes high. This lifts C1's negative input and grounds the positive input with Q7, initiating normal circuit action.

Because the charge pump is directly coupled to C1's output, response is fast. The output settles within one cycle for a fast input step. To calibrate this circuit, apply 50mV and select the value at C1's input for a 100Hz output. Then, apply 5V and trim the input potentiometer for a 10kHz output.

Bipolar (AC) Input V-F Converter

No currently available V-F converter will accept bipolar (AC) inputs. This feature is desirable in power line monitoring and other applications. Figure 24's V-F converter accepts ±10V inputs, producing a 0kHz to 10kHz output. Linearity is 0.04%, and temperature coefficient measures about 50ppm/°C. To understand circuit operation, assume a bipolar square wave (trace A, Figure 25) is applied to the input. During the input's positive phase, A1's output (trace B) swings negative, driving current through C1 via the full wave diode bridge. A1's current causes C1 to ramp linearly. Instrumentation amplifier A2, operating at a gain of 10, looks differentially across C1. A2's output (trace C) biases comparator A3's negative input. When A2's output crosses zero, A3 fires (trace D). AC positive feedback to A3's positive input (trace E) "hangs up" A3's output for about 20μs. The Q1 level shifter drives ground referred inverters I_1 and I_2 to deliver biphase drive (traces G and H) to the LTC201 switch. The LTC201, set up as a charge pump, places C2 across C1 each time the inverters switch, resetting C1 to a lower voltage. The LT1004 reference, along with C2's value, determines how much charge is removed from C1 each time the charge pump cycles. Thus, each time A2's output tries to cross zero, C2 is switched across C1, resetting it to a small negative voltage and forcing A1 to begin recharging it. The frequency of this oscillatory behavior is directly proportional to the input derived current into A1. During the time C1 is ramping toward zero the LTC201 switches C2 across the LT1004, preparing it for the next discharge cycle. The action is the same for negative input excursions (see Figure 25), except that A1's output phasing is reversed. A2, looking differentially across A1's diode bridge, sees the same signal as for positive inputs and circuit action is identical. A4, detecting A1's output polarity, provides a sign bit output (trace F).
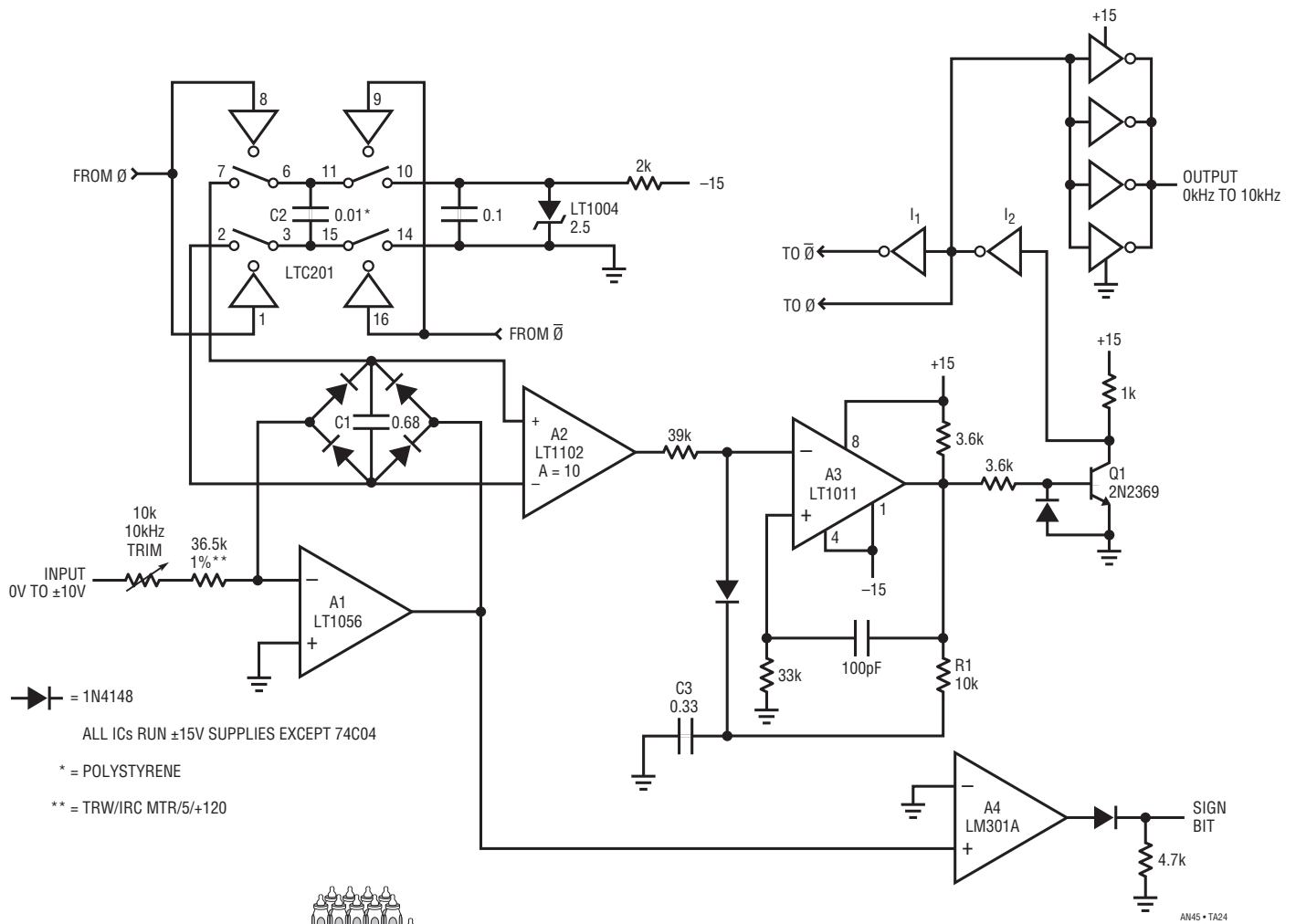
Figure 24. Bipolar (AC) Input V-to-F Converter

A = 20V/DIV

B = 1V/DIV

C = 0.5V/DIV

D = 100V/DIV
E = 50V/DIV
F = 50V/DIV
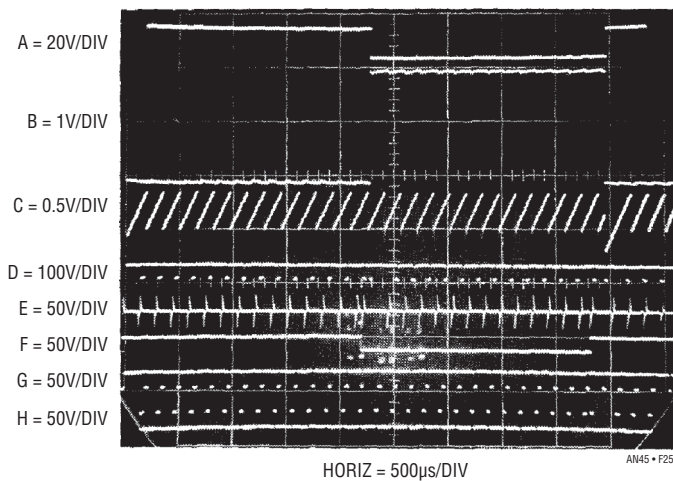G = 50V/DIV
H = 50V/DIV

HORIZ = 500µs/DIV

AN45 • F25

Figure 25. Waveforms for the Bipolar Input V-to-F Converter

Figure 26, an amplitude expanded version of A1 and A2's outputs, shows detail. Trace A is the input, while trace B and trace C are A1 and A2's outputs, respectively. Complementary bias points and ramping action are clearly visible in A1's output, while A2 responds identically for both input phases. A1's output bias points are established by the two conducting bridge diodes. When the input switches polarity, A1 responds immediately and oscillation frequency settles within 1 to 2 cycles of final value.

Start-up or overdrive conditions could cause this loop to latch. A start-up mechanism, adapted from oscilloscope trigger circuitry, precludes latch-up.[2] If C1 charges past the point where C2 can reset it, loop closure ceases. A2's

Note 2: See References 5 and 6.

output saturates positive, causing A3 to go negative. A3's prolonged negative state, detected by the R1-C3 filter, pulls its negative input toward –15V. When A3's negative input crosses zero, its output changes state and charges R1-C3 positively. A3's input rises above zero, causing output reversal and free-running oscillation commences. As in normal mode, the 100pF-33k RC aids transitions. A3's oscillations are transmitted to the LTC201 based charge pump via A1 and the inverters. C2 pumps charge out of C1, driving the voltage across it toward zero. A2 comes out of positive saturation and heads negative, eliminating

A = 50V/DIV

B = 0.5V/DIV

C = 0.2V/DIV

HORIZ = 500µs/DIV

AN45 • F26

Figure 26. Detail of Integrator and Differential Amplifier Outputs

positive bias at A3's input. A3's free-running oscillation stops, and normal loop action begins.

To calibrate this circuit apply either a –10V or a +10V input and set the 10kΩ trimmer for exactly 10kHz output. The low offsets of A1 and A2 permit operation down to a few hertz with no zero trim required.

1.5V Powered, 350ps Rise Time Pulse Generator

Verifying the rise time limit of wideband test equipment setups is a difficult task. In particular, the "end-to-end" rise time of oscilloscope-probe combinations is often required to assure measurement integrity. Conceptually, a pulse generator with rise times substantially faster than the oscilloscope-probe combination can provide this information. Figure 27's circuit does this, providing a 1ns pulse with rise and fall times inside 350ps. Pulse amplitude is 10V with a 50Ω source impedance. This circuit, built into a small box and powered by a 1.5V battery, provides a simple, convenient way to verify the rise time capability of almost any oscilloscope-probe combination.

The LT1073 switching regulator and associated components supply the necessary high voltage. The LT1073 forms a flyback voltage boost regulator. Further voltage step-up is obtained from a diode-capacitor voltage doubler network. L1 periodically receives charge, and its flyback discharge
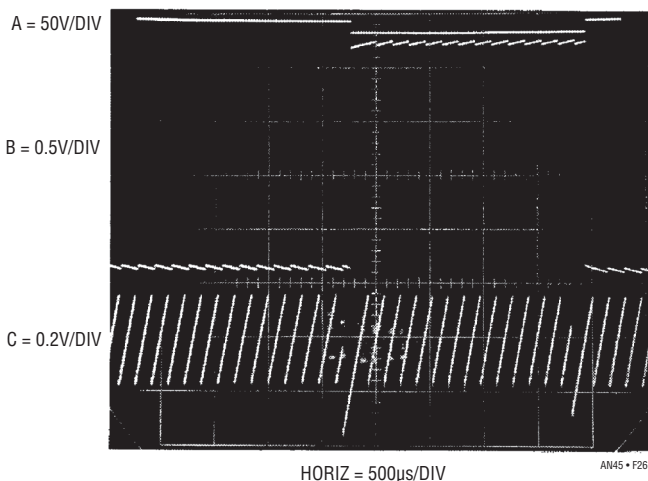

Figure 27. 350ps Rise Time Pulse Generator

L1 = TOKO #262-LYF-0095K

 = MUR120

SELECT Q1 AND 2pF VALUE — SEE TEXT

AN45 • F27
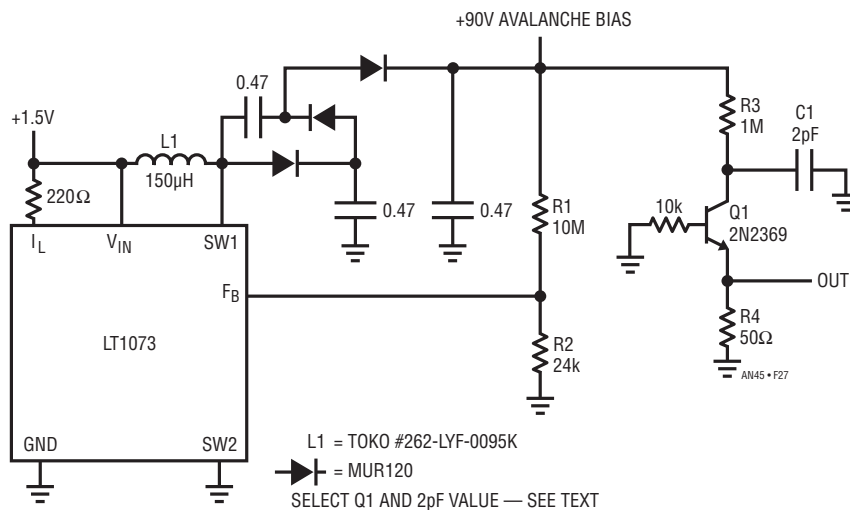
delivers high voltage events to the doubler network. A portion of the doubler network's DC output is fed back to the LT1073 via the R1, R2 divider, closing a control loop.

The regulator's 90V output is applied to Q1 via the R3-C1 combination. Q1, a 40V breakdown device, non-destructively avalanches when C1 charges high enough.[3] The result is a quickly rising, very fast pulse across R4. C1 discharges, Q1's collector voltage falls and breakdown ceases. C1 then recharges until breakdown again occurs. This action causes free-running oscillation at about 200kHz. Figure 28 shows the output pulse. A 1GHz sampling oscilloscope (Tektronix 556 with 1S1 sampling plug-in) measures the pulse at 10V high with about a 1ns base. Rise time is 350ps, with fall time also indicating 350ps. The figures may actually be faster, as the 1S1 is specified with a 350ps rise time limit.[4]

VERT = 2V/DIV

HORIZ = 200ps/DIV

AN45 • F28
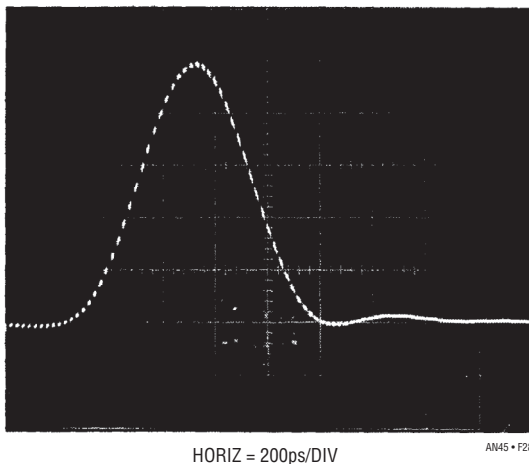
Figure 28. Avalanche Pulse Generator Output Pulse. Waveform Has 350ps Rise and Fall Times. Slightly Under Damped Turn-Off Is Probably Due to Test Fixture Limitations

Q1 may require selection to get avalanche behavior. Such behavior, while characteristic of the device specified, is not guaranteed by the manufacturer. A sample of 50 Motorola 2N2369s, spread over a 12 year date code span, yielded 82%. All "good" devices switched in less than 600ps. C1 is selected for a 10V amplitude output. Value spread is typically 2pF to 4pF. Ground plane type construction with high speed layout techniques are essential for good results from this circuit. Current drain from the 1.5V battery version is about 5mA.

Note 3: See References 7.
Note 4: I'm sorry, but 1GHz is the fastest scope in my house.
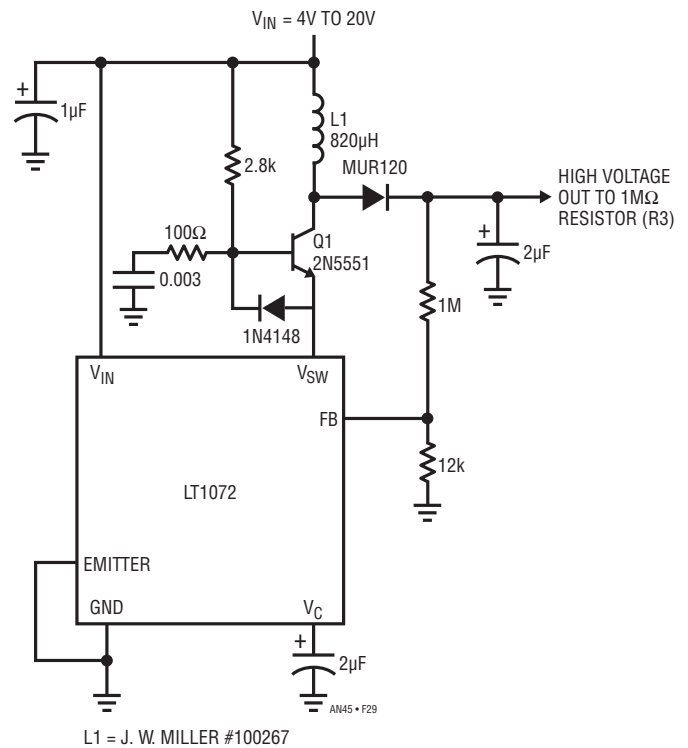
Figure 29. Alternate 90V DC-DC Converter

For those applications which must run from higher voltage inputs, Figure 29 is included. This circuit, which operates from inputs of 4V to 20V, will also power the avalanche stage. Cascoded high voltage transistor Q1 combines with the LT1072 switching regulator to form a high voltage switched mode control loop. The LT1072 pulse width modulates Q1 at its 40kHz clock rate. L1's inductive events are rectified and stored in the 2µF output capacitor. The 1MΩ to 12kΩ divider provides feedback to the LT1072. The diode and RC at Q1's base damp inductor related parasitic behavior. The circuit's output drives the avalanche stage in similar fashion to the LT1073 based circuit.

A Simple Ultralow Dropout Regulator

Switching regulator post regulators, battery-powered apparatus, and other applications frequently require low dropout linear regulators. Often, battery life is significantly affected by the regulator's dropout performance. Figure 30's simple circuit offers lower dropout voltage than any monolithic regulator. Dropout is below 50mV at 1A, increasing to only 450mA at 5A. Line and load regulation are within 5mV, and initial output accuracy is inside 1%.

Additionally, the regulator is fully short-circuit protected, and has a no load quiescent current of 600µA.

Circuit operation is straightforward. The 3-pin LT1123 regulator (TO-92 package) servo controls Q1's base to maintain its feedback pin (FB) at 5V. The 10µF output capacitor provides frequency compensation. If the circuit is located more than six inches from the input source, the optional 10µF capacitor should bypass the input. The optional 20Ω resistor limits LT1123 power dissipation and is selected based upon the maximum expected input voltage (see Figure 31).
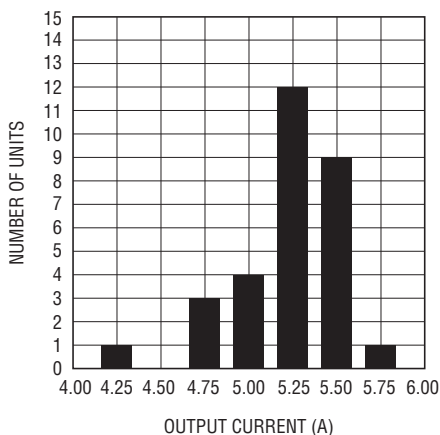
Normally, configurations of this type offer unpredictable short-circuit protection. Here, the MJE1123 transistor shown has been specially designed for use with the LT1123. Because of this, beta based current limiting is practical. Excessive output current causes the LT1123 to pull down harder on Q1 until beta limiting occurs. Under these conditions the controlled pull-down current combines with Q1's beta and safe operating area characteristics to provide reliable short-circuit limiting. Figure 32 details current limit characteristics for 30 randomly selected transistors.
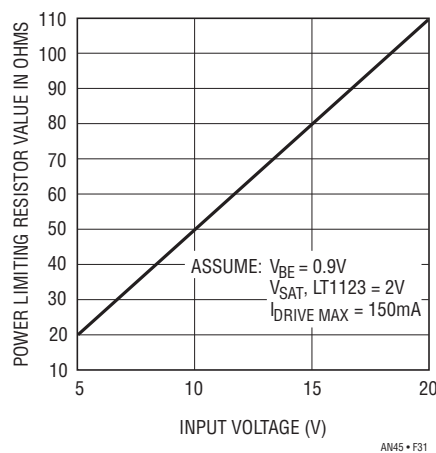
Figure 33 shows dropout characteristics. Even at 5A, dropout is about 450mV, decreasing to only 50mV at 1A. Monolithic regulators cannot approach these figures, primarily because monolithic power transistors do not offer Q1's combination of high beta and excellent saturation. For
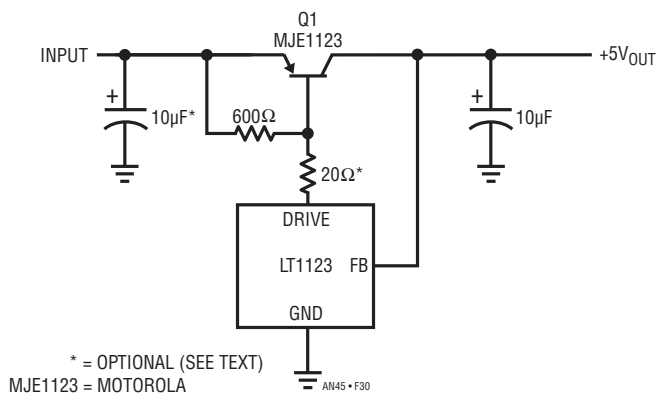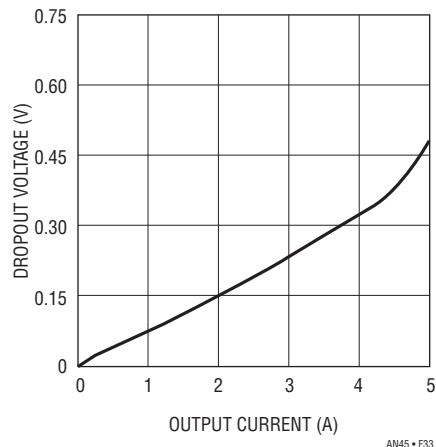

Figure 30. The Ultralow Dropout Regulator. LT1123 Combines with Specially Designed Transistor for Low Dropout and Short-Circuit Protection
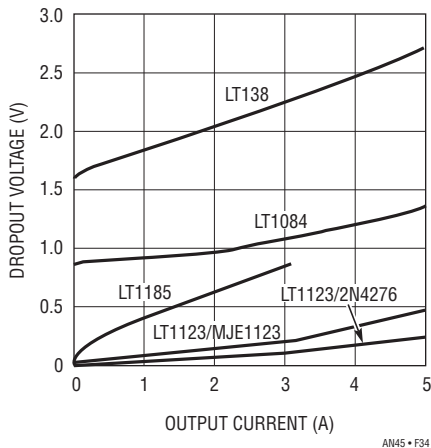

Figure 31. LT1123 Power Dissipation Limiting Resistor Value vs Input Voltage

Figure 32. Short Circuit Current for 30 Randomly Selected MJE1123 Transistors at V_{IN} = 7V


Figure 33. Dropout Voltage vs Output Current

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Figure 34. Dropout Voltage vs Output Current for Various Regulators

comparison, Figure 34 compares the circuit's performance against some popular monolithic regulators. Dropout is 10 times better than 138 types, and significantly better than the other types shown. Because of Q1's high beta, base drive loss is only 1% to 2% of output current, even at full 5A output. This maintains high efficiency under the low $V_{IN} - V_{OUT}$ conditions the circuit will typically operate at. As an exercise, the MJE1123 was replaced with a 2N4276, a Germanium device. This combination provided even lower dropout performance, although current limit characteristics cannot be guaranteed.

Figure 35 shows a simple way to add shutdown to the regulator. A CMOS inverter or gate biases Q2 to control LT1123 bias. When Q2's base is driven, the loop functions normally. With Q2 unbiased, the circuit goes into shutdown and pulls no current.
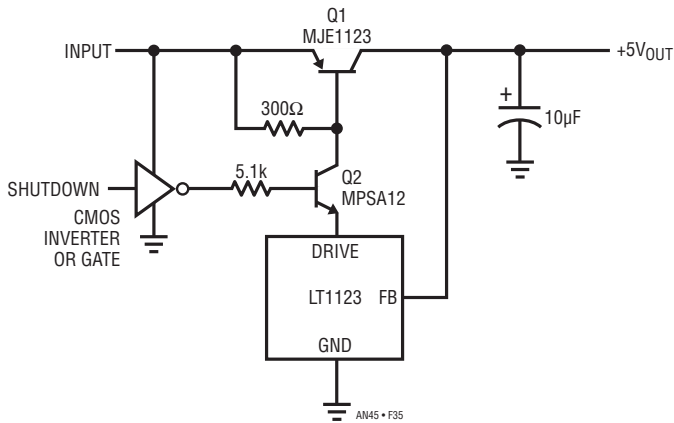

Figure 35. Shutdown for the Low Dropout Regulator

Cold Cathode Fluorescent Lamp Power Supply

Current generation portable computers utilize back-lit LCD displays. Cold Cathode Fluorescent Lamps (CCFL) provide the highest available efficiency for back lighting the display. These lamps require high voltage AC to operate, mandating an efficient, high voltage DC/AC converter. In addition to good efficiency, the converter should deliver the lamp drive in the form of a sine wave. This is desirable to minimize RF emissions. Such emissions can cause interference with other devices, as well as degrading overall operating efficiency.

Figure 36 meets these requirements. Efficiency is 78%, with an input voltage range of 4.5V to 20V. 82% efficiency is possible if the LT1072 is driven from a low voltage (e.g., 3V to 5V) source. Additionally, lamp intensity is continuously and smoothly variable from zero to full intensity.
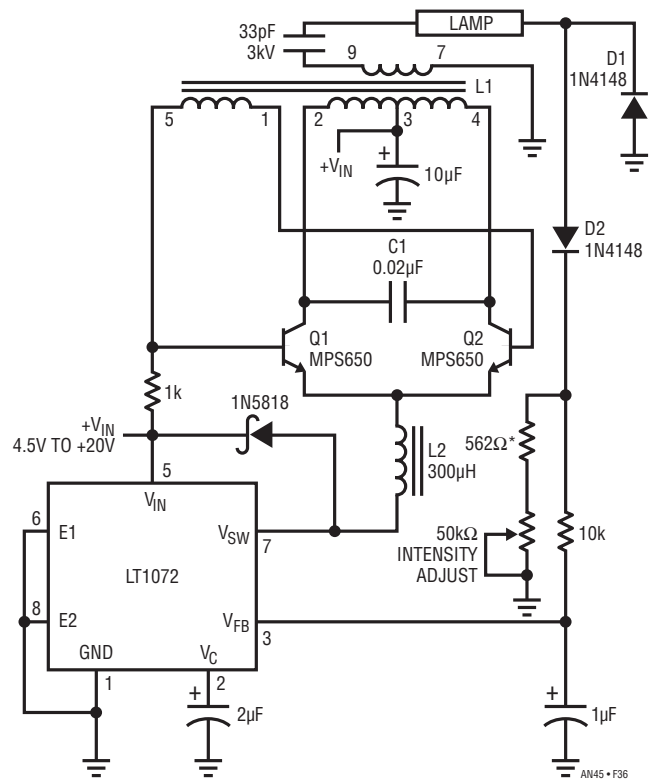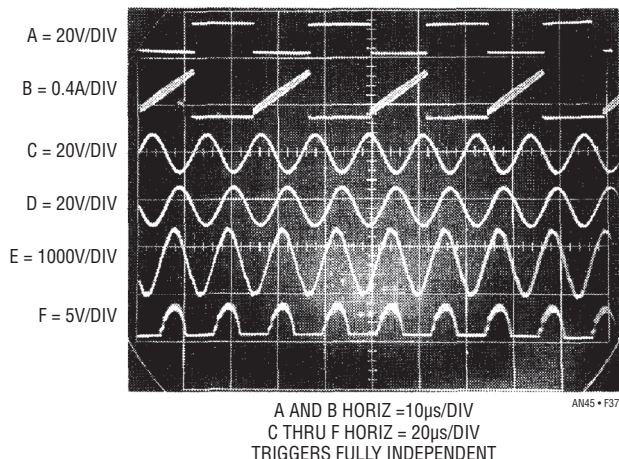

C1 = MUST BE A LOW LOSS CAPACITOR.
METALIZED POLYCARB
WIMA FKP2 (GERMAN) RECOMMENDED.
L1 = SUMIDA-6345-020 OR COILTRONICS-CTX110092-1.
PIN NUMBERS SHOWN FOR COILTRONICS UNIT
L2 = COILTRONICS-CTX300-4
 * = 1% FILM RESISTOR
DO NOT SUBSTITUTE COMPONENTS
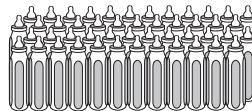
Figure 36. Cold Cathode Fluorescent Lamp Power Supply

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When power is applied the LT1072 switching regulator's feedback pin is below the devices internal 1.23V reference, causing full duty cycle modulation at the V_{SW} pin (trace A, Figure 37). L2 conducts current (trace B), which flows

A = 20V/DIV
B = 0.4A/DIV
C = 20V/DIV
D = 20V/DIV
E = 1000V/DIV
F = 5V/DIV

A AND B HORIZ =10µs/DIV
C THRU F HORIZ = 20µs/DIV
TRIGGERS FULLY INDEPENDENT

AN45 • F37

Figure 37. Waveforms for the Cold Cathode Fluorescent Lamp Power Supply. Note Independent Triggering on Traces A and B and C Through F.

from L1's center tap, through the transistors, into L2. L2's current is deposited in switched fashion to ground by the regulator's action.

L1 and the transistors comprise a current driven Royer class converter[5] which oscillates at a frequency primarily set by L1's characteristics and the 0.02µF capacitor. LT1072 driven L2 sets the magnitude of the Q1-Q2 tail current, and hence L1's drive level. The 1N5818 diode maintains L2's current flow when the LT1072 is off. The LT1072's 40kHz clock rate is asynchronous from the Royer converters (≈60kHz) rate, accounting for trace B's waveform thickening.

The 0.02µF capacitor combines with L1's characteristics to produce sine wave voltage drive at the Q1 and Q2 collectors (traces C and D, respectively). L1 furnishes voltage step-up, and about $1400V_{P-P}$ appears at its secondary (trace E). Current flows through the 33pF capacitor into

the lamp. On negative waveform cycles the lamp's current is steered to ground via D1. Positive waveform cycles are directed, via D2, to the ground referred 562Ω-50k potentiometer chain. The positive half-sine appearing across these resistors (trace F) represents 1/2 the lamp current. This signal is filtered by the 10k-1µF pair and presented to the LT1072's feedback pin. This connection closes a control loop which regulates lamp current. The 2µF capacitor at the LT1072's V_C pin provides stable loop compensation. The loop forces the LT1072 to switch-mode modulate L2's average current to whatever value is required to maintain a constant current in the lamp. The constant current's value, and hence lamp intensity, may be varied with the potentiometer. The constant current drive allows full 0% to 100% intensity control with no lamp dead zones or "pop-on" at low intensities. Additionally, lamp life is enhanced because current cannot increase as the lamp ages.

Several points should be kept in mind when observing this circuit's operation. L1's high voltage secondary can only be monitored with a wideband, high voltage probe fully specified for this type of measurement. *The vast majority of oscilloscope probes will break down and fail if used for this measurement.*[6] Tektronix probe type P-6009 (acceptable) or types P6013A and P6015 (preferred) probes must be used to read L1's output.

Another consideration involves observing waveforms. The LT1072's switching frequency is completely asynchronous from the Q1-Q2 Royer converter's switching. As such, most oscilloscopes cannot simultaneously trigger and display all the circuit's waveforms. Figure 37 was obtained using a dual beam oscilloscope (Tektronix 556). LT1072 related traces A and B are triggered on one beam, while the remaining traces are triggered on the other beam. Single beam instruments with alternate sweep and trigger switching (e.g., Tektronix 547) can also be used, but are less versatile and restricted to four traces.

Note 5: See References 8.
Note 6: Don't say we didn't warn you!

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