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High Speed Amplifier Techniques

A Designer's Companion for Wideband Circuitry

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PREFACE

This publication represents the largest LTC commitment to an application note to date. No other application note absorbed as much effort, took so long or cost so much. This level of activity is justified by our belief that high speed monolithic amplifiers greatly interest users.

Historically, monolithic amplifiers have represented packets of inexpensive, precise and controllable gain. They have partially freed engineers from the constraints and frustrations of device level design. Monolithic operational amplifiers have been the key to practical implementation of high level analog functions. As good as they are, one missing element in these devices has been speed.

Devices presently coming to market are addressing monolithic amplifiers' lack of speed. They bring with them the ease of use and inherent flexibility of op amps. When Philbrick Researches introduced the first mass produced op amp in the 1950's (K2-W) they knew it would be used. What they couldn't possibly know was just how widely, and how many different types of applications there were. As good a deal as the K2-W was (I paid $24.00 for mine - or rather, my father did), monolithic devices are far better. The combination of ease of use, economy, precision and versatility makes modern op amps just too good to be believed.

Considering all this, adding speed to op amps' attractions seems almost certain to open up new application areas. We intend to supply useful high speed products and the level of support necessary for their successful application (such high minded community spirit is, of course, capitalism's deputy). We hope you are pleased with our initial efforts and look forward to working together.

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INTRODUCTION

Most monolithic amplifiers have been relatively slow devices. Wideband operation has been the province of discrete and hybrid technologies. Some fast monolithic amplifiers have been available, but the exotic and expensive processing required has inflated costs, precluding widespread acceptance. Additionally, many of the previous monolithic designs were incapable of high precision and prone to oscillation or untoward dynamics, making them unattractive.

Recent processing and design advances have made inexpensive, precision wideband amplifiers practical. Figure 1 lists some amplifiers, along with a summary of their characteristics. Reviewing this information reveals extraordinarily wideband devices, with surprisingly good DC characteristics. All of these amplifiers utilize standard op amp architecture, except the LT1223 and LT1228, which are so-called current mode feedback types (see Appendix H, "About Current Mode Feedback"). It is clear that the raw speed capabilities of these devices, combined with their inherent flexibility as op amps, permit a wide range of applications. What is required of the user is a familiarity with the devices and respect for the requirements of high speed circuitry.

This effort's initial sections are devoted to familiarizing the reader with the realities and difficulties of high speed circuit work. The mechanics and subtleties of achieving precision circuit operation at DC and low frequency have been well documented. Relatively little has appeared which discusses, in practical terms, how to get fast circuitry to work. In developing such circuits, even veteran designers sometimes feel that nature is conspiring against them. In some measure this is true. Like all engineering endeavors, high speed circuits can only work if negotiated compromises with nature are arranged. Ignorance of, or contempt for, physical law is a direct route to frustration. Mother Nature laughs at dilettantism and crushes arrogance without even knowing she did it. Even without Einstein's revelations, the world of high speed is full of surprises. Working with events measured in nanoseconds requires the greatest caution, prudence and respect for Mother Nature. Absolutely nothing should be taken for granted, because nothing is. Circuit design is very much the art of compromise with parasitic effects. The "hidden schematic" (this descriptive was originated by Charly Gullett of Intel Corporation) usually dominates the circuit's form, particularly at high speed.

In this regard, much of the text and appendices are directed at developing awareness of, and respect for, circuit parasitics and fundamental limitations. This approach is maintained in the applications section, where the notion of negotiated compromises is expressed in terms of resistor values and compensation techniques. Many of the application circuits use the amplifier's speed to improve on a standard circuit. Some utilize the speed to implement a traditional function in a non-traditional way, with attendant advantages. A (very) few operate at or near the state-of-the-art for a given circuit type, regardless of approach. Substantial effort has been expended in developing these examples and documenting their operation. The resultant level of detail is justified in the hope that it will be catalytic. The circuits should stimulate new ideas to suit particular needs, while demonstrating fast amplifiers' capabilities in an instructive manner.

PERSPECTIVES ON HIGH SPEED DESIGN

A substantial amount of design effort has made Figure 1's amplifiers relatively easy to use. They are less prone to oscillation and other vagaries than some much slower amplifiers. Unfortunately, laws of physics dictate that the circuit's *environment* must be properly prepared. The performance limits of high speed circuitry are often determined by parasitics such as stray capacitance, ground impedance and layout. Some of these considerations are present in digital systems where designers are comfortable describing bit patterns, delays and memory access times in terms of nanoseconds. Figure 2's test circuit provides valuable perspective on just how fast these amplifiers are. Here, the pulse generator (Trace A, Figure 3) drives a 74S04 Schottky TTL inverter (Trace B), an LT1223 op amp connected as an inverter (Trace C), and a 74HC04 high speed CMOS inverter (Trace D). The LT1223 doesn't fare too badly. Its delay and fall times are about 2ns slower than the 74S04, but significantly faster than the 74HC04. In fact, the LT1223 has completely finished its transition before the 74HC04 even begins to move! Linear circuits operating with this kind of speed make many engineers justifiably wary. Nanosecond domain linear circuits are widely associated with oscillations, mysterious shifts in

					LT1193	LT1194					
PARAMETER	**LT1122**	**LT1190**	**LT1191**	**LT1192**	**DIFFERENTIAL**	**DIFFERENTIAL**	**LT1220**	**LT1221**	**LT1222**	**LT1223**	**LT1224**
Slew Rate	60V/µs	450V/µs	450V/µs	450V/µs	450V/µs	450V/µs	250V/µs	250V/µs	200V/µs	1000V/µs	300V/µs
Bandwidth	14MHz	50MHz	90MHz	400MHz	70MHz	70MHz	45MHz	150MHz	350MHz	100MHz	45MHz
Delay-Rise Time	15ns-65ns	4ns-7ns	3.5ns-1.6ns	5ns-7ns	4ns-7ns	4ns-7ns	4ns-4ns	5ns-5ns	5ns-5ns	3.5ns-3.5ns	4ns-4ns
Settling Time	340ns-0.01%	100ns-0.1%	100ns-0.1%	80ns-0.1%	100ns-0.1%	100ns-0.1%	90ns-0.1%	90ns-0.1%	90ns-0.1%	75ns-0.1%	90ns-0.1%
Output Current	6mA	50mA	50mA	50mA	50mA	50mA	24mA	24mA	24mA	50mA	40mA
Offset	600µV	4mV	2mV	2mV	3mV	3mV	2mV	1mV	1mV	3mV	1mV
Drift	6µV/°C						20µV/°C	15µV/°C	10µV/°C		20µV/°C
Bias Current	75pA	500nA	500nA	500nA	500nA	500nA	300nA	300nA	300nA	3µA	6µA
Gain	500,000	22,000	45,000	200,000	Adjustable	10	20,000	50,000	100,000	90dB	80dB
Gain Error (Minimum Gain)				A_{VMIN} = 10	0.1%	0.1%		A_{VMIN} = 4	A_{VMIN} = 10		A_{VMIN} = 1
Gain Drift											
Power Supply	40V	$18V_{MAX}$	$18V_{MAX}$	$18V_{MAX}$	$18V_{MAX}$	$18V_{MAX}$	36V	36V	36V	$36V_{MAX}$	36V

Figure 1. Characteristics of Some Different Fast IC Amplifiers

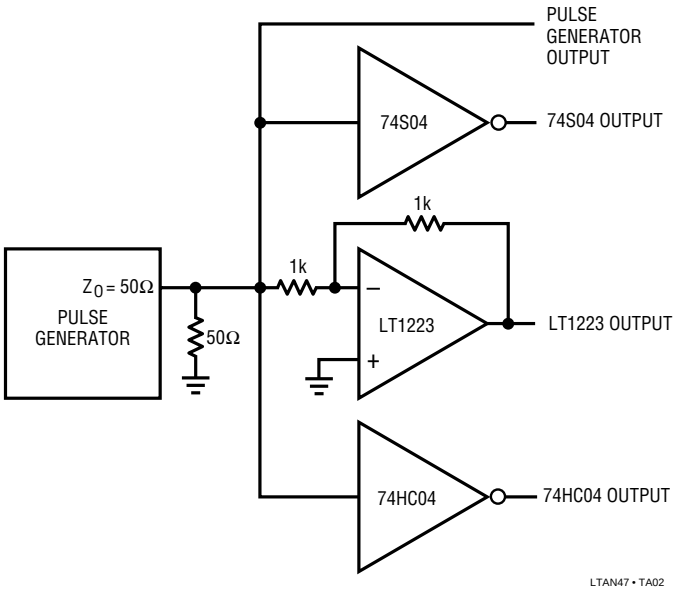


Figure 2. A Race Between the LT1223 Amplifier and Some Fast Logic Inverters

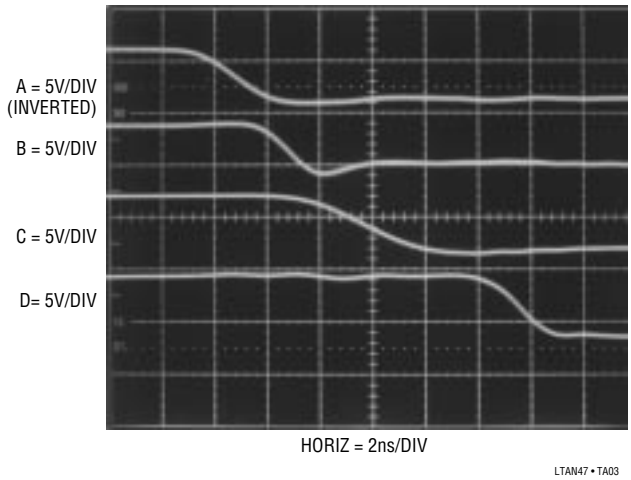


Figure 3. The Amplifier (Trace C) is 3ns Slower than 74S Logic (Trace B), but 5ns Faster than High Speed HCMOS (Trace D)!

circuit characteristics, unintended modes of operation and outright failure to function.

Other common problems include different measurement results using various pieces of test equipment, inability to make measurement connections to the circuit without inducing spurious responses, and dissimilar operation between two identical circuits. If the components used in the circuit are good and the design is sound, all of the above problems can usually be traced to failure to provide a proper circuit environment. To learn how to do this requires studying the causes of the aforementioned difficulties.

The following segments, "Mr. Murphy's Gallery of High Speed Amplifier Problems" and the "Tutorial Section", address this. The "Problems" section alerts the reader to trouble areas, while the "Tutorial" highlights theory and techniques which may be applied towards solving the problems shown. The tutorials are arranged in roughly the same order as the problems are presented.

MR. MURPHY'S GALLERY OF HIGH SPEED AMPLIFIER PROBLEMS

It sometimes seems that Murphy's Law dominates all physical law. For a complete treatise on Murphy's Law, see Appendix J, "The Contributions of Edsel Murphy to the Understanding of the Behavior of Inanimate Objects", by D.L. Klipstein. The law's consequences weigh heavily in high speed design. As such, a number of examples are given in the following discussion. The average number of phone calls we receive per month due to each "Murphy" example appears at the end of each figure caption.

Problems can start even before power is applied to the amplifier. Figure 4 shows severe ringing on the pulse edges at the output of an unterminated pulse generator cable. This is due to reflections and may be eliminated by terminating the cable. *Always terminate the source in its characteristic impedance when looking into cable or long PC traces. Any path over 1 inch long is suspect.*

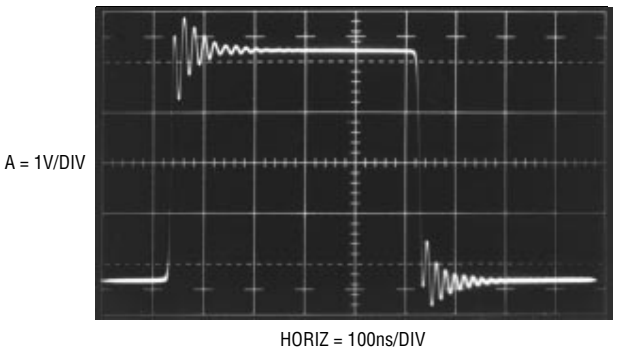


Figure 4. An Unterminated Pulse Generator Cable Produces Ringing Due to Reflections – 3

In Figure 5 the cable is terminated, but ripple and aberration are still noticeable following the high speed edge transitions. In this instance the terminating resistor's leads are lengthy (≈3/4"), preventing a high integrity wideband termination.

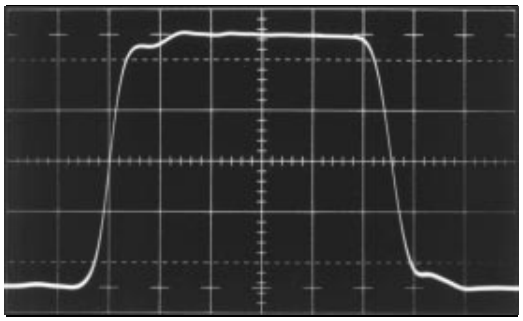


Figure 5. Poor Quality Termination Results in Pulse Corner Aberrations – 1

The best termination for 50Ω cable is the BNC coaxial type. These devices should not simply be resistors in an enclosure. Good grade 50Ω terminators maintain true coaxial form. They use a carefully designed 50Ω resistor with significant effort devoted to connections to the actual resistive element. In particular, the largest possible connection surface area is utilized to minimize high speed losses. While these type terminators are practical on the test bench, they are rarely used as board level components. In general, the best termination resistors for PC board use are carbon or metal film types with the shortest possible lead lengths. These resistor's end-cap connections provide better high speed characteristics than the rod-connected composition types. Wirewound resistors, because of their inherent and pronounced inductive characteristics, are completely unsuitable for high speed work. This includes so-called non-inductive types.

Another termination consideration is disposal of the current flowing through the terminator. The terminating resistor's grounded end should be placed so that the high speed currents flowing from it do not disrupt circuit operation. For example, it would be unwise to return terminator current to ground near the grounded positive input of an inverting op amp. The high speed, high density (5V pulses through a 50Ω termination generates 100mA current spikes) current flow could cause serious corruption of the desired zero volt op amp reference. This is another reason why, for bench testing, the coaxial BNC terminators are far preferable to discrete, breadboard mounted resistors. With BNC types in use the termination current returns directly to the source generator and never flows in the breadboard. (For more information see the Tutorial section.) *Select terminations carefully and evaluate the effects of their placement in the test set-up.*

Figure 6 shows an amplifier output which rings and distorts badly after rapid movement. In this case, the probe ground lead is too long. For general purpose work, most probes come with ground leads about 6 inches long. At low frequencies this is fine. At high speed, the long ground lead looks inductive, causing the ringing shown. High quality probes are always supplied with some short ground straps to deal with this problem. Some come with very short spring clips which fix directly to the probe tip to facilitate a low impedance ground connection. For fast work, the ground connection to the probe should not exceed 1 inch in length. (Probes are covered in the Tutorial section; also see Appendix A, "ABC's of Probes", guest written by the engineering staff of Tektronix, Inc.). *Keep the probe ground connection as short as possible. The ideal probe ground connection is purely coaxial. This is why probes mated directly to board mounted coaxial connectors give the best results.*

In Figure 7 the probe is properly grounded, but a new problem pops up. This photo shows an amplifier output

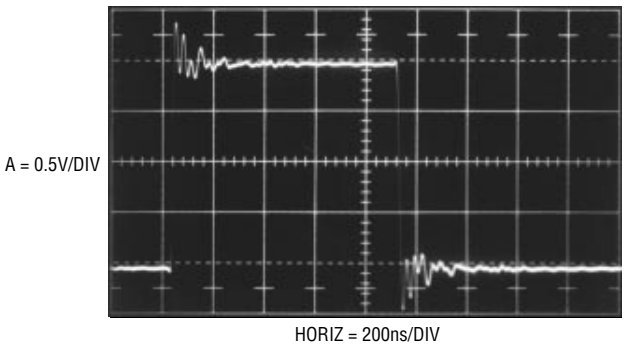


Figure 6. Poor Probe Grounding Badly Corrupts the Observed Waveform – 53

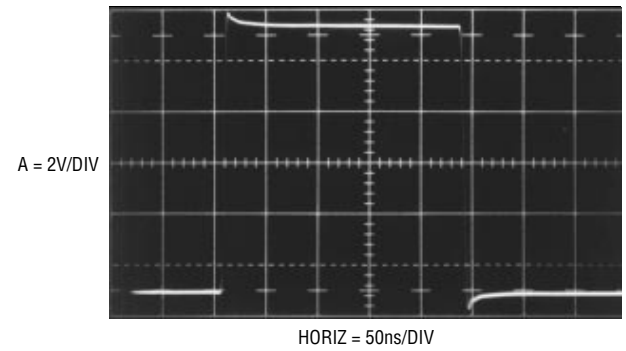


Figure 7. Improper Probe Compensation Causes Seemingly Unexplainable Amplitude Error – 12

excursion of 11V — quite a trick from an amplifier running from ±5V rails. This is a commonly reported problem in high speed circuits and can be quite confusing. It is not due to suspension of natural law, but is traceable to a grossly miscompensated or improperly selected oscilloscope probe. *Use probes which match your oscilloscope's input characteristics and compensate them properly.* (For discussions on probes, see Appendix A, "ABC's of Probes", guest written by the engineering staff of Tektronix, Inc. and the Tutorial section.) Figure 8 shows another probe-induced problem. Here the amplitude seems correct but the amplifier appears slow with pronounced edge rounding. In this case, the probe used is too heavily compensated or slow for the oscilloscope. Never use 1X or straight probes. Their bandwidth is 20MHz or less and capacitive loading is high. *Check probe bandwidth to ensure it is adequate for the measurement. Similarly, use an oscilloscope with adequate bandwidth.*

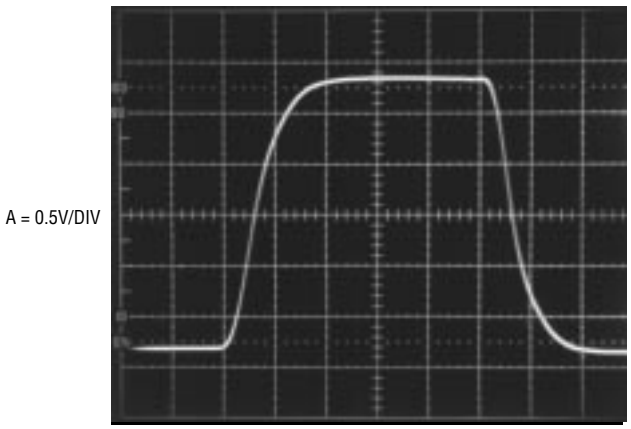


Figure 8. Overcompensated or Slow Probes Make Edges Look Too Slow – 2

Mismatched probes account for the apparent excessive amplifier delay in Figure 9. Delay of almost 12ns (Trace A is the input, Trace B the output) is displayed for an amplifier specified at 6ns. Always keep in mind that various types of probes have different signal transit delay times. At high sweep speeds, this effect shows up in multi-trace displays as time skewing between individual channels. Using similar probes will eliminate this problem, but measurement requirements often dictate dissimilar probes. In such cases the differential delay should be measured and then mentally factored in to reduce error when interpreting the display. It is worth noting that active probes,

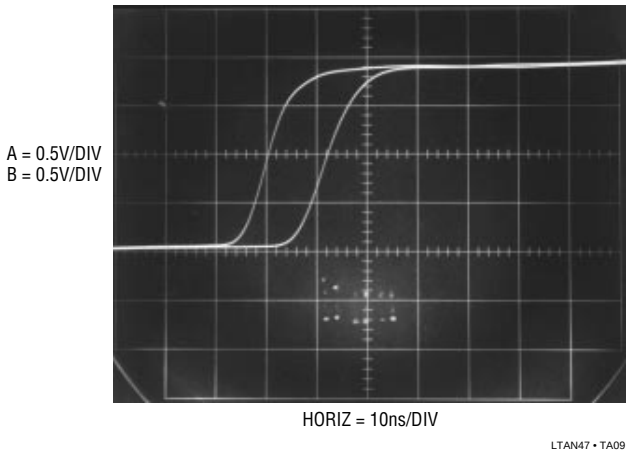


Figure 9. Probes with Mismatched Delays Produce Apparent Time Skewing in the Display – 4

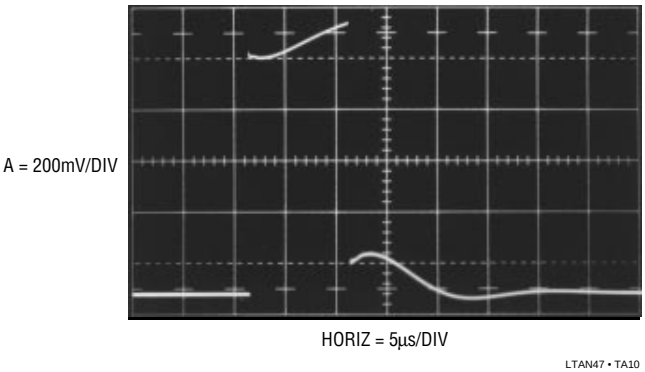


Figure 10. Overdriven FET Probe Produces Excessive Waveform Distortion and Tailing. Saturation Effects can Also Cause Delayed Response – 1

such as FET and current probes, have signal transit times as long as 25ns. A fast 10X or 50Ω probe delay can be inside 3ns. *Account for probe delays in interpreting oscilloscope displays.*

The difficulty shown in Figure 10 is a wildly distorted amplifier output. The output slews quickly, but the pulse top and bottom recoveries have lengthy, tailing responses. Additionally, the amplifier output seems to clip well below its nominal rated output swing. A common oversight is responsible for these conditions. A FET probe monitors the amplifier output in this example. The probe's common-mode input range has been exceeded, causing it to overload, clip and distort badly. When the pulse rises, the probe is driven deeply into saturation, forcing internal circuitry away from normal operating points. Under these conditions the displayed pulse top is illegitimate. When the output falls, the probe's overload recovery is lengthy and uneven, causing the tailing. More subtle forms of FET

probe overdrive may show up as extended delays with no obvious signal distortion. *Know your FET probe. Account for the delay of its active circuitry. Avoid saturation effects due to common-mode input limitations (typically ±1V). Use 10X and 100X attenuator heads when required.*

Figure 11's probe-caused problem results in amplifier output peaking and ringing. In other respects the display is acceptable. This output peaking characteristic is caused by a second 10X probe connected to the amplifier's summing junction. Because the summing point is so central to analyzing op amp operation, it is often monitored. At high speed the 10pF probe input capacitance causes a significant lag in feedback action, forcing the amplifier to overshoot and hunt as it seeks the null point. Minimizing this effect calls for the lowest possible probe input capacitance, mandating FET types or special passive probes. (Probes are covered in the Tutorial section; also see Appendix A, "ABC's of Probes", guest written by the engineering staff of Tektronix, Inc.). *Account for the effects of probe capacitance, which often dominates its impedance characteristics at high speeds. A standard 10pF 10X probe forms a 10ns lag with a 1KΩ source resistance.*

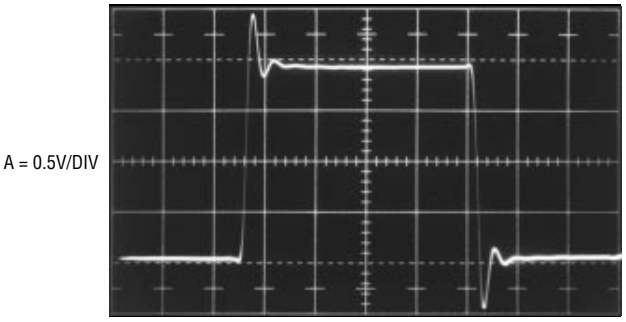


Figure 11. Effect of a 10X, 10pF 'Scope Probe at the Summing Point – 2

A peaked, tailing response is Figure 12's characteristic. The photo shows the final 40mV of a 2.5V amplifier excursion. Instead of a sharp corner which settles cleanly, peaking occurs, followed by a lengthy tailing decay. This waveform was recorded with an inexpensive off-brand 10X probe. Such probes are often poorly designed, and constructed from materials inappropriate for high speed work. The selection and integration of materials for wideband probes is a specialized and difficult art. Substantial design effort is required to get good fidelity at high speeds. *Never use probes unless they are fully specified for wideband operation. Obtain probes from a vendor you trust.*

Figure 13 shows the final movements of an amplifier output excursion. At only 1mV per division the objective is to view the settling residue to high resolution. This response is characterized by multiple time constants, nonlinear slew recovery and tailing. Note also the high speed event just before the waveform begins its negative going transition. What is actually being seen is the oscilloscope recovering from excessive overdrive. Any observation that requires off-screen positioning of parts of the waveform should be approached with the greatest caution. Oscilloscopes vary widely in their response to overdrive, bringing displayed results into question. Complete treatment of high resolution settling time measurements and oscilloscope overload characteristics is given in the Tutorial section, "About Oscilloscopes" and Appendix B "Measuring Amplifier Settling Time". *Approach all oscilloscope*

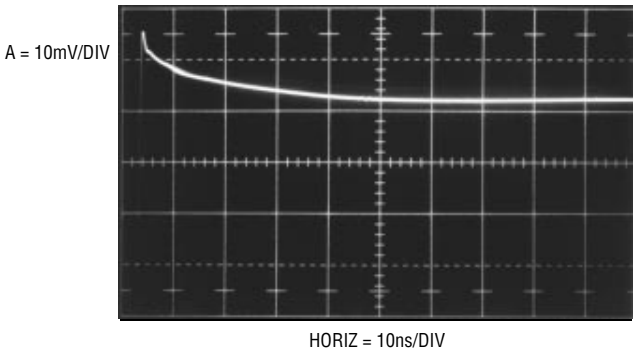


Figure 12. Poor Quality 10X Probe Introduces Tailing – 2

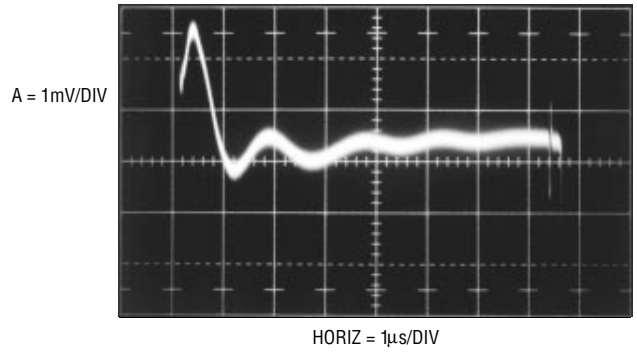


Figure 13. Overdriven Oscilloscope Display Says More About the Oscilloscope than the Circuit it's Connected to – 6

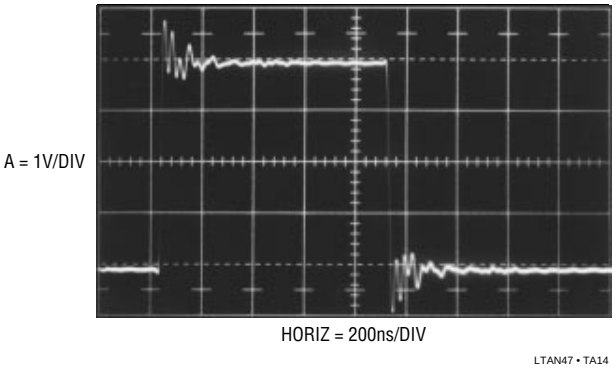


Figure 14. Instabilities Due to No Ground Plane Produce a Display Similar to a Poorly Grounded Probe – 62

measurements which require off-screen activity with caution. Know your instrument's capabilities and limitations.

Sharp eyed readers will observe that Figure 14 is a duplicate of Figure 6. Such lazy authorship is excusable because almost precisely the same waveform results when no ground plane is in use. A ground plane is formed by using a continuous conductive plane over the surface of the circuit board. (The theory behind ground planes is discussed in the Tutorial section). The only breaks in this plane are for the circuit's necessary current paths. The ground plane serves two functions. Because it is flat (AC currents travel along the surface of a conductor) and covers the entire area of the board, it provides a way to access a low inductance ground from anywhere on the board. Also, it minimizes the effects of stray capacitance in the circuit by referring them to ground. This breaks up potential unintended and harmful feedback paths. *Always use a ground plane with high speed circuitry.*

By far the most common error involves power supply bypassing. Bypassing is necessary to maintain low supply impedance. DC resistance and inductance in supply wires and PC traces can quickly build up to unacceptable levels. This allows the supply line to move as internal current levels of the devices connected to it change. This will almost always cause unruly operation. In addition, several devices connected to an unbypassed supply can "communicate" through the finite supply impedances, causing erratic modes. Bypass capacitors furnish a simple way to eliminate this problem by providing a local reservoir of energy at the device. The bypass capacitor acts as an electrical flywheel to keep supply impedance low at high frequencies. The choice of what type of capacitors to use for bypassing is a critical issue and should be approached carefully (see Tutorial, "About Bypass Capacitors"). An unbypassed amplifier with a 100Ω load is shown in Figure 15. The power supply the amplifier sees at its terminals has high impedance at high frequency. This impedance forms a voltage divider with the amplifier and its load, allowing the supply to move as internal conditions in the comparator change. This causes local feedback and oscillation occurs. *Always use bypass capacitors.*

In Figure 16 the 100Ω load is removed, and a pulse output is displayed. The unbypassed amplifier responds surprisingly well, but overshoot and ringing dominate. *Always use bypass capacitors.*

Figure 17's settling is noticeably better, but some ringing remains. This response is typical of lossy bypass capacitors, or good ones placed too far away from the amplifier. *Use good quality, low loss bypass capacitors, and place them as close to the amplifier as possible.*

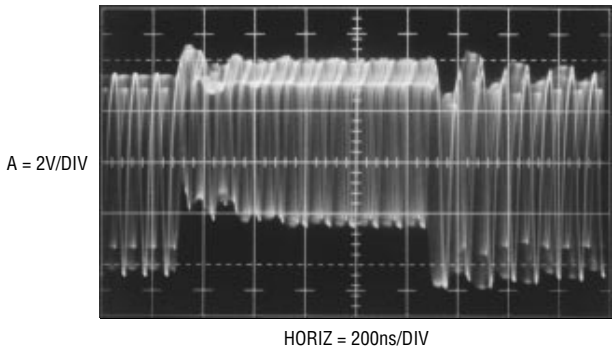


Figure 15. Output of an Unbypassed Amplifier Driving a 100Ω Load Without Bypass Capacitors – 58

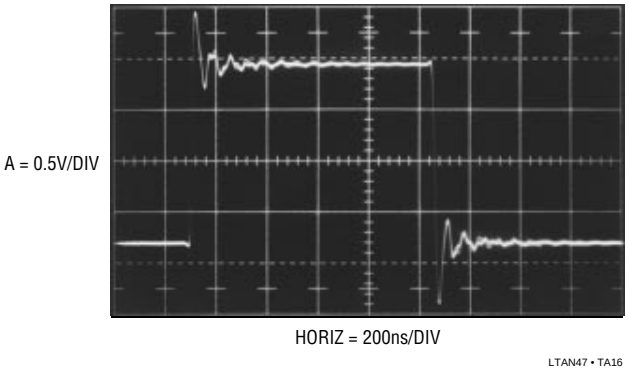


Figure 16. An Unbypassed Amplifier Driving No Load is Surprisingly Stable…at the Moment – 49

The multiple time constant ringing in Figure 18 often indicates poor grade paralleled bypassing capacitors or excessive trace length between the capacitors. While paralleling capacitors of different characteristics is a good way to get wideband bypassing, it should be carefully considered. Resonant interaction between the capacitors can cause a waveform like this after a step.

This type response is often aggravated by heavy amplifier loading. *When paralleling bypass capacitors, plan the layout and breadboard with the units you plan to use in production.*

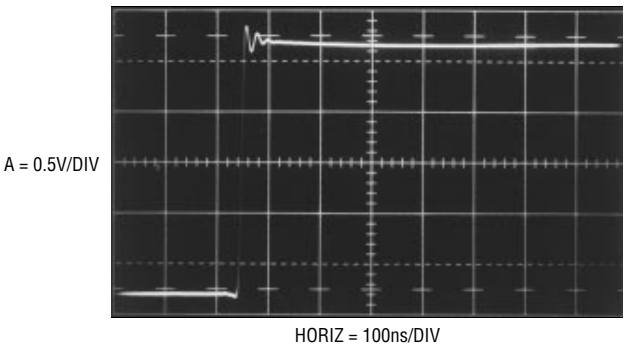


Figure 17. Poor Quality Bypass Capacitor Allows Some Ringing – 28

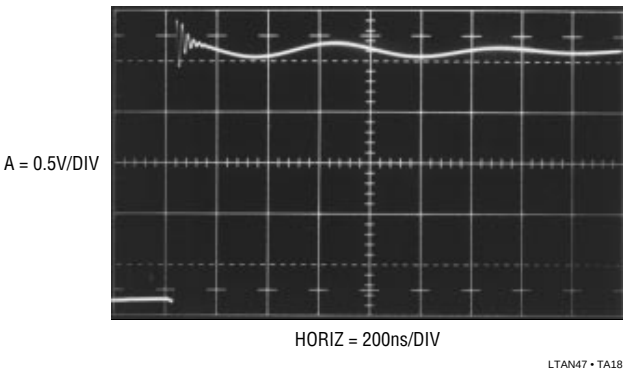


Figure 18. Paralleled Bypass Capacitors Form a Resonant Network and Ring – 2

Figure 19 addresses a more subtle bypassing problem. The trace shows the last 40mV excursion of a 5V step almost settling cleanly in 300ns. The slight overshoot is due to a loaded (500Ω) amplifier without quite enough bypassing. Increasing the total supply bypassing from 0.1µF to 1µF cured this problem. *Use large value paralleled bypass capacitors when very fast settling is required, particularly if the amplifier is heavily loaded or sees fast load steps.*

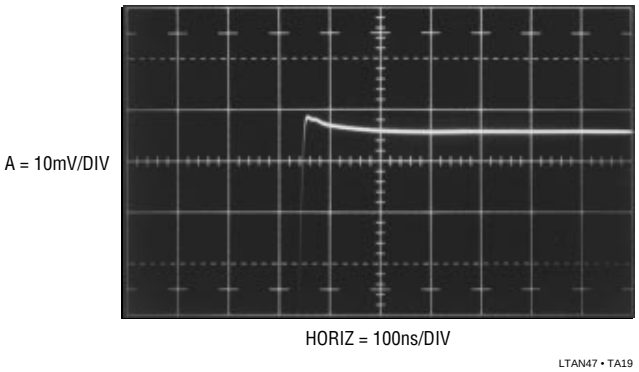


Figure 19. A More Subtle Bypassing Problem. Not-Quite-Good-Enough Bypassing Causes a Few Millivolts of Peaking – 1

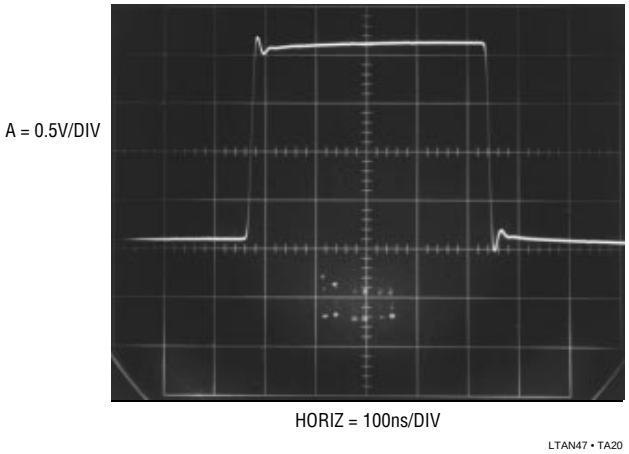


Figure 20. 2pF Stray Capacitance at the Summing Point Introduces Peaking – 4

The problem shown in Figure 20, peaking on the leading and trailing corners, is typical of poor layout practice (see Tutorial section on “Breadboarding Techniques”). This unity gain inverter suffers from excessive trace area at the summing point. Only 2pF of stray capacitance caused the peaking and ring shown. *Minimize trace area and stray capacitance at critical nodes. Consider layout as an integral part of the circuit and plan it accordingly.*

Figure 21’s low level square wave output appears to suffer from some form of parasitic oscillation. In actuality, the disturbance is typical of that caused by fast digital clocking or switching regulator originated noise getting into critical circuit nodes. *Plan for parasitic radiative or conductive paths and eliminate them with appropriate layout and shielding.*

Figure 22 underscores the previous statement. This output was taken from a gain-of-ten inverter with 1kΩ input

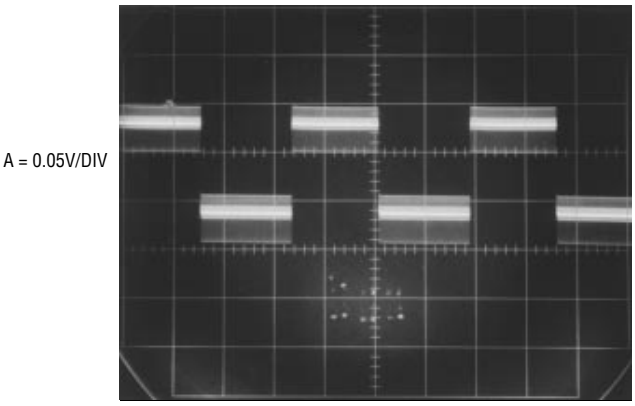


Figure 21. Clock or Switching Regulator Noise Corrupts Output Due to Poor Layout – 3

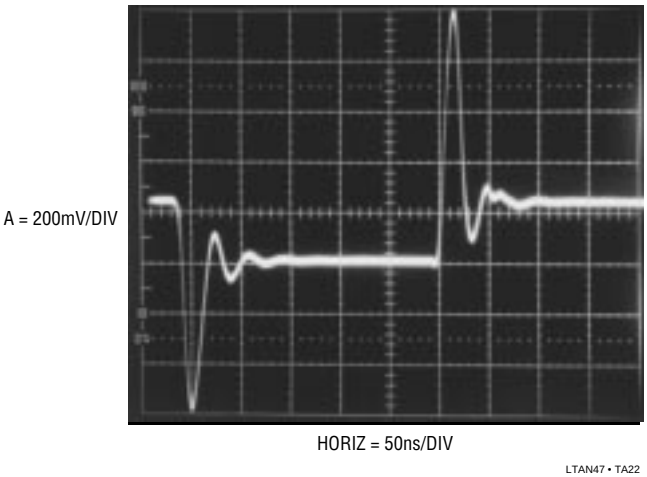


Figure 22. Output of an X10 Amplifier with 1pF Coupling from the Summing Point to the Input. Careful Shielding of the Input Resistor Will Eliminate the Peaked Edges and Ringing – 2

resistance. It shows severe peaking induced by *only 1pF* of parasitic capacitance across the 1k resistor. The 50Ω terminated input source provides only 20mV of drive via a divider, but that's more than enough to cause problems, even with only 1pF stray coupling. In this case the solution was a ground referred shield at a right angle to, and encircling, the 1kΩ resistor. *Plan for parasitic radiative paths and eliminate them with appropriate shielding.*

A decompensated amplifier running at too low a gain produced Figure 23's trace. The price for decompensated amplifiers' increased speed is restrictions on minimum allowable gain. Decompensated amplifiers are simply not stable below some (specified) minimum gain, and no amount of ignorance or wishing will change this. This is a common applications oversight with these devices, although the amplifier never fails to remind the user. *Observe gain restrictions when using decompensated amplifiers.*

Oscillation is also the problem in Figure 24, and it is due to excessive capacitive loading (see Tutorial section on "Oscillation"). Capacitive loading to ground introduces lag in the feedback signal's return to the input. If enough lag is introduced (e.g., a large capacitive load) the amplifier may oscillate. Even if a capacitively loaded amplifier doesn't oscillate, it's always a good idea to check its response with step testing. It's amazing how close to the edge of the cliff you can get without falling off, except when you build 10,000 production units. *Avoid capacitive loading. If such loading is necessary, check performance margins and isolate or buffer the load if necessary.*

Figure 25 appears to contain one cycle of oscillation. The output waveform initially responds, but abruptly reverses direction, overshoots and then heads positive again. Some

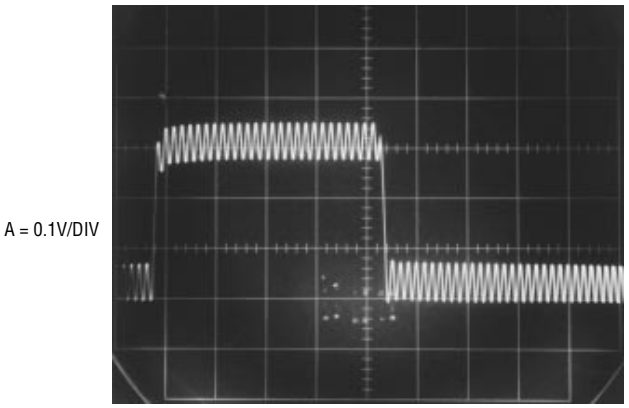


Figure 23. Decompensated Amplifier Running at Too Low a Gain – 22

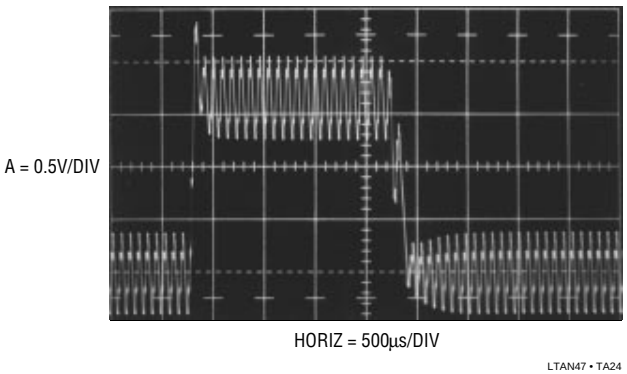


Figure 24. Excessive Capacitive Load Upsets the Amplifier – 165

overshoot again occurs, with a long tail and a small dip well before a non-linear slew returns the waveform to zero. Ugly overshoot and tailing completes the cycle. This is certainly strange behavior. What is going on here? The input pulse is responsible for all these anomalies. Its amplitude takes the amplifier outside its common-mode limits, inducing the bizarre effects shown. *Keep inputs inside specified common-mode limits at all times.*

Figure 26 shows an oscillation laden output (Trace B) trying to unity gain invert the input (Trace A). The input's form is distinguishable in the output, but corrupted with very high frequency oscillation and overshoot. In this case the amplifier includes a booster within its loop to provide increased output current. The disturbances noted are traceable to local instabilities within the booster circuit. (See Appendix C, "The Oscillation Problem — Frequency Compensation Without Tears"). *When using output booster stages, insure they are inherently stable before placing them inside an amplifier's feedback loop. Wideband booster stages are particularly prone to device level parasitic high frequency oscillation.*

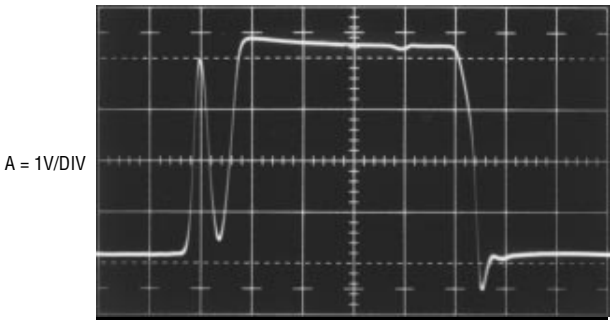


Figure 25. Input Common Mode Overdrive Generates Odd Outputs – 3

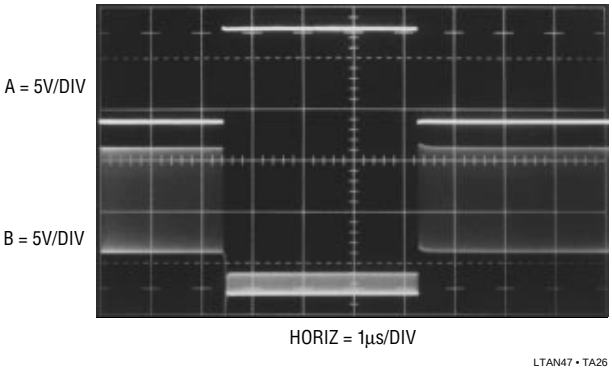


Figure 26. Local Oscillations in a Booster Stage. Frequency is Typically High – 12

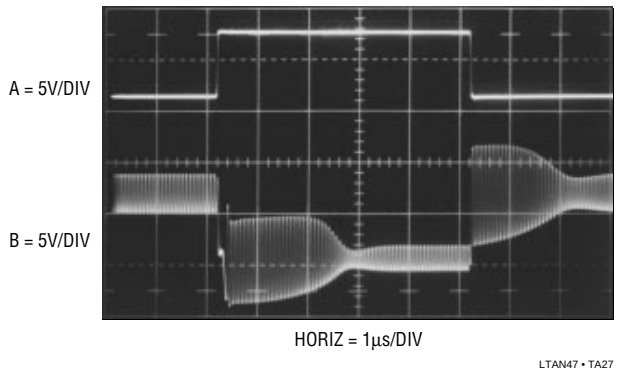


Figure 27. Loop Oscillations in a Booster Stage. Note Lower Frequency than Local Oscillations in Previous Example – 28

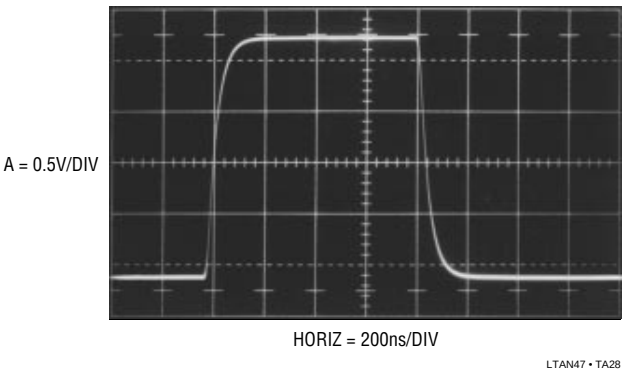


Figure 28. Excessive Source Impedance Gives Serene But Undesired Response – 6

Figure 27's booster augmented unity gain inverting op amp also oscillates, but at a much lower frequency. Additionally, overshoot and non-linear recovery dominate the waveform's envelope. Unlike the previous example, this behavior is not due to local oscillations within the booster stage. Instead, the booster is simply too slow to be included in the op amp's feedback loop. It introduces enough lag to force oscillation, even as it hopelessly tries to maintain loop closure. *Insure booster stages are fast enough to maintain stability when placed in the amplifier's feedback loop.*

The serene rise and fall of Figure 28's pulse is a welcome relief from the oscillatory screaming of the previous photos. Unfortunately, such tranquilized behavior is simply too slow. This waveform, reminiscent of Figure 8's bandlimited response, is due to excessive source impedance. The high source impedance combines with amplifier input capacitance to band limit the input and the output reflects this action. *Minimize source impedance to levels*

which maintain desired bandwidth. Keep stray capacitance at inputs down.

TUTORIAL SECTION

An implied responsibility in raising the aforementioned issues is their solution or elimination. What good is all the rabble-rousing without suggestions for fixes? It is in this spirit that this tutorial section is presented. Theory, techniques, prejudice and just plain gossip are offered as tools which may help avoid or deal with difficulties. As previously mentioned, the tutorials appear in roughly the same order as the problems were presented.

About Cables, Connectors and Terminations

Routing of high speed signals to and from the circuit board should always be done with good quality coaxial cable. The cable should be driven and terminated in the system's characteristic impedance at the drive and load points. The driven end is usually an instrument (e.g., pulse or signal generator), presumably endowed with proper characteristics by its manufacturer. It is the cable and its termination, selected by the experimenter, that often cause problems.

All coaxial cable is not the same. Use cable appropriate to the system's characteristic impedance and of good quality. Poorly chosen cable materials or construction methods can introduce odd effects at very high speeds, resulting in observed waveform distortion. A poor cable choice can adversely effect 0.01% settling in the 100ns-200ns region. Similarly, poor cable can preclude maintenance of even the cleanest pulse generator's 1ns rise time or purity. Typically, inappropriate cable can introduce tailing, rise time degradation, aberrations following transitions, nonlinear impedance and other undesirable characteristics.

Termination choice is equally important. Good quality BNC coaxial type terminators are usually the best choice for breadboarding. Their impedance vs frequency is flat into the GHz range. Additionally, their construction insures that the (often substantial) drive current returns directly to the source, instead of being dumped into the breadboard's ground system. As previously discussed, BNC coaxial terminators are not simply resistors in a can. Special construction techniques insure optimum wideband response. Figures 29 and 30 demonstrate this nicely. In Figure 29 a 1ns pulse with 350ps rise and fall times[1] is monitored on a 1GHz sampling 'scope (Tektronix 556 with 1S1 sampling plug-in and P6032 probe). The waveform is clean, with only a slight hint of ring after the falling edge. This photo was taken with a high grade BNC coaxial type terminator in use. Figure 30 does not share these attributes. Here, the generator is terminated with a 50Ω carbon composition resistor with lead lengths of about 1/8 inch. The waveform rings and tails badly on turn-off before finally settling. Note that the sweep speed required a 2.5X reduction to capture these unwanted events.

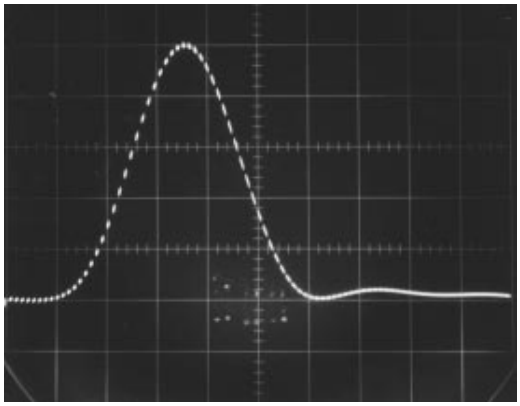


Figure 29. 350ps Rise and Fall Times are Preserved by a Good Quality Termination

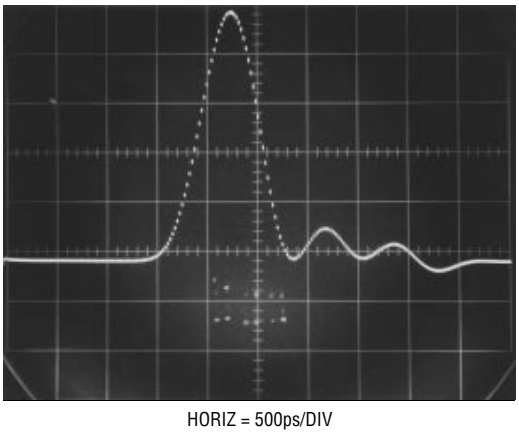


Figure 30. Poor Grade Termination Produces Pronounced Ringing and Tailing in the GHz Range

Note 1: The ability to generate such a pulse proves useful for a variety of tasks, including testing terminators, cables, probes and oscilloscopes for response. The requirements for this pulse generator are surprisingly convenient and inexpensive. For a discussion and construction details see Appendix D "Measuring Probe - Oscilloscope Response".

Connectors, such as BNC barrel extensions and tee-type adaptors, are convenient and frequently employed. Remember that these devices represent a discontinuity in the cable, and can introduce small but undesirable effects. In general it is best to employ them as close as possible to a terminated point in the system. Use in the middle of a cable run provides minimal absorption of their mismatch and reflections. The worst offenders among connectors are adapters. This is unfortunate, as these devices are necessitated by the lack of connection standardization in wideband instrumentation. The mismatch caused by a BNC-to-GR874 adaptor transition at the input of a wideband sampling 'scope is small, but clearly discernible in the display. Similarly, mismatches in almost all adaptors, and even in "identical" adaptors of different manufacture, are readily measured on a high-frequency network analyzer such as the Hewlett-Packard 4195A[2] (for additional wisdom and terror along these lines see Reference 1).

BNC connections are easily the most common, but not necessarily the most desirable, wideband connection mechanism. The ingenious GR874 connector has notably superior high frequency characteristics, as does the type N. Unfortunately, it's a BNC world out there.

About Probes and Probing Techniques

The choice of which oscilloscope probe to use in a measurement is absolutely crucial. The probe must be considered as an inherent part of the circuit under test. Rise time, bandwidth, resistive and capacitive loading, delay and other limitations must be kept in mind.

Sometimes, the best probe is no probe at all. In some circumstances it is possible and preferable to connect critical breadboard points *directly* to the oscilloscope (see Figure 31). This arrangement provides the highest possible grounding integrity, eliminates probe attenuation, and maintains bandwidth. In most cases this is mechanically inconvenient, and often the oscilloscope's electrical characteristics (particularly input capacitance) will not permit it. This is why oscilloscope probes were developed, and why so much effort has been put into their development (Reference 42 is excellent). In addition to the material presented here, an in-depth treatment of probes appears in Appendix A, "ABC's of Probes", guest written by the engineering staff of Tektronix, Inc.

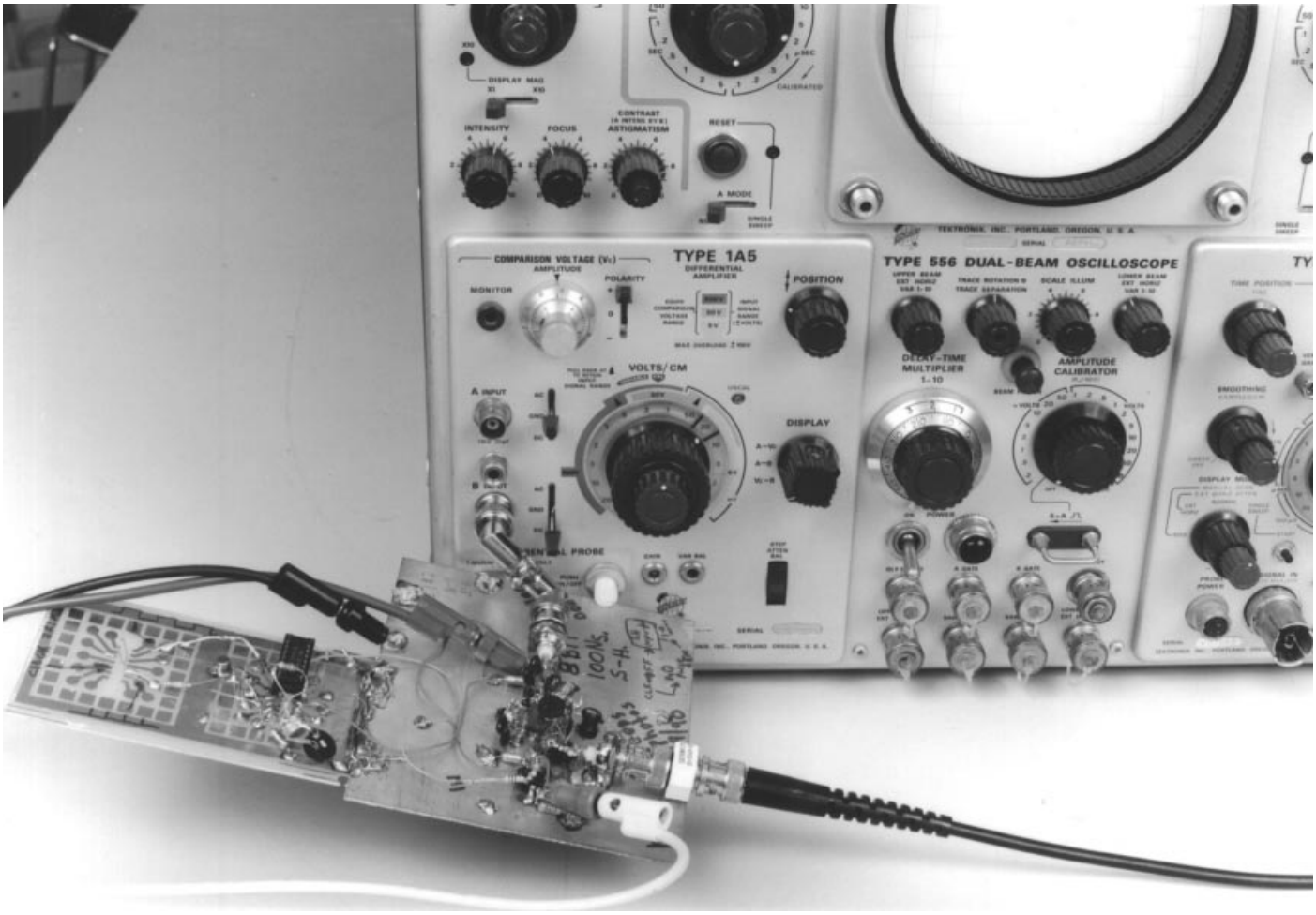
Probes are the most overlooked cause of oscilloscope mismeasurement. All probes have some effect on the point they are measuring. The most obvious is input resistance, but input capacitance usually dominates in a high speed measurement. Much time can be lost chasing circuit events which are actually due to improperly selected or applied probes. An 8pF probe looking at a 1kΩ source impedance forms an 8ns lag — substantially longer than a fast amplifier's delay time! Pay particular attention to the probe's input capacitance. Standard 10MΩ, 10X probes typically have 8pF-10pF of input capacitance, with 1X types being much higher. In general, 1X probes are not suitable for fast work because their bandwidth is limited to about 20MHz. Remember that all 10X probes cannot be used with all oscilloscopes; the probe's compensation range must match the oscilloscope's input capacitance. Low impedance probes (with 500Ω to 1kΩ resistance), designed for 50Ω inputs, usually have input capacitance of 1pF or 2pF. They are a very good choice if you can stand the low resistance. FET probes maintain high input resistance and keep capacitance at the 1pF level but have substantially more delay than passive probes. FET probes also have limitations on input common-mode range which must be adhered to or serious measurement errors will result. Contrary to popular belief, FET probes *do not* have extremely high input resistance — some types are as low as 100kΩ. It is possible to construct a wideband FET probe with very high input impedance, although input capacitance is somewhat higher than standard FET probes. For measurements requiring these characteristics, such a probe is useful. See Appendix E, "An Ultra Fast High Impedance Probe".

Regardless of which type probe is selected remember that they all have bandwidth and rise time restrictions. The displayed rise time on the oscilloscope is the vector sum of source, probe and 'scope rise times.

$$t_{RISE} = \sqrt{(t_{RISE}\ \text{Source})^2 + (t_{RISE}\ \text{Probe})^2 + (t_{RISE}\ \text{Oscilloscope})^2}$$

This equation warns that some rise time degradation must occur in a cascaded system. In particular, if probe and oscilloscope are rated at the same rise time, the system response will be slower than either.

Note 2: Almost no one believes any of this until they see it for themselves. I didn't. Photos of the network analyzer's display aren't included in the text because no one would believe them. I wouldn't.



LTAN47 • TA31

Figure 31. Sometimes the Best Probe is No Probe. Direct Connection to the Oscilloscope Eliminates a 10X Probe's Attenuation and Possible Grounding Problems in a Sample-Hold (Figure 124) Settling Time Measurement

Current probes are useful and convenient.[3] The passive transformer-based types are fast and have less delay than the Hall effect-based versions. The Hall types, however, respond at DC and low frequency and the transformer types typically roll off around 100Hz to 1kHz. Both types have saturation limitations which, when exceeded, cause odd results on the CRT which will confuse the unwary. The Tektronix type CT-1 current probe, although not nearly as versatile as the clip-on probes, bears mention. Although this is not a clip-on device, it may be the least electrically intrusive way of extracting wideband signal information. Rated at 1GHz bandwidth, it produces 5mV/mA output with only 0.6pF loading. Decay time constant of this AC current probe is ≈1%/50ns, resulting in a low frequency limit of 35kHz.

Note 3: A more thorough discussion of current probes is given in LTC Application Note 35, "Step Down Switching Regulators". See Reference 2.

A very special probe is the differential probe. A differential probe may be thought of as two matched FET probes contained within a common probe housing. This probe literally brings the advantage of a differential input oscilloscope to the circuit board. The probes matched, active circuitry provides greatly improved high frequency common mode rejection over single ended probing or even matched passive probes used with a differential amplifier. The resultant ability to reject common-mode signals and ground noise at high frequency allows this probe to deliver exceptionally clean results when monitoring small, fast signals. Figure 32 shows a differential probe being used to verify the waveshape of a 2.5mV input to a wideband, high gain amplifier (Figure 76 of the Applications section).

When using different probes, remember that they all have different delay times, meaning that apparent timing errors

will occur on the CRT. Know what the individual probe delays are and account for them in interpreting the CRT display.

By far the greatest source of error in probe use is grounding. Poor probe grounding can cause ripples and discontinuities in the waveform observed. In some cases the choice and placement of a probe's ground strap will affect waveforms on another channel. In the worst case, connecting the probe's ground wire will virtually disable the circuit being measured. The cause of these problems is due to parasitic inductance in the probe's ground connection. In most oscilloscope measurements this is not a problem, but at nanosecond speeds it becomes critical. Fast probes are always supplied with a variety of spring clips and accessories designed to aid in making the lowest possible inductive connection to ground. Most of these attachments assume a ground plane is in use, which it should be. Always try to make the shortest possible connection to ground – anything longer than 1 inch may cause trouble. Sometimes it's difficult to determine if probe grounding is the cause of observed waveform aberrations. One good test is to disturb the grounding set-up and see if changes occur. Nominally, touching the ground plane or jiggling probe ground connectors or wires should have no effect. If a ground strap wire is in use try changing its orientation or simply squeezing it together to change and minimize its loop area. *If any waveform change occurs while doing this the probe grounding is unacceptable, rendering the oscilloscope display unreliable.*

The simple network of Figure 33 shows just how easy it is for poorly chosen or used probes to cause bad results. A 9pF input capacitance probe with a 4 inch long ground

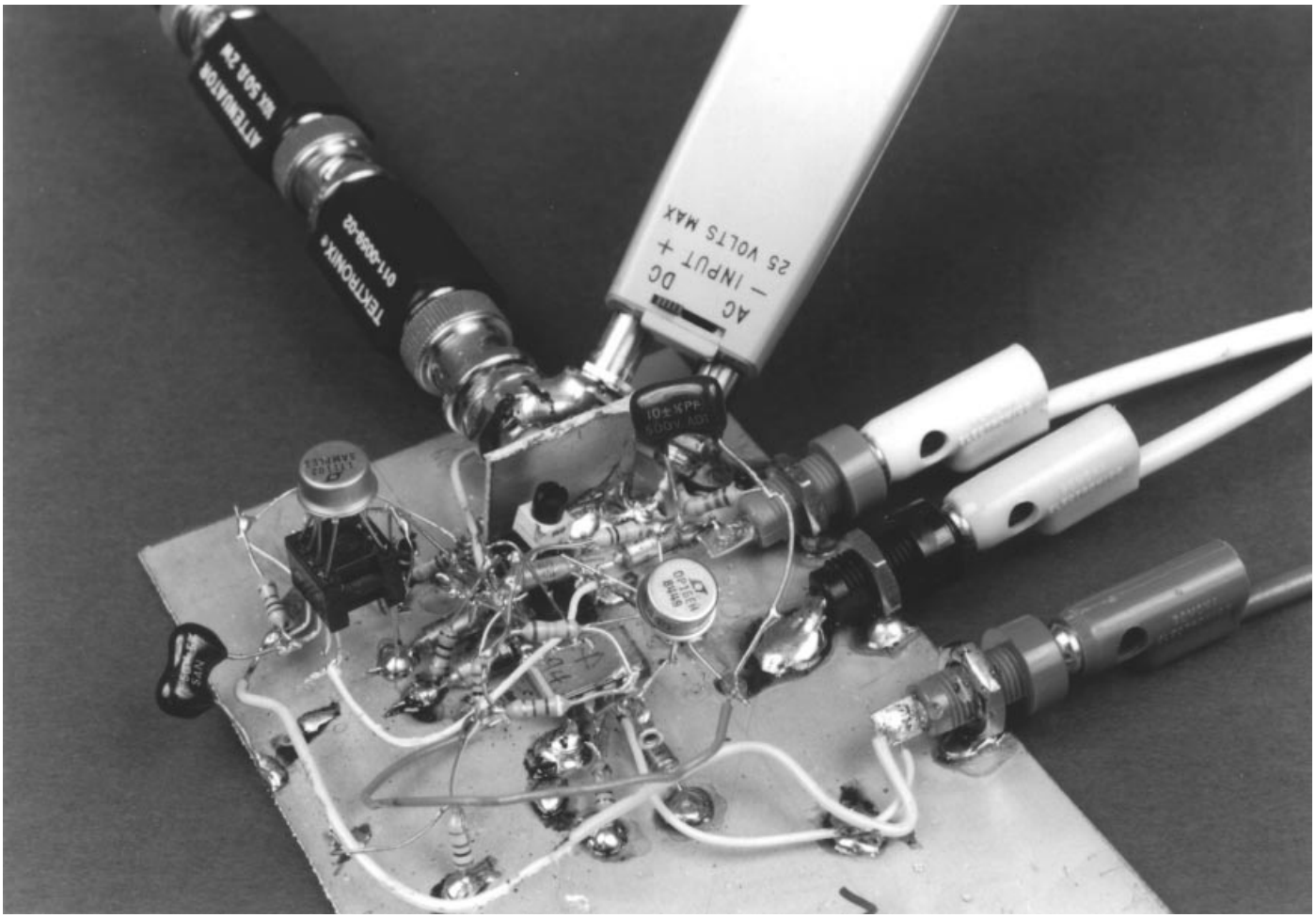


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Figure 32. Using a Differential Probe to Verify the Integrity of a 2.5mV High Speed Input Pulse (Figure 76's X1000 Amplifier)

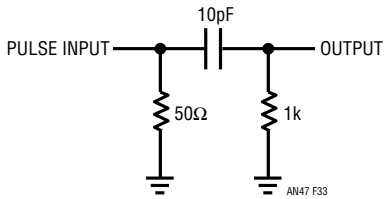

Figure 33. Probe Test Circuit

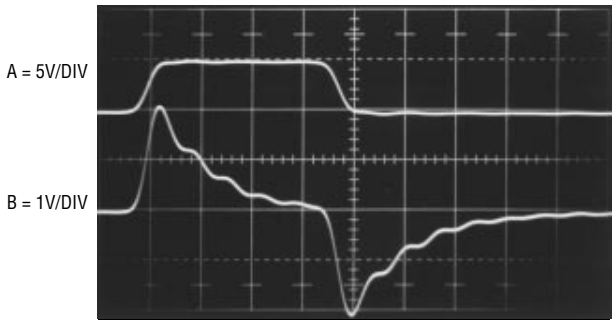

Figure 34. Test Circuit Output with 9pF Probe and 4 Inch Ground Strap

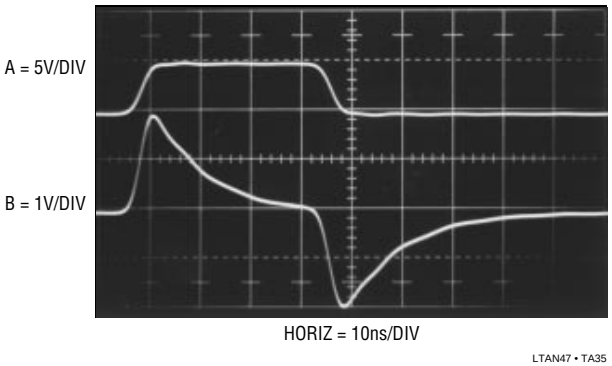

Figure 35. Test Circuit Output with 9pF Probe and 0.25 Inch Ground Strap

strap monitors the output (Trace B, Figure 34). Although the input (Trace A) is clean, the output contains ringing. Using the same probe with a 1/4 inch spring tip ground connection accessory seemingly cleans up everything (Figure 35). However, substituting a 1pf FET probe (Figure 36) reveals a 50% output amplitude error in Figure 35! The FET probe's low input capacitance allows a more accurate version of circuit action. The FET probe does, however, contribute its own form of error. Note that the probe's response is tardy by 5ns due to delay in its active circuitry. Hence, separate measurements with each probe are required to determine the output's amplitude and timing parameters.

A final form of probe is the human finger. Probing the circuit with a finger can accentuate desired or undesired effects, giving clues that may be useful. The finger can be used to introduce stray capacitance to a suspected circuit node while observing results on the CRT. Two fingers, lightly moistened, can be used to provide an experimental resistance path. Some high speed engineers are particularly adept at these techniques and can estimate the capacitive and resistive effects created with surprising accuracy.

Examples of some of the probes discussed, along with different forms of grounding implements, are shown in Figure 37. Probes A, B, E, and F are standard types equipped with various forms of low impedance grounding attachments. The conventional ground lead used on G is more convenient to work with but will cause ringing and

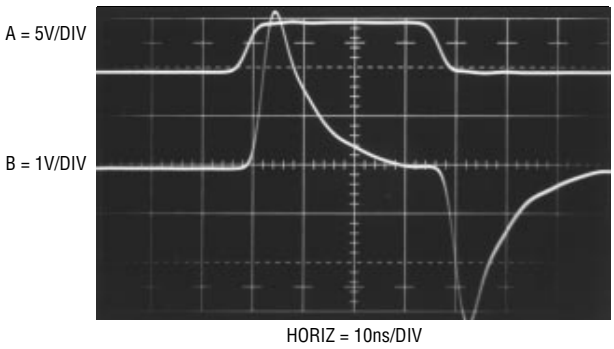

Figure 36. Test Circuit Output with FET Probe

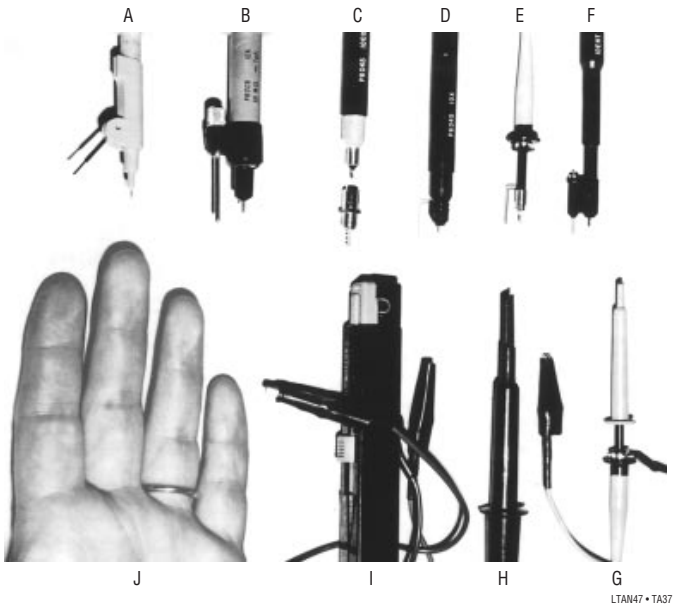

Figure 37. Various Probe-Ground Strap Configurations

other effects at high frequencies, rendering it useless. H has a very short ground lead. This is better, but can still cause trouble at high speeds. D is a FET probe. The active circuitry in the probe and a very short ground connector ensure low parasitic capacitance and inductance. C is a separated FET probe attenuator head. Such heads allow the probe to be used at higher voltage levels (e.g., ±10V or ±100V). The miniature coaxial connector shown can be mounted on the circuit board and the probe mated with it. This technique provides the lowest possible parasitic inductance in the ground path and is especially recommended. I is a current probe. A ground connection is not usually required. However, at high speeds the ground connection may result in a cleaner CRT presentation. Because no current flows in the ground lead of these probes, a long strap is usually permissible. J is typical of the finger probes described in the text. Note the ground strap on the third finger.

The low inductance ground connectors shown are available from probe manufacturers and are always supplied with good quality, high frequency probes. Because most oscilloscope measurements do not require them, they invariably become lost. There is no substitute for these devices when they are needed, so it is prudent to take care of them. This is especially applicable to the ground strap on the finger probe.

About Oscilloscopes

The modern oscilloscope is one of the most remarkable instruments ever constructed. The protracted and intense development effort put toward these machines is perhaps equaled only by the fanaticism devoted to timekeeping.[4] It is a tribute to oscilloscope designers that instruments manufactured over 25 years ago still suffice for over 90% of today's measurements. The oscilloscope-probe combination used in high speed work is the most important equipment decision the designer must make. Ideally, the oscilloscope should have at least 150MHz bandwidth, but slower instruments are acceptable if their limitations are well understood. Be certain of the characteristics of the probe-oscilloscope combination. Rise time, bandwidth, resistive and capacitive loading, delay, noise, channel-to-channel feedthrough, overdrive recovery, sweep nonlinearity, triggering, accuracy and other limitations must be kept in mind. High speed linear circuitry demands a great deal from test equipment and countless hours can be saved if the characteristics of the instruments used are well known. Obscene amounts of time have been lost pursuing "circuit problems" which in reality are caused by misunderstood, misapplied or out-of-spec equipment. Intimate familiarity with your oscilloscope is invaluable in getting the best possible results with it. In fact, it is possible to use seemingly inadequate equipment to get good results if the equipment's limitations are well known and respected. All of the circuits in the Applications section involve rise times and delays well above the 100MHz-200MHz region, but 90% of the development work was done with a 50MHz oscilloscope. Familiarity with equipment and thoughtful measurement technique permit useful measurements seemingly beyond instrument specifications. A 50MHz oscilloscope cannot track a 5ns rise time pulse, but it can measure a 2ns delay between two such events. Using such techniques, it is often possible to deduce the desired information. There are situations where no amount of cleverness will work and the right equipment (e.g., a faster oscilloscope) must be used. Sometimes, "sanity-checking" a limited bandwidth instrument with a higher bandwidth oscilloscope is all that is required. For high speed work, brute force bandwidth is indispensable when needed, and no amount of features or computational sophistication will substitute. Most high speed circuitry does not require more than two traces to get where you are going. Versatility and many channels are desirable, but if the budget is limited, spend for bandwidth!

Dramatic differences in displayed results are produced by probe-oscilloscope combinations of varying bandwidths. Figure 38 shows the output of a very fast pulse[5] monitored with a 1GHz sampling 'scope (Tektronix 556 with 1S1 sampling plug-in). At this bandwidth the 10V amplitude appears clean, with just a small hint of ringing after the falling edge. The rise and fall times of 350ps are suspicious, as the sampling oscilloscope's rise time is also specified at 350ps.[6]

Note 4: In particular, the marine chronometer received ferocious and abundant amounts of attention. See References 4, 5, and 6. For an enjoyable stroll through the history of oscilloscope vertical amplifiers, see Reference 3. See also Reference 41.

Note 5: See Appendix D, "Measuring Probe - Oscilloscope Response", for complete details on this pulse generator.

Note 6: This sequence of photos was shot in my home lab. I'm sorry, but 1GHz is the fastest 'scope in my house.

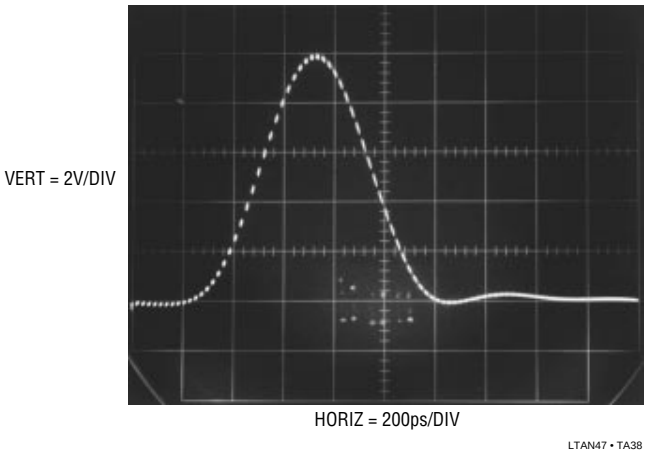

Figure 38. A 350ps Rise/Fall Time 10V Pulse Monitored on 1GHz Sampling Oscilloscope. Direct 50Ω Input Connection is Used

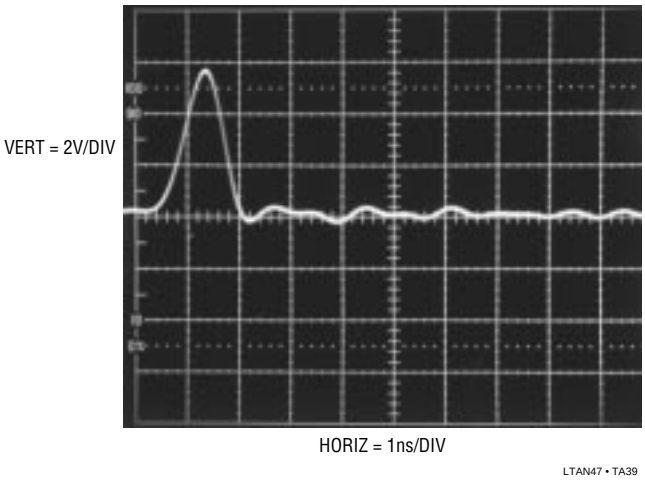

Figure 39. The Test Pulse Appears Smaller and Slower On a 350MHz Instrument (t_{RISE} = 1ns). Deliberate Poor Grounding Creates Rippling After the Pulse Falls. Direct 50Ω Connection is Used

Figure 39 shows the same pulse observed on a 350MHz instrument with a direct connection to the input (Tektronix 485/50Ω input). Indicated rise time balloons to 1ns, while displayed amplitude shrinks to 6V, reflecting this instrument's lesser bandwidth. To underscore earlier discussion, poor grounding technique (1 1/2" of ground lead to the ground plane) created the prolonged rippling after the pulse fall.

Figure 40 shows the same 350MHz (50Ω input) oscilloscope with a 3GHz 10X probe (Tektronix P6056). Displayed results are nearly identical, as the probe's high bandwidth contributes no degradation. Again, deliberate poor grounding causes overshoot and rippling on the pulse fall.

Figure 41 equips the same oscilloscope with a 10X probe specified at 290MHz bandwidth (Tektronix P6047). Additionally, the oscilloscope has been switched to its 1MΩ input mode, reducing bandwidth to a specified 250MHz. Amplitude degrades to less than 4V and edge times similarly increase. The deliberate poor grounding contributes the undershoot and underdamped recovery on pulse fall.

In Figure 42 a 100MHz 10X probe (Hewlett-Packard Model 10040A) has been substituted for the 290MHz unit. The oscilloscope and its set-up remain the same. Amplitude shrinks below 2V, with commensurate rise and fall times. Cleaned up grounding eliminates aberrations.

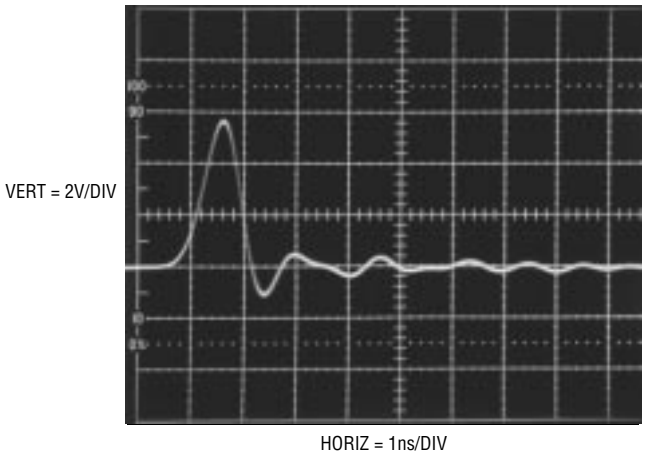

Figure 40. Test Pulse on the Same 350MHz Oscilloscope Using a 3GHz 10X Probe. Deliberate Poor Grounding Maintains Rippling Residue

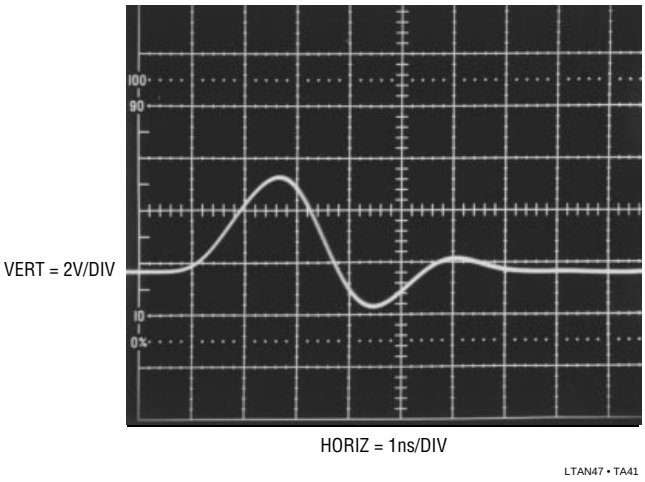

Figure 41. Test Pulse Measures Only 3V High on a 250MHz 'Scope with Significant Waveform Distortion. 250MHz 10X Probe Used

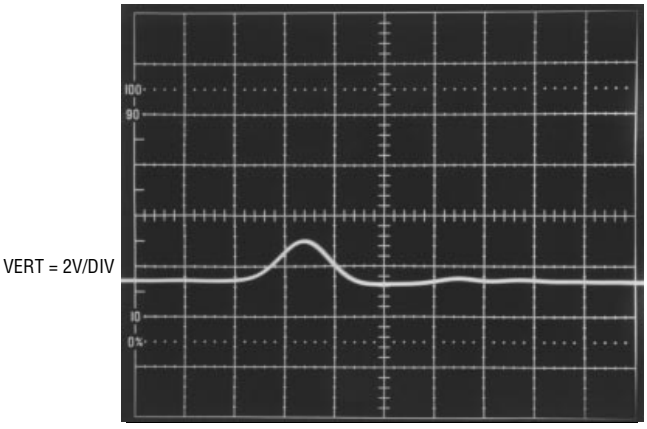

Figure 42. Test Pulse Measures Under 2V High Using 250MHz 'Scope and a 100MHz Probe

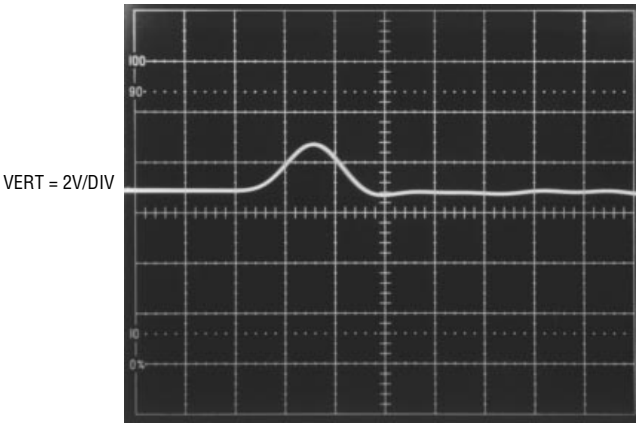

Figure 43. 150MHz Oscilloscope (t_{RISE} = 2.4ns) with Direct Connection Responds to the Test Pulse

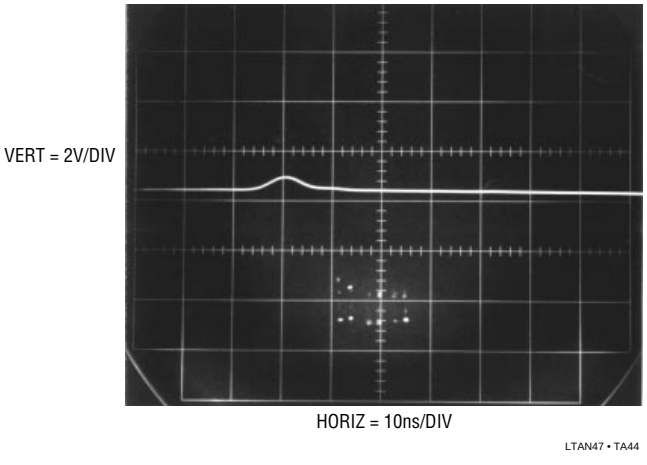

Figure 44. A 50MHz Instrument Barely Grunts. 10V, 350ps Test Pulse Measures Only 0.5V High with 7ns Rise and Fall Times!

A Tektronix 454A (150MHz) produced Figure 43's trace. The pulse generator was directly connected to the input. Displayed amplitude is about 2V, with appropriate 2ns edges. Finally, a 50MHz instrument (Tektronix 556 with 1A4 plug-in) just barely grunts in response to the pulse (Figure 44). Indicated amplitude is 0.5V, with edges reading about 7ns. That's a long way from the 10V and 350ps that's really there!

A final oscilloscope characteristic is overload performance. It is often desirable to view a small amplitude portion of a large waveform. In many cases the oscilloscope is required to supply an accurate waveform after the display has been driven off screen. How long must one wait after an overload before the display can be taken seriously? The answer to this question is quite complex. Factors involved include the degree of overload, its duty cycle, its magnitude in time and amplitude, and other considerations. Oscilloscope response to overload varies widely between types and markedly different behavior can be observed in any individual instrument. For example, the recovery time for a 100X overload at 0.005V/division may be very different than at 0.1V/division. The recovery characteristic may also vary with waveform shape, DC content and repetition rate. With so many variables, it is clear that measurements involving oscilloscope overload must be approached with caution. Nevertheless, a simple test can indicate when the oscilloscope is being deleteriously affected by overdrive.

The waveform to be expanded is placed on the screen at a vertical sensitivity which eliminates all off-screen activity. Figure 45 shows the display. The lower right hand portion is to be expanded. Increasing the vertical sensitivity by a factor of two (Figure 46) drives the waveform off-screen, but the remaining display appears reasonable. Amplitude has doubled and waveshape is consistent with the original display. Looking carefully, it is possible to see small amplitude information presented as a dip in the waveform at about the third vertical division. Some small disturbances are also visible. This observed expansion of the original waveform is believable. In Figure 47, gain has been further increased and all the features of Figure 46 are amplified accordingly. The basic waveshape appears clearer and the dip and small disturbances are also easier to see. No new waveform characteristics are observed. Figure 48 brings some unpleasant surprises. This increase in gain

causes definite distortion. The initial negative-going peak, although larger, has a different shape. Its bottom appears less broad than in Figure 47. Additionally, the peak's positive recovery is shaped slightly differently. A new rippling disturbance is visible in the center of the screen. This kind of change indicates that the oscilloscope is having trouble. A further test can confirm that this waveform is being influenced by overloading. In Figure 49 the gain remains the same, but the vertical position knob has been used to reposition the display at the screen's bottom. This shifts the oscilloscope's DC operating point which, under normal circumstances, should not affect the displayed waveform. Instead, a marked shift in waveform amplitude and outline occurs. Repositioning the waveform to the screen's top produces a differently distorted waveform (Figure 50). It is obvious that for this particular waveform, accurate results cannot be obtained at this gain.

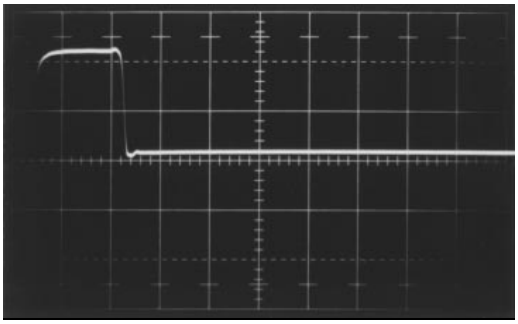

Figure 45

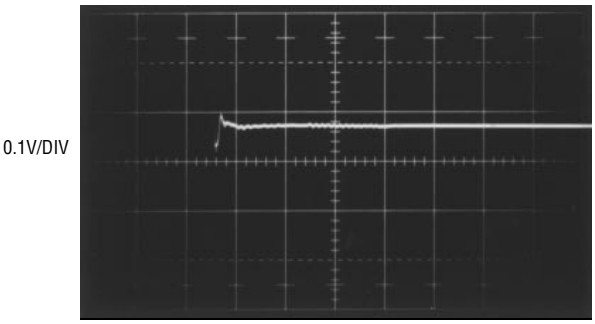

Figure 48

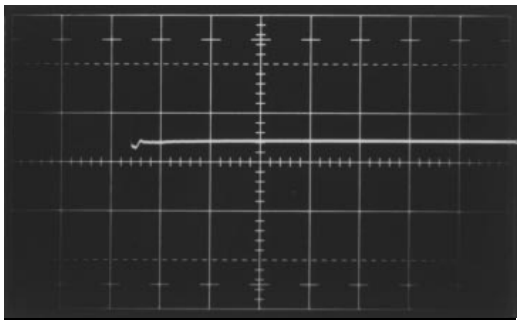

Figure 46

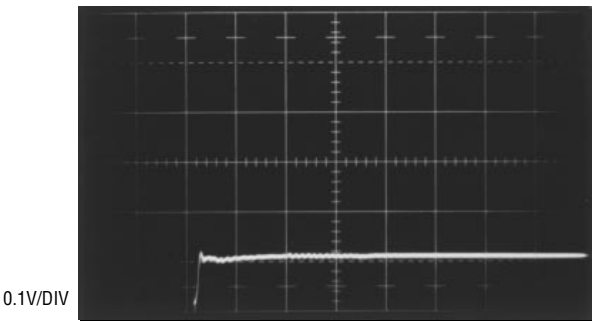

Figure 49

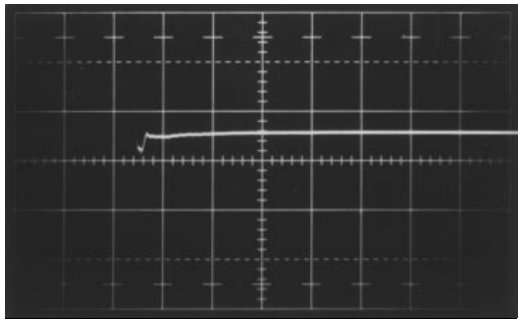

Figure 47

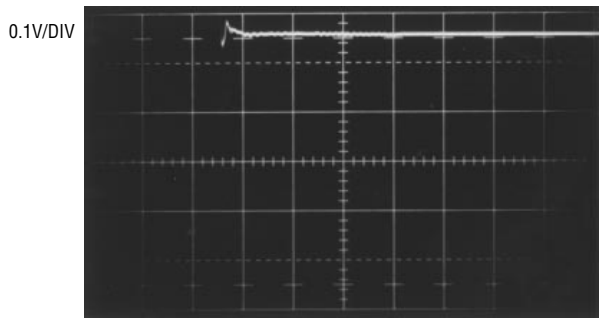

Figure 50

Figures 45-50. The Overdrive Limit is Determined by Progressively Increasing Oscilloscope Gain and Watching for Waveform Aberrations

Differential plug-ins can address some of the issues associated with excessive overdrive, although they cannot solve all problems. Two differential plug-in types merit special mention. At low level, a high sensitivity differential plug-in is indispensable. The Tektronix 1A7, 1A7A and 7A22 feature 10μV sensitivity, although bandwidth is limited to 1MHz. The units also have selectable high and low pass filters and good high frequency common-mode rejection. Tektronix type 1A5, W and 7A13 are differential comparators. They have calibrated DC nulling (slideback) sources, allowing observation of small, slowly moving events on top of common-mode DC or fast events riding on a waveform.

A special case is the sampling oscilloscope. By nature of its operation, a sampling 'scope in proper working order is inherently immune to input overload, providing essentially instantaneous recovery between samples. Appendix B, "Measuring Amplifier Settling Time", utilizes this capability. See Reference 8 for additional details.

The best approach to measuring small portions of large waveforms, however, is to eliminate the large signal swing seen by the oscilloscope. Appendix B, "Measuring Amplifier Settling Time" shows ways to do this when measuring DAC-amplifier settling time to very high accuracy at high speed.

In summary, while the oscilloscope provides remarkable capability, its limitations must be well understood when interpreting results.[7]

About Ground Planes

Many times in high frequency circuit layout, the term "ground plane" is used, most often as a mystical and ill-defined cure to spurious circuit operation. In fact, there is little mystery to the usefulness and operation of ground planes, and like many phenomena, their fundamental operating principle is surprisingly simple.

Ground planes are primarily useful for minimizing circuit inductance. They do this by utilizing basic magnetic theory. Current flowing in a wire produces an associated magnetic field. The field's strength is proportional to the current and inversely related to the distance from the conductor. Thus, we can visualize a wire carrying current (Figure 51) surrounded by radii of magnetic field. The unbounded field becomes smaller with distance. A wire's inductance is defined as the energy stored in the field set up by the wire's current. To compute the wire's inductance requires integrating the field over the wire's length and the total radial area of the field. This implies integrating on the radius from $R = R_W$ to infinity, a very large number. However, consider the case where we have two wires in space carrying the same current in either direction (Figure 52). The fields produced cancel.

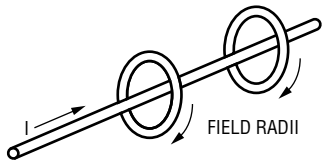

Figure 51. Single Wire Case

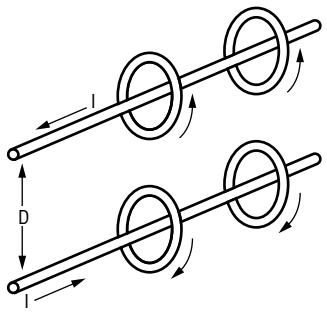

Figure 52. Two Wire Case

In this case, the inductance is much smaller than in the simple wire case and can be made arbitrarily smaller by reducing the distance between the two wires. This reduction of inductance between current carrying conductors is the underlying reason for ground planes. In a normal circuit, the current path from the signal source through its conductor and back to ground includes a large loop area. This produces a large inductance for this conductor which can cause ringing due to LRC effects. It is worth noting that 10nH at 100MHz has an impedance of 6Ω. At 10mA a 60mV drop results.

A ground plane provides a return path directly under the signal carrying conductor through which return current can flow. The conductor's small physical separation means the inductance is low. Return current has a direct path to ground, regardless of the number of branches associated with the conductor. Currents will always flow through the return path of lowest impedance. In a properly designed

Note 7: Additional discourse on oscilloscopes will be found in References 1 and 7 through 11.

ground plane, this path is directly under the signal conductor. In a practical circuit, it is desirable to ground plane one whole side of the PC card (usually the component side for wave solder considerations) and run the signal conductors on the other side. This will give a low inductance path for all the return currents.

Aside from minimizing parasitic inductance, ground planes have additional benefits. Their flat surface minimizes resistive losses due to AC skin effect (AC currents travel along a conductor's surface). Additionally, they aid the circuit's high frequency stability by referring stray capacitances to ground.

Some practical hints for ground planes are:

1. Ground plane as much area as possible on the component side of the board, especially under traces that operate at high frequency.
2. Mount components that conduct substantial fast rise currents (termination resistors, ICs, transistors, decoupling capacitors) as close to the board as possible.
3. Where common ground potential is important (i.e., at comparator inputs), try to single point the critical components into the ground plane to avoid voltage drops.

   For example, in Figure 53's common A/D circuit, good practice would dictate that grounds 2, 3, 4 and 6 be as close to single point as possible. Fast, large currents must flow through R1, R2, D1 and D2 during the DAC settle time. Therefore, D1, D2, R1 and R2 should be mounted close to the ground plane to minimize their inductance. R3 and C1 don't carry any current, so their inductance is less important; they could be vertically inserted to save space and to allow point 4 to be single point common with 2, 3 and 6. In critical circuits, the designer must often trade off the beneficial effects of lowered inductance versus the loss of single point ground.
4. Keep trace length short. Inductance varies directly with length and no ground plane will achieve perfect cancellation.

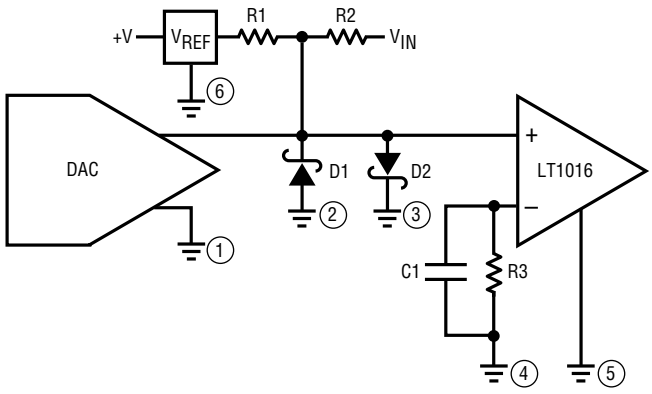

Figure 53. Typical Grounding Scheme

About Bypass Capacitors

Bypass capacitors are used to maintain low power supply impedance at the point of load. Parasitic resistance and inductance in supply lines mean that the power supply impedance can be quite high. As frequency goes up, the inductive parasitic becomes particularly troublesome. Even if these parasitic terms did not exist, or if local regulation is used, bypassing is still necessary because no power supply or regulator has zero output impedance at 100MHz. What type of bypass capacitor to use is determined by the application, frequency domain of the circuit, cost, board space and many other considerations. Some useful generalizations can be made.

All capacitors contain parasitic terms, some of which appear in Figure 54. In bypass applications, leakage and dielectric absorption are second order terms but series R and L are not. These latter terms limit the capacitor's ability to damp transients and maintain low supply impedance. Bypass capacitors must often be large values so they can absorb long transients, necessitating electrolytic types which have large series R and L.

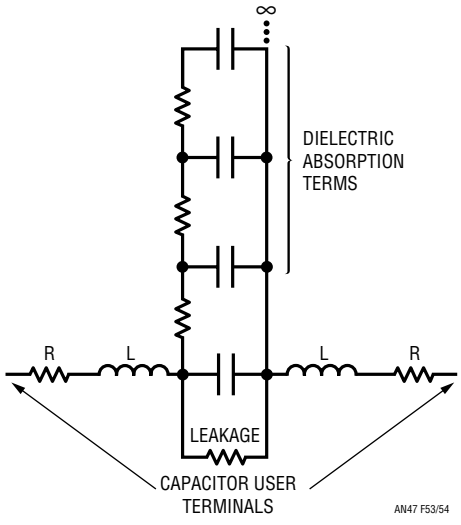

Figure 54. Parasitic Terms of a Capacitor

Different types of electrolytics and electrolytic-non-polar combinations have markedly different characteristics. Which type(s) to use is a matter of passionate debate in some circles and the test circuit (Figure 55) and accompanying photos are useful. The photos show the response of 5 bypassing methods to the transient generated by the test circuit. Figure 56 shows an unbypassed line which sags and ripples badly at large amplitudes. Figure 57 uses an aluminum 10µF electrolytic to considerably cut the disturbance, but there is still plenty of potential trouble. A tantalum 10µF unit offers cleaner response in Figure 58 and the 10µF aluminum combined with a 0.01µF ceramic type is even better in Figure 59. Combining electrolytics with non-polarized capacitors is a popular way to get good response but beware of picking the wrong duo. The right (wrong) combination of supply line parasitics and paralleled dissimilar capacitors can produce a resonant, ringing response, as in Figure 60. Caveat!

Breadboarding Techniques

The breadboard is both the designer's playground and proving ground. It is there that Reality resides, and paper (or computer) designs meet their ruler. More than anything else, breadboarding is an iterative procedure, an odd amalgam of experience guiding an innocent, ignorant,

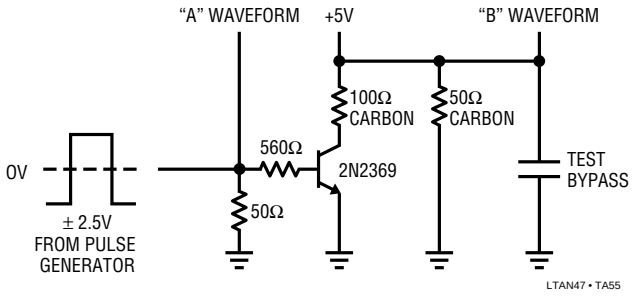

Figure 55. Bypass Capacitor Test Circuit

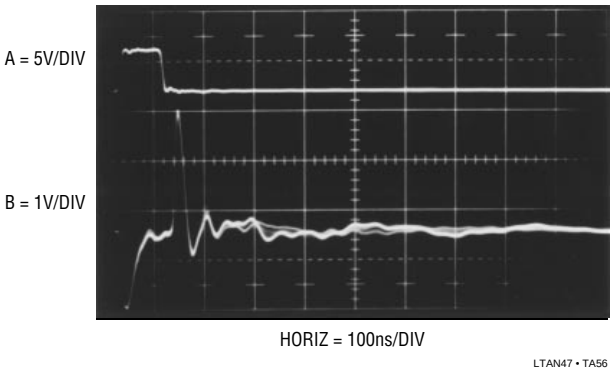

Figure 56. Response of Unbypassed Line

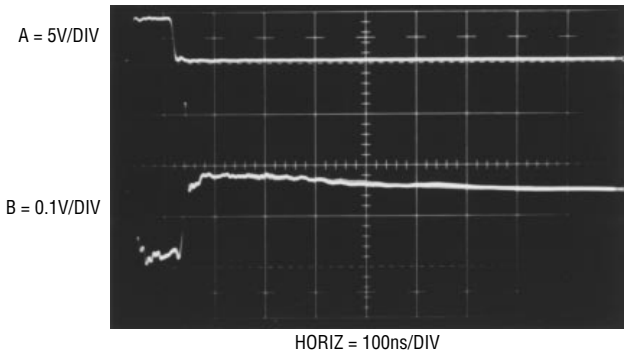

Figure 57. Response of 10µF Aluminum Capacitor

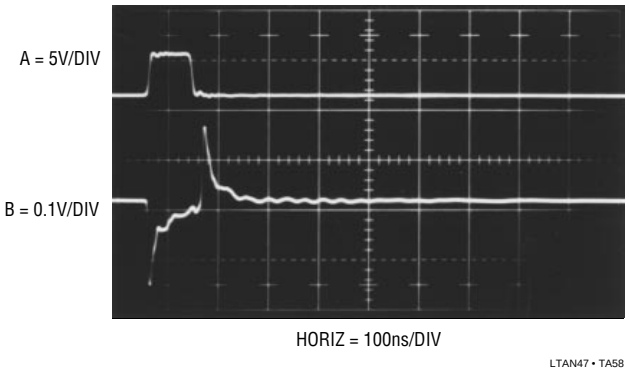

Figure 58. Response of 10µF Tantalum Capacitor

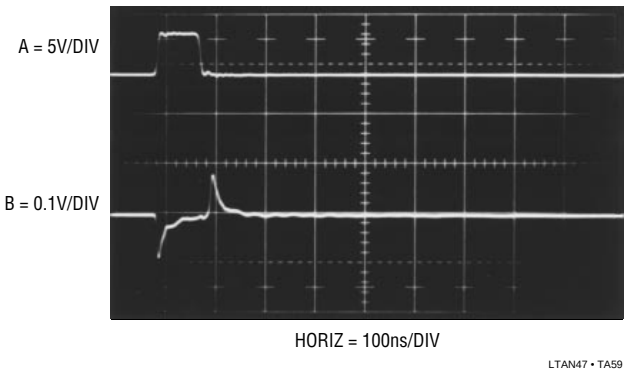

Figure 59. Response of 10µF Aluminum Paralleled by 0.01µF Ceramic

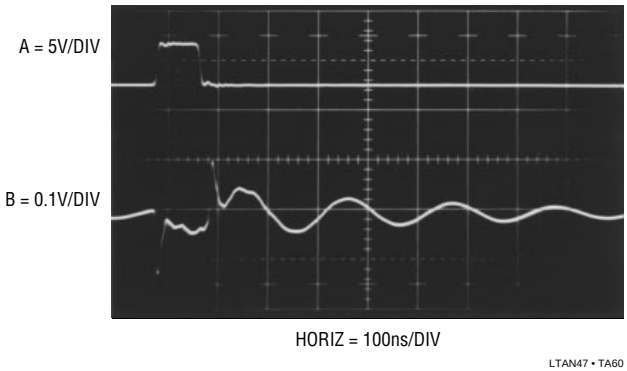

Figure 60. Some Paralleled Combinations can Ring. Try before Specifying!

explorative spirit. A key is to be willing to try things out, sometimes for not very good reasons. Invent problems and solutions, guess carefully and wildly, throw rocks and see what comes loose. Invent and design experiments, and follow them wherever they lead. Reticence to try things is probably the number one cause of breadboards that "don't work".[8] Implementing the above approach to life begins with the physical construction methods used to build the breadboard.

A high speed breadboard must start with a ground plane. Additionally, bypassing, component layout and connections should be consistent with high speed operations. Because of these considerations there is a common misconception that breadboarding high speed circuits is time consuming and difficult. This is simply not true. For high speed circuits of moderate complexity a complete and electrically correct breadboard can be assembled in 10 minutes if all necessary components are on hand. The key to rapid breadboarding is to identify critical circuit nodes and design the layout to suit them. This permits most of the breadboard's construction to be fairly sloppy, saving time and effort. Additionally, use all degrees of freedom in making connections and mounting components. Don't be bashful about bending I.C. pins to suit desired low capacitance connections, or air wiring components to achieve rapid or electrically optimum layout. Save time by using components, such as bypass capacitors, as mechanical supports for other components, such as amplifiers. It is true that eventual printed circuit construction is required, but when initially breadboarding forget about PC and production constraints. Later, when the circuit works, and is well understood, PC adaptations can be taken care of.

Figure 61's amplifier circuit is a good working example. This circuit, excerpted from the Applications section (where its electrical operation is more fully explained) is a high impedance, wideband amplifier with low input capacitance. Q1 and A1 form the high frequency path, with the 900Ω-100Ω feedback divider setting gain. A2 and Q2 close a DC stabilization loop, minimizing DC offset between the circuit's input and output. Critical nodes in this circuit include Q1's gate (because of the desired low input capacitance) and A1's input related connections (because of their high speed operation). Note that the connections associated with A2 serve at DC and are much less sensitive to layout. These determinations dominate the breadboard's construction.

Figure 62 shows initial breadboard construction. The copper clad board is equipped with banana type connectors. The connector's mounting nuts are simply soldered to the clad board, securing the connectors. Figure 63 adds A1 and the bypass capacitors. Observe that A1's leads have been bent out, permitting the amplifier to sit down on the ground plane, minimizing parasitic capacitance. Also, the bypass capacitors are soldered to the amplifier power pins right at the capacitor's body. The capacitor's lead lengths are returned to the banana power jacks. This connection method provides good amplifier bypassing

Note 8: A much more eloquently stated version of this approach is found in Reference 12.

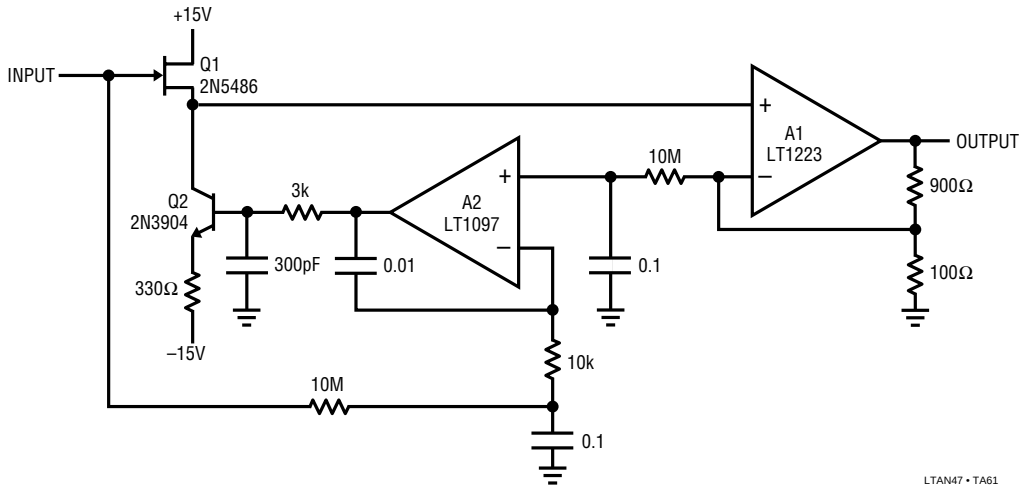

Figure 61. The Stabilized FET Input Amplifier (Applications Figure 73) to be Breadboarded

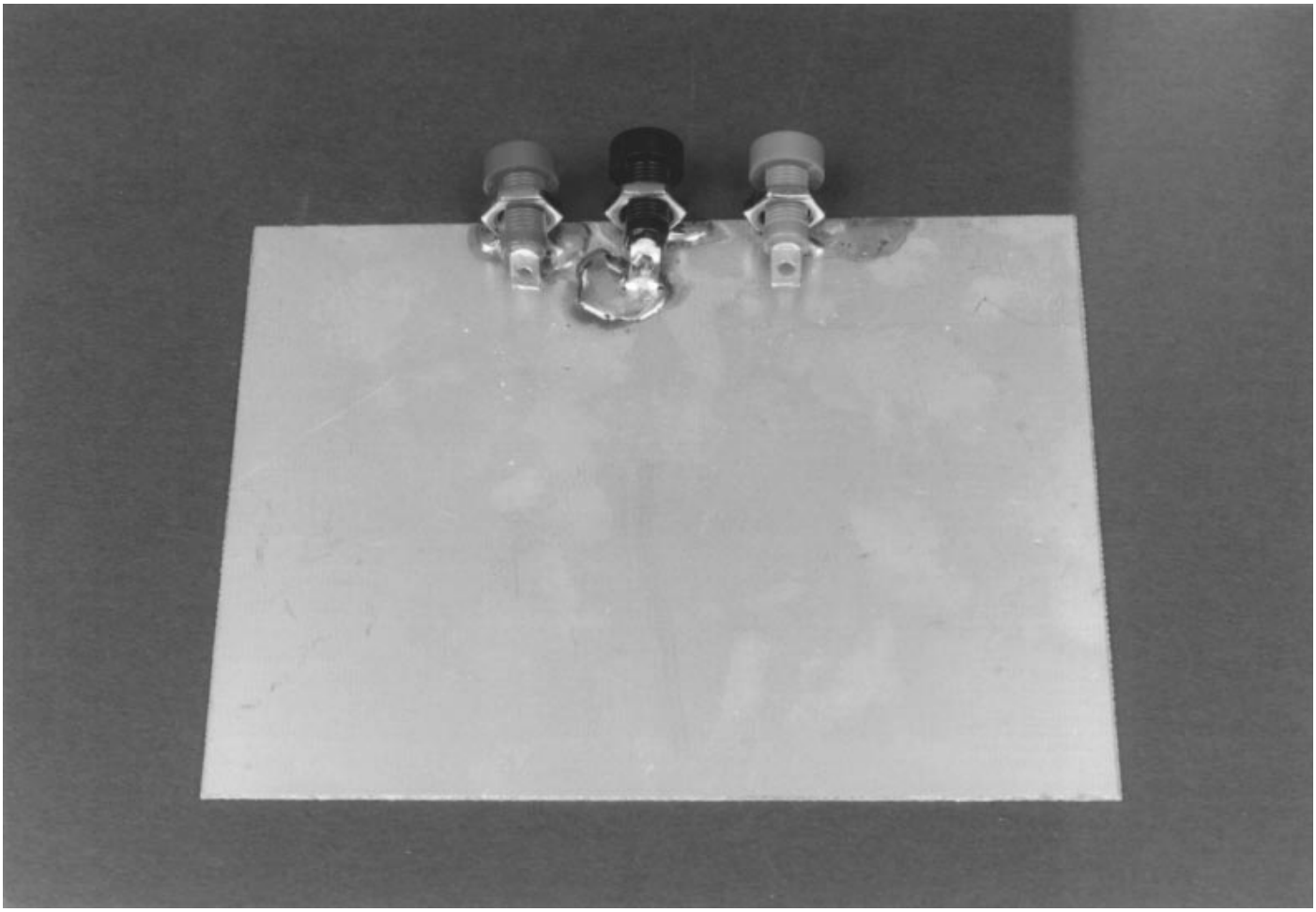

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Figure 62. The Banana Jacks are Soldered to the Copper Clad Board

while mechanically supporting the amplifier. It also eliminates separate wire runs to the power pins.

Figure 64 adds the discrete components in the high speed path. Q1's gate is connected directly to the input BNC, as is the 10MΩ resistor associated with A2's negative input. Note that the end of this resistor that sees high frequency is cut very short, while the other end is left uncut. The 900Ω-100Ω divider is installed at A1, with very short connections to A1's negative input. A1's 10MΩ resistor receives similar treatment to the BNC connected 10MΩ unit; the high frequency end is cut short, while the end destined for connection to A2 remains uncut. Q2's collector and Q1's source, high speed points, are tied closely together with A1's positive input.

Finally, DC amplifier A2 and its associated components are air wired into the breadboard (Figure 65). Their DC operation permits this, while the construction technique makes connections to the previously wired nodes easy. The previously uncommitted ends of the 10MΩ resistors may be bent in any way necessary to make connections. All other components associated with A2 receive similar treatment and the circuit is ready for experimentation.

Despite the breadboard's seemingly haphazard construction, the circuit worked well. Input capacitance measured a few pF (including BNC connector) with bias current of about 100pA. Slew rate was 1000V/μs, with bandwidth approaching 100MHz. Output, even with 50mA loading, was clean, with no sign of oscillation or other instabilities. Full details on this circuit appear in the Applications section. Additional examples of breadboard construction techniques appear in Appendix F, "Additional Comments on Breadboarding".

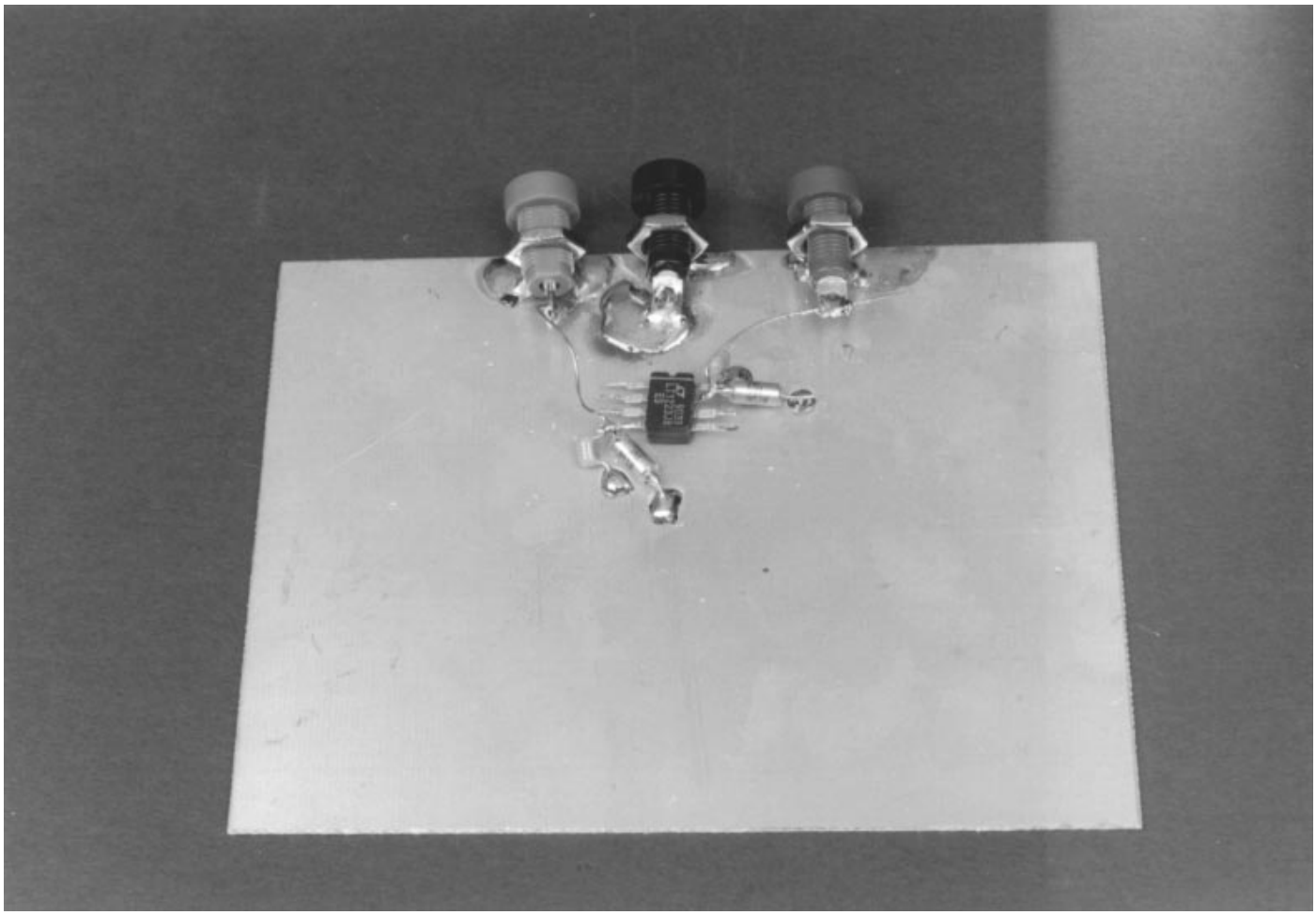

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Figure 63. High Speed Amplifier A1 is Connected to Power. Bypass Capacitors Provide Support. Bending Amplifier Pins Eases Connections and Minimizes Distance to the Ground Plane

Once the breadboard seems to work, it's useful to begin thinking about PC layout and component choice for production. Experiment with the existing layout to determine just how sensitive nominally critical points are. Add controlled parasitic terms (e.g., resistors, capacitors and physical layout changes) to test for sensitivity. Gentle touching of suspect points with a finger can yield preliminary indication of sensitivity, giving clues that can be quite valuable.

In conclusion, when breadboarding, design the breadboard to be quick and easy to build, work with and modify. Observe the circuit and listen to what it is telling you before trying to get it to some desired state. Finally, don't hesitate to try just about anything; that's what the breadboard is for. Almost anything you do will cause some result — whether it's good or bad is almost irrelevant. Anything you do that enhances your ability to correlate events occurring on the breadboard can only be beneficial.

Oscillation

The forte of the operational amplifier is negative feedback. It is feedback which stabilizes the operating point and fixes the gain. However, positive feedback or delayed negative feedback can cause oscillation. Thus, a properly functioning amplifier constantly lives in the shadow of oscillation.

When oscillation occurs, several major candidates for blame are present. Power supply impedance must be low. If the supply is unbypassed, the impedance the amplifier sees at its power terminals is high, particularly at high

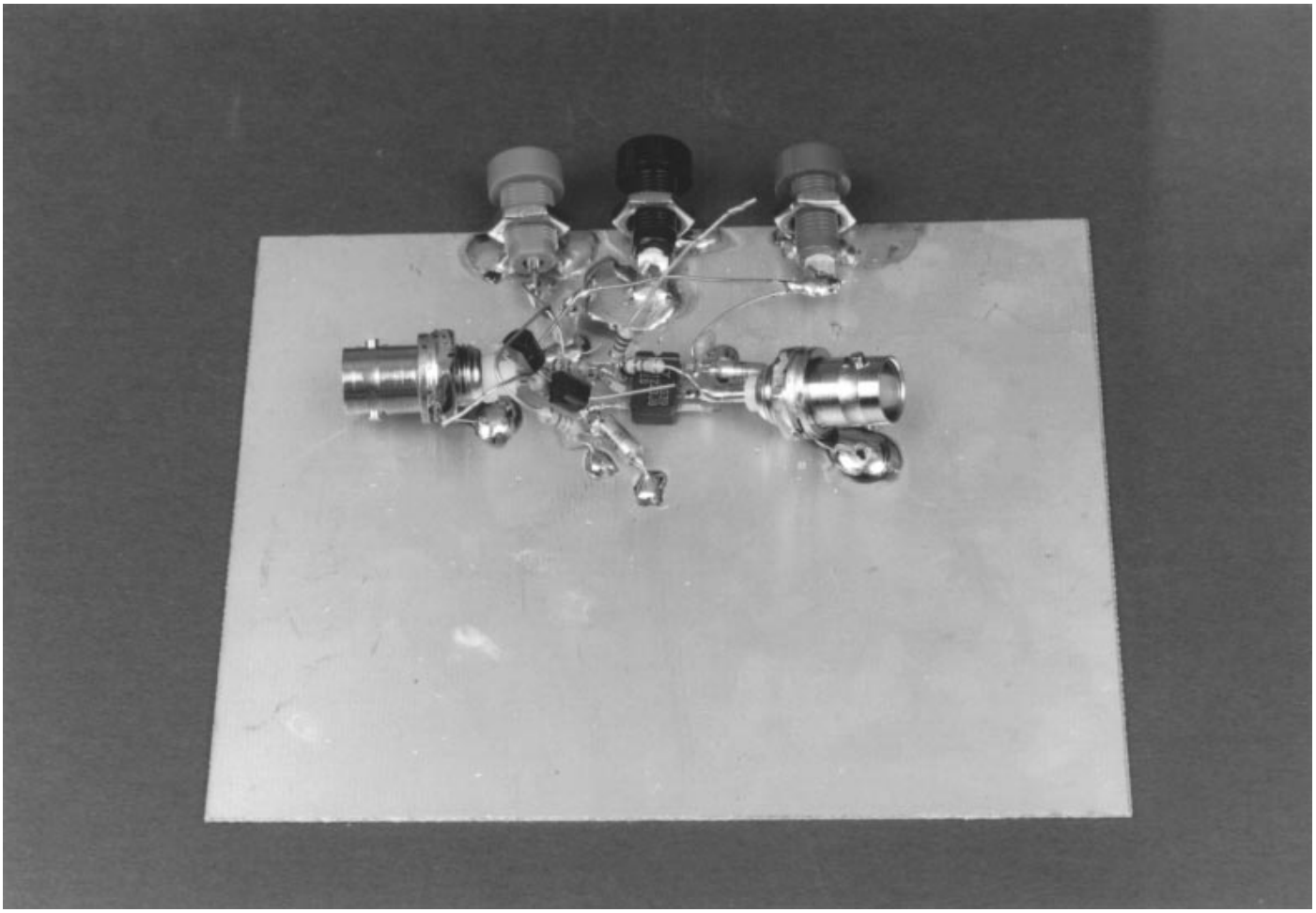

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Figure 64. Additional High Speed Discrete Components and Connectors are Added. Note Short Connections at Amplifier Input Pins (Left Side of Package). 10M Resistors Uncommitted Ends are Just Visible

frequency. This impedance forms a voltage divider with the amplifier, allowing the supply to move as internal conditions in the amplifier change. This can cause local feedback and oscillation occurs. The obvious cure is to bypass the amplifier.

A second common cause of oscillation is positive feedback. In most amplifier circuits feedback is negative, although controlled amounts of positive feedback may be used. In a circuit that nominally has only negative feedback unintended positive feedback may occur with poor layout. Check for possible parasitic feedback paths and unwanted or overlooked feedback action. Always minimize (to the extent possible) impedances seen by amplifier inputs. This helps attenuate the effects of parasitic feedback paths to the inputs. Similarly, minimize exposed input trace area. Route amplifier outputs and other signals well away from sensitive nodes. Sometimes no amount of layout finesse will work and shielding is required. Use shielding only when required — extensive shielding is a sloppy substitute for good layout practice.

A final cause of oscillation is negative feedback arriving well delayed in time. Under these conditions the amplifier hopelessly tries to servo a feedback signal which consistently arrives too late. The servo action takes the form of an electronic tail chase, with oscillation centered around the ideal servo point. The most common causes of this problem are reactive loading of the amplifier (most notably capacitive loads such as cable) and circuitry, such as power amplifiers, placed within the amplifier's feedback path. Reactive loads should be isolated from the amplifier's output (and feedback path) with a resistor or power amplifier. Sometimes rolling off the amplifier's frequency

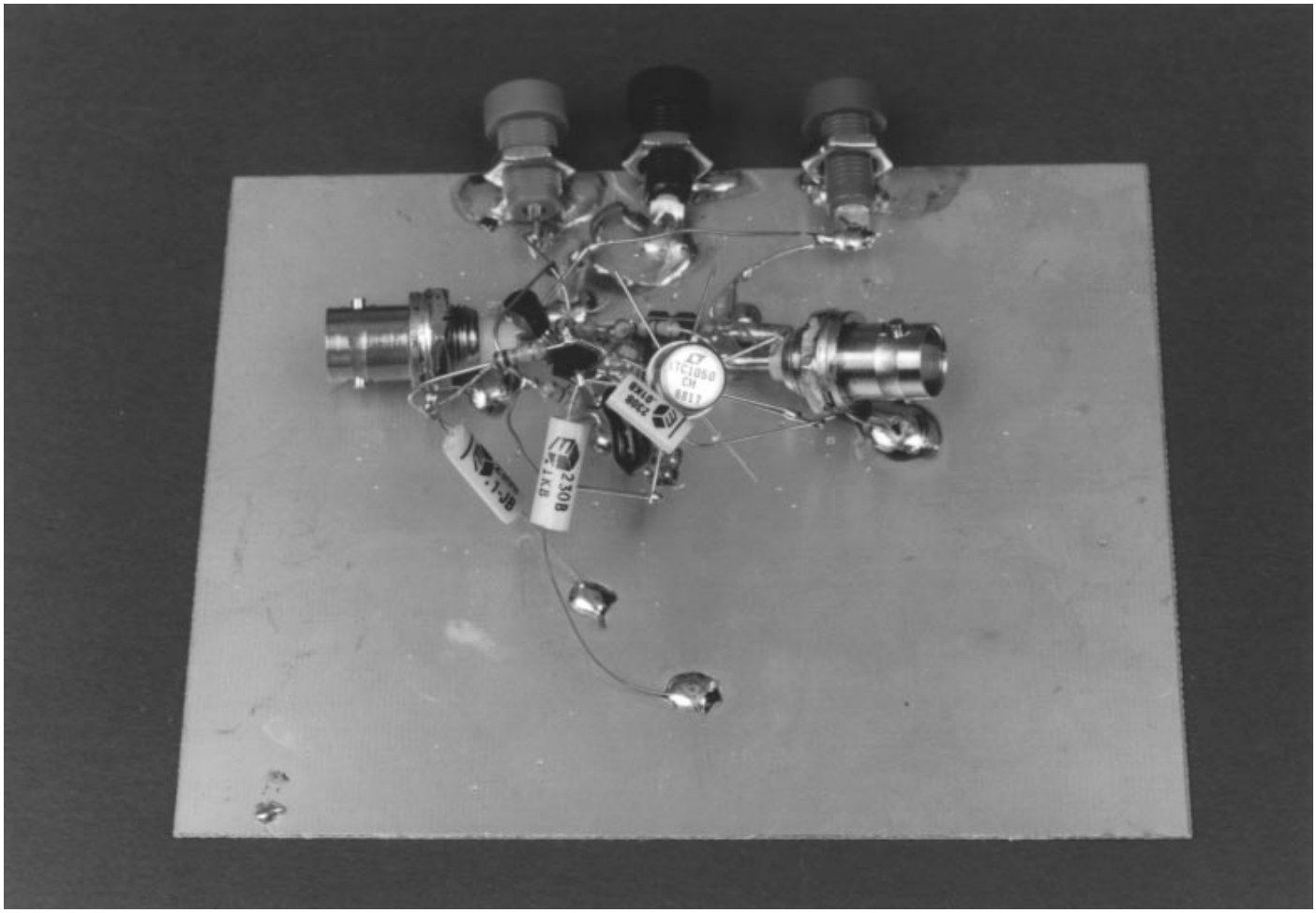

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Figure 65. DC Servo Amplifier is Wired In and Connections to 10M Resistors Completed. This Part of the Circuit is Not Layout Sensitive

response will fix the problem, but in high speed circuits this may not be an option.

Placing power gain or other type stages within the amplifier's feedback path adds time delay to the stabilizing feedback. If the delay is significant, oscillation commences. Stages operating within the amplifier's loop must contribute minimum time lag compared to the amplifier's speed capability. At lower speeds this is not too difficult, but something destined for operation within a 100MHz amplifier's loop must be *fast*. As mentioned before, rolling off the amplifier's frequency response eases the job, but is usually undesirable in a wideband circuit. Every effort should be expended to maximize the added stages bandwidth before resorting to roll-off of the amplifier. In this way the fastest overall bandwidth is achieved while maintaining stability. Appendix C, "The Oscillation Problem – Frequency Compensation Without Tears", discusses considerations surrounding operating power gain and other type stages within amplifier loops.

This completes the tutorial section. Hopefully, several notions have been imparted. First, in any measurement situation, test equipment characteristics are an integral part of the circuit. At high speed and high precision this is particularly the case. As such, it is imperative to know your equipment and how it works. There is no substitute for intimate familiarity with your tool's capabilities and limitations.[9]

In general, use equipment you trust and measurement techniques you understand. Keep asking questions and

Note 9: Further exposition and *kvetching* on this point is given in Reference 13.

don't be satisfied until everything you see on the oscilloscope is accounted for and makes sense.

Fast monolithic amplifiers, combined with the precautionary notes listed above, permit fast linear circuit functions which are difficult or impractical using other approaches. Some of the applications presented represent the state-of-the-art for a particular circuit function. Others show simplified and/or improved ways to implement standard functions by utilizing the amplifier's easily accessed speed. All have been carefully (and painfully) worked out and should serve as good idea sources for potential users of the device. Have fun. I did.

APPLICATIONS SECTION I - AMPLIFIERS

Fast 12-Bit Digital-to-Analog Converter (DAC) Amplifier

One of the most common applications for a high speed amplifier, transforming a 12-bit DAC's current output into a voltage, is also one of the most difficult. Although an op amp can easily do this, care is required to obtain good dynamic performance. A fast DAC can settle to 0.01% in 200ns or less, but its output also includes a parasitic capacitance term, making the amplifier's job more difficult. Normally, the DAC's current output is unloaded directly into the amplifier's summing junction, placing the parasitic capacitance from ground to the amplifier's input. The capacitance introduces feedback phase shift at high frequencies, forcing the amplifier to hunt and ring about the final value before settling. Different DACs have different values of output capacitance. CMOS DACs have the highest output capacitance, in the 100pF-150pF range, and it varies with code. Bipolar DACs typically have 20pF-30pF of capacitance, stable over all codes. As such, bipolar DACs are almost always used where high speed is required. Figure 66 shows the popular AD565A 12-bit DAC with an LT1220 output op amp. Figure 67 shows clean 0.01% settling in 280ns (Trace B) to an all-bits-on input step (Trace A). The requirements for obtaining Trace B's display are not trivial, and are fully detailed in Appendix B, "Measuring Amplifier Settling Time".

2-Channel Video Amplifier

Figure 68 shows a simple way to multiplex two video amplifiers onto a single 75Ω cable. The appropriate amplifier is activated in accordance with the truth table in the figure[10]. Amplifier performance includes 0.02% differential gain error and 0.1° differential phase error. The 75Ω back termination looking into the cable means the amplifiers must swing 2Vp-p to produce 1Vp-p at the cable output, but this is easily handled.

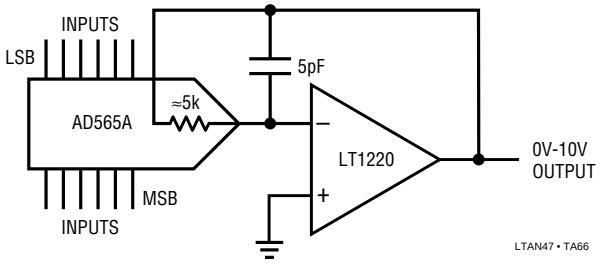


Figure 66. Typical Output Amplifier Configuration for a 12-Bit D-to-A Converter

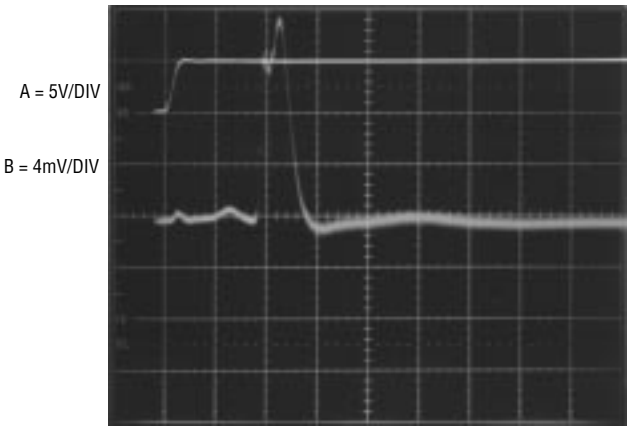


Figure 67. Settling Residue (Trace B) for All Bits Switched On (Trace A). Output is Fully Settled in 280ns

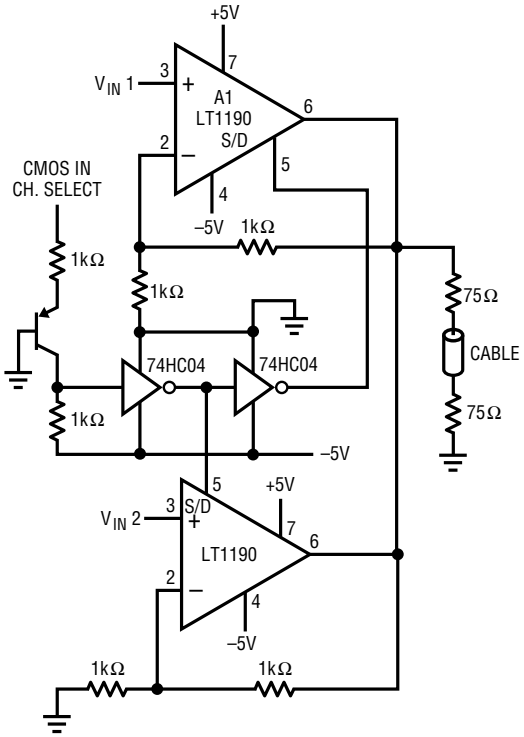
Simple Video Amplifier

Figure 69 is a simpler version of Figure 68. This is a single channel video amplifier, arranged (in this case) for a gain of ten. The double cable termination is retained and the circuit delivers a bandwidth of 55MHz.

Loop Through Cable Receivers

Figure 70 is another cable related circuit. Here, the LT1193 differential amplifier simply hangs across a distribution cable, extracting the signal. The amplifier's true differential inputs reject common-mode signals. As in the previous

Note 10: A truth table in an op amp circuit! *Et tu*, LTC!!



TRUTH TABLE

INPUT SELECT	A1 OUTPUT	A2 OUTPUT
5V	ACTIVE	INACTIVE
0V	INACTIVE	ACTIVE

LTAN47 • TA68

Figure 68. 2-Channel Multiplexed Video Amplifier

circuit, differential gain and phase errors measure 0.2% and 0.1°, respectively. A separate input permits DC level adjustment.

DC Stabilization – Summing Point Technique

Often it is desirable to obtain the precision offset of a DC amplifier with the bandwidth of a fast device. There are a variety of techniques for doing this. Which method is best is heavily application dependent, so several configurations are presented.

Figure 71 shows a composite made up of an LT1097 low drift device and an LT1191 high speed amplifier. The overall circuit is a unity gain inverter with the summing node located at the junction of the two 1k resistors. The LT1097 monitors this summing node, compares it to ground and drives the LT1191's positive input, completing a DC stabilizing loop around the LT1191. The 100kΩ-0.01μF time constant at the LT1097 limits its response to low frequency signals. The LT1191 handles high frequency inputs while the LT1097 stabilizes the DC operating point. The 4.7k-220Ω divider at the LT1191 prevents excessive input overdrive during start-up. This circuit combines the LT1097's 35μV offset and 1.5V/°C drift with the LT1191's 450V/μs slew rate and 90MHz bandwidth. Bias current, dominated by the LT1191, is about 500nA.

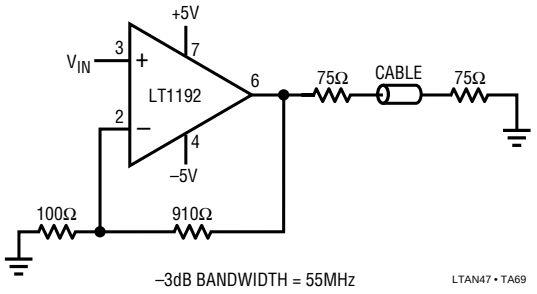


Figure 69. Double Terminated Cable Driver

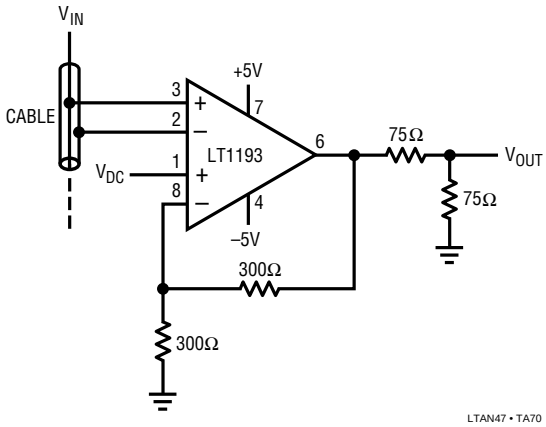


Figure 70. Cable Sense Amplifier for Loop Through Connections with DC Adjust

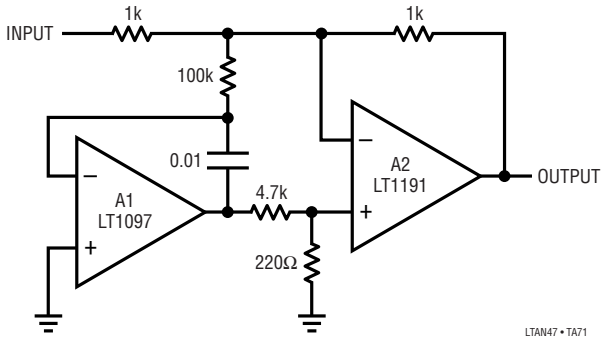


Figure 71. A1 DC Stabilizes A2 by Forcing the Summing Point to Zero

DC Stabilization – Differentially Sensed Technique

Figure 72 is similar to Figure 71, except that the sensing is done differentially, preserving access to both fast amplifier inputs. The LT1097 measures the DC error at the LT1220's input terminals and biases its offset pins to force offset within 50μV. The offset pin biasing at the LT1220 is arranged so the LT1097 will always be able to find the servo point. The 0.01μF capacitor rolls off the LT1097 at low frequency and the LT1220 handles high frequency signals. The combined characteristics of these amplifiers yield the following performance:

Offset Voltage 50μV

Offset Drift ..... 1μV/°C

Slew Rate 250V/μs

Gain-Bandwidth 45MHz

DC Stabilization – Servo Controlled FET Input Stage

Figure 73 shows a wideband, highly stable gain-of-ten with high input impedance. Input capacitance is about 3pF. Q1 and Q2 constitute a simple, high speed FET input buffer. Q1 functions as a source follower, with the Q2 current source load setting the drain-source channel current. The LT1223 provides a 100MHz bandwidth gain of ten. Normally, this open loop configuration would be quite drifty because there is no DC feedback. The LT1097 contributes this function to stabilize the circuit. It does this by comparing the filtered circuit output to a similarly filtered version of the input signal. The amplified difference between these signals is used to set Q2's bias, and hence Q1's channel current. This forces Q1's V_{GS} to whatever voltage is required to match the circuit's input and output potentials. The capacitor at A1 provides stable loop compensation. The RC network in A1's output prevents it from seeing high speed edges coupled through Q2's collector-base junction.

This circuit constitutes an extremely wideband (Q1 does not degrade A2's 100MHz performance), high input impedance amplifier. With an input capacitance of 3pF and

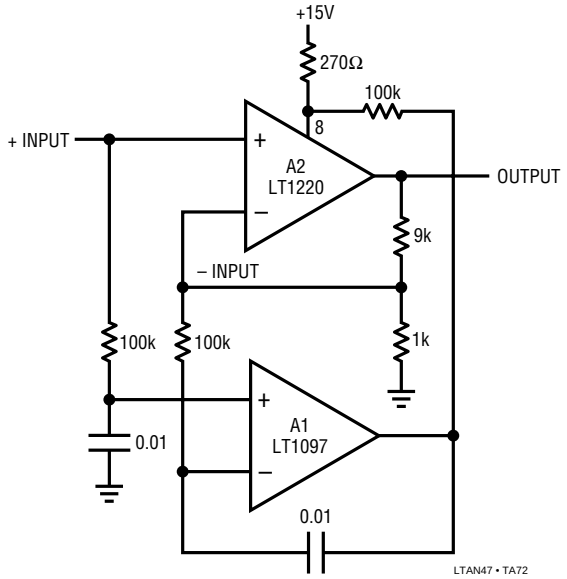


Figure 72. A1 DC Stabilizes A2 by Forcing the Offset Pins to Produce a 0V Difference at A2's Inputs

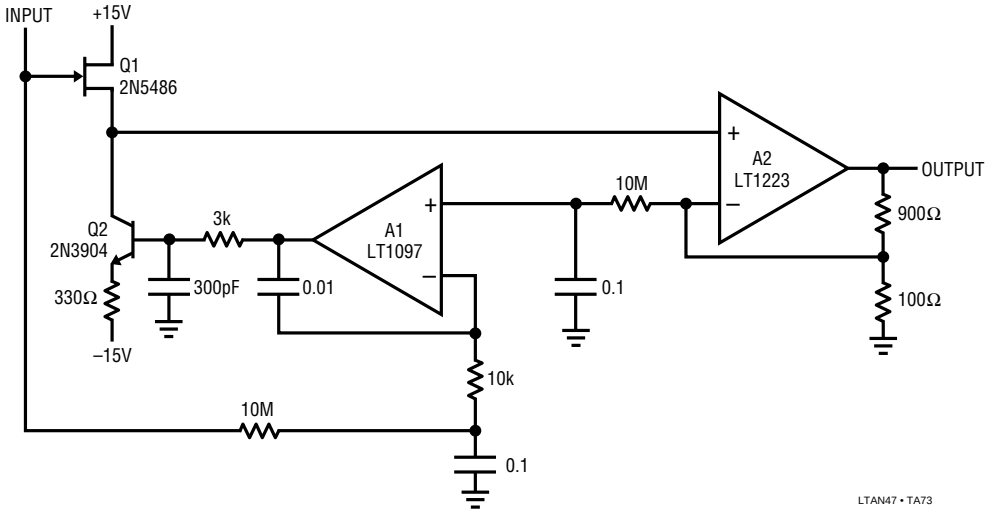


Figure 73. A1 DC Stabilizes the Circuit by Controlling Q1's Channel Current

bias current of 100pA, it is well suited for probing or as an ATE pin amplifier. As shown, gain is ten, but other gains are possible by varying the feedback ratio.

DC Stabilization – Full Differential Inputs with Parallel Paths

Figure 74 shows a way to get full differential inputs with DC stabilized operation. This circuit combines the output of two differential input amplifiers for overall DC corrected wideband operation. A1 and A2 both differentially sense the input at gains of ten. Wideband A1 feeds output amplifier A3 via a highpass network, while the slower A2 contributes DC and low frequency information to A3. A2 does not see high frequency inputs, because they are filtered by the 2k-200pF lowpass networks at its inputs. If the gain and bandwidth of the high and low frequency paths complement each other, A3's output should be an undistorted, amplified version (in this case × 10) of the input. Figure 75 shows this to be the case. Trace A is one side of a differential input applied to the circuit. Trace B is A1's output taken at the 500Ω potentiometer - 0.001μF junction. Trace C is A2's output. With the AC gain and DC gain match trims properly adjusted, the two paths' contributions match up and Trace D is singularly clean, with no residue. The adjustments are optimized by trimming the AC gain for the squarest corners and the DC gain match for a flat top. Bandwidth for this circuit exceeds 35MHz, slew rate is 450V/μs and DC offset about 200μV.

Note 11: For assistance in following circuit signal flow, the schematic of this device is included in the figure.

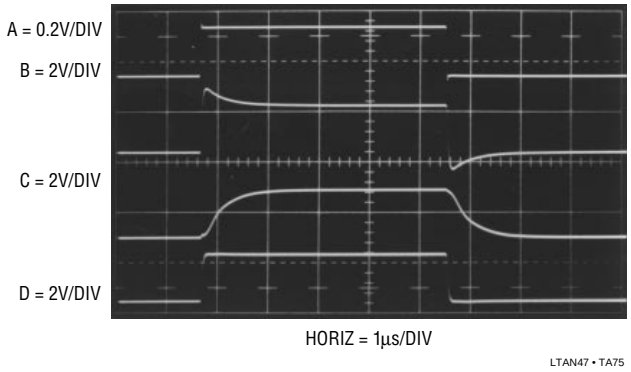


Figure 75. Waveforms for the Parallel Path Differential Amplifier. Trace A is the Input; B, C and D are the High Pass, Low Pass and Output Nodes, Respectively

DC Stabilization – Full Differential Inputs, Gain-of-1000 with Parallel Paths

Figure 76 is a very powerful extension of the previous circuit. Operation is similar, but gain is increased to 1000. Bandwidth is about 35MHz, rise time equals 7ns and delay is inside 7.5ns. Full power response is available to 10MHz, with input noise about 15μV broadband. This kind of speed, coupled with full differential inputs, the gain of 1000, DC stability, and low cost make the circuit broadly applicable in wideband instrumentation. As before, two differential amplifiers, A1 and A2, simultaneously sense the inputs. In this case A1 is the popular and economical 592-733 type, operating at a gain of 100.[11] A1's differential outputs feed output amplifier A3 via 1μF-1kΩ high pass networks which strip off A1's DC content. A2, a precision DC differential type, operates in similar fashion to the previous circuit, supplying DC and low frequency

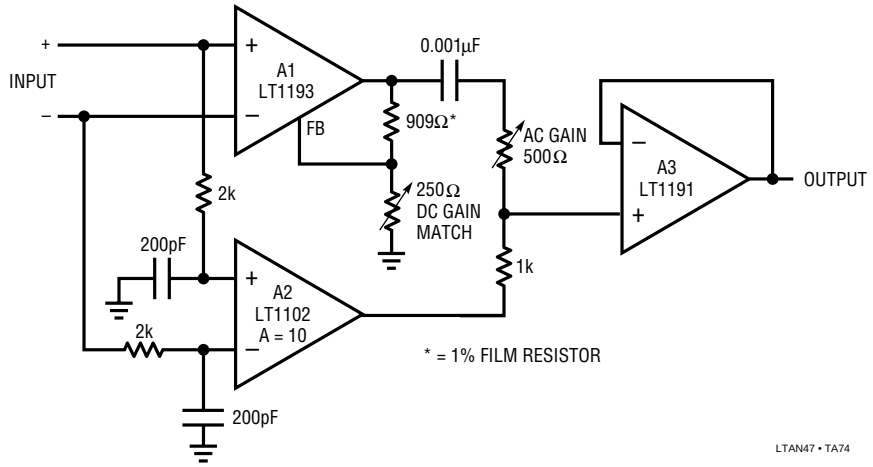


Figure 74. A Parallel Path DC Stabilized Differential Amplifier. High Frequency Signals Go through A1, while A2 Handles DC and Low Frequency. A3 Sums Both Paths

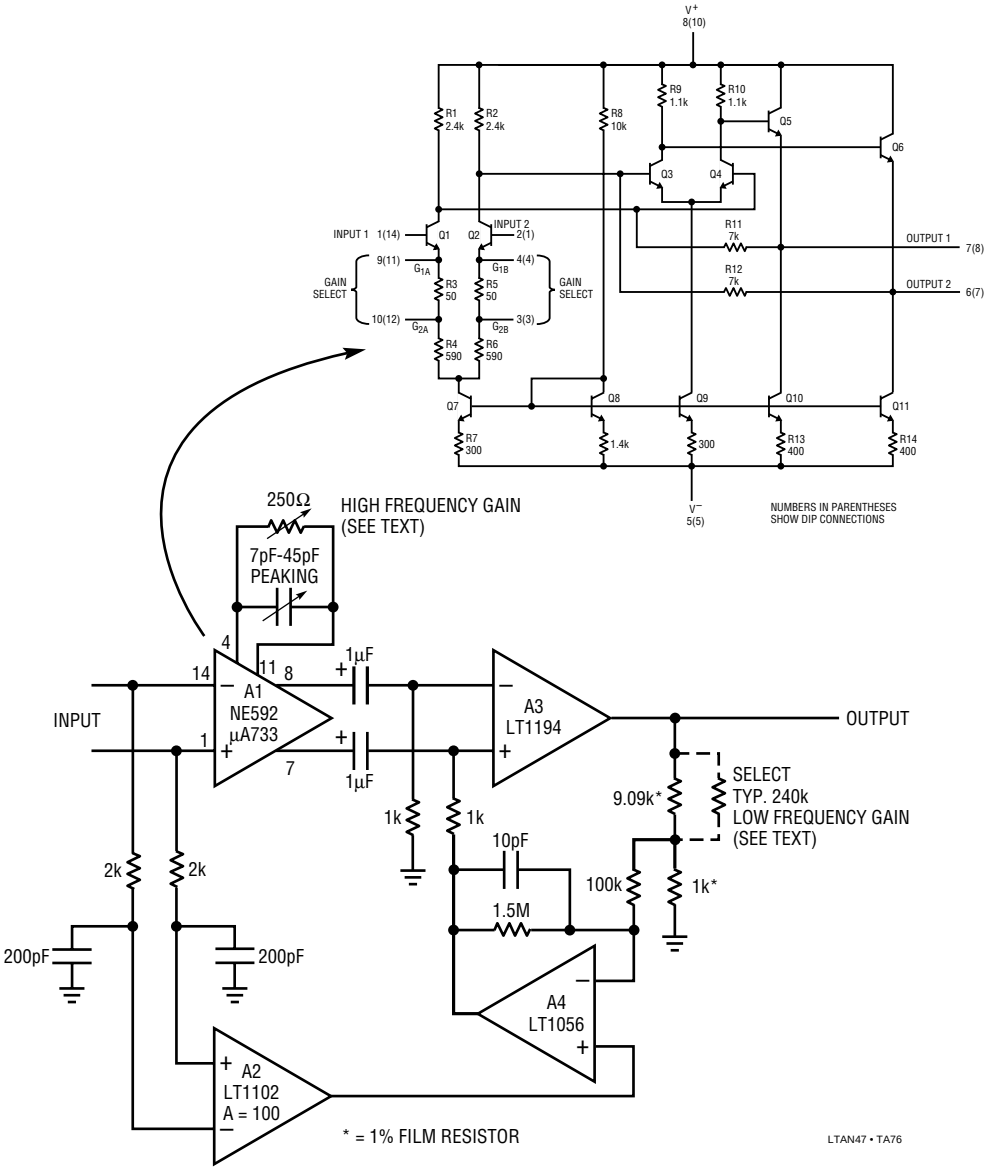


Figure 76. A Full Differential, Parallel Path Amplifier. Gain is 1000, with 38MHz Bandwidth. Delay is Inside 7.5ns and Rise Time Under 7ns

information to A3 at a trimmed gain of 100. In this case output amplifier A3 is a differential gain block with a nominal committed gain of 10. This change is necessitated by A1's differential output, which must be single-ended to obtain the circuit's output. As such A2 does not directly apply its low frequency information to A3 as it did before. Instead, A4 measures the difference between A2's output and a divided down portion of A3's output. A4's output, biasing A3's positive input via the 1kΩ resistor, closes a loop around the circuit's DC-low frequency path. The divider feeding A4's negative input is adjusted so that the circuit's DC gain is known and equal to its AC gain.

Figure 77 shows the circuit's response to a 60ns, 2.5mV amplitude pulse (Trace A). The X1000 output (Trace B) responds cleanly, with delay and rise time in the 5ns-7ns range. Some small amount of peaking is evident, although it may be trimmed with the peaking adjustment at A1. Figure 78 plots the circuit's gain vs frequency. Gain is flat within 1/2dB to 20MHz, with the –3dB point at 38MHz. Figure 77's edge peaking shows up here as a very slight gain increase starting around 1MHz and continuing out to about 15MHz. The peaking trim will eliminate this effect.

To use this circuit, put in a low frequency or DC signal of known amplitude and adjust the low frequency gain for a

X1000 output after the output has settled. Next, adjust the high frequency gain so that the signal's front and rear corners have amplitudes identical to the settled portion. Finally, trim the peaking adjustment for best settling of the output pulse's front and rear corners.

Figure 79 shows input (Trace A) and output (Trace B) waveforms with all adjustments properly set. Fidelity is excellent, with no aberrations or other artifacts of the parallel path operation evident. Figure 80 shows the effects of too much AC gain; excessive peaking on the edges with proper amplitude indicated only after the AC channel transitions through its highpass cut off. Similarly, excessive DC gain produces Figure 81's traces. The AC gain path

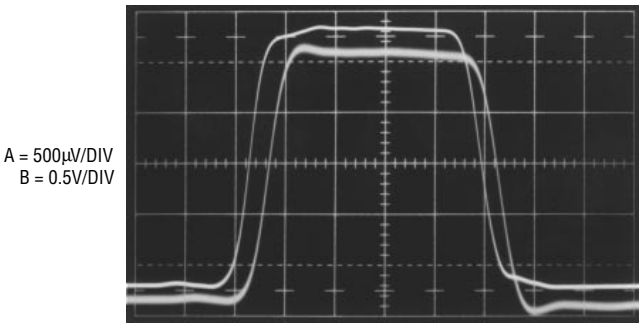


Figure 77. Pulse Response for the X1000 Differential Amplifier. Fidelity is Quite Good, with Only Slight Output Peaking (Trace B)

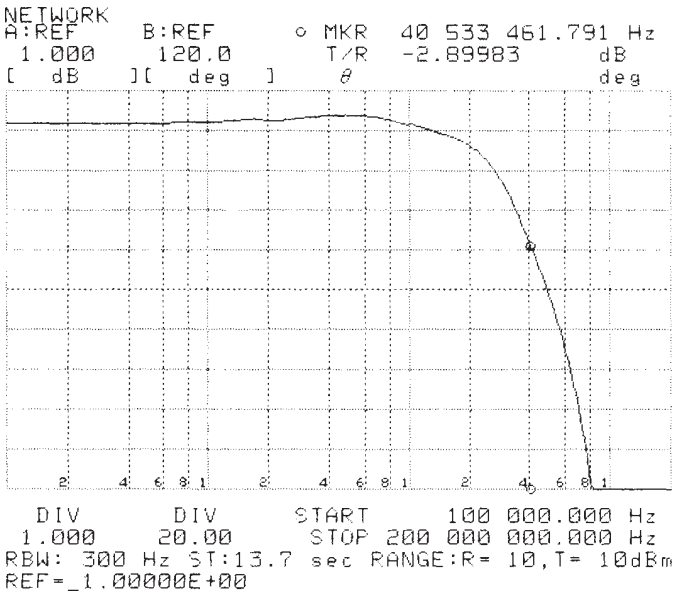


Figure 78. Gain vs Bandwidth for the X1000 Differential Amplifier. Peaking Noted in Figure 77 Shows up as 0.25dB Peak at 5MHz, Which Could be Trimmed Out

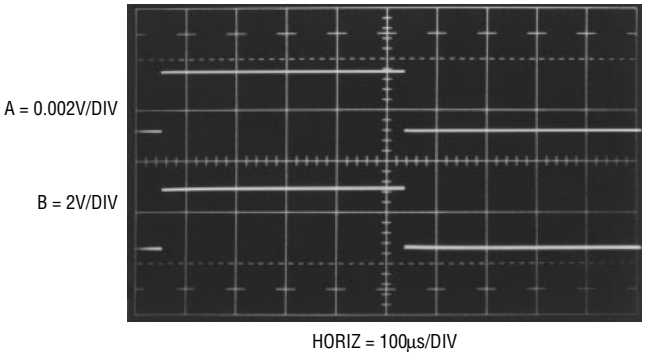


Figure 79. Response of X1000 Amplifier with Bandwidth Crossover Points Properly Adjusted. A = Input; B = Output

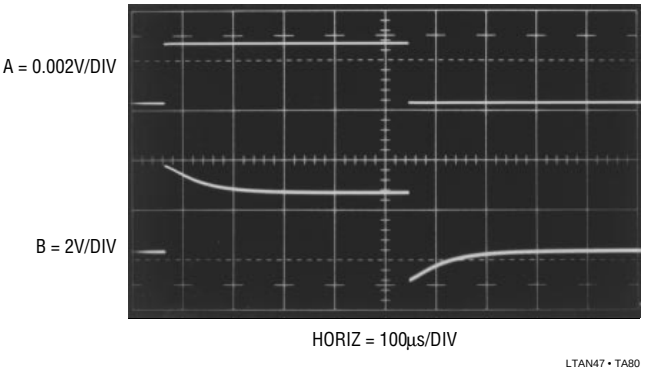


Figure 80. Response of X1000 Amplifier with Excessive AC Gain. A = Input; B = Output

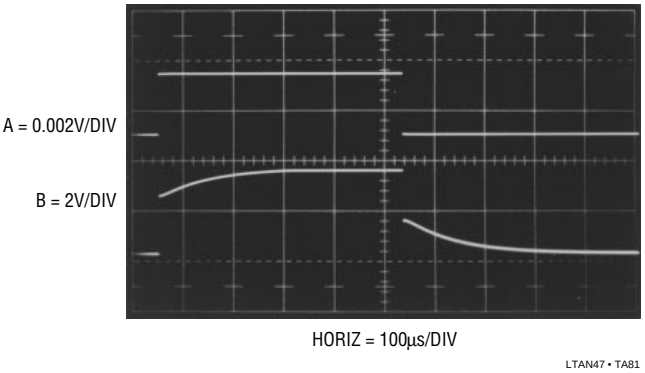


Figure 81. Response of X1000 Amplifier with Too Much DC Gain. A = Input; B = Output

provides proper initial response, but too much DC gain forces a long, tailing response to an incorrect amplitude.

High Speed Differential Line Receiver

High speed analog signals transmitted on a line often pick up substantial common-mode noise. Figure 82 shows a simple, fast differential line receiver using the LT1194

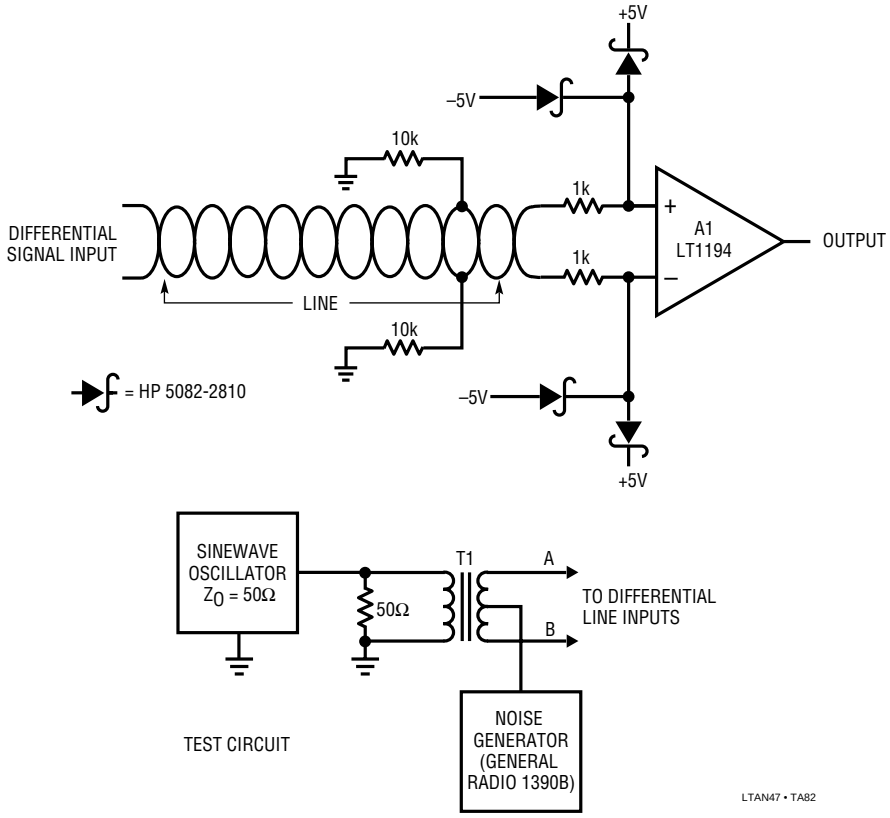


Figure 82. Simple, Full Differential Line Receiver

gain-of-ten differential amplifier. The differential line is fed to A1. The resistor-diode networks prevent overload and insure input bias for A1 under all conditions. A1's output represents the difference of the two line input times a gain of ten. In theory, all common-mode noise should be rejected. The test circuit shown in the figure confirms this. The sinewave oscillator drives T1 (Trace A, Figure 83), producing a differential line output at its secondary. T1's secondary is returned to ground through a broadband noise generator, flooding the line inputs with common-mode noise (traces B and C are A1's inputs). Trace D, A1's X10 version of the differential signal at its inputs, is clean with no visible noise or disturbances. This circuit will easily provide a clean output with DC-5MHz noise dominating signal by a 100:1 ratio.

Transformer Coupled Amplifier

Figure 84 shows another way to achieve high common-mode rejection. Additionally, this circuit has the advantage of true 3 port isolation. The input, gain stage, and output are all galvanically isolated from each other. As such, this configuration is useful where large common-mode differences are encountered or where ground integrity is uncertain. A1 is set up in a simple gain of 11. T1 feeds its input, and the output is taken from T2. Figure 85 shows results for a 4MHz input, with all "•" designated transformer leads referred to ground. The input (Trace A, Figure 85) is applied to T1, whose output (Trace B) feeds A1. A1 takes gain, and its output (Trace C) feeds T2. T2's output

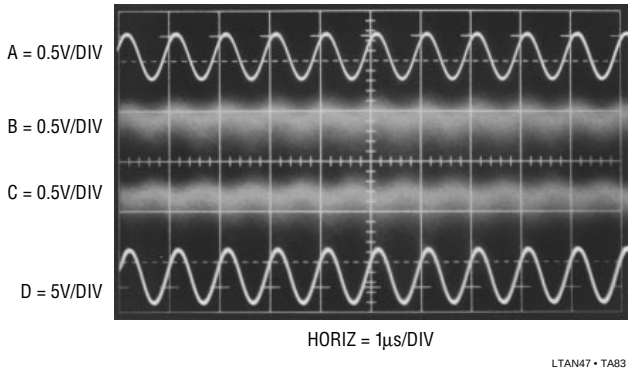


Figure 83. Differential Line Receiver Easily Pulls Out a Signal Buried in Common-Mode Noise. Output is Clean, Despite 100:1 Noise-to-Signal Ratio

(Trace D) is the circuit's output. Phase shift is evident, although tolerable. T1 and T2 are very wideband devices, with low phase shift. Note the negligible phase difference between the A-B and C-D trace pairs. A1 contributes essentially the entire phase error. Using the transformers specified, the circuit's low frequency cut-off is about 10kHz.

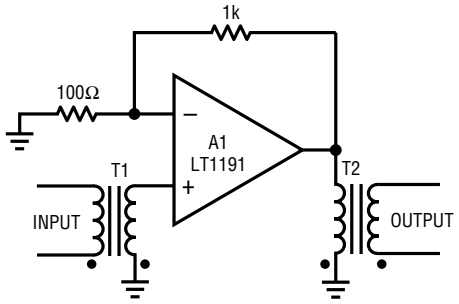


Figure 84. Transformer Coupled Amplifier. Note That A1 is Galvanically Isolated From Input and Output Nodes

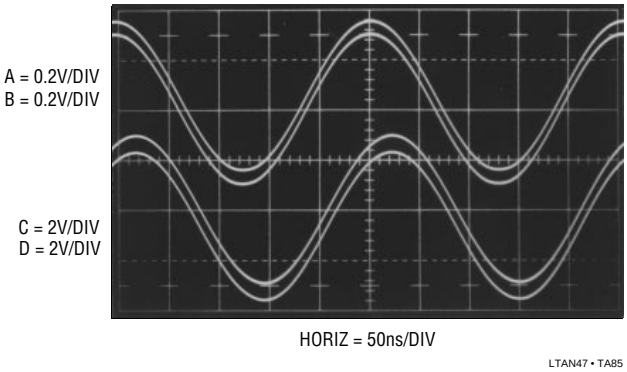


Figure 85. Transformer Coupled Amplifier Responds to an Input (Trace A) with A Slightly Phase Shifted Output (Trace D). Traces B and C are T1 Secondary and T2 Primary, Respectively

Differential Comparator Amplifier with Adjustable Offset

It is often desirable to examine or amplify one particular portion of a signal while rejecting all other portions. At high speed this can be difficult, because the amplifier may see fast, large common-mode swings. Recovery from such activity usually is dominated by saturation effects, making the amplifier's output questionable. The LT1193's differential amplifier's fast overload recovery permits this function, maintaining output fidelity to the input signal. Additionally, the input level amplitude at which amplification begins is settable, allowing any amplitude defined point to be selected. In Figure 86, A1, the LT1019 reference and associated components form an adjustable, bipolar voltage source which is coupled to differential amplifier A2's negative input. The input signal biases A2's positive input with A2's gain set by R1 and R2, in accordance with the equation given.

Input signals below A2's negative input levels maintain A2's output in saturation, and no signal is seen at the output. When the positive input rises above the negative input's bias point A2 becomes active, providing an amplified version of the instantaneous difference between its inputs. Figure 87 shows what happens when the output of a triangle wave generator (Trace A) is applied to the circuit. Setting the bias level just below the triangle peak permits high gain, detailed operation of the turnaround at the peak. Switching residue in the generator's output is clearly observable in Trace B. Appropriate variations in the voltage source setting would permit more of the triangle

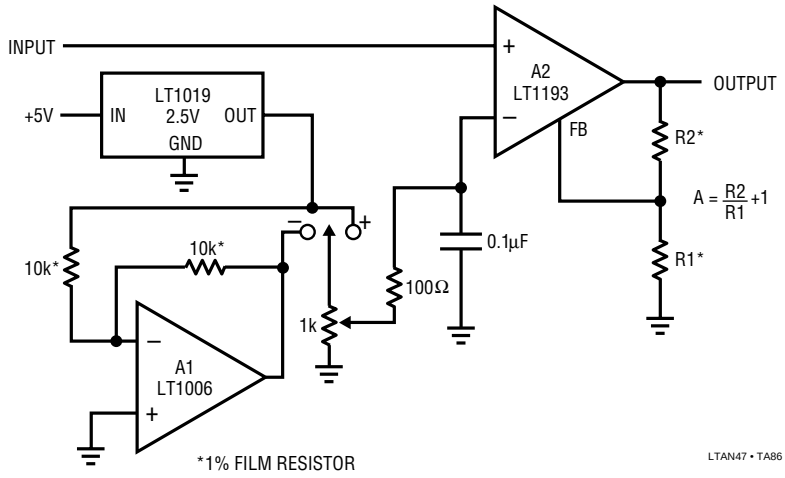


Figure 86. Fast Differential Comparator Amplifier with Settable Offset

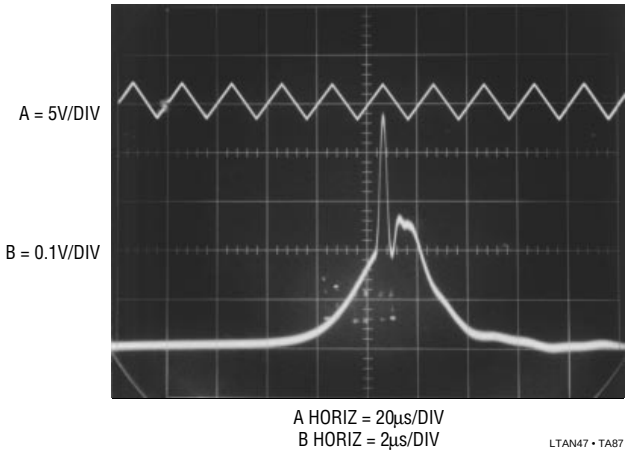


Figure 87. The Differential Comparator Amplifier Extracting Signal Detail From a Triangle Waveform's Peak. Triangle Generator's Switching Artifacts are Clearly Evident

slopes to be observed, with attendant loss of resolution due to oscilloscope overload limitations. Similarly, increasing A2's gain allows more amplitude detail while placing restrictions on how much of the waveform can be displayed. It is worth noting that this circuit performs the same function as differential plug-in units for oscilloscopes. This circuit's output is accurate and settled to 0.1% 100ns after it enters its linear region.

Differential Comparator Amplifier with Settable Automatic Limiting and Offset

Figure 88 extends the previous circuit's operation, allowing amplified observation of information between two settable, amplitude defined points. The amplitude setpoints are settable in both magnitude and sign. In this circuit the polarity of the offset applied to A2's negative input is

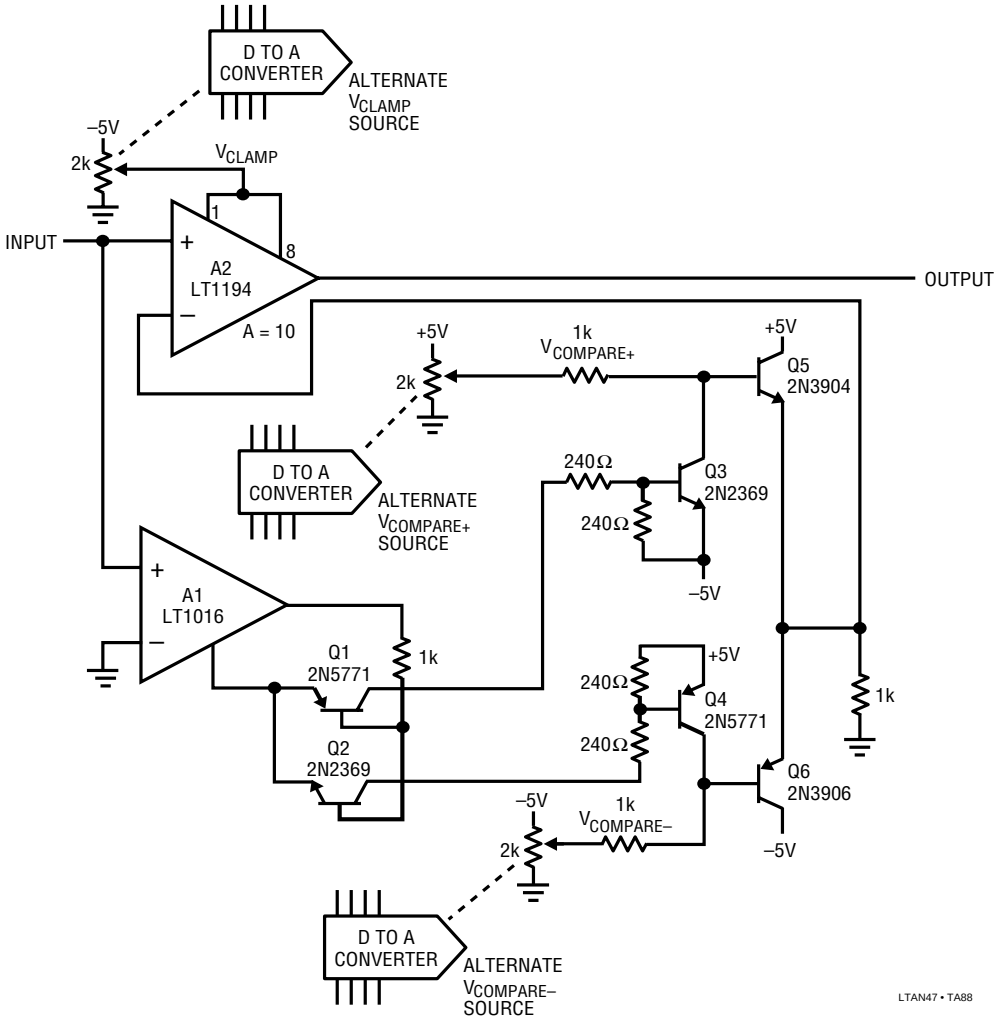


Figure 88. Differential Comparator Amplifier with Settable Automatic Limiting and Offset

determined by comparator A1's output state. A1 compares the circuit's input to ground, generating polarity information at its outputs. Level shifters Q1-Q3 and Q2-Q4 bias followers Q5 and Q6. Positive circuit inputs result in Q5 supplying the "$V_{COMPARE+}$" potential to A2, while negative inputs route "$V_{COMPARE–}$" to A2. This eliminates the previous circuit's manual polarity switch, permitting automatic selection of the differencing polarity and amplitude. Additionally, this circuit takes advantage of A2's input clamp feature. This feature (See LT1194 Data Sheet) limits the dynamic range of the input, clamping the amplifier's input operating range. Signals inside the clamp limit are processed normally, while signals outside the limit are precluded from influencing the amplifier. This combination of circuit controls allows very tightly defined windows on a waveform to be selected for accurate amplification without overload restrictions.

Figure 89 shows the circuit output for a sine input (Trace A) from the same function generator used to test the previous circuit. The V^+ and V^- compare voltages are set just below the sinewave peaks, with "V_{clamp}" programmed to restrict amplification to the peak's excursion. Trace B, the circuit's output, simultaneously shows amplitude detail of *both* sine peaks. The observed distortion is directly traceable to this generator's imperfect internal triangle waveform (see Figure 87), as well as its sine shaper characteristics.

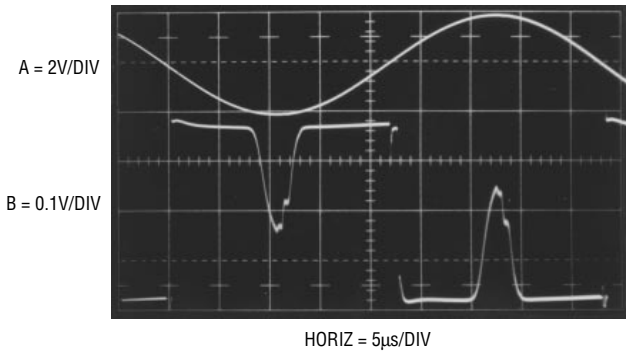


Figure 89. The Automatic Differential Comparator Amplifier Finds Triangle Wave and Switching Residuals (Trace B) in Trace A's Peaks

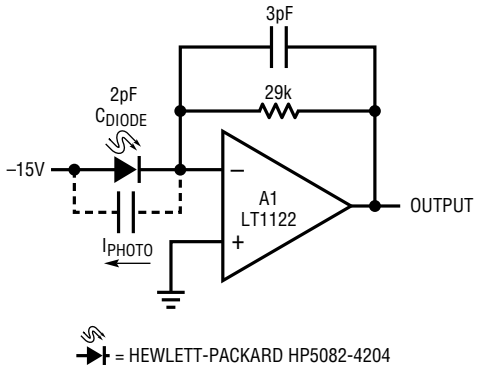
Photodiode Amplifier

Amplification of fast photodiode signals over a wide range of intensity is a common requirement. Figure 90's fast FET amplifier serves well, giving wideband operation with 5 decades of photocurrent. The photodiode is set up in the conventional manner. Photocurrent is fed directly to A1's summing point, causing A1's output to move to the level required to maintain virtual ground at the negative input. The –15V diode bias aids diode response. The table in the figure details circuit operating characteristics with the diode specified.

Some care in frequency compensating this configuration is required. The diode has about 2pF of parasitic capacitance, forming a significant lag at A1's summing point. If no feedback capacitor is used, high speed dynamics are poor. Figure 91 shows circuit response to a photo input (Trace A) with the indicated 3pF feedback capacitor removed. A1's output overshoots and saturates before finally ringing down to final value. In contrast, replacing the 3pf capacitor provides Figure 92's results. The same input pulse (Trace A, Figure 92) produces a cleanly damped output (Trace B). The capacitor imposes a 50% speed penalty (note faster horizontal scale for Figure 92). This is unavoidable because suppressing the parasitic ringing's relatively low frequency mandates significant roll-off.

Fast Photo Integrator

A related circuit to the photodiode amplifier is Figure 93's photo integrator. Here, the output represents the integral of the diode's photocurrent over some period of time. This



RESPONSE DATA

LIGHT (900nM)	DIODE CURRENT	CIRCUIT OUTPUT
1mW	350µA	10.0V
100µW	35µA	1V
10µW	3.5µA	0.1V
1µW	350nA	0.01V
100nW	35nA	0.001V

Figure 90. A Simple Photodiode Amplifier

circuit is particularly applicable in situations where the total energy in a light pulse (or pulses) must be measured. The circuit is a very fast integrator, with S1 used as a reset switch. S2, switched simultaneously with S1, compensates S1's charge injection error. With the control input (Trace A, Figure 94) low and no photocurrent, S1 is closed and A1 looks like a grounded follower. Under these conditions A1's output (Trace C) sits at 0V. When the control input goes high, A1 becomes an integrator as soon as S1 opens. Due to switch delay, this occurs about 150ns after the control input goes high. When S1 opens it delivers some parasitic charge to A1's summing point. S2 provides a compensatory charge based pulse at A1's positive terminal to cancel the effects of S1's charge error. This action shows up as a fast, small amplitude event in A1's output which settles rapidly back to 0V.

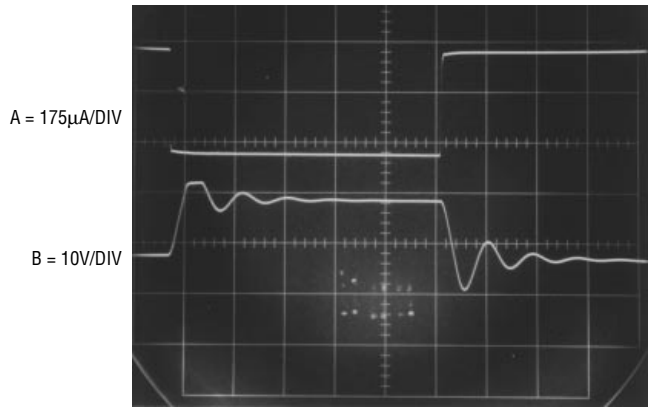


Figure 91. Response of Figure 90 Without a Feedback Capacitor

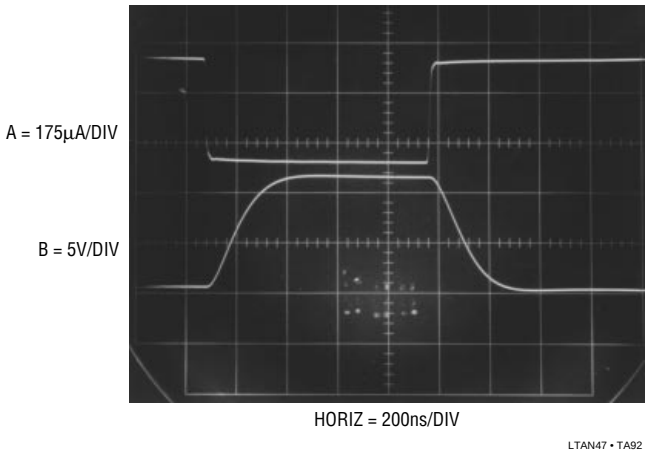


Figure 92. Figure 90 Responding with a Feedback Capacitor

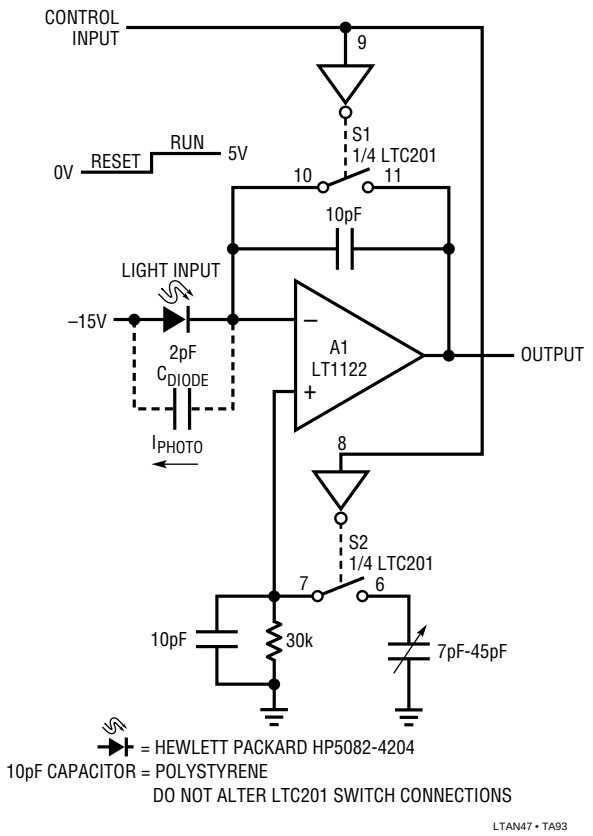


Figure 93. A Very Fast Photo Integrator. S2 Compensates Reset Switch S1's Small Charge Injection

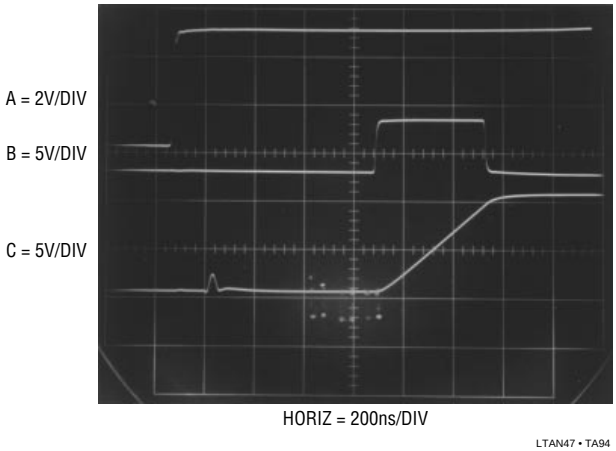


Figure 94. The Photo Integrator Acquires (Trace C) an Input Light Pulse (Trace B) with the Control Line (Trace A) in the Run Mode. Charge Cancellation Action is Evident at Trace C's 400ns Point

At this point in time the integrator is ready to receive and record a photo pulse. When light falls on the photodiode (Trace B triggers a light pulse seen by the photodiode) A1 responds by integrating. In this case A1's output integrates rapidly until the light pulse ceases. A1's voltage after the light event is over is related to the total energy seen by the diode during the event. A monitoring A-D converter can acquire A1's output. In typical operation the control line returns low, resetting A1 until the next event is to be integrated.

With only 10pF of integration capacitor, the circuit has an output droop rate of about 0.2V/µs. This can be increased, although integration speed will suffer accordingly. Integration times of nanoseconds to milliseconds and photocurrents ranging from nanoamperes to hundreds of microamperes are accommodated by the circuit as shown. Thus, light intensities spanning microwatts to milliwatts over wide ranges of duration are practical inputs. The primary accuracy restrictions are A1's 75pA bias current, its 12V output swing and the effectiveness of the charge cancellation network. Typically, full-scale accuracy of several percent is achievable if the charge cancellation network is trimmed. To do this, assure that the diode sees no light while repetitively pulsing the control line. Adjust the trimmer capacitor for 0V output at A1 immediately after the disturbance associated with the S1-S2 switching settles.

Fiber Optic Receiver

A simple high speed fiber optic receiver appears in Figure 95. A1, a photocurrent-to-voltage converter similar to Figure 90, feeds comparator A2. A2 compares A1's output

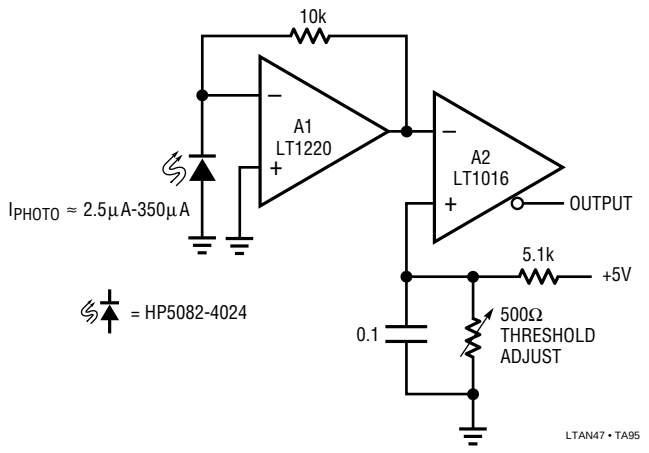


Figure 95. A Simple Fiber Optic Receiver

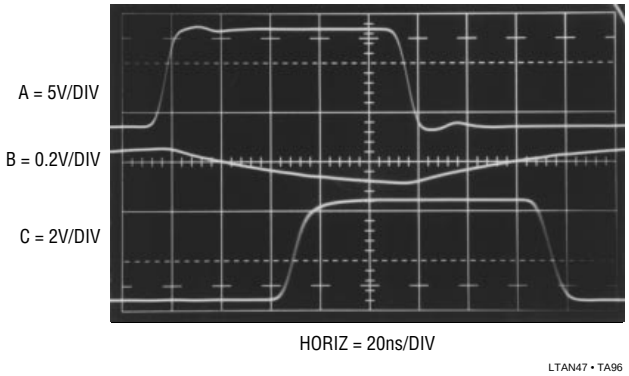


Figure 96. Waveforms for the Simple Fiber Optic Receiver. A1 (Trace B) Lags the Input (Trace A), but Output (Trace C) is Clean

to a DC level established by the threshold adjust setting, producing a logic compatible output. Figure 96 shows typical waveforms. Trace A is a pulse associated with a photo input. Trace B is A1's response and Trace C is A2's output. The phase shift between the photo input and A2's output is due to A1's delay in reaching the threshold level. Reducing the threshold level will help, but moves operation closer to the noise floor. Additionally, the fixed threshold level cannot account for response changes in the emitter and detector diodes and fiber optic line over time and temperature.

40MHz Fiber Optic Receiver with Adaptive Trigger

Receiving high speed fiber optic data with wide input amplitude variations is not easy. The high speed data and uncertain intensity of the light level can cause erroneous results unless the receiver is carefully designed. Figure 97 addresses the previous circuit's limitations, offering significant performance advantages. This receiver will reliably condition fiber optic inputs of up to 40MHz with input amplitude varying by >40dB. Its digital output features an adaptive threshold trigger which accommodates varying signal intensities due to component aging and other causes. An analog output is also available to monitor the detector output. The optical signal is detected by the PIN photodiode and amplified by A1. A second stage, A2, gives further amplification. The output of this stage biases a 2-way peak detector (Q1-Q4). The maximum peak is stored in Q2's emitter capacitor, while the minimum excursion is retained in Q4's emitter capacitor. The DC value of A2's output signal's mid-point appears at the junction of the 500pF capacitor and the 22MΩ units. This point will always sit midway between the signal's excursions, re-

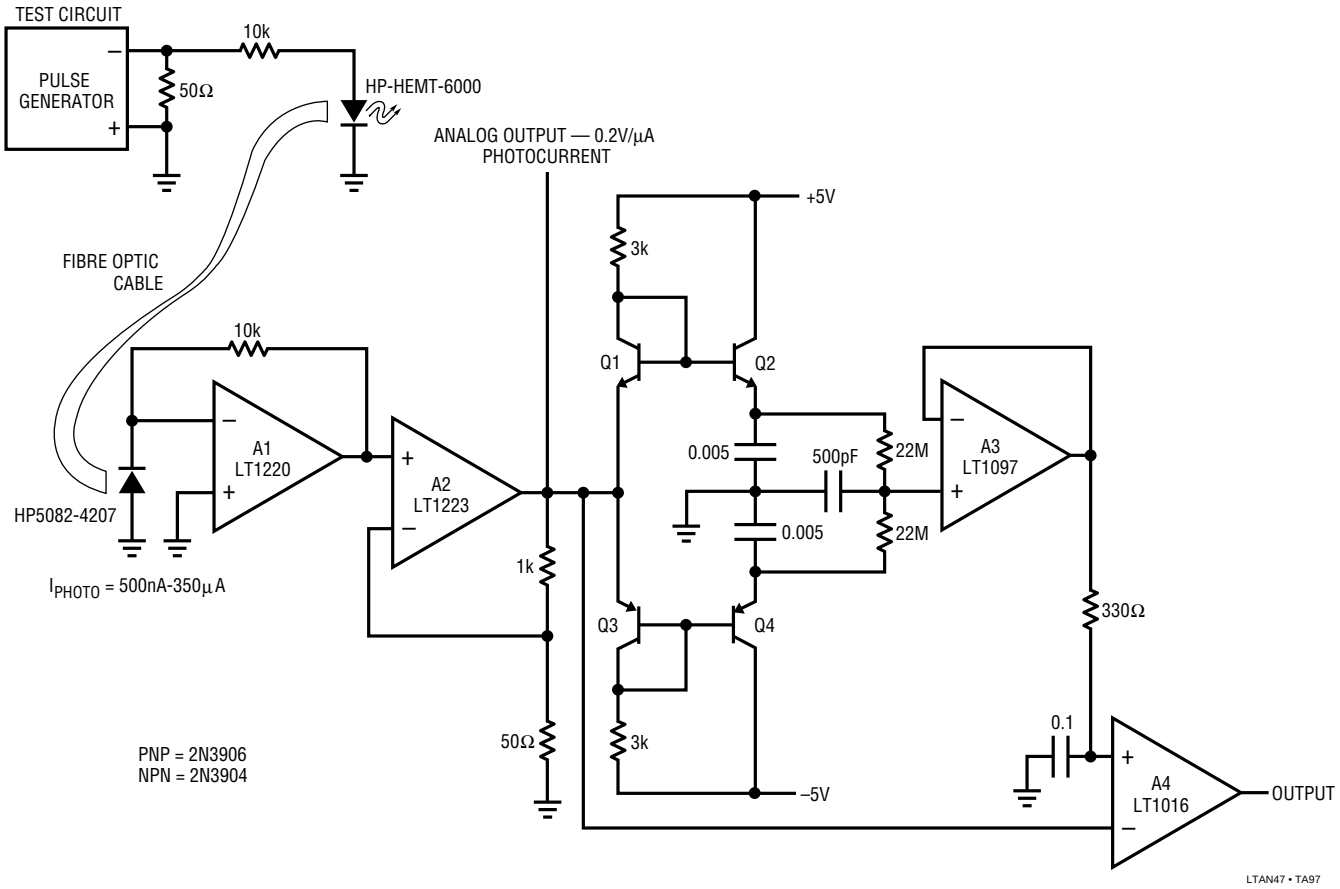


Figure 97. Adaptively Triggered 40MHz Fiber Optic Receiver is Immune to Shifts in Operating Point

gardless of absolute amplitude. This signal-adaptive voltage is buffered by the low bias LT1097 to set the trigger voltage at the LT1016's positive input. The LT1016's negative input is biased directly from A2's output. Figure 98 shows the results using the test circuit indicated in Figure 97. The pulse generator's output is Trace A, while A2's output (analog output monitor) appears in Trace B. The LT1016 output is Trace C. The waveforms were recorded with a 5μA photocurrent at about 20MHz. Note that A4's output transitions correspond with the midpoint of A2's output (plus A4's 10ns propagation delay) in accordance with the adaptive trigger's operation.

50MHz High Accuracy Analog Multiplier

Although highly accurate, very wideband analog multipliers are available, their output takes a differential form. These differential outputs, which have substantial common mode content, are frequently inconvenient to work with. RF transformers can be used to single end the outputs, but DC and low frequency information is lost. Figure 99 uses the LT1193 differential amplifier to accomplish the differential-to-single ended transition. The AD834 is set up in the recommended configuration (see Analog Devices AD834 Data Sheet, Reference 26). The LT1193 takes the differential signal from the AD834's 50Ω terminated output and provides a single ended output. The gain of two yields a ±1V output at full-scale.

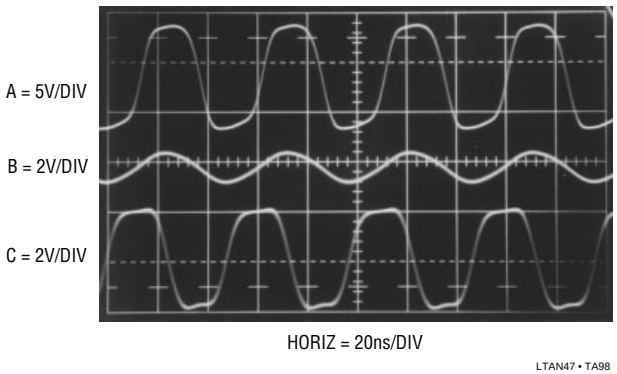


Figure 98. Adaptively Triggered Fiber Optic Receiver's Waveforms at 20MHz with 5μA Diode Current

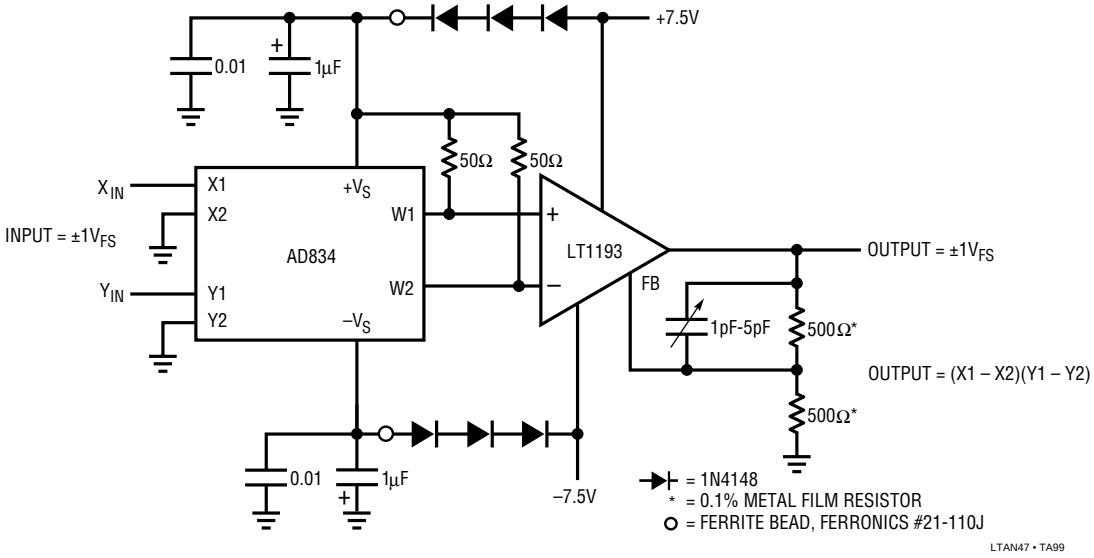


Figure 99. Analog Multiplier with 2% Accuracy Over DC to 50MHz Has a Single Ended Output

The AD834 outputs come out riding on a common-mode level very close to the devices positive supply. This common-mode level falls outside the LT1193's input common-mode range. The diodes in the 7.5V supply rails drop the supply at the AD834, biasing its outputs within the LT1193's input range. This scheme avoids the attenuation and matching problems presented by placing a level shift between the multiplier and amplifier. The ferrite beads combine with the diode's impedance to ensure adequate bypassing for the multiplier, a very wideband device.

Performance for this circuit is quite impressive. Error remains within 2% over DC-50MHz, with feedthrough below –50dB. Trimming the circuit involves adjusting the variable capacitor at the amplifier for minimal output square wave peaking. Figure 100 shows performance when a 20MHz sine input is multiplied by Trace A's waveform. The output (Trace B) is a singularly clean instantaneous representation of the X•Y input products, with strict fidelity to their components.

Power Booster Stage

Occasionally, it is necessary to supply larger output currents than an amplifier is capable of delivering. The power gain stage, sometimes called a booster, is usually placed within the monolithic amplifier's feedback loop, preserving the IC's low drift and stable gain characteristics.

Because the output stage resides in the amplifier's feedback path, loop stability is a concern. This is particularly the case with high speed amplifiers. The output stage's gain and AC characteristics must be considered if good dynamic performance is to be achieved. Overall circuit phase shift, frequency response and dynamic load handling capabilities are issues that cannot be ignored when designing a power gain stage for a monolithic amplifier. The output stage's added gain and phase shift can cause poor AC response or outright oscillation. Judicious application of frequency compensation methods is needed for good results (see Appendix C, "The Oscillation Problem – Frequency Compensation Without Tears", for discussion and details on compensation methods).

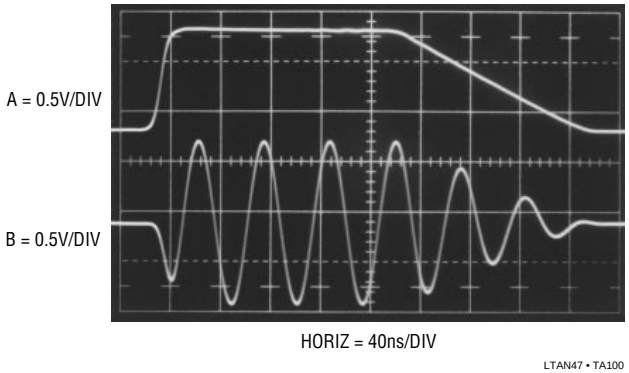


Figure 100. The Multiplier Produces a Modulated Sine Output (Trace B) in Accordance with Trace A's Envelope

Figure 101 shows a 200mA power booster used with an LT1220 amplifier. Complementary emitter followers Q1-Q5 provide current gain for positive signals, with Q2 and Q6 handling negative excursions. Q3 and Q4 are V_{BE} based current limits, coming on and robbing drive from the appropriate output transistor when current exceeds about 300mA. The diodes prevent Q1 and Q2 from seeing reverse V_{BE} during current limit. The 100Ω resistor and ferrite beads prevent the low impedance amplifier output from causing oscillation in Q1 and Q2 (see Appendix C).

To be effective, the booster must be exceptionally fast. A slow design will obviate the AC performance of the amplifier controlling it, or in the worst case, cause oscillation (again, see Appendix C). Figure 102 shows booster performance with the LT1220 removed from the circuit. The input pulse (Trace A) is applied to the booster input, with the output (Trace B) taken at the indicated spot. Evaluation of the photograph shows that booster rise and fall times are limited by the input pulse generator. Additionally, delay is in the 1ns range. This kind of speed makes the circuit a good candidate for acceptable AC performance within a fast amplifier's loop.

Figure 103 shows pulse response with the LT1220 installed in the circuit with a 50Ω load. The booster's high speed contributes negligible delay and overall response is clean and predictable. The local 3pF roll-off at the LT1220 optimizes response, but is not absolutely necessary in this circuit. The input (Trace A) produces a nicely shaped LT1220 slew-limited output (Trace B).

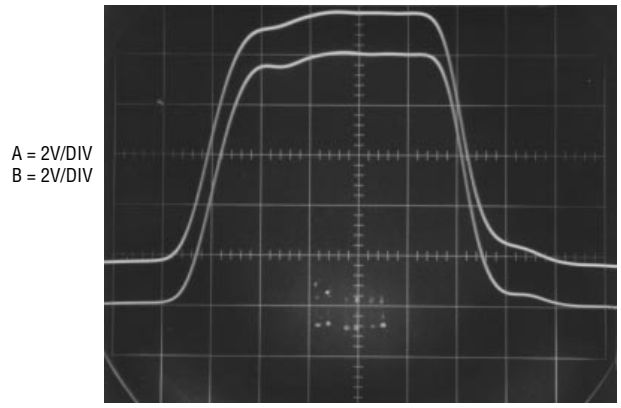


Figure 102. Response of Figure 101's Booster Stage

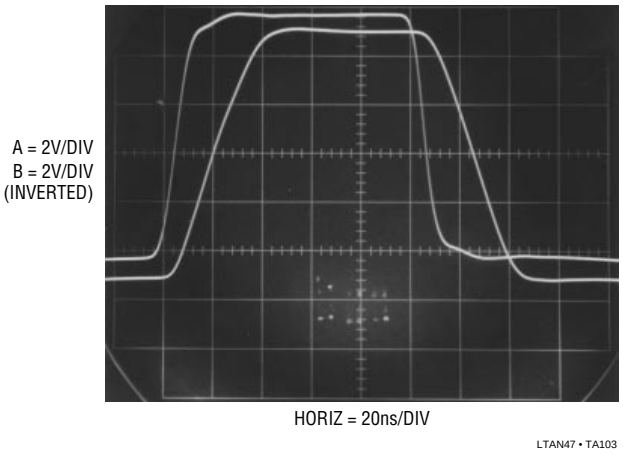


Figure 103. The Booster's Response When Inside an Amplifier's Loop

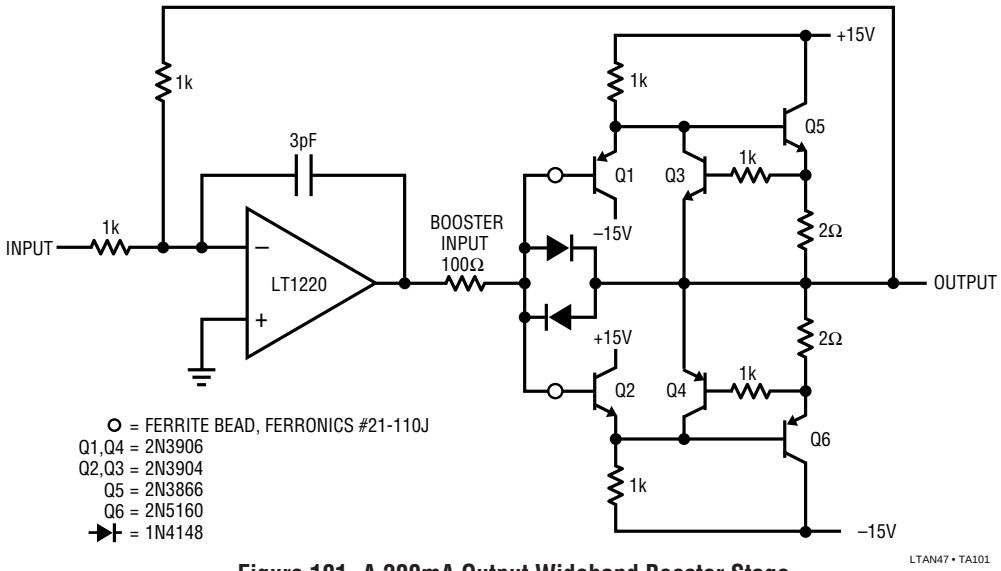


Figure 101. A 200mA Output Wideband Booster Stage

High Power Booster Stage

In theory, higher power booster stages should be achievable by utilizing bigger devices. This is partly the case, but lack of availability of wideband PNP power transistors is an issue. Figure 104 shows a way around this problem.

The circuit is essentially a 1A output version of Figure 101, with several differences. In the positive signal path output transistor Q4 is an RF power type, driven by Darlington connected Q3. The diode in Q1's emitter compensates the additional V_{BE} introduced by Q3, preventing crossover distortion.

The negative signal path substitutes the Q5-Q6 connection to simulate a fast PNP power transistor. Although this configuration acts like a fast PNP follower, it has voltage gain and tends to oscillate. The local 2pF feedback capacitor suppresses these parasitic oscillations and the composite transistor is stable.

This circuit also includes a feedback capacitor trim to optimize AC response. This difference from the previous circuit is necessitated by this circuit's slightly slower characteristics and much heavier loading. Current limit operation and other characteristics are similar to the lower power circuit.

Figure 105 shows waveforms for a 10V negative input step (Trace A) with a 10Ω load. The amplifier responds (Trace B), driving the booster to the voltage required to close the loop. For this positive step, the amplifier provides about 1.5V overdrive to overcome Q3 and Q4's V_{BE} drops. The booster output, lagging by a few nanoseconds (Trace C), drives the load cleanly, with only minor peaking. This peaking may be minimized with the feedback capacitance trimmer.

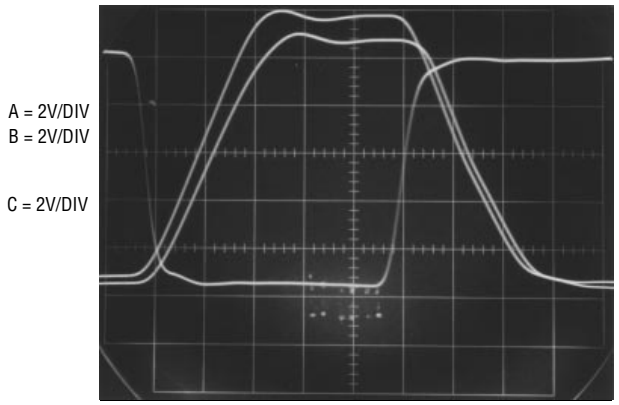


Figure 105. The Boosted Op Amp Drives a 1A Load to 10V in 50ns

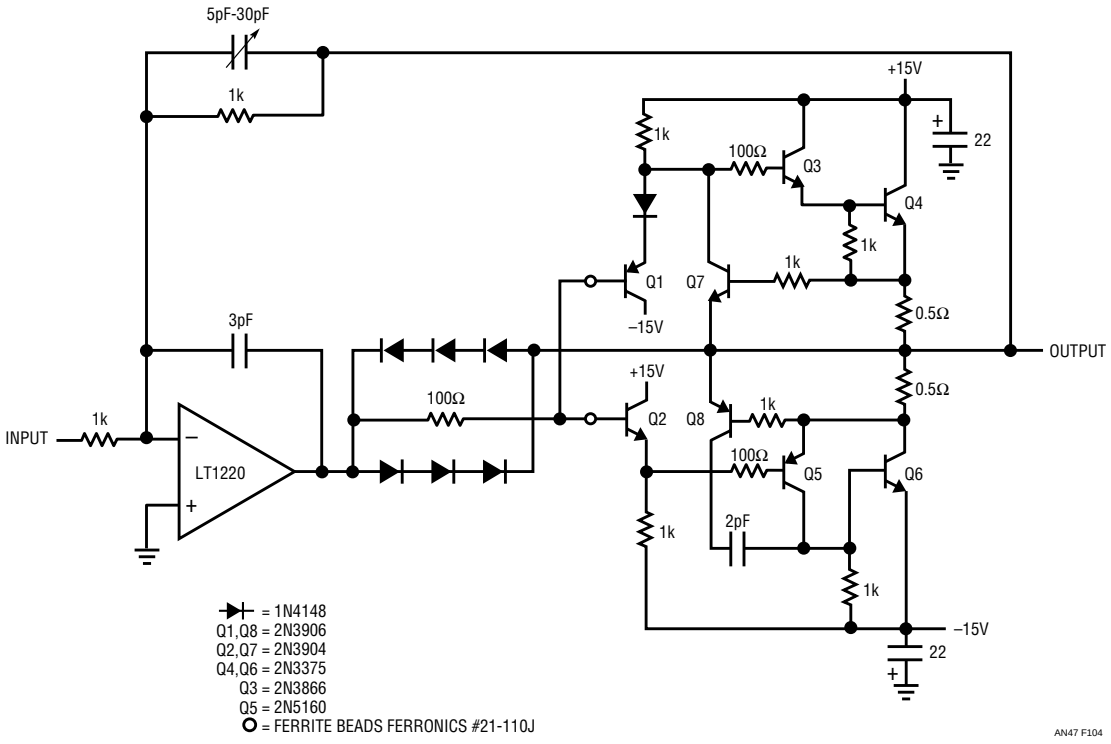


Figure 104. Fast, 1A Booster Stage

Ceramic Bandpass Filters

Figure 106 is a highly selective bandpass filter using a resonant ceramic element and a single amplifier. The ceramic element nominally looks like a high impedance off its resonant frequency, in this case 400kHz. For off resonance inputs, A1 acts like a grounded follower, producing no output. At resonance, the ceramic element has a low impedance and A1 responds as an inverter with gain. The 100Ω resistor isolates the ceramic element's capacitance from A1's summing point. This capacitance is quite substantial and limits the circuits out of band rejection capability. Figure 107 shows this. This plot shows very steep rejection, with A1's output down almost 20dB at 300kHz and 40dB at 425kHz. The device's stray parasitic capacitance causes the gentle rise in output at higher frequencies and also sets the –20dB floor at 300kHz.

Figure 108 partially corrects this problem with a nulling technique. This circuit is similar to the previous one, except that a portion of the input is fed to A1's positive input. The RC network at this input is scaled to look like the ceramic resonator's off null impedance. As such, A1's inputs see similar signals for out of band components,

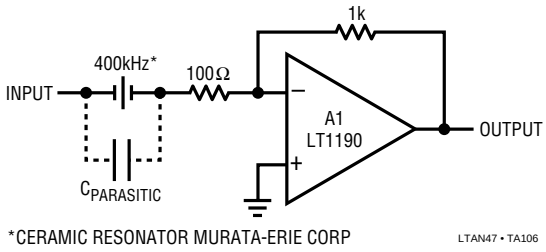


Figure 106. A Piezo-Ceramic Based Filter

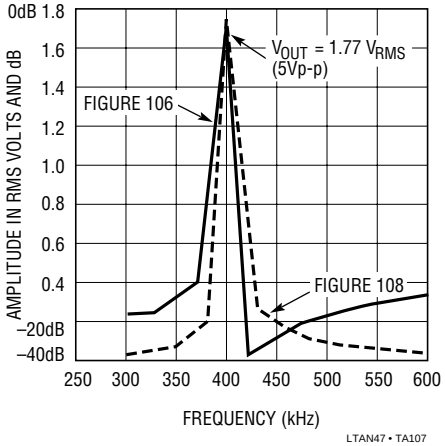


Figure 107. Response of Both Piezo-Ceramic Filters. Differential Network's Activity is Evident in Figure 108's Performance

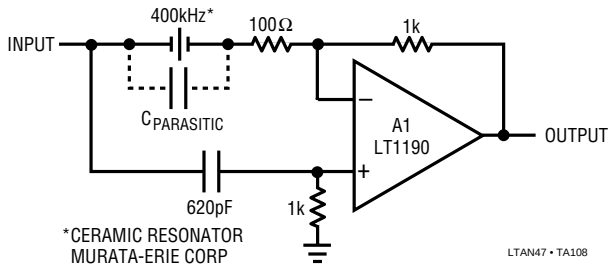


Figure 108. Differential Network Nulls Parasitic Capacitance of Ceramic Element

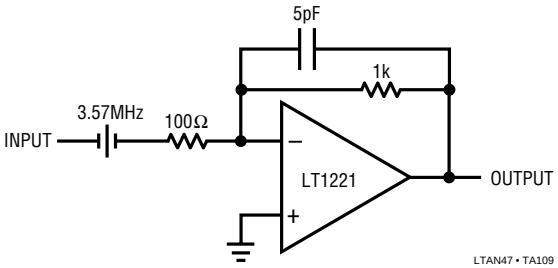


Figure 109. Crystal Filter

resulting in attenuation via A1's common-mode rejection. At resonance, the added RC network appears as a much higher impedance than the ceramic element and filter response is similar to Figure 106's circuit. Figure 107 shows that this circuit has much better out of band rejection than Figure 106. The high frequency roll-off is smooth, and over 20dB deeper than Figure 106 at 475kHz. The low frequency side of resonance has similar characteristics at 375kHz and below.

Crystal Filter

Quartz crystals can also be used to make even higher selectivity filters at higher frequencies. Figure 109 replaces Figure 106's ceramic element with a 3.57MHz quartz crystal. Figure 110 shows almost 30dB attenuation only a few kHz on either side of resonance! The differential nulling technique used with the ceramic elements is less effective with quartz crystals. Crystals have significantly lower parasitic terms, making the cancellation less effective.

APPLICATIONS SECTION II - OSCILLATORS

Sine Wave Output Quartz Stabilized Oscillator

Figure 111 places a crystal within the amplifier's feedback path, creating an oscillator. With the crystal removed, the

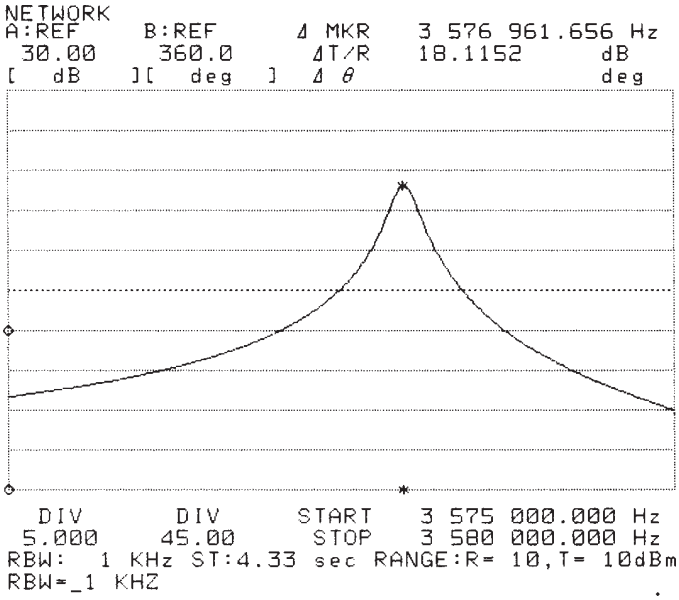


Figure 110. The Crystal Filter's Response

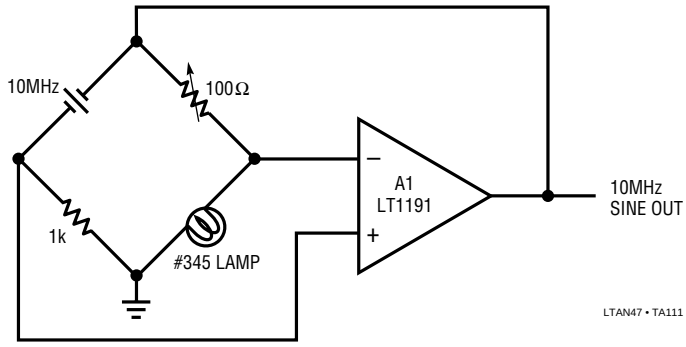


Figure 111. 10MHz Quartz Stabilized Sine Wave Oscillator

circuit is a familiar non-inverting amplifier with a grounded input. Gain is set by the impedance ratio of the elements associated with A1's negative input. Inserting the crystal closes a positive feedback path at the crystal's resonant frequency and oscillations commence.

In any oscillator it is necessary to control the gain as well as the phase shift at the frequency of interest. If gain is too low, oscillation will not occur. Conversely, too much gain produces saturation limiting. Here, gain control comes from the positive temperature coefficient of the lamp at A1's negative input. When power is applied, the lamp is at a low resistance value, gain is high and oscillation amplitude builds. As amplitude builds, lamp current increases, heating occurs, and the lamp's resistance goes up. This causes a reduction in amplifier gain and the circuit finds a stable operating point. This circuit's sine wave output has all the stability advantages associated with quartz crystals. Although shown at 10MHz, it works well with a wide variety of crystal types over a 100kHz-20MHz range. The use of the lamp to control amplifier gain is a classic technique, first described by Meacham in 1938.[12] Electronic gain control, while more complex, offers more precise control of amplitude.

Sine Wave Output Quartz Stabilized Oscillator with Electronic Gain Control

Figure 112's quartz stabilized oscillator replaces the lamp with an electronic amplitude stabilization loop. A2 compares the A1 oscillator's positive output peaks with a DC reference. The diode in the DC reference path temperature compensates the rectifier diode. A2 biases Q1, controlling its channel resistance. This influences loop gain, which is reflected in oscillator output amplitude. Loop closure around A1 occurs, stabilizing oscillator amplitude. The 1μF capacitor compensates the gain control loop.

The DC reference network is set up to provide optimum temperature compensation for the rectifier diode, which sees a 2Vp-p 20MHz waveform out of A1. A1's small amplitude swing minimizes distortion introduced by channel resistance modulation in Q1. To use this circuit, adjust the 50Ω trimmer until 2Vp-p oscillations appear at A1's output.

Figure 113 is a spectrum analysis of the oscillator's output. The fundamental sits at 20MHz, with the second harmonic 47dB down at 40MHz. A third harmonic, 50dB down, occurs at 60MHz. Resolution bandwidth for the spectrum analysis is 1kHz.

DC Tuned 1MHz-10MHz Wien Bridge Oscillator

In Figure 114 the quartz crystal is replaced with a Wien network at A2's positive input. A1 controls Q1 to amplitude stabilize A2's oscillations in identical fashion to the previous figure. Although the Wien network is not nearly as stable as a quartz crystal, it has the advantage of a variable frequency output. Normally, this is facilitated by varying either R, C, or both. Usually, manually adjustable elements such as dual potentiometers and two section variable

Note 12: See Reference 20, as well as References 19 and 21 for supplemental information.

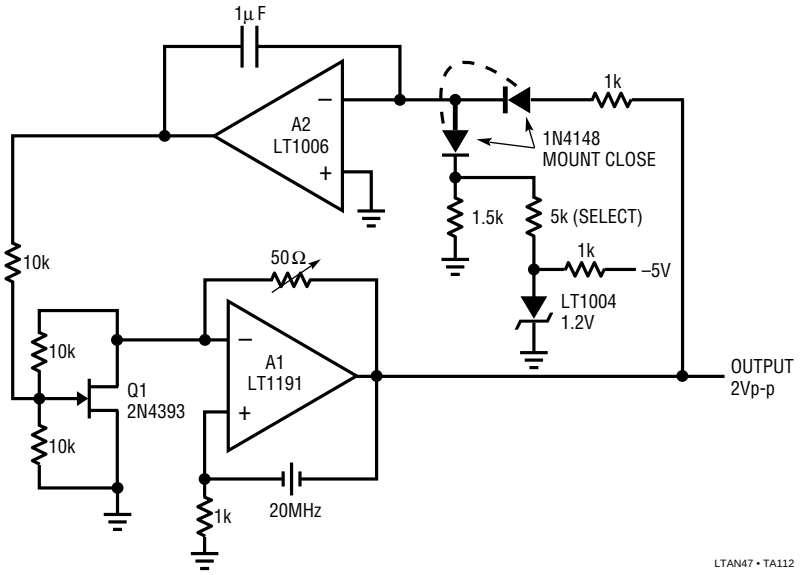


Figure 112. 20MHz Quartz Stabilized Sine Wave Oscillator with Electronic AGC

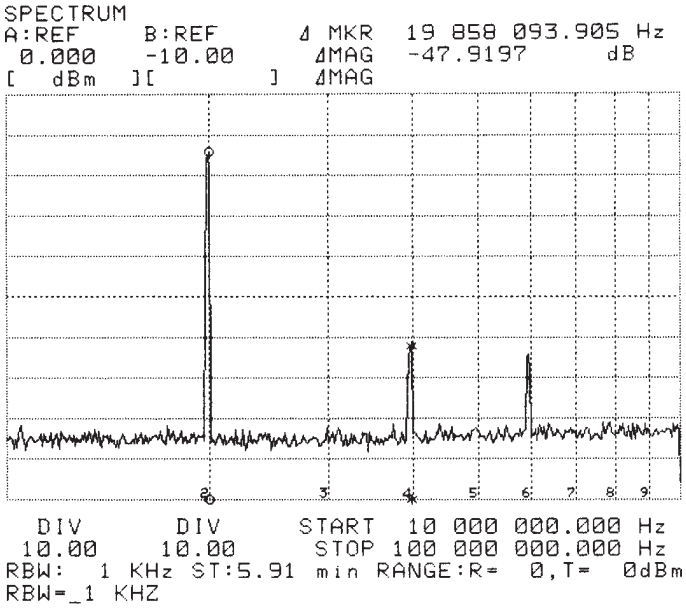


Figure 113. Spectrum Analysis of the 20MHz Quartz Oscillator. Harmonic Content is at Least 47dB Down

capacitors are used. Here, the Wien network resistors are fixed at 360Ω, while the capacitive elements are realized with varactor diodes. The varactor diodes voltage-variable-capacitance characteristic allows DC tuning of the oscillator. DC inputs of 0V-10V to the varactors result in a 1MHz to 10MHz shift in oscillation frequency. The 0.1µF capacitor blocks the DC bias from A2's positive input while permitting the Wien network to function normally. A2's 2Vp-p output minimizes the varactor's junction effects, aiding distortion.

This ±5V powered circuit requires voltage step-up to develop adequate varactor drive. A3 and the LT1172 switching regulator form a simple voltage step-up regulator. A3 controls the LT1172 to produce the output voltage required to close a loop at A3's negative input. L1's high voltage inductive flyback events, rectified by the diode and zener connected Q2, are stored in the 22µF output capacitor. The 7.5k-2.5k divider provides a sample of the output's value to A3's negative input, closing the loop. The 0.1µF capacitor stabilizes this feedback action. Q2's zener drop allows the circuit to produce controlled outputs all the way down to 0V. This arrangement permits a 0V-2.5V input at A3 to produce a corresponding 0V-10V varactor bias. Figure 115, a spectral plot of the circuit running at 7.6MHz, shows the second harmonic down 35dB, with the third harmonic down almost 60dB. Resolution bandwidth is 3kHz.

Complete AM Radio Station

A complete microphone-to-antenna AM radio station appears in Figure 116.[13] The carrier is generated by A1, set up as a quartz stabilized oscillator similar to the one described in Figure 111. A1's output feeds A2, functioning as a modulated RF power output stage. A2's input signal range is restricted by the bias applied to offset pins 1 and

Note 13: The construction and operation of this apparatus may require Federal Communications Commission review and/or licensing. See Appendix G for FCC licensing and application information.

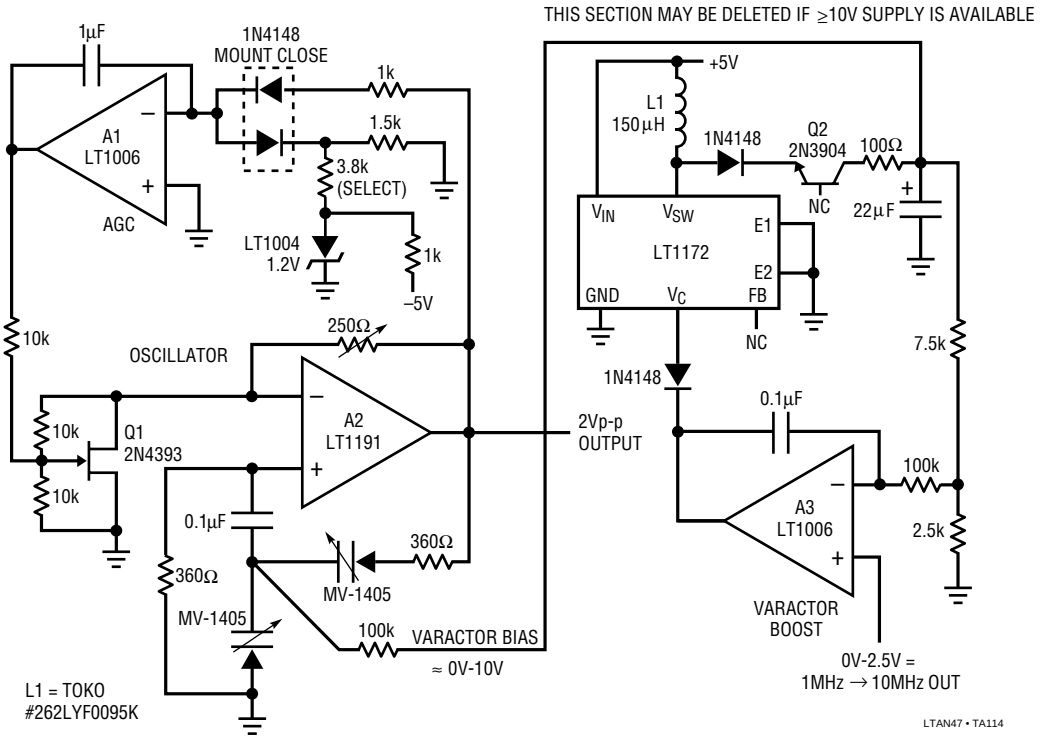


Figure 114. Varactor Tuned 1MHz-10MHz Wien Bridge Oscillator

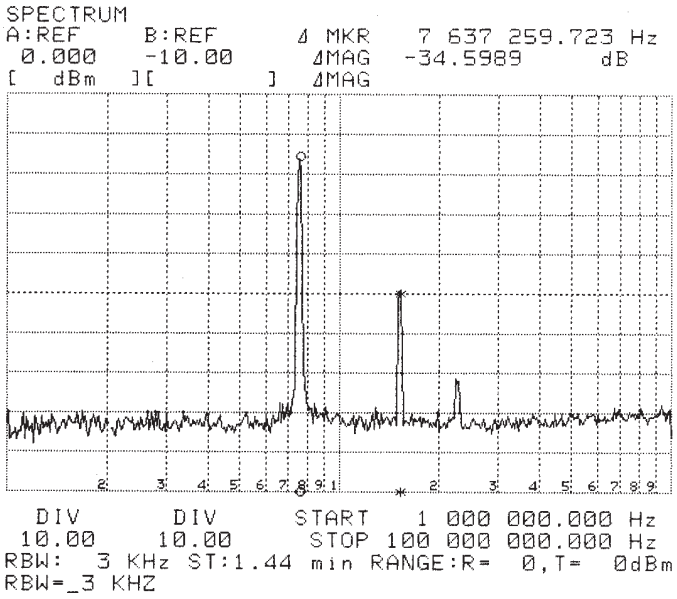


Figure 115. Spectrum Analysis for the Varactor Tuned Wien Bridge. Harmonics are at Least 34dB Down From Fundamental

8 (see LT1194 data sheet for details). A3, a microphone amplifier, supplies bias to these pins, resulting in an amplitude modulated RF carrier at A2's output. The DC term summed with the microphone biases A3's output to the appropriate level for good quality modulation characteristics. Calibration of this circuit involves trimming the 100Ω potentiometer in the oscillator for a stable 1Vp-p 1MHz A1 output.[14]

Figure 117 shows typical AM carrier output at the antenna. In this case the modulation is supplied by Mr. Chuck Berry, singing "Johnny Be Goode".

APPLICATIONS SECTION III - DATA CONVERSION

1Hz-1MHz Voltage-Controlled Sine Wave Oscillator

The oscillators presented to this point have limited frequency tuning range. Although Figure 118 is not a true oscillator, it produces a synthesized sine wave output over a wide dynamic range. Many applications such as audio, shaker table driving and automatic test equipment require voltage-controlled oscillators (VCO) with a sine wave output. This circuit meets this need, spanning a 1Hz-1MHz range (120dB or 6 decades) for a 0V to 10V input. It maintains 0.25% frequency linearity and 0.40% distortion specifications.[15] To understand the circuit, assume Q5 is

Note 14: Operating frequency subject to FCC approval and assignment. See Footnote 13 and Appendix G.

Note 15: Seasoned readers of LTC literature, a hardened corps, may recognize this and other circuits in this publication as updated versions of previous LTC applications. The partial repetition is justified based on improved specifications and/or simplification of the original circuit.

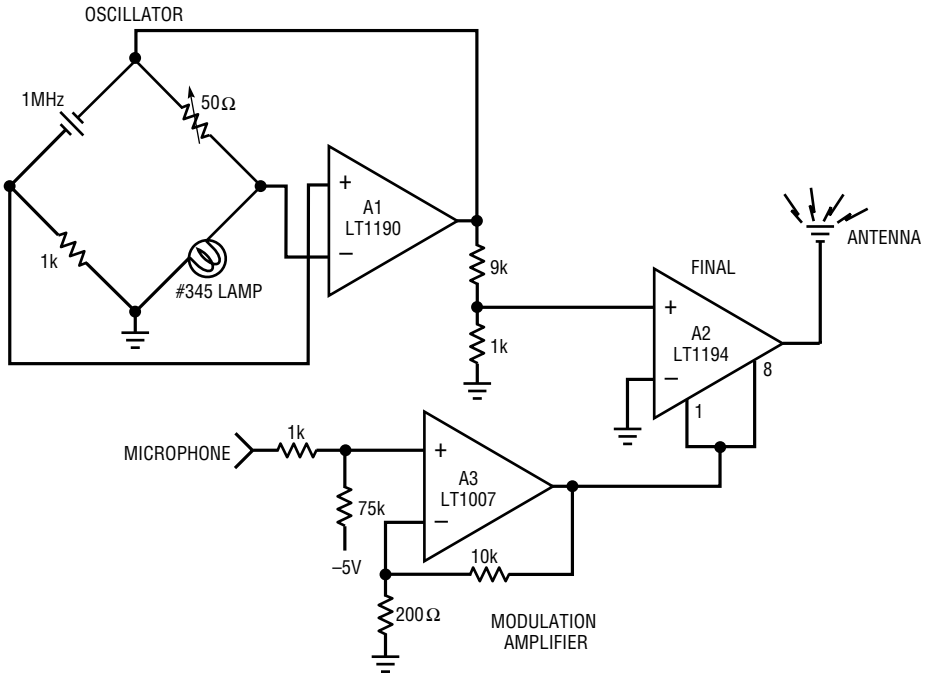


Figure 116. A Complete AM Radio Station. Don't Forget Your Advertisers and FCC License (See Appendix G)

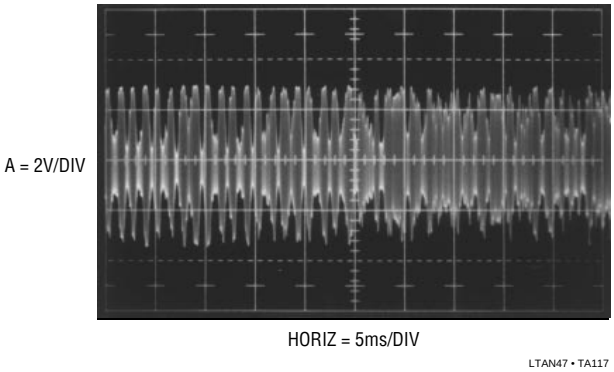


Figure 117. Chuck Berry Lays a Little Modulation on the 1MHz Carrier

on and its collector (Trace A, Figure 119) is at –15V, cutting off Q1. The positive input voltage is inverted by A3, which biases the summing node of integrator A1 through the 3.6k resistor and the self-biased FETs. A current, –I, is pulled from the summing point. A2, a precision op amp, DC stabilizes A1. A1's output (Trace B, Figure 119) integrates positive until C1's input (Trace C) crosses 0V. When this happens, C1's inverting output goes negative, the Q4-Q5 level shifter turns off, and Q5's collector goes to +15V. This allows Q1 to come on. The resistors in Q1's path are scaled to produce a current, +2I, exactly twice the absolute magnitude of the current, –I, being removed from the summing node. As a result, the net current into the junction becomes +I and A1 integrates negatively at the same rate as its positive excursion.

When A1 integrates far enough in the negative direction, C1's "+" input crosses zero and its outputs reverse. This switches the Q4-Q5 level shifter's state. Q1 goes off and the entire cycle repeats. The result is a triangle waveform at A1's output. The frequency of this triangle is dependent on the circuit's input voltage and varies from 1Hz to 1MHz with a 0V-10V input. The LT1009 diode bridge and the series-parallel diodes provide a stable bipolar reference which always opposes the sign of A1's output ramp. The Schottky diodes bound C1's "+" input, assuring it clean recovery from overdrive.

The AD639 trigonometric function generator, biased via A4, converts A1's triangle output into a sine wave (Trace D).

The AD639 must be supplied with a triangle wave which does not vary in amplitude or output distortion will result. At higher frequencies, delays in the A1 integrator switching loop result in late turn on and turn off of Q1. If these delays are not minimized, triangle amplitude will increase with frequency, causing distortion level to also increase with frequency. The total delay generated by the LT1016,

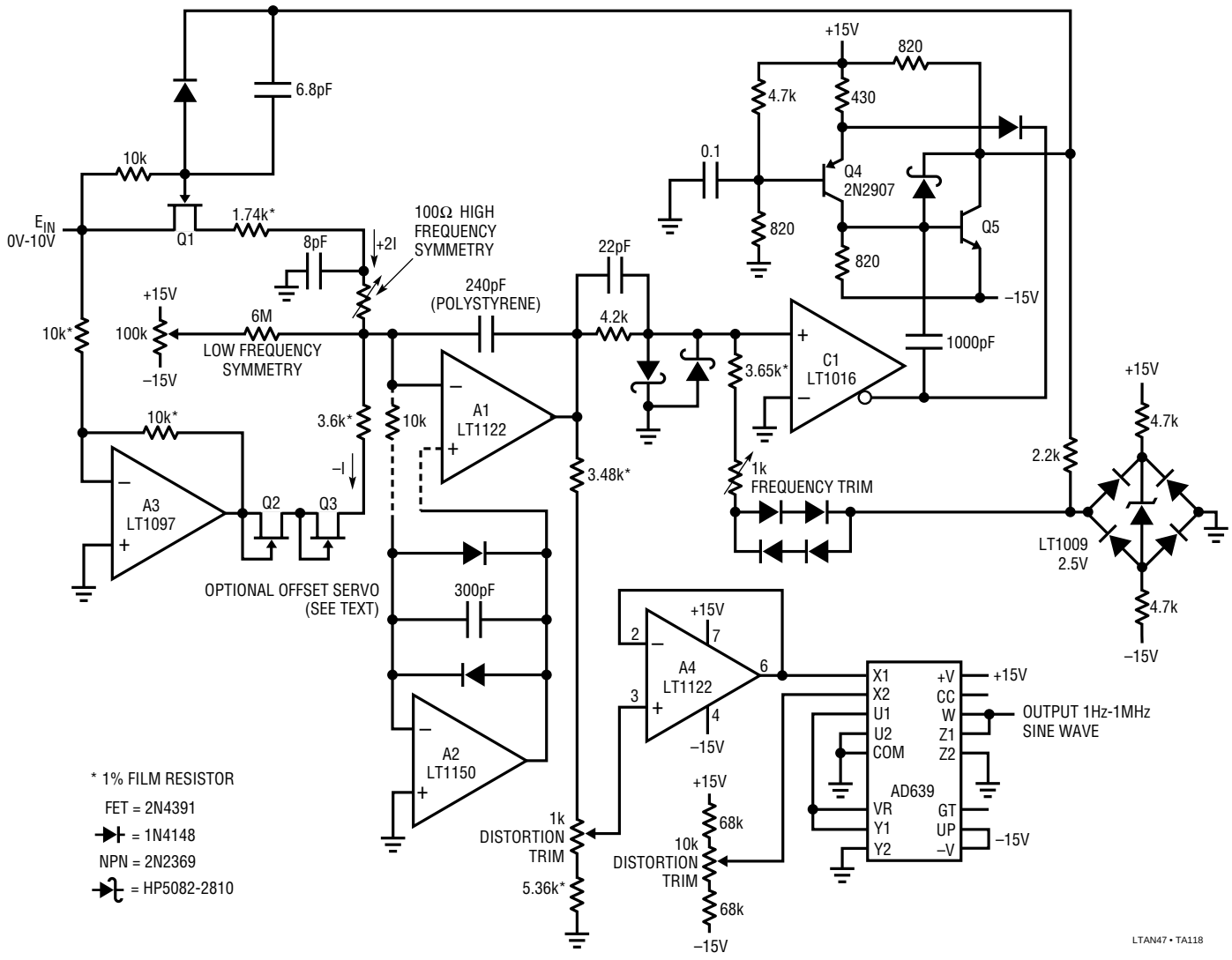


Figure 118. 1Hz-1MHz Sine Wave Output VCO Has 0.25% Linearity and 0.4% Distortion

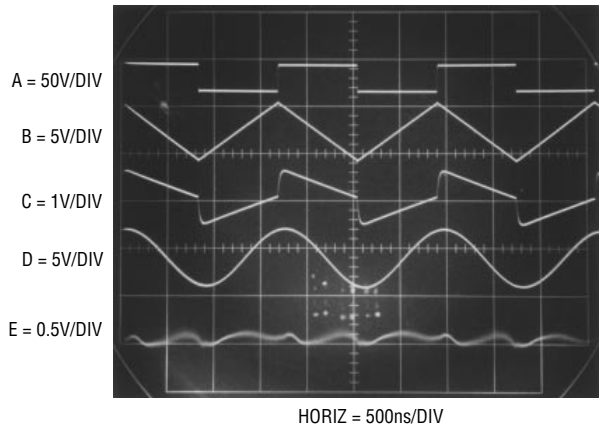


Figure 119. Sine Wave VCO Waveforms

the Q4-Q5 level shifter, and Q1 is 14ns. This small delay, combined with the 22pF feedforward network at the LT1016's input, keeps distortion to just 0.40% over the entire 1MHz range. At 100kHz, distortion is typically inside 0.2%. The effects of gate-source charge transfer, which happens whenever Q1 switches, are minimized by the 8pF unit in Q1's source line. Without this capacitor, a sharp spike would occur at the triangle peaks, increasing distortion. The Q2-Q3 FETs compensate the temperature-dependent on-resistance of Q1, keeping the +2I/–I relationship constant with temperature.

This circuit features extremely fast response to input changes, something most sine wave circuits cannot do.

Figure 120 shows what happens when the input switches between two levels (Trace A). A1's triangle output (Trace B) shifts frequency immediately, with no glitching or poor dynamics. The sine output (Trace C), reflecting this action, is similarly clean. To adjust this circuit, put in 10.00V and trim the 100Ω pot for a symmetrical triangle output at A1.

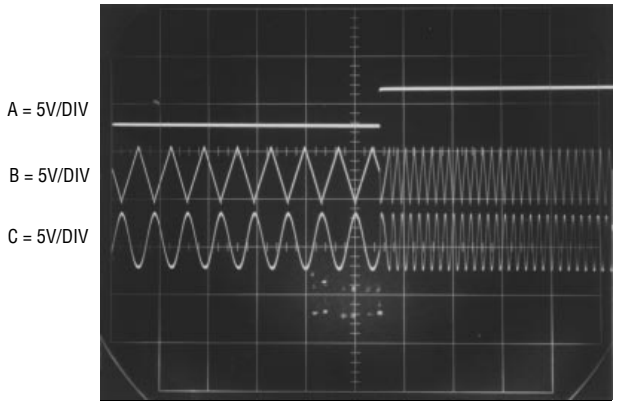


Figure 120. Sine Wave Output VCO Step Response is Quick and Clean

Next, put in 100µV and trim the 100k pot for triangle symmetry. Then, put in 10.00V again and trim the 1k frequency trim adjustment for a 1MHz output frequency. Finally, adjust the distortion trim potentiometers for minimum distortion as measured on a distortion analyzer (Trace E, Figure 119). Slight readjustment of the other potentiometers may be required to get lowest possible distortion. If operation below 100Hz is not required, the A2 based DC stabilization stage may be deleted. If this is done, A1's positive input should be grounded.

1Hz-10MHz V → F Converter

The LT1016 and the LT1122 high speed FET amplifier combine to form a high speed V → F converter in Figure 121. A variety of circuit techniques are used to achieve a 1Hz to 10MHz output. Overrange to 12MHz (V_{IN} = 12) is provided. This circuit has a wider dynamic range (140dB or 7 decades) than any commercially available unit. The 10MHz full-scale frequency is 10 times faster than currently available monolithic V → Fs. The theory of operation is based on the identity Q = CV.

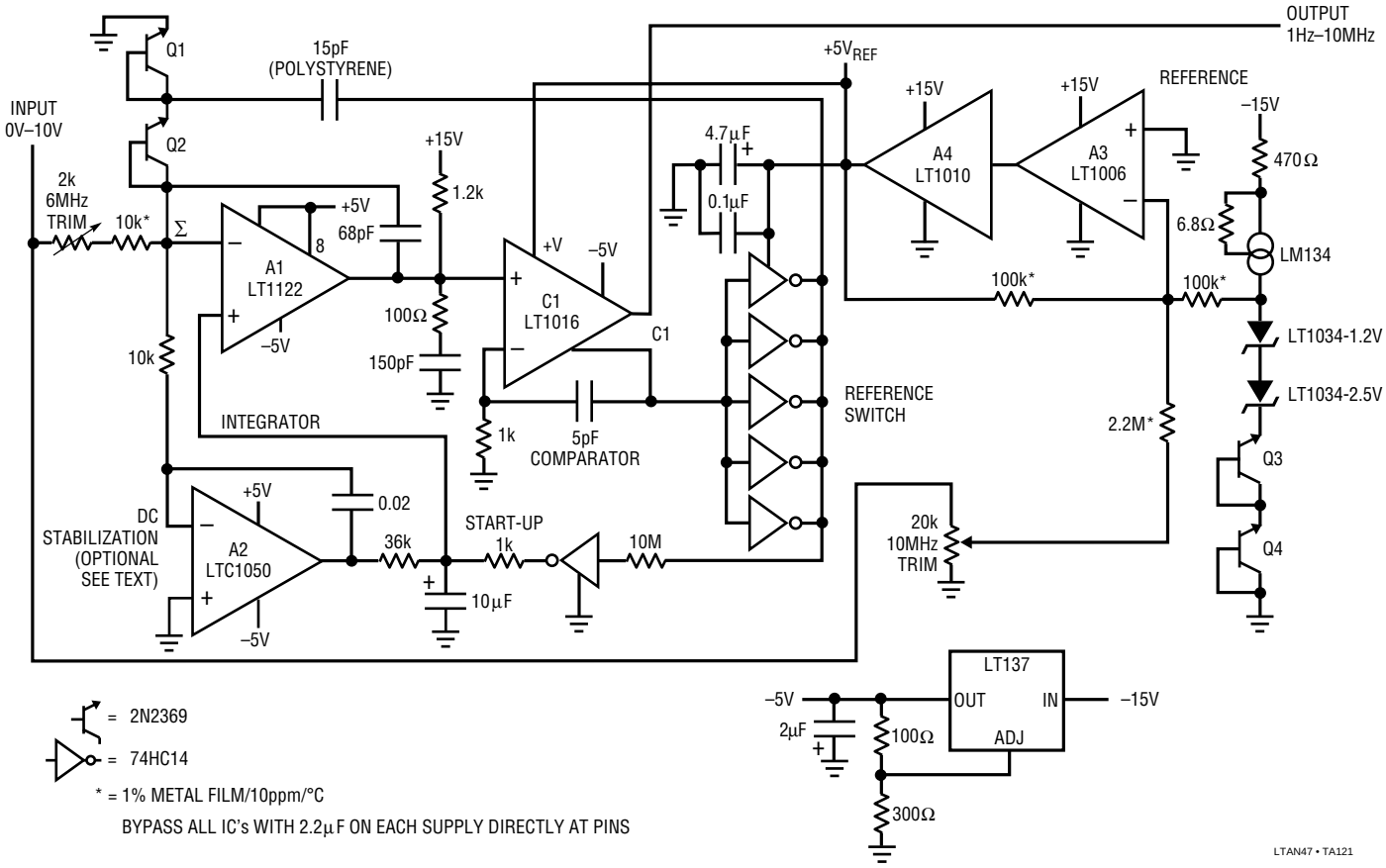


Figure 121. 1Hz-10MHz V-to-F Converter. Linearity is 0.03% with 50ppm/°C Drift

Each time the circuit produces an output pulse, it feeds back a fixed quantity of charge (Q) to a summing node (Σ). The circuit's input furnishes a comparison current at the summing node. The difference signal at the node is integrated in a monitoring amplifier's feedback capacitor. The amplifier controls the circuit's output pulse generator, completing a feedback loop around the integrating amplifier. To maintain the summing node at zero, the pulse generator runs at a frequency which permits enough charge pumping to offset the input signal. Thus, the output frequency will be linearly related to the input voltage. A1 is the integrating amplifier.

0.05μV/°C offset drift performance is obtained by stabilizing A1 with A2, a chopper stabilized op amp. A2 measures the DC value of the negative input, compares it to ground, and forces the positive input to maintain offset balance in A1. Note that A2 is configured as an integrator and cannot see high frequency signals. It functions only at DC and low frequency.

A1 is arranged as an integrator with a 68pF feedback capacitor. When a positive voltage is applied to the input, A1's output integrates in a negative direction (Trace A, Figure 122). During this period, C1's inverting output is low. The paralleled HCMOS inverters form a reference voltage switch. The reference voltage is established by the LM134 current source driven LT1034's and the Q3-Q4 combination. Additionally, a small input voltage related term is summed into the reference, improving overall circuit linearity. A3-A4 provides low drift buffering, presenting a low impedance reference to the paralleled inverter's supply pin. The HCMOS outputs give low resistance, essentially errorless switching. The reference switch's output charges the 15pF capacitor via Q1's path.

When A1's output crosses zero, C1's inverting output goes high and the reference switch (Trace B) goes to ground. This causes the 15pF unit to dispense charge into the summing node via Q2's V_{BE}. The amount of charge dispensed is a direct function of the voltage the 15pF unit was charged to (Q = CV). Q1 and Q2 are temperature compensated by Q3 and Q4 in the reference string. The current through the 15pF unit (Trace C) reflects the charge pumping action. The removal of current from A1's summing junction (Trace D) causes the junction to be driven very quickly negative. The initial negative-going 15ns

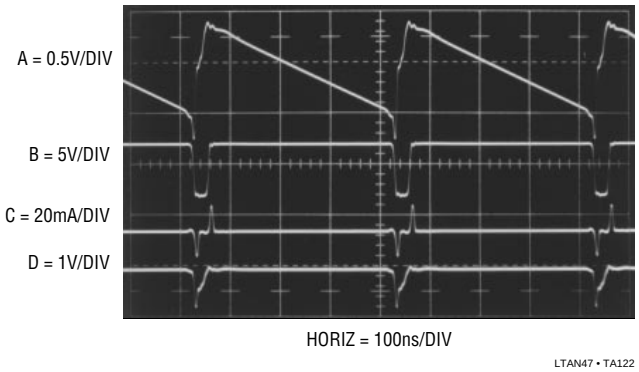


Figure 122. 10MHz V-to-F's Operating Waveforms. LT1122 Integrator is Completely Reset in 60ns

transient at A1's output is due to amplifier delay. The input signal feeds directly through the feedback capacitor and appears at the output. When the amplifier finally responds, its output (Trace A) slew limits as it attempts to regain control of the summing node. The class A 1.2kΩ pull-up and the RC damper at A1's output minimizes erroneous output movement, enhancing this slew recovery. The amount of time the reference switch remains at ground depends on how long it takes A1 to recover and the 5pF-1000Ω hysteresis network at C1. This 60ns interval is long enough for the 15pF unit to fully discharge. After this, C1 changes state, the reference switch swings positive, the capacitor is recharged and the entire cycle repeats. The frequency at which this oscillation occurs is directly related to the voltage-input-derived current into the summing junction. Any input current will require a corresponding oscillation frequency to hold the summing point at an average value of 0V.

Maintaining this relationship at megahertz frequencies places severe restrictions on circuit timing. The key to achieving 10MHz full-scale operating frequency is the ability to transmit information around the loop as quickly as possible. The discharge-reset sequence is particularly critical and is detailed in Figure 123. Trace A is the A1 integrator output. Its ramp output crosses 0V at the first left vertical graticule division. A few nanoseconds later, C1's inverting output begins to rise (Trace B), switching the reference switch to ground (Trace C). The reference switch begins to head towards ground about 16ns after A1's output crosses 0V. 2ns later, the summing point (Trace D) begins to go negative as current is pulled from it through the 15pF capacitor. At 25ns, C1's inverting

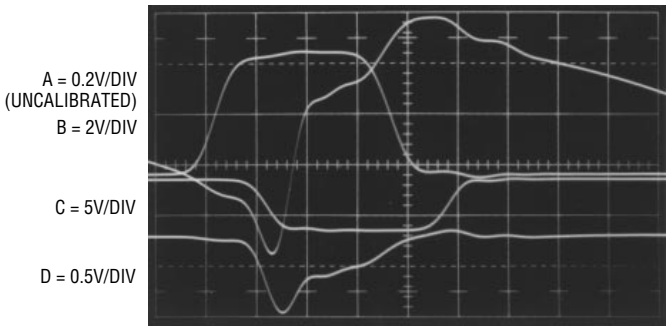


Figure 123. Detail of 60ns Reset Sequence (Whoosh!)

output is fully up, the reference switch is at ground, and the summing point has been pulled to its negative extreme. Now, A1 begins to take control. Its output (Trace A) slews rapidly in the positive direction, restoring the summing point. At 60ns, A1 is in control of the summing node and the integration ramp begins again.

Start-up and overdrive conditions could force A1's output to go to the negative rail and stay there. The AC-coupled nature of the charge dispensing loop can preclude normal operation and the circuit may latch. The remaining HCMOS inverter provides a watchdog function for this condition. If A1's output rails negative the reference switch tries to stay at ground. The remaining inverter goes high, lifting A1's positive input. This causes A1's output to slew positive, initiating normal circuit action. The 1k-10µF combination and the 10M-inverter input capacitance limit start-up loop bandwidth, preventing unwanted outputs.

The LM134 current source driving the reference string has a built in 0.33%/°C thermal coefficient, causing slight voltage modulation in the Q3-Q4 pair over temperature. This small change (≈+120 ppm/°C) opposes the –120ppm/°C drift in the 15pF polystyrene capacitor, aiding overall circuit tempco.

To trim this circuit, apply exactly 6V at the input and adjust the 2kΩ potentiometer for 6.000MHz output. Next, put in exactly 10V and trim the 20k unit for 10.000MHz output. Repeat these adjustments until both points are fixed. A2's low drift eliminates a zero adjustment. If operation below 600Hz is not required, A2 and its associated components may be deleted.

Linearity of this circuit is 0.03% with full-scale drift of 50ppm/°C. Zero point error, controlled by A2, is 0.05Hz/°C.

8-Bit, 100ns Sample-Hold

Figure 124 shows a simple, very fast sample-hold circuit. This circuit will acquire a ±5V input to 8-bit accuracy in 100ns. Hold step is inside 1/4 LSB with hold settling inside 25ns. Aperture time is 4ns and droop rate about 1/2 LSB/µs.

The input is fed to a Schottky switching bridge via inverting buffer A1. The Schottky bridge, similar to types used in sampling oscilloscopes[16], gives 1ns switching and eliminates the charge pump-through that a FET switch would contribute. The switching bridge's output feeds output amplifier A2. A2, configured as an integrator, is the actual hold amplifier. Its output is fed back to the switching bridge's input, forming a summing point with A1's output resistor. This feedback loop places the bridge within a loop, enhancing accuracy.

The bridge is switched by driving the sample-hold input line. Q1 and Q2 drive L1's primary. L1's secondaries provide complementary drive to the bridge with almost no time skewing.

Figure 125 shows the circuit acquiring a full scale step. Trace A is the input command while Trace B is A2's output. The aberration visible in A2's output when switching into hold (hold step) is due to minute residual AC imbalances in the bridge. Figure 126 studies this effect in high resolution detail, with the hold step trim deliberately disconnected. After A2's output nominally settles at final value, the circuit is switched into hold. The bridge imbalance allows a small parasitic charge to be displaced into A2's summing point, causing A2 to step 10mV higher (in this case). If the trim is connected and properly adjusted, it supplies a small compensatory charge during switching. Figure 127 shows the effect of this on the output. The settled hold output is the same as the acquired value. To trim this circuit, ground the input while pulsing the sample-hold control line. Next, adjust the trim for minimal amplitude step between the sample and hold states.

In contrast to low frequency sample-hold circuits this design cannot pass signal if left in the sample mode. The transformer's inherent AC coupling precludes such operation. Similarly, extended sample mode duration (e.g., >500ns) will cause transformer saturation, resulting in erroneous outputs and excessive Q1-Q2 dissipation. If

Note 16: See References 7, 8 and 28.

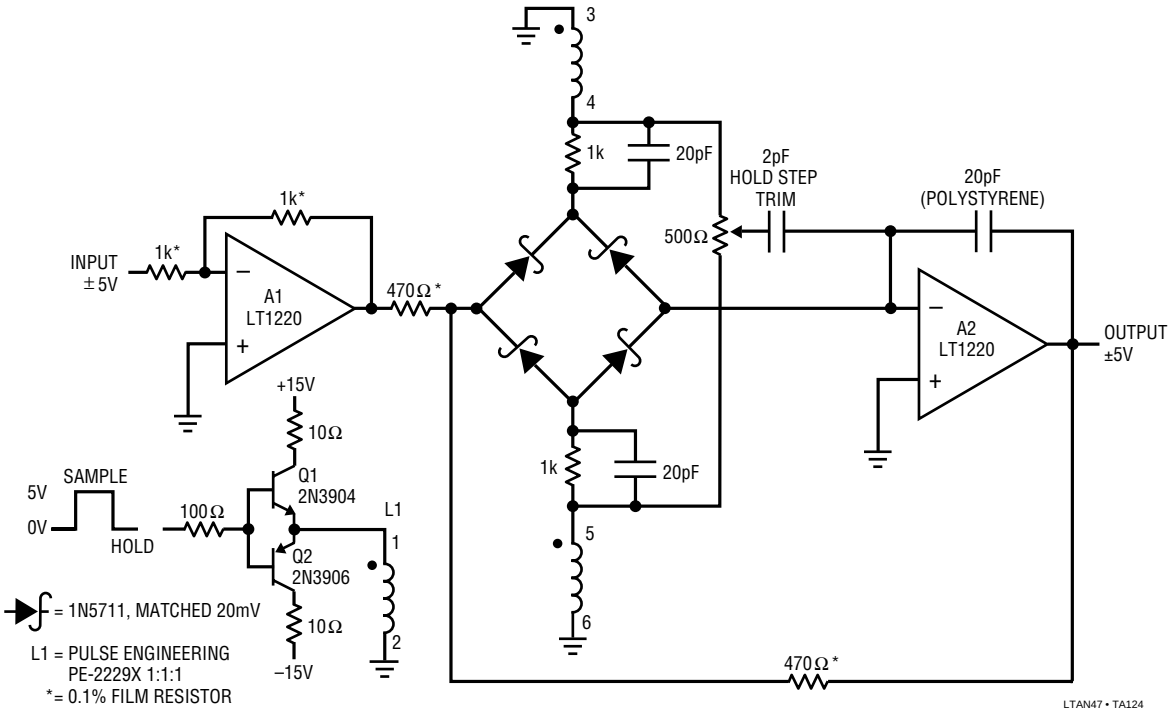


Figure 124. 8-Bit, 100ns Sample-Hold

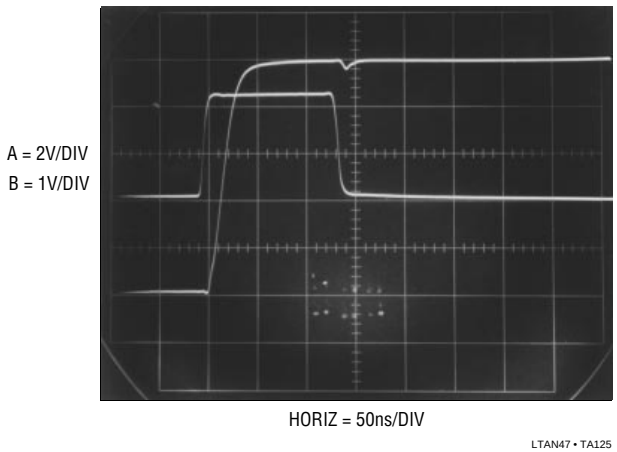


Figure 125. Fast Sample-Hold Acquiring a Full-Scale Input

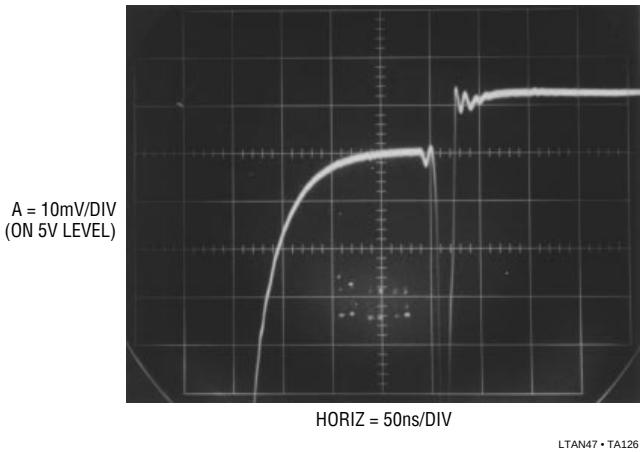


Figure 126. Hold Step with Mis-Adjusted Compensation

extended logic high durations are possible at the control input, it should be AC coupled.

15ns Current Summing Comparator

Figure 128 shows a way to build a high speed current comparator with resolution in the 12-bit range. Current comparison, the fastest way to compare D→A outputs and analog values, is commonly used in high speed A→D converters and instrumentation. A1 is set up as a Schottky bounded amplifier. The bound diodes prevent A1 from saturating due to excessive summing point overdrive, aiding response time. The 3pF capacitor, a typical value, compensates DAC output capacitance and is selected for best amplifier damping. The 10k feedback resistor, also typical, is chosen for best gain-bandwidth performance. Voltage gains of 4 to 10 are common. Figure 129 shows performance. Trace A, a test input, causes A1's output (Trace B) to slew through zero (screen center horizontal line). When A1 crosses zero, C1's input biases negative and it responds (C1's output is Trace C) 10ns later with a TTL

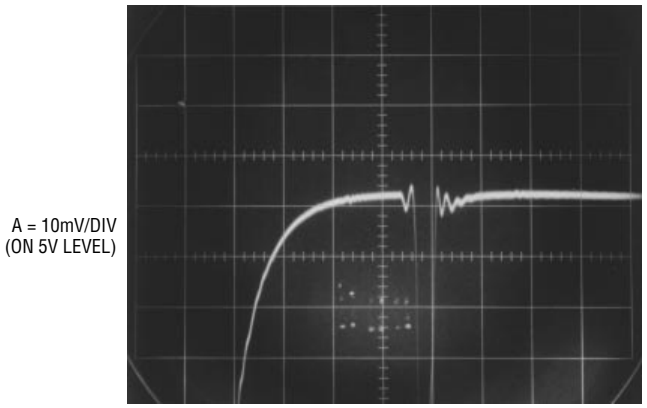


Figure 127. Hold Step with Properly Adjusted Compensation

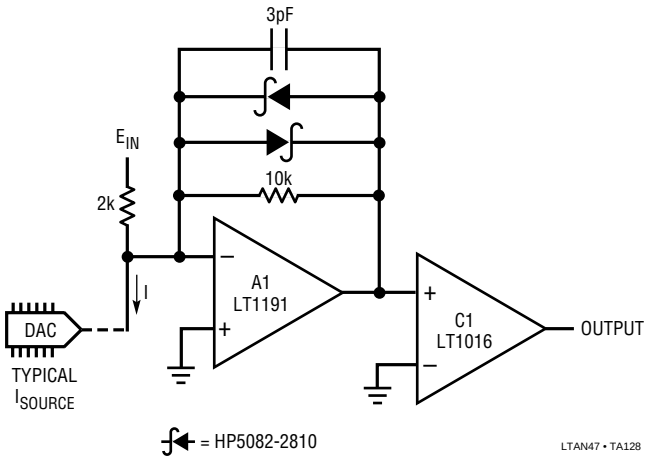


Figure 128. Fast Summing Comparator

output. Total elapsed time from the test input arriving at a TTL high until the comparator output achieves a TTL high is inside 15ns.

50MHz Adaptive Threshold Trigger Circuit

Figure 130 is an extremely versatile trigger circuit. Designing a fast, stable trigger is not easy and often entails a considerable amount of discrete circuitry. This circuit reliably triggers from DC-50MHz over a 2mV-300mV input range with no level adjustment required.

A1, a gain of ten preamplifier, feeds an adaptive trigger configuration identical to the one described in Figure 97's fiber optic receiver. The adaptive trigger maintains the A3 output comparator's trip point at 1/2 input signal amplitude, regardless of its magnitude. This insures reliable automatic triggering over a wide input amplitude range, even for very low level inputs. As an option, the network shown in dashed lines permits changing the trip threshold. This allows any point on the input waveform edge to be selected as the actual trigger point.[17]

Figure 131 shows performance for a 40MHz input sine wave (Trace A). A1's output (Trace B) takes gain and the A3 comparator gives a clean logic output (Trace C). At the highest frequencies, any bandwidth limiting in A1 is irrelevant; the adaptive trigger threshold will simply vary ratiometrically to maintain circuit output.

Fast Time-to-Height (Pulsewidth-to-Voltage) Converter

The circuit of Figure 132 allows very short pulsewidths (in this case 250ns full-scale) to be determined to a typical accuracy of 1%. Digital methods of achieving similar results dictate clock speeds of 1GHz, which is cumbersome. In addition, processor based approaches using averaging techniques require repetitive pulses which this circuit does not. Circuits of this type are frequently required in automatic test equipment and nuclear and high energy physics work where determination of short pulsewidths is a common requirement.

The circuit functions by charging a capacitor during the period of a pulsewidth. When the pulse ends, charging ceases and the voltage across the capacitor is proportional to the width of the pulse.

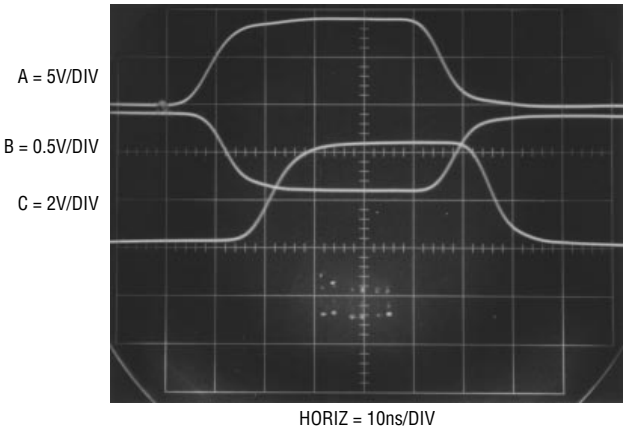


Figure 129. Fast Summing Comparator's Waveforms. Total Delay is 15ns

Note 17: This technique is borrowed from oscilloscope trigger circuitry. See Reference 29.

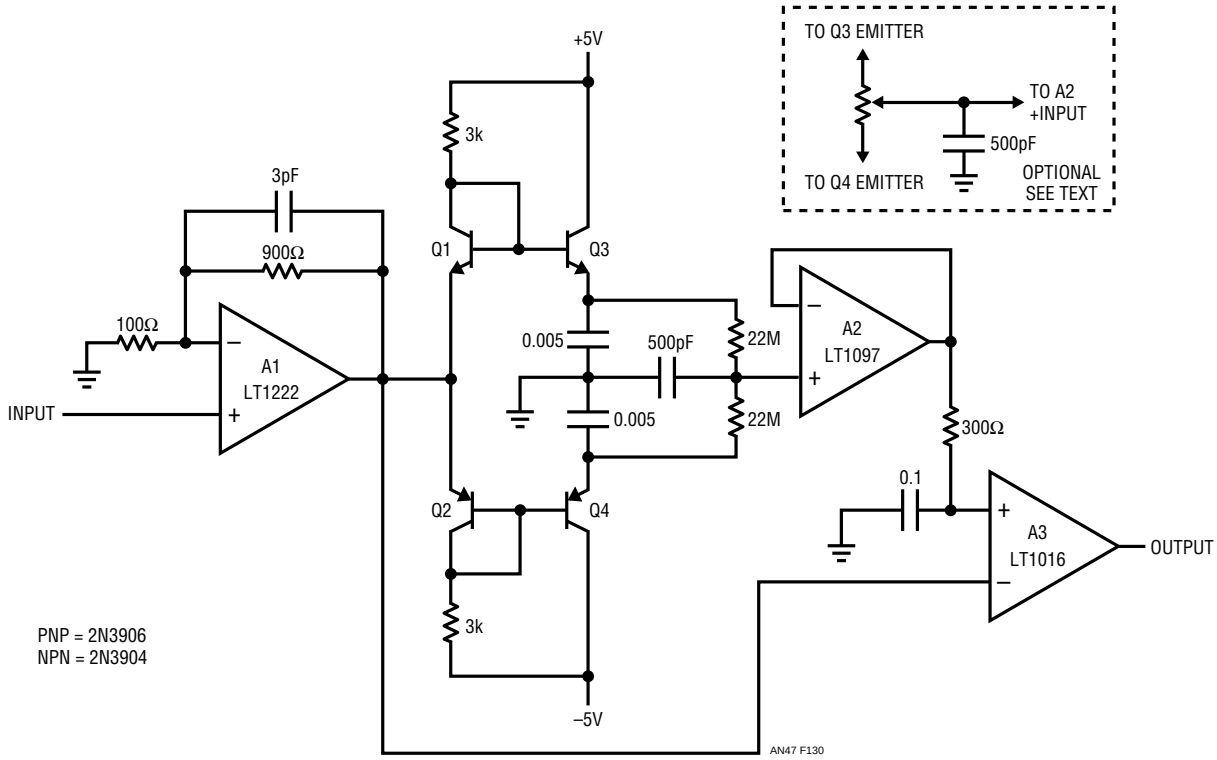


Figure 130. 50MHz Trigger with Adaptive Threshold

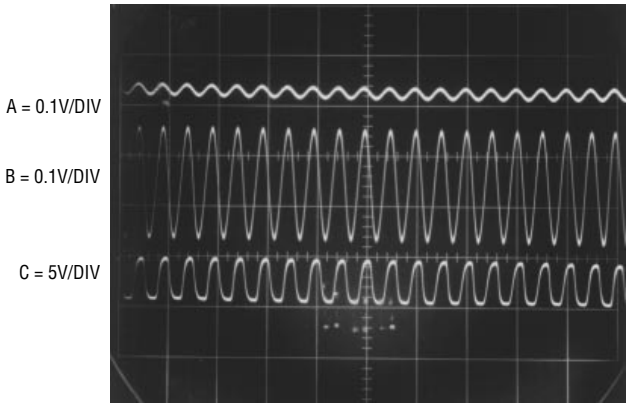


Figure 131. The Trigger Responds to a 40MHz Input. Input Amplitude Variations from 2mV-300mV Have No Effect

The input pulse to be measured (Trace A, Figure 133) simultaneously biases the 74C221 dual one shot and Q3. Q3, aided by Baker[18] clamping, capacitive feedforward and optimized DC base biasing, turns off in a few nanoseconds. Current source Q2's emitter forward biases and Q2 supplies constant current to the 100pF integrating capacitor. Q1 supplies temperature compensation for Q2, with the 2.5V LT1009 referencing the current source. Q2's collector (e.g., the 100pF capacitor) charges in ramp fashion (Trace B). A1 supplies a buffered output (Trace C). When the input pulse ends, Q3 rapidly turns on, reverse biasing Q2's emitter and turning off the current source. A1's voltage is directly proportional to the input pulse width. A monitoring A → D converter can acquire this data.

After a time set by the 74C221's RC programmed delay, a pulse appears at its Q2 output (Trace D). This pulse turns on Q4, discharging the 100pF capacitor to zero and readying the circuit for the next input pulse.

This circuit's accuracy and resolution are crucially dependent on minimizing delay in switching the Q1-Q2 current source. Figure 134 provides amplitude and time expanded versions of critical circuit waveforms. Trace A is the input pulse and Trace B is A1's input, showing the beginning of the ramp's ascent. Trace C, A1's output, shows about 13ns delay from A1's input. Traces D and E, A1's input and

Note 18: See Reference 45.

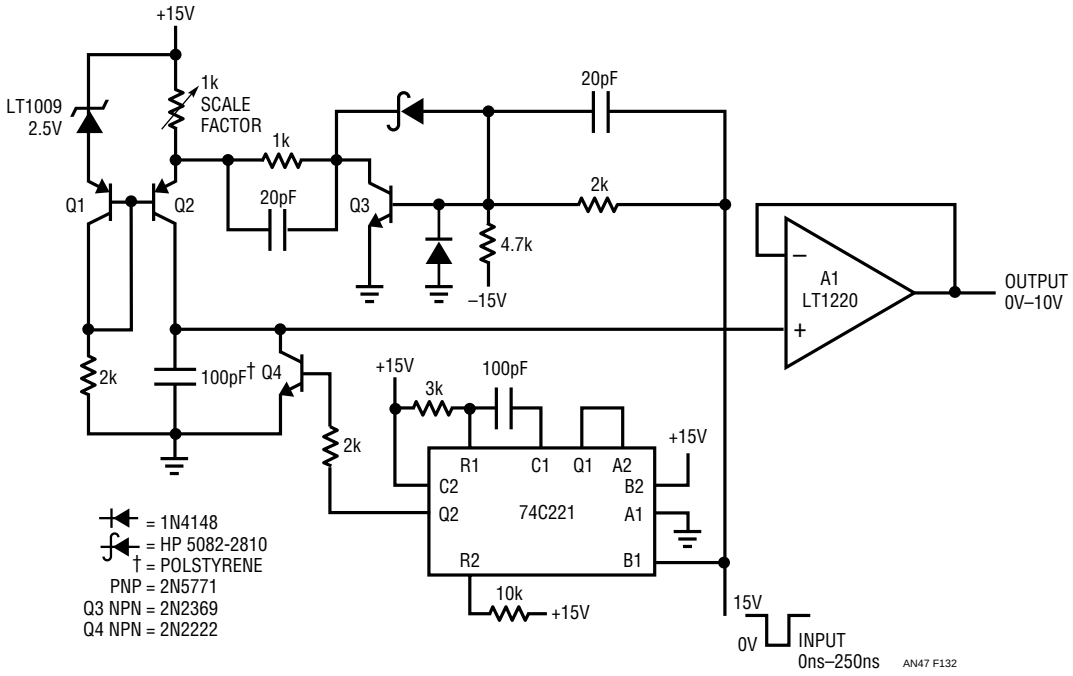


Figure 132. Fast Time-to-Height Converter

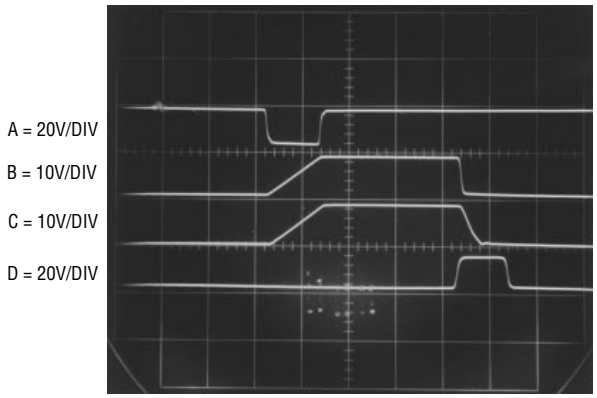


Figure 133. Time-to-Height Converter Acquires a 250ns Pulse

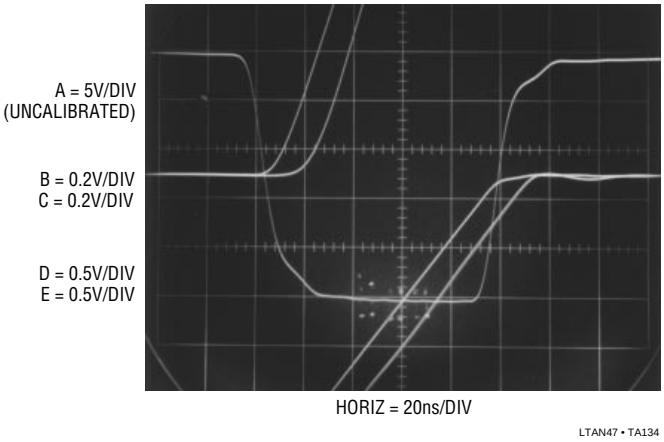


Figure 134. Detail of Time-to-Height Converter's Ramp Switching

output respectively, record similar A1 delays for ramp turn-off. The photo reflects the extremely fast current source switching; the vast majority of delay is due to A1's delay. A1's delay is far less critical than current source switching delays; A1 will always settle to the correct value well before the one shot resets the circuit. In practice, a monitoring A → D converter should not be triggered until about 50ns after the circuit's input pulse has ceased. This gives A1 plenty of time to catch up to the 100pF capacitor's settled value.

As mentioned, current source switching speed is essential for good results. Figure 135 details current source turn off. Trace A is the circuit's input pulse rising edge and Trace B shows the top of the ramp. Turn off occurs in a few nanoseconds. Similar speed is characteristic of the input's falling edge (current source turn on). Additionally, it is noteworthy that circuit accuracy and resolution limits are set by the *difference* in current source turn on and off delays. As such, the *effective* overall delay is extremely small.

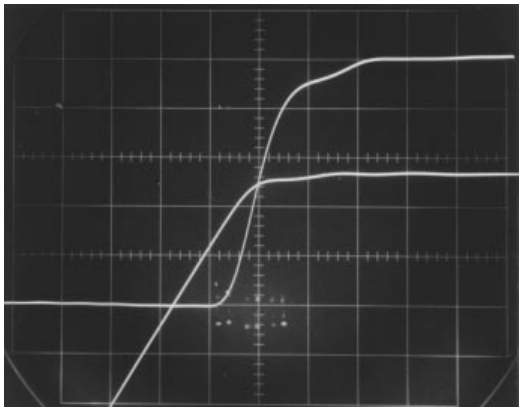


Figure 135. Current Source Turn-Off Detail for the Time-to-Height Converter

To calibrate this circuit, put in a 250ns width pulse and trim the 1kΩ potentiometer for 10V output. The circuit will convert pulse widths from 20ns to 250ns to a typical accuracy of 1%. The 20ns minimum measurable width is due to inability to fully discharge the 100pF capacitor. If this is objectionable, Q4 can be replaced with a lower saturation device or A1's output can be offset.

True RMS Wideband Voltmeter

Most AC RMS measurements use logarithmic techniques to compute the waveform's RMS value. This method limits bandwidth to below 1MHz and crest factor performance to about 10:1. Practically speaking, a waveform's RMS value is defined as its heating value in the load. Specialized instruments employ thermally based assemblies that compute the RMS value of the input. The thermal method provides substantially improved bandwidth and crest factor capability compared to logarithmically based converters.

Thermal RMS-DC converters are direct acting, thermoelectronic analog computers. The thermal technique is explicit, relying on first principles. The simple operation permits wideband performance unattainable with implicit, indirect methods based on logarithmic computing.

Figure 136 shows a classic scheme for implementing a thermally based RMS-DC converter. Here, the DC amplifier forces a second, identical, heater-sensor pair to the same thermal conditions as the input driven pair. This differentially sensed, feedback enforced loop makes ambient temperature shifts a common-mode term, eliminating their effect. Also, although the voltage and thermal interaction is non-linear, the input-output voltage relationship is linear with unity gain. The ability of this arrangement to reject ambient temperature shifts depends on the heater-sensor pairs being isothermal. This is achievable by thermally insulating them with a time constant well below that of ambient shifts. If the time constants to the heater-sensor pairs are matched, ambient temperature terms will affect the pairs equally in phase and amplitude. The DC amplifier will reject this common-mode term. Note that, although the pairs are isothermal, they are insulated from each other. Any thermal interaction between the pairs reduces the system's thermally based gain terms. This would cause unfavorable signal-to-noise performance, limiting dynamic operating range. Figure 136's output is linear because the matched thermal pair's non-linear voltage-temperature relationships cancel each other.

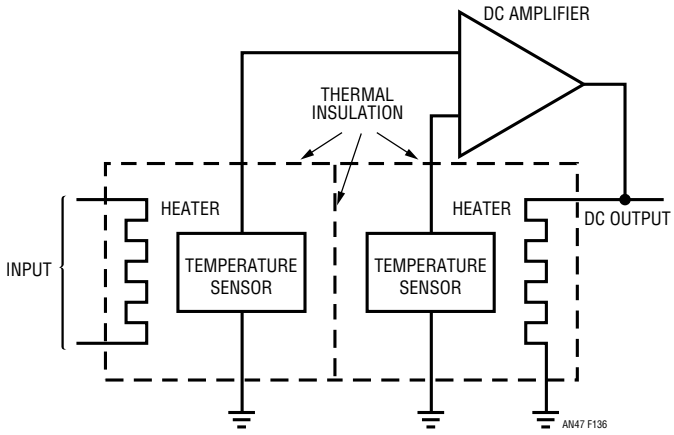


Figure 136. Conceptual Thermal RMS-DC Converter

The advantages of this approach have made its use popular in thermally based RMS-DC measurements. Typically, the assembly is composed of matched heater resistors, sensors and thermal insulation. These assemblies are relatively large and expensive to produce. Figure 137's economical wideband thermally based voltmeter is based on a monolithic thermal converter. The LT1223 provides gain, and drives the LT1088 RMS-DC thermal converter.[19] The LT1088's temperature sensing diodes are biased from the supply. A1, set up as a differential servo amplifier with a gain of 9000, extracts the diode's difference signal and biases Q1. Q1 drives one of the LT1088's heaters, completing a loop. The 3300pF capacitor gives a stable roll-off.

Note 19: Complete details on this device and a discussion on thermal conversion considerations are found in Reference 40.

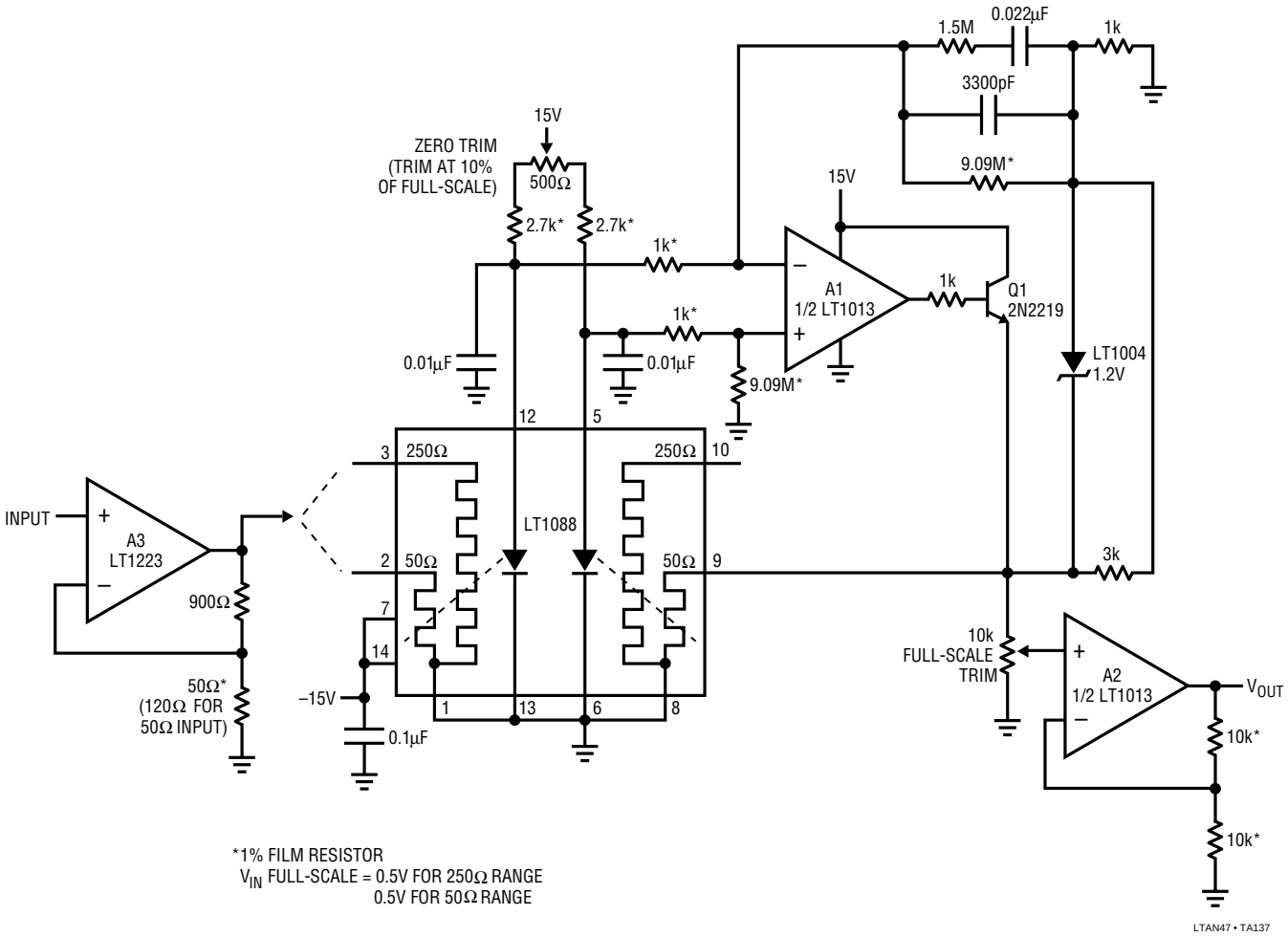


Figure 137. Wideband True RMS Voltmeter

The 1.5M-0.022µF combination improves settling by reducing gain during output slew. The LT1088's square-law thermal gain means overall loop gain is lower for small inputs. Normally, this would result in slow settling for values below about 10%-20% of scale. The LT1004 1k-3k network is a simple breakpoint, boosting amplifier gain in this region to improve settling. A2, a gain trimmable output stage, serves to compensate for gain variations in the two sides of the LT1088. To trim the circuit, put in about a 10% scale DC signal (e.g., 0.05V). Adjust the zero trim so that $V_{OUT} = V_{IN}$. Next, apply a full-scale DC input and set the full-scale trim to that value at the output. Repeat the trims until both are fixed well within 1% of full-scale. An alternate trim scheme involves applying no input, grounding Q1's base and setting the zero trim until A1's output is active. Then, unground Q1's base, apply a full-scale input and trim the full-scale adjustment for that value at the output.

Figure 138 is a plot of error vs input frequency. The LT1088 is specified at 2% to 100MHz (50Ω heater) or 1% to 20MHz (250Ω heater). As such, most of the error shown is due to bandwidth restrictions in A3, but performance is still impressive. The plots include data taken at various input levels into both heaters. A 500mV input into 250Ω dips to 1% at 8MHz and 2.5% at 14MHz before peaking badly beyond 17MHz. This input level forces a 9.5 V_{RMS} output at A3, introducing large signal bandwidth limitations. The 400mV input to the 250Ω heater shows essentially flat results to 20MHz, the LT1088's 250Ω heater specification limit.

The 50Ω heater provides significantly wider bandwidth, although A3's 50mA output limits maximum input to about 100mV$_{RMS}$ (1.76V$_{RMS}$ at the LT1088).

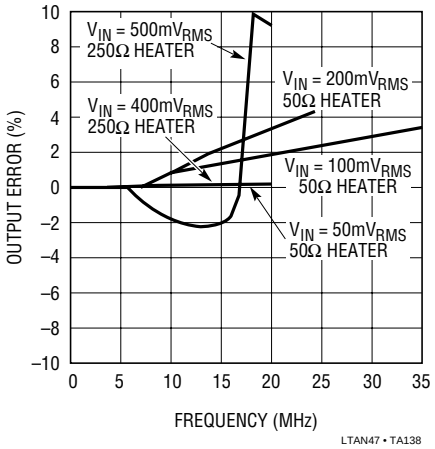


Figure 138. Accuracy Plot for the RMS Voltmeter

APPLICATIONS SECTION IV - MISCELLANEOUS CIRCUITS

RF Leveling Loop

Figure 137's wideband AC conversion can be applied in other areas. A common RF requirement is to stabilize the amplitude of a waveform against variations in input, time and temperature. Instruments and transmitters frequently require this function, which is not easy if waveform purity must be maintained. Figure 139A shows a 25MHz RF leveling loop. The RF input is applied to the AD539 wideband multiplier. The multiplier's output drives A1. A1's output is converted to DC by the LT1088 based RMS-DC converter (see previous circuit). A servo amplifier compares this output with a settable DC reference and biases the multiplier's control channel, completing a loop. The 0.33µF capacitor provides frequency compensation by rolling off gain at a frequency well below the response of the LT1088 servo. The loop maintains the output's 25MHz RMS amplitude at the DC reference's value. Changes in load, input, power supply and other variables are rejected.

Figure 139B, a similar circuit, offers significantly lower cost although performance is not quite as good. The RF input is applied to LT1228 A1, an operational transconductance amplifier. A1's output feeds LT1228 A2, a current feedback amplifier. A2's output, the circuit's output, is sampled by the A3 based gain control configuration. This arrangement, similar to the gain control loops described in Figures 112 and 114, closes a gain control loop back at A1. The 4pF capacitor compensates rectifier diode capacitance, enhancing output flatness vs frequency. A1's I_{SET} input current controls its gain, allowing overall output level control. This approach to RF leveling is simple and inexpensive, although output drift, distortion and regulation are somewhat higher than in the previous circuit.

Voltage Controlled Current Source

Figure 140 shows a voltage controlled current source with load and control voltage referred to ground. This simple, powerful circuit produces output current in accordance with the sign and magnitude of the control voltage. The circuit's scale factor is set by resistor R. A1, biased by V_{IN}, drives current through R (in this case 10Ω) and the load. A2, sensing differentially across R, closes a loop back to A1. The load current is constant because A1's loop forces a fixed voltage across R. The 2k-100pF combination sets roll off and the configuration is stable. Figure 141 shows dynamic response. Trace A is the voltage control input while Trace B is the output current. Response is quick and clean, with delay of 5ns and no slew residue or aberration.

High Power Voltage Controlled Current Source

Figure 142 is identical to the basic current source, except that it adds a 1A booster stage (adapted from Figure 104) for increased output power. Including the booster inside A1's feedback loop eliminates its DC errors. Note that the booster's current limiting features have been removed, because of this circuit's inherent current limiting nature of operation. Figure 143 shows this circuit's response to be as clean as the lower power version, although delay is about 20ns slower. It is worth mentioning that the loop stability considerations involved in placing A2 *and* the booster in A1's feedback path are significant. This circuit receives treatment in Appendix C, "The Oscillation Problem - Frequency Compensation Without Tears".

18ns Circuit Breaker

Figure 144 shows a simple circuit which will turn off current in a load 18ns after it exceeds a preset value. This circuit has been used to protect integrated circuits during developmental probing and is also useful for protecting expensive loads during trimming and calibration. The circuit's versatility is enhanced because one side of the load is grounded. Under normal conditions, Q1's emitter (Trace A, Figure 145, is Q1's current, and Trace C is its

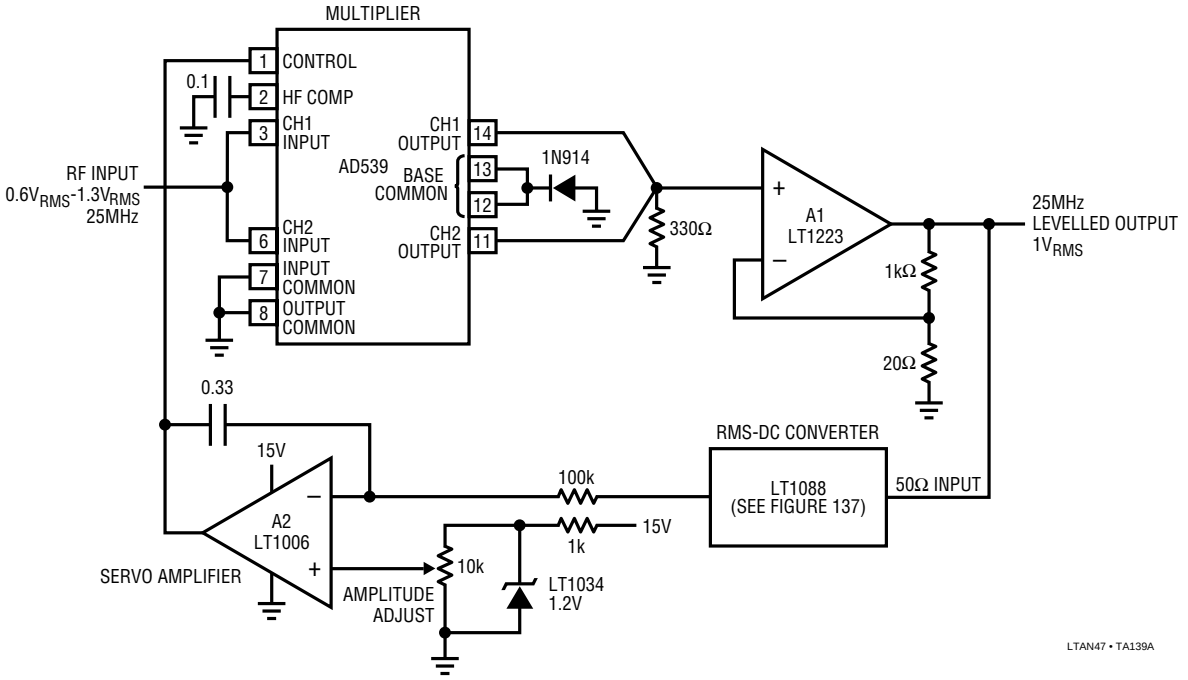


Figure 139A. RF Leveling Loop

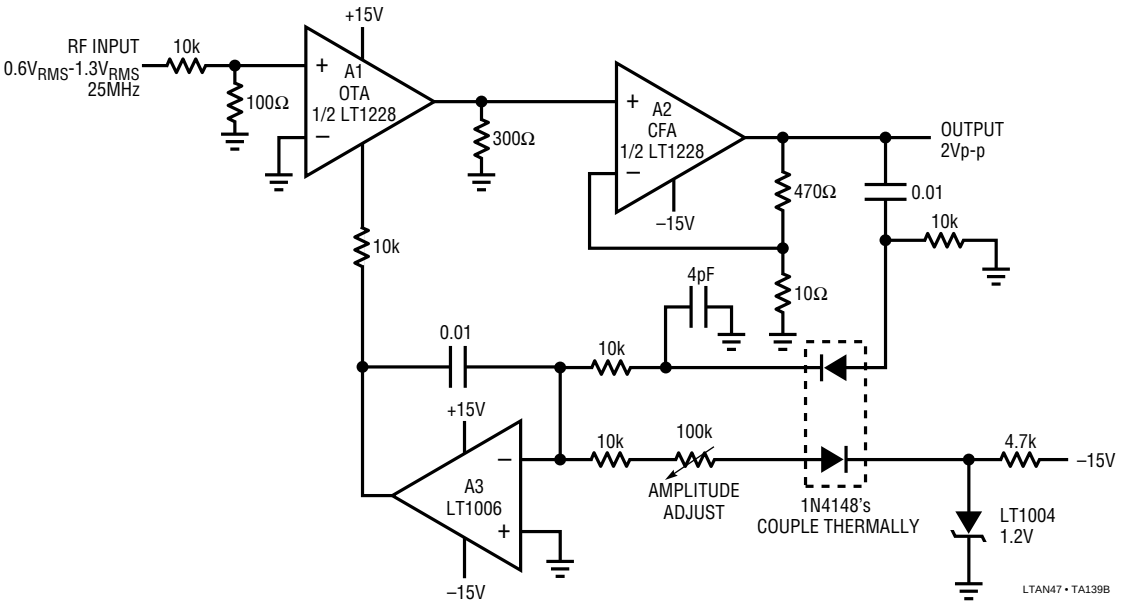


Figure 139B. Simple RF Leveling Loop

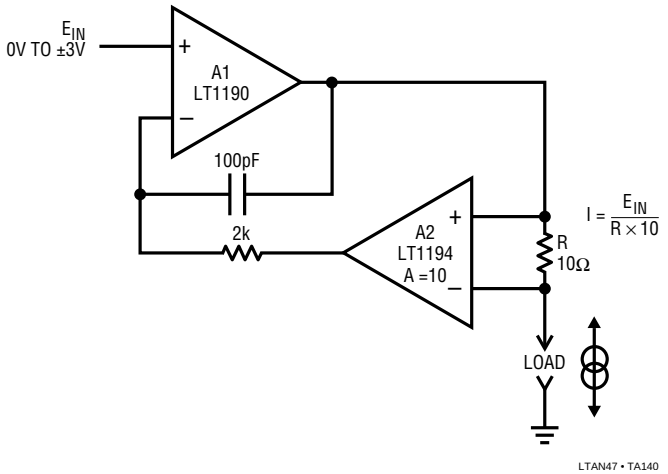


Figure 140. Fast, Precise, Voltage Controlled Current Source with Grounded Load

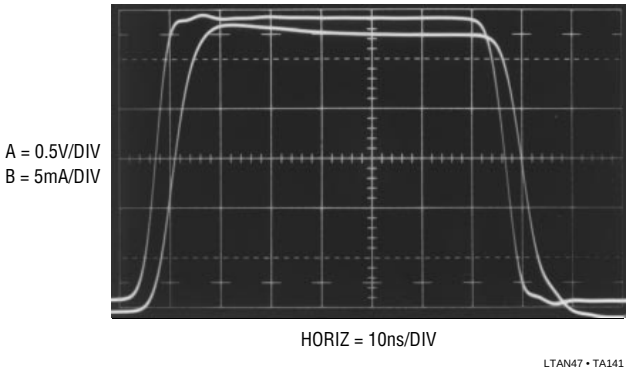


Figure 141. Dynamic Response of the Current Source. Delay is 4ns, with Clean Settling

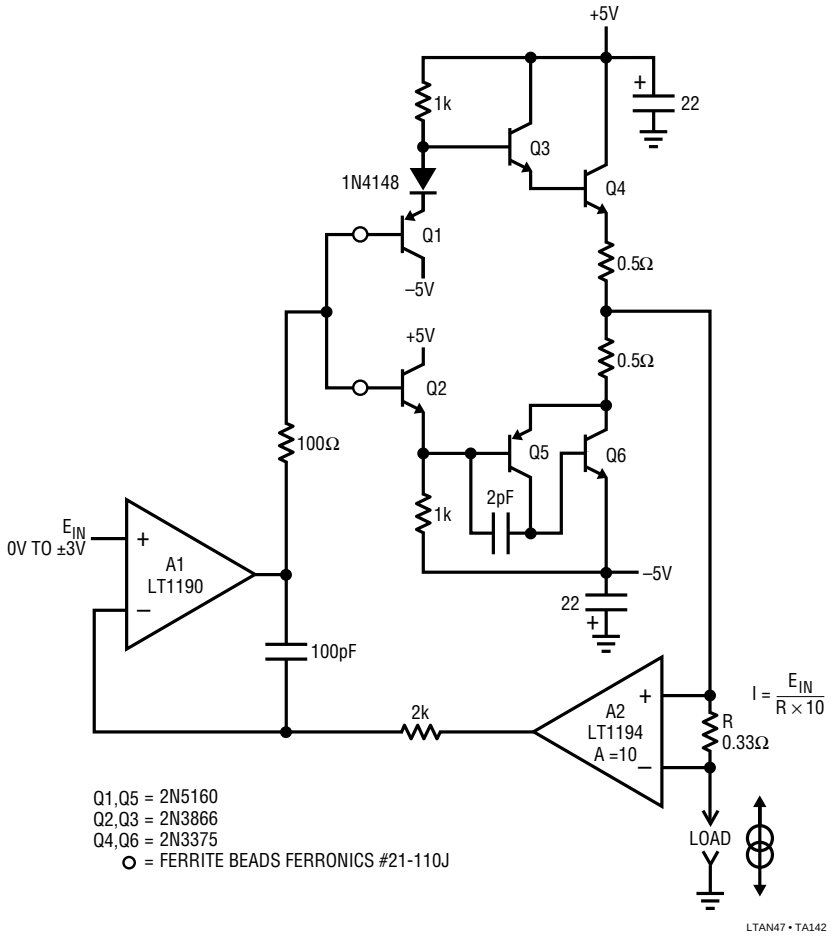


Figure 142. High Power, Wideband Voltage Controlled Current Source

voltage) is biased on, supplying power to the load via the 10Ω current shunt. Differential amplifier A1's output resides below comparator A2's voltage programmed trip point and Q2 is off. When an overload occurs, Q1's emitter current begins to increase (Trace A, just prior to the third vertical division). A1's output (Trace B) begins to rise as it tracks the increase in the 10Ω shunt's voltage. The 9k-1k dividers keep A1 inputs inside their common-mode range. Simultaneously, Q1's emitter voltage (Trace C) begins to drop as it beta limits. When A1's version of the load current exceeds A2's trip point, A2 (Trace D) goes high, turning on Q2. Q2's turn on steals Q1's base drive, turning off the load

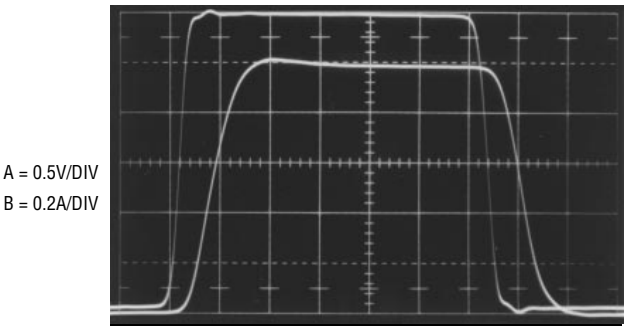


Figure 143. 1A Pulse Response of the High Power Current Source

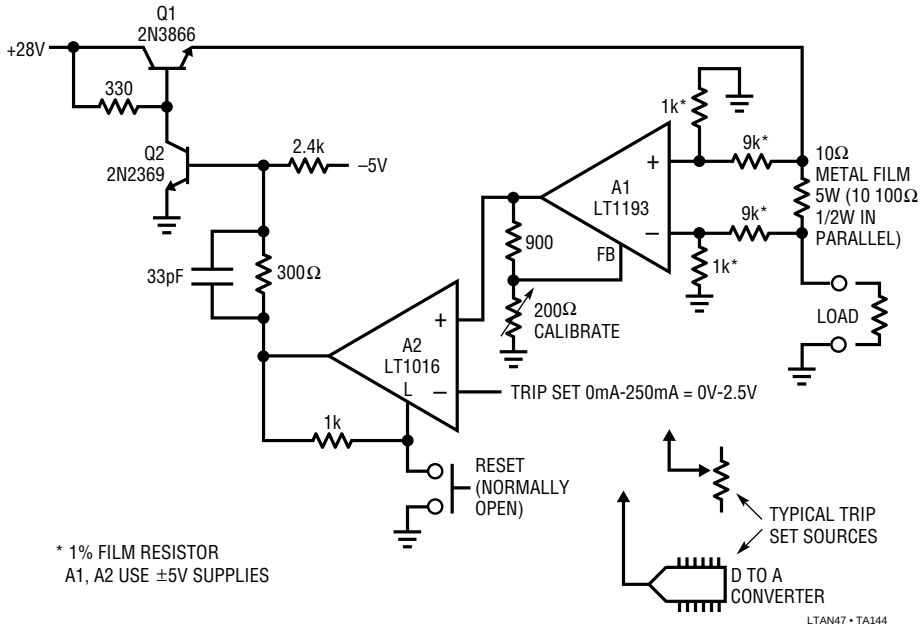


Figure 144. 18ns Circuit Breaker with Voltage Programmable Trip Point

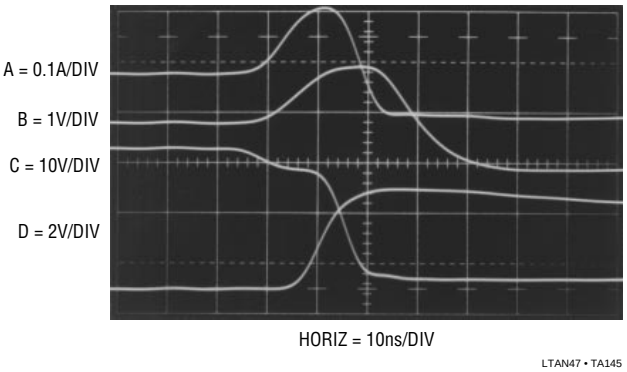


Figure 145. Operating Waveforms for the 18ns Circuit Breaker. Circuit Output (Trace C) is Shut Down 18ns After Output Current (Trace A) Begins to Rise

current. Local positive feedback at A2's latch pin causes it to latch in this off state. When the load fault has been cleared, the pushbutton can be used to reset the circuit. The delay from the onset of excessive load current to complete shutdown is inside 18ns. The 4ns delay of Trace A's current probe should be factored in when interpreting waveforms. To calibrate this circuit, ground Q2's base and install a 250mA load. Adjust the 200Ω trim for a 2.5V output at A1. Next, remove the load, unground Q2's base and press the reset button. Finally, put in the desired trip set voltage and the circuit is ready for use.

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Note: *This application note was derived from a manuscript originally prepared for publication in EDN Magazine.*

APPENDIX A

ABC's of Probes – Tektronix, Inc.

This appendix, guest written by the engineering staff of Tektronix, Inc., is a distillation of their booklet, "ABC's of Probes". The complete booklet is available, at no charge, through any Tektronix sales office or call 800-835-9433 ext. 170. For excellent technical background on probe theory see Reference 42.

PART I: UNDERSTANDING PROBES

The vital link in your measurement system

Probes connect the measurement test points in a DUT (device under test) to the inputs of an oscilloscope. Achieving optimized system performance depends on selecting the proper probe for your measurement needs.

Though you could connect a scope and DUT with just a wire, this simplest of connections would not let you realize the full capabilities of your scope. By the same token, a probe that is not right for your application can mean a significant loss in measurement results, plus costly delays and errors.

Why not use a piece of wire?

Good question: There are legitimate reasons for using a piece of wire or, more correctly, two pieces of wire; some low bandwidth scopes and special purpose plug-in amplifiers only provide binding post input terminals, so they offer a convenient means of attaching wires of various lengths.

DC levels associated with battery operated equipment could be measured. Low frequency (audio) signals from the same equipment could also be examined. Some high output transducers could also be monitored. However, this type of connection should be kept away from line-operated equipment for two basic reasons, safety and risk of equipment damage.

Safety: Attachment of hookup wires to line-operated equipment could impose a health hazard, either because the "hot" side of the line itself could be accessed, or because internally generated high voltages could be contacted. In both cases, the hookup wire offers virtually no operator protection, either at the equipment source or at the scope's binding posts.

Risk of Equipment Damage: Two unidentified hookup wires, one signal lead and one ground, could cause havoc in line-operated equipment. If the "ground" wire is attached to **any** elevated signal in line-operated equipment, various degrees of damage will result simply because both the scope and the equipment are (or should be) on the same three-wire outlet system, and short-circuit continuity is completed through one common ground.

Performance Considerations: In addition to the hazards just mentioned, there are two major performance limitations associated with using hookup wires to transfer the signal to the scope: circuit loading and susceptibility to external pickup.

Circuit Loading: This subject will be discussed in detail later, but circuit loading by the test equipment (scope-probe) is a combination of resistance and capacitance. Without the benefit of using an attenuator (10X) probe, the loading on the device under test (DUT) will be 1M ohm (the scope input resistance) and more than 15 picofarad (15pF), which is the typical scope input capacitance plus the stray capacitance of the hookup wire.

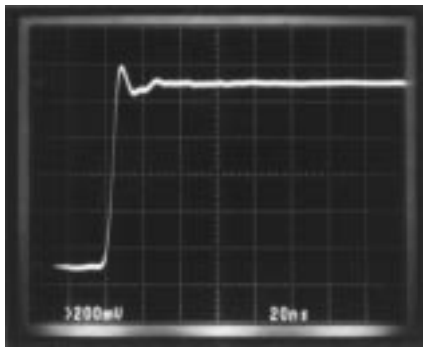


Figure 1-1

Figure 1-1 shows what a "real world" signal from a 500 ohm impedance source looks like when loaded by a 10M ohm, 10 pF probe: the scope-probe system is 300MHz. Observed risetime is 6 nSec.

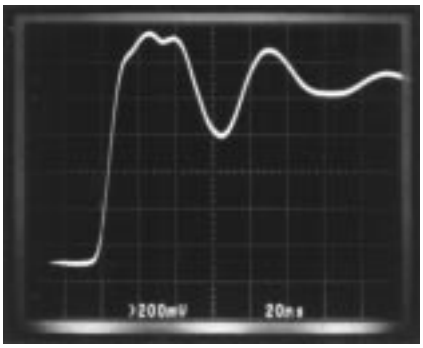


Figure 1-2

Figure 1-2 shows what happens to the same signal when it is accessed by two 2-meter lengths of hookup wire: loading is 1M ohm (the scope input resistance) and about 20 pF (the scope input capacitance, plus the stray capacitance of the wires). Observed risetime has slowed to 10 nSec and the transient response of the system has become unusable.

Susceptibility to External Pickup: An unshielded piece of wire acts as an antenna for the pickup of external fields, such as line frequency interference, electrical noise from fluorescent lamps, radio stations and signals from nearby equipment. These signals are not only injected into the scope along with the wanted signal, but can also be injected into the device under test (DUT) itself.

The source impedance of the DUT has a major effect on the level of interference signals developed in the wire. A very low source impedance would tend to shunt any induced voltages to ground, but high frequency signals could still appear at the scope input and mask the wanted signal. The answer, of course, is to use a probe which, in addition to its other features, provides coaxial shielding of the center conductor and virtual elimination of external field pickup.

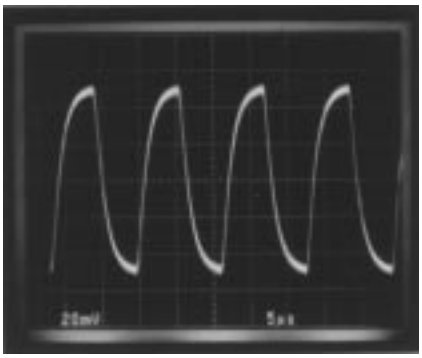


Figure 1-3

Figure 1-3 shows what a low level signal from a high impedance source (100mV from 100K ohm) looks like when accessed by a 300MHz scope-probe system. Loading is 10M ohm and 10 pF. This is a true representation of the signal, except that probe resistive loading has reduced the amplitude by about 1%: the observed high frequency noise is part of the signal at the high impedance test point and would normally be removed by using the BW (bandwidth) limit button on the scope. (See Figure 1-4.)

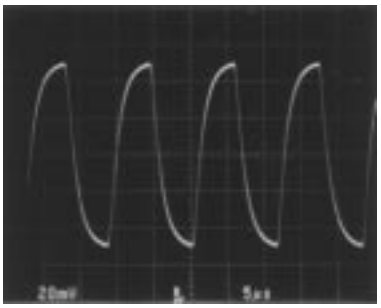


Figure 1-4

If we look at the same test point with our pieces of wire, two things happen. The amplitude drops due to the increased resistive and capacitive loading, and noise is added to the signal because the hookup wire is completely unshielded. (See Figure 1-5)

Most of the observed noise is line frequency interference from fluorescent lamps in the test area.

Probably the most annoying effect of using hookup wire to observe high frequency signals is its unpredictability. Any touching or rearrangement of the leads can produce different and nonrepeatable effects on the observed display.

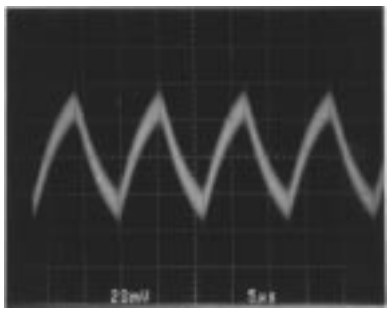


Figure 1-5

Benefits of using probes

Not all probes are alike and, for any specific application, there is no one ideal probe; but they share common features and functions that are often taken for granted.

Probes are convenient. They bring a scope's vertical amplifier to a circuit. Without a probe, you would either need to pick up a scope and attach it to a circuit, or pick up the circuit and attach it to the scope. Properly used, probes are convenient, flexible and safe extensions of a scope.

Probes provide a solid mechanical connection. A probe tip, whether it's a clip or a fine solid point, makes contact at just the place you want to examine.

Probes help minimize loading. To a certain extent, all probes load the DUT—the source of the signal you are measuring. Still, probes offer the best means of making the connections needed. A simple piece of wire, as we have just seen, would severely load the DUT; in fact, the DUT might stop functioning altogether.

Probes are designed to minimize loading. Passive, non-attenuating 1X probes offer the highest capacitive loading of any probe type—even these, however, are designed to keep loading as low as possible.

Probes protect a signal from external interference. A wire connection, as described earlier, in addition to loading the circuit, would act as an antenna and pick up stray signals such as 60Hz power, CBers, radio and TV stations. The scope would display these stray signals as well as the signal of interest from the DUT.

Probes extend a scope's signal amplitude-handling ability. Besides reducing capacitive and resistive loading, a standard passive 10X (ten times attenuation) probe extends the on-screen viewability of signal amplitudes by a factor of ten.

A typical scope minimum sensitivity is 5V/division. Assuming an eight-division vertical graticule, a 1X probe (or a direct connection) would allow on-screen viewing of 40V p-p maximum. The standard 10X passive probe provides 400V p-p viewing. Following the same line, a 100X probe should allow 4kV on-screen viewing. However, most 100X probes are rated at 1.5kV to limit power dissipation in the probe itself.

Check the specs. Bandwidth is the probe specification most users look at first, but plenty of other features also help to determine which probe is right for your application. Circuit loading, signal aberrations, probe dynamic range, probe dimensions, environmental degradation and ground-path effects will all impact the probe selection process, as discussed in the pages that follow.

By giving due consideration to probe characteristics that your application requires, you will achieve successful measurements and derive full benefit from the instrument capabilities you have at hand.

How probes affect your measurements

Probes affect your measurements by loading the circuit you are examining. The loading effect is generally stated in terms of impedance at some specific frequency, and is made up of a combination of resistance and capacitance.

Source Impedance. Obviously, source impedance will have a large impact on the net affect of any specific probe loading. For example, a device under test with a near zero output impedance would not be affected in terms of amplitude or risetime to any significant degree by the use of a typical 10X passive probe. However, the same probe connected to a high impedance test point, such as the collector of a transistor, could affect the signal in terms of risetime and amplitude.

Capacitive Loading. To illustrate this effect, let's take a pulse generator with a very fast risetime. If the initial risetime was assumed to be zero (tr = 0), the output tr of the generator would be limited by the

associated resistance and capacitance of the generator. This integration network produces an output rise time equal to 2.2 RC. This limitation is derived from the universal time-constant curve of a capacitor.

Figure 1-6 shows the effect of internal source resistance and capacitance on the equivalent circuit. At no time can the output risetime be faster than 2.2 RC or 2.2 nSec.

If a typical probe is used to measure this signal, the probe's specified input capacitance and resistance is added to the circuit as shown in Figure 1-7.

Because the probe's 10M ohm resistance is much greater than the generator's 50 ohm output resistance, it can be ignored.

Figure 1-8 shows the equivalent circuit of the generator and probe, appling the 2.2 RC formula again. The actual risetime has slowed from 2.2 n Sec. to 3.4 nSec.

Percentage change in risetime due to the added probe tip capacitance:

$$\%\ \text{change}\ \frac{tr_2 - tr_1}{tr_1} \times 100 = \frac{3.4 - 2.2}{2.2} \times 100 = 55\%$$

Another way of estimating the affect of probe tip capacitance on a source is to take the ratio of probe tip capacitance (marked on the probe compensation box) to the known or estimated source capacitance.

Using the same values:

$$\frac{C_{probe\ tip}}{C_1} \times 100 = \frac{11pF}{20pF} \times 100 = 55\%$$

To summarize, any added capacitance slows the source risetime when using high impedance passive probes. In general, the greater the attenuation ratio, the lower the tip capacitance. Here are some examples:

Probe	Attenuation	Tip Capacitance
Tektronix P6101A	X1	54 pF
Tektronix P6105A	X10	11.2 pF
Tektronix P6007	X100	2 pF

Capacitive Loading: Sinewave. When probing continuous wave (CW) signals, the probe's capacitive reactance at the operating frequency must be taken into account.

The total impedance, as seen at the probe tip, is designated Rp and is a function of frequency. In addition to the capacitive and resistive elements, designed-in inductive elements serve to offset the pure capacitive loading to some degree.

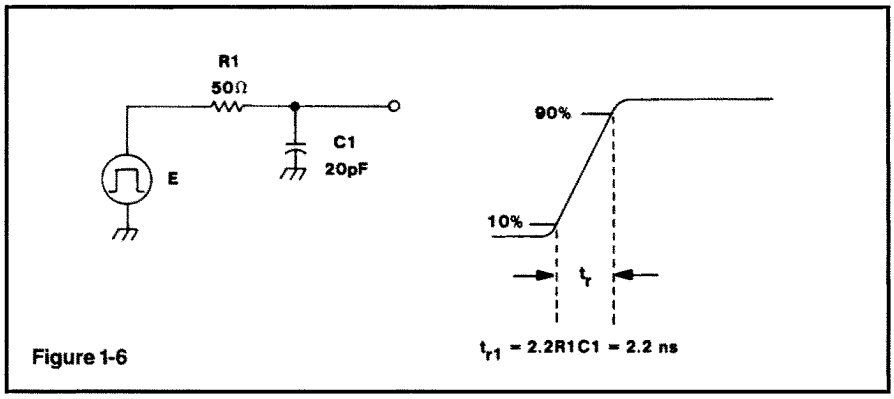


Figure 1-6

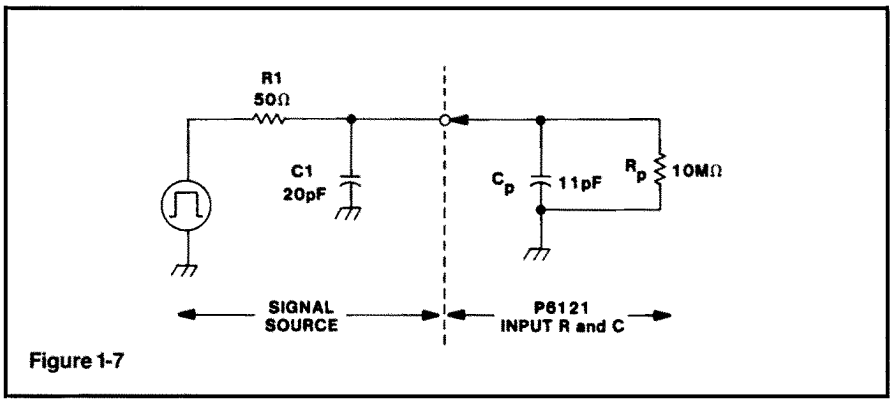


Figure 1-7

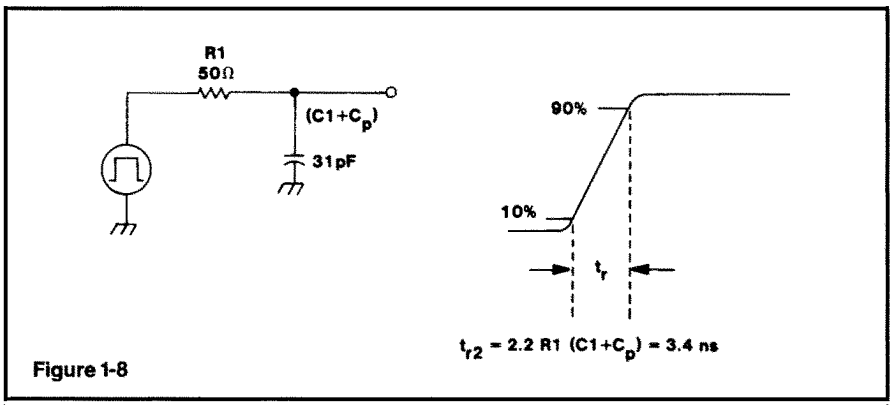


Figure 1-8

Curves showing typical input impedance vs frequency, or typical Xp and Rp vs frequency are included in most Tektronix probe instruction manuals. Figure 1-9A shows the typical input impedance and phase relationship vs frequency of the Tektronix P6203 Active Probe. Note that the 10 KΩ input impedance is maintained to almost 10 MHz by careful design of the associated resistive, capacitive and inductive elements.

Figure 1-9B shows a plot of Xp and Rp vs frequency for a typical 10 MΩ passive probe. The dotted line (Xp) shows capacitive reactance vs frequency. The total loading is again offset by careful design of the associated R, C and L elements.

If you do not have ready access to the information and need a worst-case guide to probe loading, use the following formula:

$$Xp = \frac{1}{2\pi FC}$$

Xp= Capacitive reactance (ohms)
F = Operating frequency
C = Probe tip capacitance (marked on the probe body or compensation box.)

For example, a standard passive 10M ohm probe with a tip capacitance of 11 pF will have a capacitive reactance (Xp) of about 290 ohm at 50MHz.

Depending, of course, on the source impedance, this loading could have a major effect on the

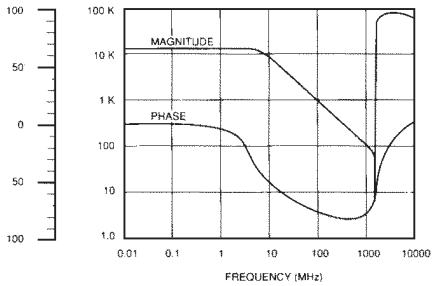


Figure 1-9A. Typical Input Impedance vs Frequency for the Tektronix P6203 Active Probe

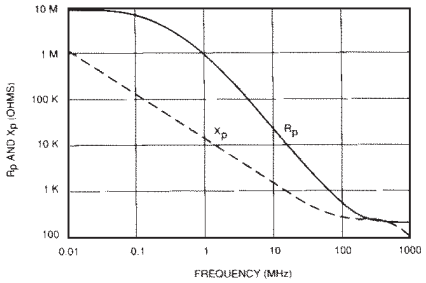


Figure 1-9B. Xp and Rp vs Frequency for a Typical 10 MΩ Passive Probe

signal amplitude (by simple divider action), and even on the operation of the circuit itself.

Resistive Loading. For all practical purposes, a 10X, 10M ohm passive probe has little effect on today's circuitry in terms of resistive loading, however, they do carry a trade-off in terms of relatively high capacitive loading as we have previously discussed.

Low Z Passive Probes. A "Low Z" passive probe offers very low tip capacitance at the expense of relatively high resistive loading. A typical 10X "50 ohm" probe has an input C of about 1 pF and a resistive loading of 500 ohm: Figure 1-10 shows the circuit and equivalent model of this type of probe.

This configuration forms a high frequency 10X voltage divider because, from transmission line theory, all that the 450 ohm tip resistor "sees" looking into the cable is a pure 50 ohm resistance, no C or L component. No low frequency compensation is necessary because it is not a capacitive divider. Low Z probes are typically high bandwidth (up to 3.5GHz and risetimes to 100 pS) and are best suited for making risetime and transit-time measurements. They can, however, affect the pulse amplitude by simple resistive divider action between the source and the load (probe). Because of its resistive loading effects, this type of probe performs best on 50 ohm or lower impedance circuits under test.

Note also that these probes operate into 50 ohm scope inputs only. They are typically teamed up with fast (500MHz to 1GHz) real time scopes or with scopes employing the sampling principle.

Bias-Offset Probes. A Bias/Offset probe is a special kind of Low Z design with the capability of providing a variable bias or offset voltage at the probe tip.

Bias/Offset probes like the Tektronix P6230 or P6231 are useful for probing high speed ECL circuitry, where resistive loading could upset the operating point. These special probes are fully described in Part 3; under Advanced Probing Techniques.

The Best of Both Worlds. From the foregoing, it can be seen that the totally "non-invasive" probe does not exist. However, one type of probe comes close—the active probe.

Active probes are discussed in the Tutorial section, but in general, they provide low resistance loading (10M ohm) with very low capacitive loading (1 to 2 pF). They do have trade-offs in terms of limited dynamic range, but under the right conditions, do indeed offer the best of both worlds.

Bandwidth. Bandwidth is the point on an amplitude versus frequency curve where the measurement system is down 3dB from a starting (reference) level. Figure 1-11 shows a typical response curve of an oscilloscope system.

Scope vertical amplifiers are designed for a Gaussian roll-off at the high end (a discussion of Gaussian response is beyond the scope of this primer). With this type of response, risetime is approximately related to bandwidth by the following equation:

$$Tr = \frac{.35}{BW}$$ or, for convenience:

$$\text{Risetime (nanoseconds)} = \frac{350}{\text{Bandwidth (MHz)}}$$

It is important to note that the measurement system is −3dB (30%) down in amplitude at the specified bandwidth limit.

Figure 1-12 shows an expanded portion of the −3dB area. The horizontal scale shows the input frequency derating factor necessary to obtain accuracies better than 30% for a specific bandwidth scope. For example, with no derating, a "100MHz" scope will have up to a 30% amplitude error at 100MHz (1.0 on the graph). If this scope is to have an amplitude accuracy better than 3%, the input frequency must be limited to about 30MHz (100MHz X .3).

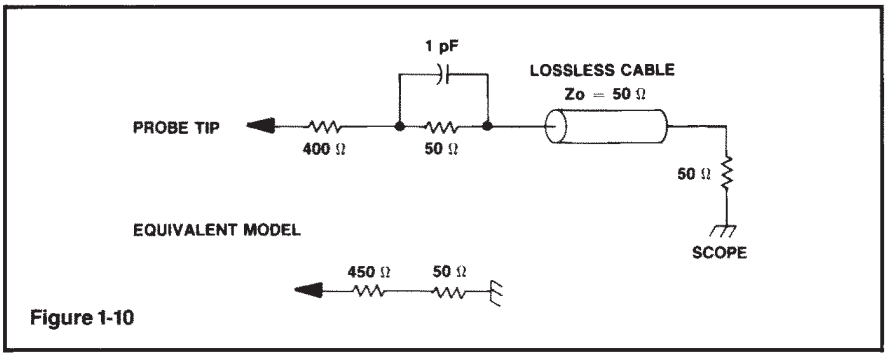


Figure 1-10

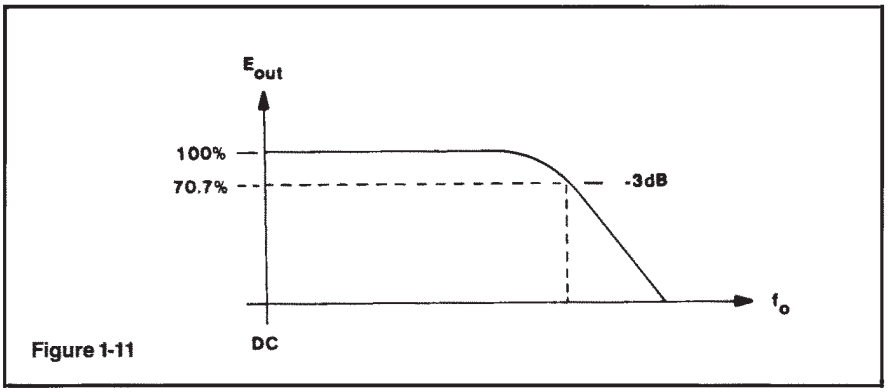


Figure 1-11

For making amplitude measurements within 3% at a specific frequency, choose a scope with at least four times the specified bandwidth as a general rule of thumb.

Probe Bandwidth. All probes are ranked by bandwidth. In this respect, they are like scopes or other amplifiers that are ranked by bandwidth. In these cases we apply the square root of the sum of the squares formula to obtain the "system risetime." This formula states that:

$$\text{Risetime system} = \sqrt{Tr^2 \text{ displayed} - Tr^2 \text{ source}}$$

Passive probes do not follow this rule and should not be included in the square root of the sum of the squares formula.

Tektronix provides a probe bandwidth ranking system that specifies "the bandwidth (frequency range) in which the probe performs within its specified limits. These limits include: total abberrations, risetime and swept bandwidth."

Both the source and the measurement system shall be specified when checking probe specifications (see Test Methods, this page).

In general, a Tektronix "100MHz" probe provides 100MHz performance (−3dB) when used on a compatible 100MHz scope. In other words, it provides full scope bandwidth **at the probe tip.**

However, not all probe/scope systems can follow this general rule. Refer to the sidebar, "Scope Bandwidth at the Probe Tip?."

Figure 1-13 shows examples of Tektronix scopes and their recommended passive probes.

Test Methods: As with all specifications, matching test methods must be employed to obtain specified performance. In the case of bandwidth and risetime measurements, it is essential to connect the probe to a properly terminated source. Tektronix specifies a 50 ohm source terminated in 50 ohm, making this a 25 ohm source impedance. Furthermore, the probe must be connected to the source via a proper probe tip to BNC adaptor. (Figure 1-14).

Figure 1-14 shows an equivalent circuit of a typical setup. The displayed risetime should be a 3.5 nSec or faster.

Figure 1-15 shows an equivalent circuit of a typical passive probe connected to a source.

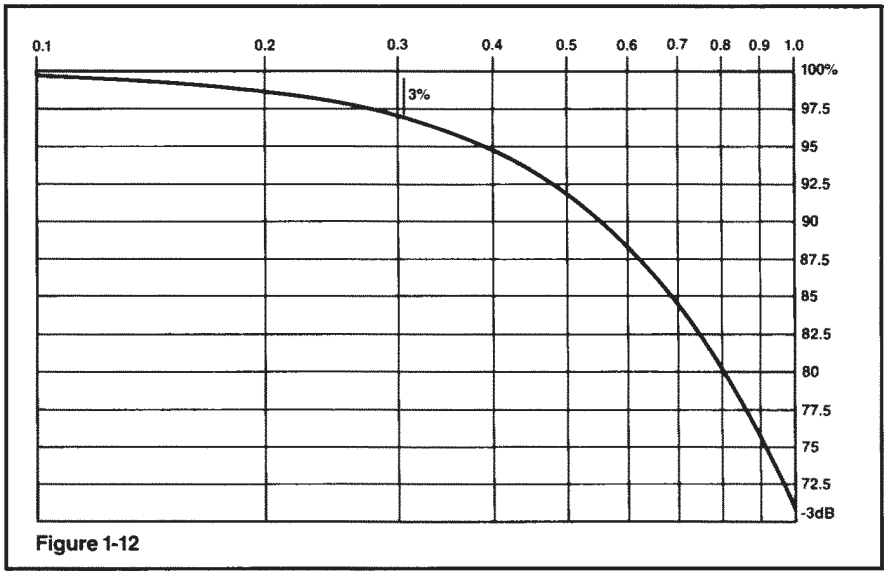


Figure 1-12

SCOPE	BW (1 MΩ input)	PROBE	BW	SYSTEM
2235	100	P6109	150	100
2245A	100	P6109	150	100
2246A	100	P6109	150	100
2445B	150	P6133 Opt 25	150	150
485	350	P6106A	250	250
2465B	400	P6137	400	400
2467B	400	P6137	400	400

Figure 1-13

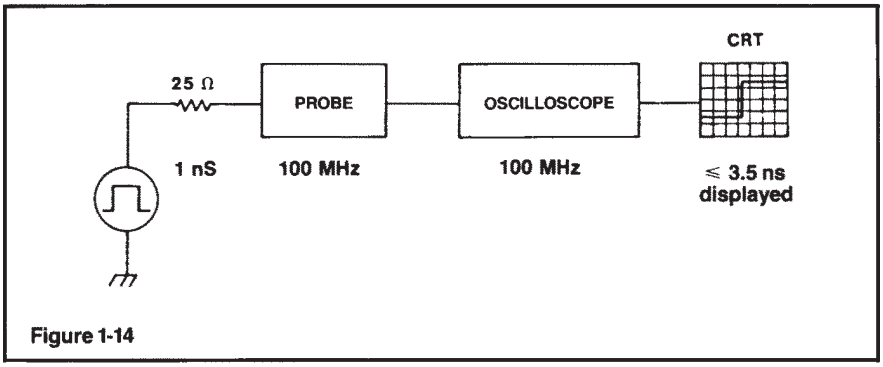


Figure 1-14

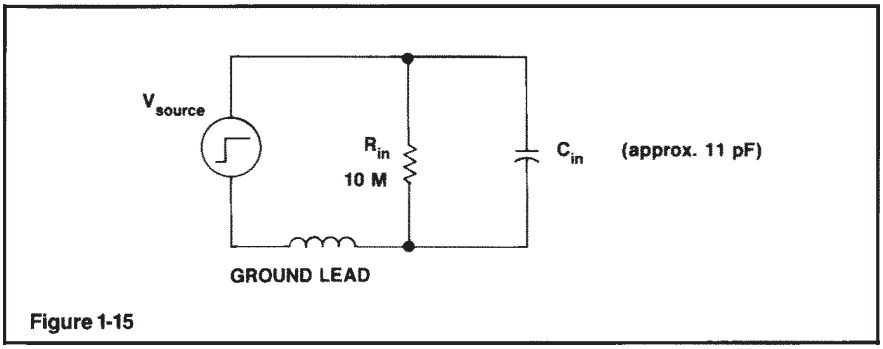


Figure 1-15

Scope Bandwidth at the Probe Tip ?

Most manufacturers of general-purpose oscilloscopes that include standard accessory probes in the package, promise and deliver the advertised scope bandwidth **at the probe tip.**

For example, the Tektronix 2465B 400 MHz Portable Oscilloscope and its standard accessory P6137 Passive Probes deliver 400 MHz (−3db) at the probe tip.

However, not all high performance scopes can offer this feature, even when used with their recommended passive probes. For example, the Tektronix 11A32 400 MHz plug-in has a system bandwidth of 300 MHz when used with its recommended P6134 passive probe. This is simply because even the highest impedance passive probes are limited to about 300 to 350 MHz, while still meeting their other specifications.

It is important to note that the above performance is only obtainable under strictly controlled, and industry recognized conditions; which states that the signal must originate from a 50 Ω back-terminated source (25 Ω), and that the probe must be connected to the source by means of a probe tip to BNC (for other) adaptor.

This method ensures the shortest ground path and necessary low impedance to drive the probe's input capacitance, and to provide the specified bandwidth at the signal acquisition point, the probe tip.

Real-world signals rarely originate from 25 Ω sources, so less than optimum transient response and bandwidth should be expected when measuring higher impedance circuits.

How ground leads affect measurements

A ground lead is a wire that provides a local ground-return path when you are measuring any signal. An inadequate ground lead (one that is too long or too high in inductance) can reduce the fidelity of the high frequency portion of the displayed signal.

What grounding system to use. When making **any** measurement, some form of ground path is required to make a basic two-terminal connection to the DUT. If you want to check the presence or absence of signals from low-frequency equipment, **and** if the equipment is line-powered and plugged into the same outlet system as the scope, then the common 3-wire ground system provides the signal ground return. However, this indirect route adds inductance in the signal path—it can also produce ringing and noise on the displayed signal and is not recommended.

When making any kind of absolute measurement, such as amplitude, risetime or time delay measurements, you should use the shortest grounding path possible, consistent with the need to move the probe among adjacent test points. The ultimate grounding system is an in-circuit ECB (etched circuit board) to probe tip adaptor. Tektronix can supply these for either miniature, compact or subminiature probe configurations.

Figure 1-15 shows an equivalent circuit of a typical passive probe connected to a source. The ground lead L and C_{in} form a series resonant circuit with only 10M ohm for damping. When hit with a pulse, it will ring. Also, excessive L in the ground lead will limit the changing current to C_{in}, limiting the risetime.

Without going into the mathematics, an 11pF passive probe with a 6-inch ground lead will ring at about 140MHz when excited by a fast pulse. As the ring frequency increases, it tends to get outside the passband of the scope and is greatly attenuated. So to increase the ring frequency, use the shortest ground lead possible and use a probe with the lowest input C.

Probe Ground Lead Effects. The effect of inappropriate grounding methods can be demonstrated several ways. Figs. 1-16A, B and C show the effect of a 12-inch ground lead when used on various bandwidth scopes.

In Figure 1-16A, the display on the 15MHz scope looks OK because the ringing abberations are beyond the passband of the instrument and are greatly attenuated. Figs. 1-16B and C show what the same signal looks like on 50MHz and 100MHz scopes.

Even with the shortest ground lead, the probe-DUT interface has the **potential** to ring. The potential to ring depends on the **speed** of the step function. The ability to **see** the resultant ringing oscillation depends on the scope system bandwidth.

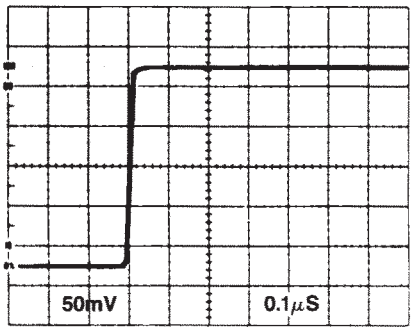


Figure 1-16A Scope BW = 15MHz, Ground lead 12 inches

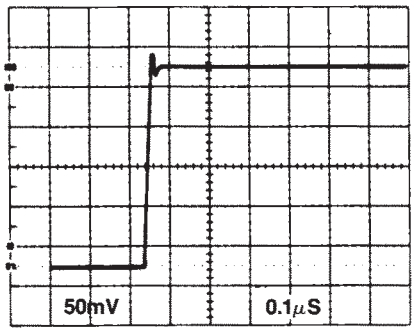


Figure 1-16B Scope BW = 50MHz, Ground lead 12 inches

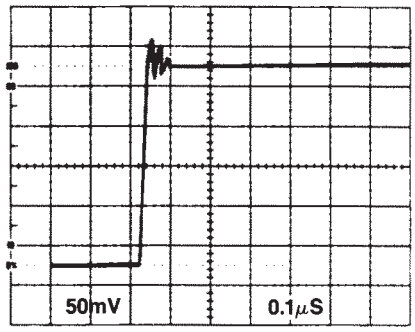


Figure 1-16C Scope BW = 100MHz, Ground lead 12 inches

Figs. 1-17A through F show the effects of various grounding methods and ground lead lengths on the display of a very fast pulse. This is the most critical way of looking at ground lead effects: we used a fast pulse, with a risetime of about 70 pico seconds and a fast (400 MHz) scope with a matching P6137 probe.

Fig. 1-17A shows the input pulse under the most optimum conditions when using 50 ohm coax cable. Scope: the Tektronix 2465B with 50 ohm input and 50 ohm cable from a 50 ohm source. Displayed risetime is < 1 nSec.

Fig. 1-17B shows the same signal when using the scope-probe combination under the most optimum conditions. A BNC to probe adaptor or an in-circuit test jack provides a coaxial ground that surrounds the probe ground ring. This sytem provides the shortest probe ground connection available. Displayed risetime is < 1nSec.

Figures 1-17C through E show the effects of longer ground leads on the displayed signal. Fig. 1-17C shows the effect of a short semi-flexible ground connection, called a "Z" lead. Finally, Fig. 1-17F shows what happens when no probe ground lead is used.

How probe design affects your measurements

Probes are available in a variety of sizes, shapes and functions, but they do share several main features: a probe head, coaxial cable and either a compensation box or a termination.

The probe head contains the signal-sensing circuitry. This circuitry may be passive (such as a 9-M ohm resistor shunted by an 11 pF capacitor in a passive voltage probe or a 125-turn transformer secondary in a current probe); or active (such as a source follower or Hall generator) in a current probe or active voltage probe.

The coaxial cable couples the probe head output to the termination. Cable types vary with probe types.

The termination has two functions:

- to terminate the cable in its characteristic impedance.
- to match the input impedance of the scope.

The termination may be passive or active circuitry. For easy connection to various test points, many probes feature interchangeable tips and ground leads.

A unique feature of most Tektronix probes is the Tektronix-patented coaxial cable that has a resistance-wire center conductor. This distributed resistance suppresses ringing caused by impedance mismatches between the cable and its terminations when you're viewing fast pulses on wideband scopes.

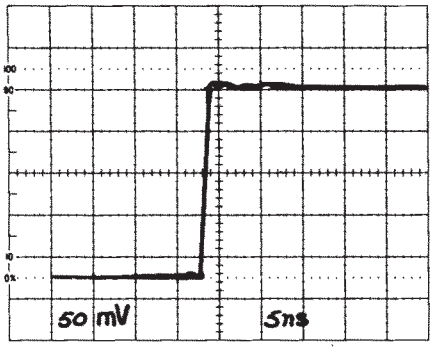


Figure 1-17A
50 ohm Source/Cable/2465B/50 ohm input

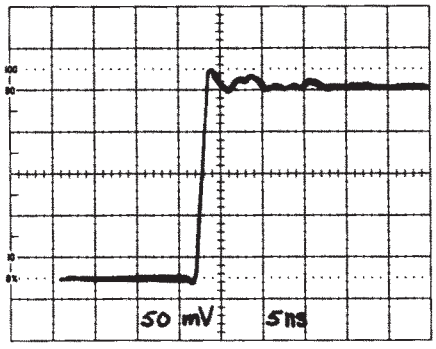


Figure 1-17B
P6137-BNC/Probe Adaptor Tr = < 1nS

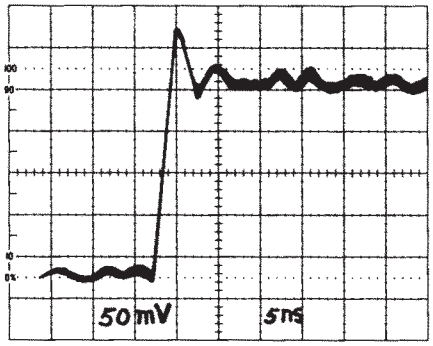


Figure 1-17C
P6137 - Probe/Z Ground Tr = 1.5 nS

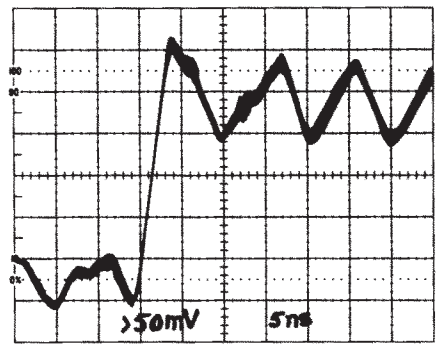


Figure 1-17D
P6137 - Probe/3" Gnd Lead Tr = 4 nS

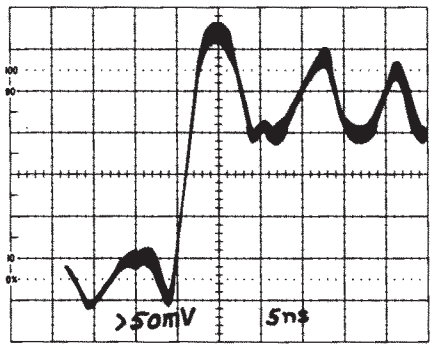


Figure 1-17E
P6137 - Probe/6" Gnd Lead Tr = 4 nS

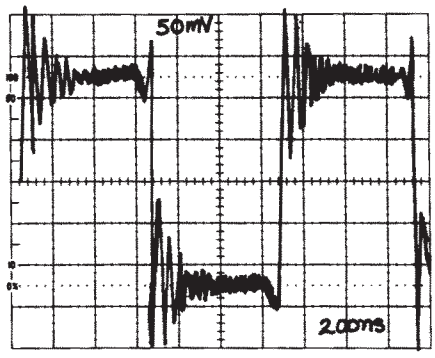


Figure 1-17F
No Ground Lead

PART II: EFFECTS OF PROBE COMPENSATION — UNDERSTANDING PROBES

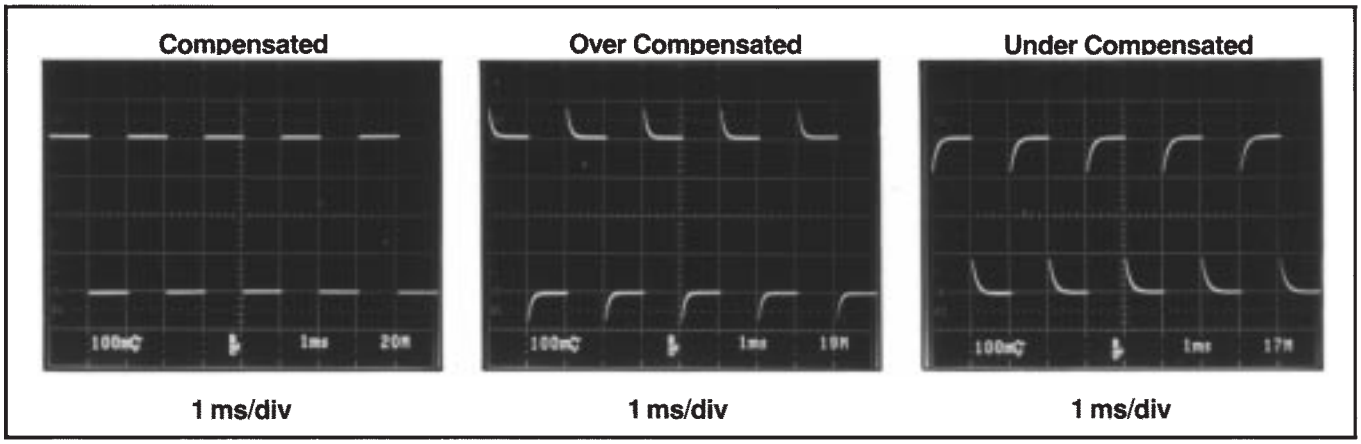


Figure 2-1. Shows the display associated with correctly and incorrectly compensated probes.

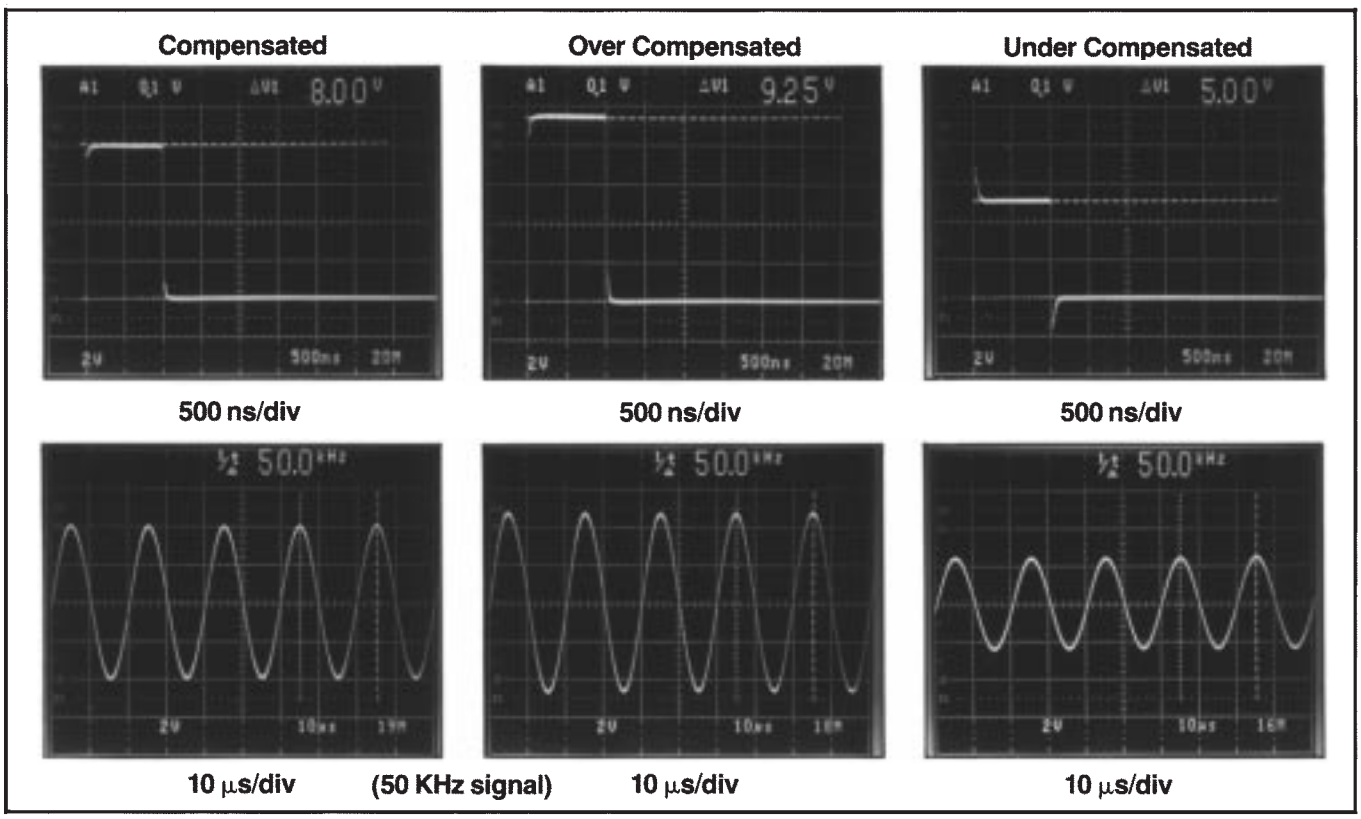


Figure 2-2. Shows the effects on faster pulses and sinewaves when an incorrectly compensated probe is used. Note that the much faster sweep rates used to correctly view these waveforms does not warn the user of an adjustment problem.

Tips on using probes

Compensating the probe. The most common mistake in making scope measurements is forgetting to compensate the probe. Improperly compensated probes can distort the waveforms displayed on the scope. The probe should be compensated as it will be used when you make the measurement.

The basic low frequency compensation (L.F. comp.) procedure is simple:

- Connect the probe tip to the scope CALIBRATOR (refer to Scope Calibrator Outputs.)
- Switch the channel 1 input coupling to dc.
- Turn on the scope and move the CH1 VOLTS/DIV switch to produce about four divisions of vertical display.
- Set the sweep rate to 1mSec/div. (for line-driven calibrators see Scope Calibrators Outputs.)
- Use a non-metalic alignment tool to turn the compensation adjust until the tops and bottoms of the square-wave are flat.

PART III: ADVANCED PROBING TECHNIQUES

Introduction:

In Part III we will examine some of the more advanced probing techniques associated with accessing high frequency and complex signals, such as fast ECL, waveforms offset from ground, and true differential signals.

Most of the techniques to be described follow recommended practices outlined throughout this Booklet, and to a large extent involve proper grounding techniques.

Workers in the audio and relatively low frequency fields may wonder what all the fuss is about, and may comment "I don't have any of these problems," or "I can't see any difference when I use different ground lead lengths, or even when I leave the ground lead completely off?"

In order to see abberrations caused by poor grounding techniques, two conditions must exist:

1. The scope system bandwidth must be great enough to handle the high frequency content existing at the probe tip.
2. The input signal must contain enough high frequency information (fast risetime) in order to cause ringing and aberrations due to poor grounding techniques.

To illustrate these points, a 20 MHz scope was used to access a 1.7 nS pulse by using a standard passive probe with a 6" ground lead.

NOTE: A fast scope can be made into a slow scope simply by pushing the Bandwidth Limit (B/W Limit) button ?.

We used a 350 MHz scope with a 20 MHz B/W Limit function.

Figure 3-1 shows the resultant clean displayed pulse with a risetime of about 20 nS (17.5 MHz).

This display does not represent conditions actually existing at the probe tip, because the 20 MHz measurement system cannot "see" what's really happening.

Figure 3-2 shows what the probe tip signal really looks like when a 350 MHz scope is used under the same conditions (B/W Limit off).

The observed risetime has improved to about 2 nS, but we have serious problems with ringing and aberrations, caused by incorrect grounding techniques.

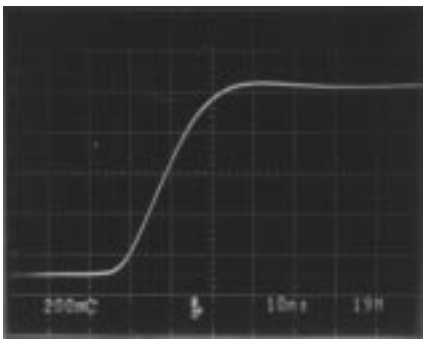


Figure 3-1. Resultant clean, but incorrect display caused by inadequate scope system bandwidth.

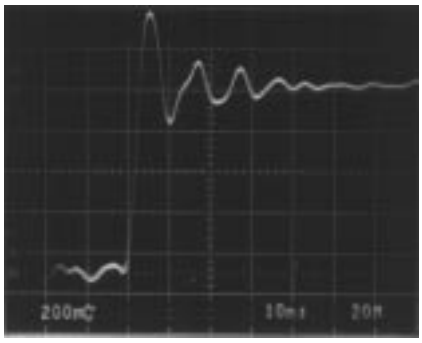


Figure 3-2. The same input signal as shown in figure 3-1, but accessed by a 350 MHz system bandwidth scope (same 6" ground lead).

The problem can now be seen because the scope system bandwidth is great enough to pass and display all the frequency content existing at the probe tip.

To further stress the points about high frequency content and scope system bandwidth, let's assume an input pulse with a risetime of about 20 nS. If the signal is accessed by the same probe /6" ground lead /350 MHz system, it would look very much like the display in figure 3-1.

There would be no frequency content higher than 17.5 MHz (20 nS Tr). The 6" ground lead would not ring, and would therefore be the correct choice for accessing this relatively slow signal.

In the following sections we discuss how to recognize signal acquisition problems, and how to avoid them.

Techniques for probing ECL, high speed 50 Ω environments, and accessing true differential signals are also discussed.

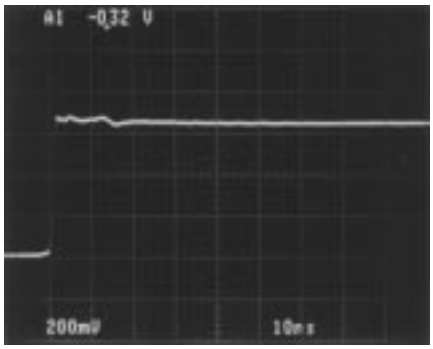


Figure 3-3. 1 nS Tr pulse accessed via an ECB to Probe Tip Adaptor (test point)

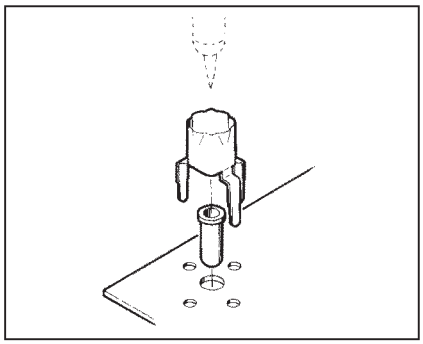


Figure 3-4. Typical ECB to Probe Tip Adaptor installation

Probe Ground Lead Effects. In Part I we discussed the basic need for probe grounding, and showed several different ways of looking at the effects of correct, and incorrect probe grounding.

In this section, we will expand upon these techniques and show how to identify problem areas.

When a probe (high Z, low Z, passive or active) is connected to the circuit under test via an ECB to Probe Tip Adaptor (test point), the coaxial environment existing at the probe tip is extended through the adaptor to the signal pick-off point, and to the ECB ground plane (or device ground).

Figure 3-3 shows what a typical 1 nS Tr pulse looks like when a suitable probe is connected to the circuit via an ECB to Probe Tip Adaptor.

Figure 3-4 shows a typical ECB to Probe Tip Adaptor (test point) installation.

These test points are available in three sizes to accept miniature, compact or sub-miniature series probes.

If a flexible ground lead is used in place of the ECB to Probe Tip Adaptor, the 1 nS Tr input step (with high frequency content up to 350 MHz) will cause the ground lead to ring at a frequency determined by the ground lead inductance and the probe tip and source capacitance.

Figure 3-5 shows the effect of using a 6" ground lead to make the ground connection.

The ring frequency for the 6" ground lead/probe tip C combination is 87.5 MHz. This signal is injected in series with the wanted signal and appears at the probe tip, as shown in figure 3-6.

Unfortunately, the problem is not this simple.

The probe's coaxial environment has been disrupted at the signal acquisition point by ground lead inductance, and is no longer correctly terminated (for high speed signal acquisition).

This abrupt transition leaves the probe's outer shield susceptible to ring frequency injection (the ground lead inductance is in series with the outer braid)

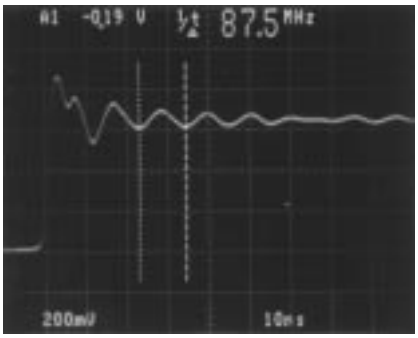


Figure 3-5. Effect of a 6" ground lead on a 1 nS Tr input step.

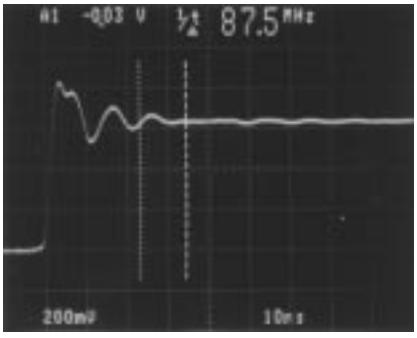


Figure 3-7. The same setup as in figure 3-5, except that the probe cable has been repositioned, and a hand has been placed over part of the probe cable.

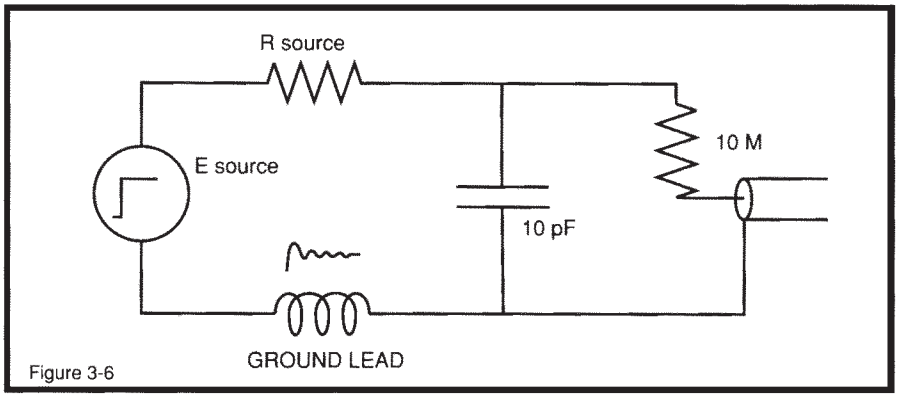


Figure 3-6. Equivalent circuit, ground lead inductance (excess inductance).

The now unterminated probe cable system develops reflections, which intermix with the ring frequency and the signal to produce a multitude of problems and unpredictable results.

Herein lies the key to the identification of ground lead problems.

Figure 3-7 shows exactly the same setup as in figure 3-5, except that the probe cable has been moved, and a hand has been placed over part of the probe cable.

KEY: If touching or moving the probe cable produces changes in the display, you have a probe grounding problem.

A correctly grounded (terminated) probe should be completely insensitive to cable positioning or touch.

Ground Lead Length. All things being equal, the shortest ground lead produces the highest ring frequency.

If the lead is very short, the ring frequency might be high enough to be outside the passband of the scope, and/or the input frequency content may not be high enough to stimulate the ground lead's resonant circuit.

In all cases, the shortest ground lead should be used, consistant with the need for probe mobility.

If possible, use 3" or shorter ground leads, such as the Low Impedance Contact (Z Lead). These are supplied with the Tektronix P613X and P623X family or probes.

One final note. The correct probe grounding method depends on the signal's high frequency content, the scope system bandwidth, and the need for mobility between test points.

A 12" ground lead may be perfect for many lower frequency applications. It will provide you with extra mobility, and nothing will be gained by using shorter leads.

If in doubt, apply the cable touch test outlined previously.

Ground Loop Noise Injection. Another form of signal distortion can be caused by signal injection into the grounding system.

This can be caused by unwanted current flow in the ground loop existing between the common scope and test circuit power line grounds, and the probe ground lead and cable.

Normally, all these points are, or should be at zero volts, and no ground current will flow.

However, if the scope and test circuit are on different building system grounds, there could be small voltage differences, or noise on one of the building ground systems.

The resulting current flow (at line frequency or noise frequency) will develop a voltage drop across the probe cable's outer shield, and be injected into the scope in series with the desired signal.

Inductive Pickup in Ground Loops. Noise can enter a common ground system by induction into long 50 Ω signal acquisition cables, or into standard probe cables.

Proximity to power lines or other current-carrying conductors can induce current flow in the probe's outer cable, or in standard 50 Ω coax. The circuit is completed through the building system common ground.

Prevention of Ground Loop Noise Problems. Keep all signal acquisition probes and/or cables away from sources of potential interference.

Verify the integrity of the building system ground.

If the problem persists, open the ground loop:

1. By using a Ground Isolation Monitor like the Tektronix A6901.
2. By using a power line isolation transformer on either the test circuit or on the scope.
3. By using an Isolation Amplifier like the Tektronix A6902B.
4. By using differential probes (see Differential Measurements).

NOTE: Never defeat the safety 3-wire ground system on either the scope or on the test circuit.

Do not "float" the scope, except by using an approved isolation transformer, or preferably, by using the Tektronix A6901 Ground Isolation Monitor.

The A6901 automatically reconnects the ground if scope ground voltages exceed ± 40 V.

Induced Noise in Probe Ground Leads. The typical probe ground lead resembles a single-turn loop antenna when it is connected to the test circuit.

The relatively low impedance of the test circuit can couple any induced voltages into the probe, as shown in figure 3-8.

High speed logic circuits can produce significant electro-magnetic (radiated) noise at close quarters.

If the probe ground lead is positioned too close to certain areas on the board, interference signals could be picked up by the loop antenna formed by the probe ground lead, and mix with the probe tip signal.

Question: Is this what my signal really looks like?

Moving the probe ground lead around will help identify the problem.

If the **noise level** changes, you have a ground lead induced noise problem.

A more positive way of identification is to disconnect the probe from the signal source and clip the ground lead to the probe tip.

Now use the probe/ground lead as a loop antenna and search the board for radiated noise.

Figure 3-9 shows what can be found on a logic board, **with the probe tip shorted to the ground lead.**

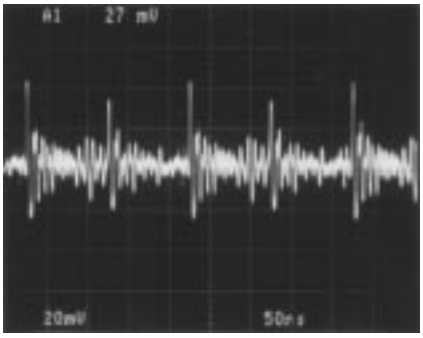


Figure 3-9. Induced noise in the probe ground loop (tip shorted to the ground clip).

This is radiated noise, induced in the single-turn loop and fed to the probe tip.

The significance of any induced or injected noise increases with reduced working signal levels, because the signal to noise ratio will be degraded. This is especially true with ECL, where signal levels are 1 V or less.

Prevention: If possible, use an ECB to Probe Tip Adaptor (test point). If not, use a Z Lead or short flexible ground lead.

Also, bunch the ground lead together to make the loop area as small as possible.

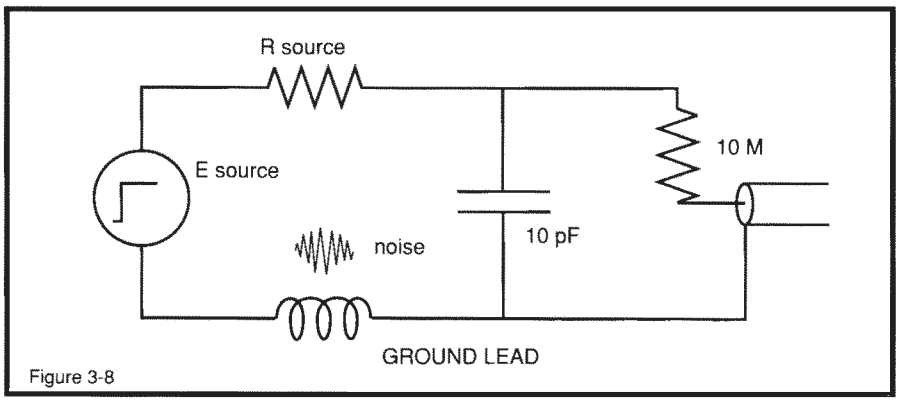


Figure 3-8. Equivalent Circuit. Ground Lead Induced Noise.

Bias Offset Probes. A Bias/Offset probe is a special kind of Low Z design with the capability of providing a variable bias or offset voltage at the probe tip.

Bias/Offset probes like the Tektronix P6230 and P6231 are useful for probing high speed ECL circuitry, where resistive loading could upset the operating point.

They are also useful for probing higher amplitude signals (up to ± 5 V), where resistive loading could affect the DC level at some point on the waveform.

Bias/Offset probes are designed with a tip resistance of 450 Ω (10X). When these probes are connected into a 50 Ω environment, this loading results in a 10% reduction in peak to peak source amplitude. This round-figure loading is more convenient to handle than that produced by a standard 500 Ω (10 X) Low Z probe, which would work out at 9.09% under the same conditions.

It is important to note that bias/offset probes always present a 450 Ω resistive load to the source, regardless of the bias/offset voltage selected.

The difference between bias/offset and standard Low Z probes lies in their ability to null current flow **at some specific and selectable point** on the input waveform (within ± 5 V).

To see how bias/offset probes work, let's take a typical 10 × 500 Ω Low Z probe and connect it in the circuit shown in figure 3-10.

By taking a current flow approach we find that at one point on the waveform the source voltage is − 4 V, therefore the load current will be;

$$I = ER = 4/Rs + Rp + R\,scope = 4/550 = 7.27\ mA.$$

Therefore the voltage drop across the 50 Ω source resistance (Rs) will be;

$$E = IR = 7.27 \times 10^{-3} \times 50 = 0.363\ V$$

And the measured pulse amplitude will be −4 −0.363 = 3.637 V (E dut), or about 9% down from its unloaded state.

If we substitute the 500 Ω Low Z probe with a 450 Ω bias/offset probe, the circuit will look like figure 3-11.

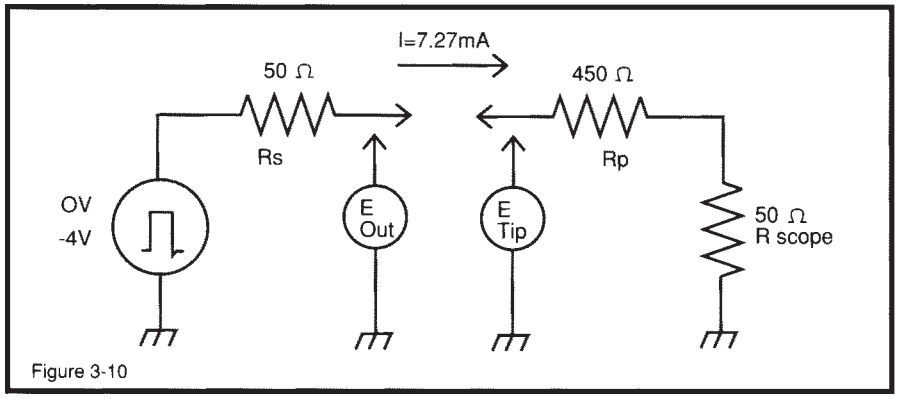


Figure 3-10. Low Z 10X 500 Ω probe connected to a 50 Ω source.

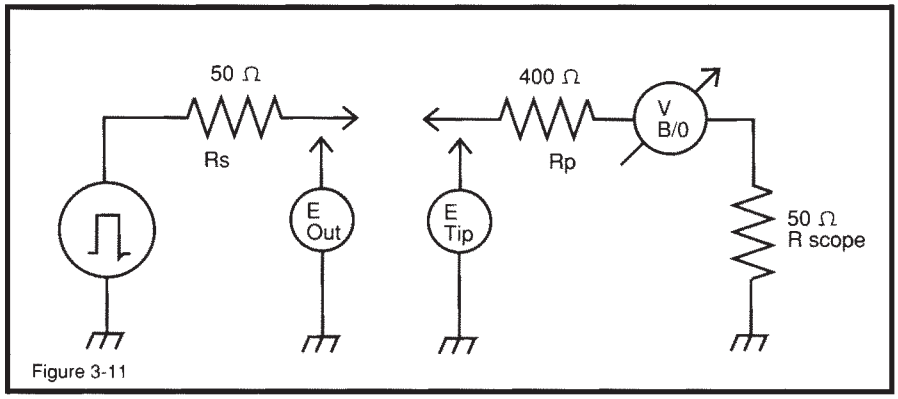


Figure 3-11. A 450 Ω Bias/Offset probe connected to a 50 Ω source.

With the bias/offset adjusted for 0 V, the effect on the circuit will be similiar to a 500 Ω Low Z probe, except for the small resistive change.

Figure 3-12 shows the source waveform acquired by a 10 MΩ probe.

Figure 3-13 shows the effect on the waveform when the 450 Ω probe is added.

As expected, the pulse amplitude has reduced from −4 V to 3.60 V, or exactly 10% down.

Figure 3-14 shows the effect of adjusting the offset to −4 V. The −4 V bias opposes the signal at the −4 V level and results in zero current flow, and the source is effectively unloaded **at this point.**

However, when the signal returns to ground level, there is a 4 V differential between the top of the pulse and the bias/offset source. Current will flow, and Ohms Law will dictate that the top of the pulse will go negative by −40 mV (10%).

Sometimes it is desirable to adjust the offset mid-way between the peak to peak excursions. This distributes the effect of resistive loading between the two voltage swings.

Figure 3-15 shows the effect of adjusting the bias/offset to −2 V. Current flow will be the same for both signal swings, and they will be equally down by 5%, for a total of 10%.

Summary:

1. Bias/Offset probes can be adjusted (within ± 5 V) to provide zero resistive (effective) loading at one selected point on the input waveform.
2. Bias/Offset probes can be used to simulate the effect of pull-up or pull-down voltages (within ± 5 V) on the circuit under test (voltage source impedance is 450 Ω).
3. Bias/Offset probes always present a total resistive load of 450 Ω, and reduce the peak to peak amplitude of 50 Ω sources by 10%.
4. For simplicity, we have ignored the effects of capacitive loading. Typically, Bias/Offset probes have less than 2 pF tip C.

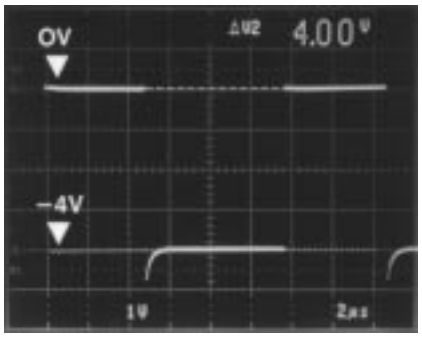


Figure 3-12. Unloaded negative-going 4 V pulse acquired by a 10 MΩ probe.

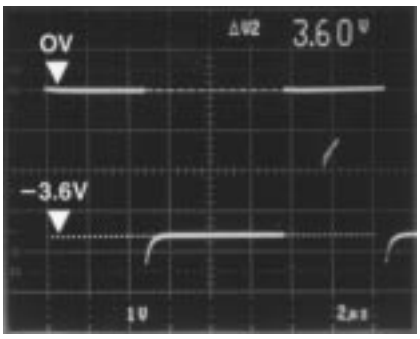


Figure 3-13. Effect of connecting a 450 Ω Bias/Offset probe (offset = 0 V). Minus level has been reduced by 10%.

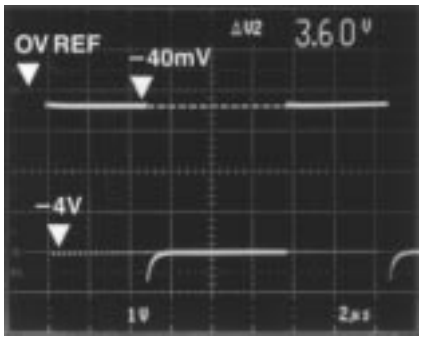


Figure 3-14. Bias/Offset adjusted for −4 V. Signal current at the −4 V level is zero. Current flow at ground level is maximum. Peak to peak amplitude remains the same (10% down).

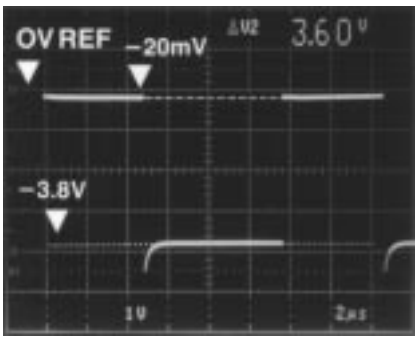


Figure 3-15. Bias/Offset adjusted for −2 V. Load current distributed between the negative and positive-going swings. Peak to peak amplitude remains the same (10% down).

Bias/Offset probes like the Tektronix P6230 or P6231 have bandwidths to 1.5 GHz, 450 Ω input R, and 1.3 pF (P6230), or 1.6 pF (P6231) input C.

They provide offset voltages of ± 5 V DC, and function with 1 MΩ or 50 Ω input systems (P6231, 50 Ω only).

The P6230 obtains operating power, either from the scope itself, or from the Tektronix 1101A or 1102 Power Supply.

The P6231 is designed to operate with the Tektronix 11000 Series scopes, and obtains operating power and bias/offset from the scope. Offset is selectable from the mainframe touch screen.

Differential Probing Techniques. Accessing small signals elevated from ground, either at an AC level or a combination of AC and DC, requires the use of differential probes and a differential amplifier system.

One of the problems associated with differential measurements is the maintenance of high common mode rejection ratio (CMRR) at high common mode frequencies.

Poor common mode performance allows a significant portion of the common (elevated) voltage to appear across the differential probe's inputs. If the common mode voltage is pure DC, the result may only be a displayed baseline shift. However, if the common mode voltage is AC, or a combination of AC and DC, a significant portion may appear across the differential input and will mix with the desired signal.

Figure 3-16 shows the basic items necessary to make a differential measurement.

In this example two similar but un-matched passive probes are used. The probe ground leads are usually either removed or clipped together. They are **never** connected to the elevated DUT (device under test).

CMRR depends upon accurate matching of the probe-pair's electrical characteristics, including cable length. System CMRR can be no better than the differential amplifier's specifications, and in all cases, CMRR degrades as a function of frequency.

Figure 3-17 shows a simplified diagram of a DUT with a pulsed output of 1 V p-p floating on a 5 V p-p 20 MHz sinewave.

CMRR at 20 MHz is a poor 10:1 because of the un-matched probes.

Observed signal. (referred to probe input) = 1 V p-p pulse + (5 V p-p sine/10) = 1 V p-p pulse + 0.5 V p-p sine.

Figure 3-18a shows what the displayed waveform might look like under the conditions shown in figure 3-17.

In comparison, figures 3-18b and 3-18c show what the displayed signal might look like at CMRR's of 100:1 and 1000:1.

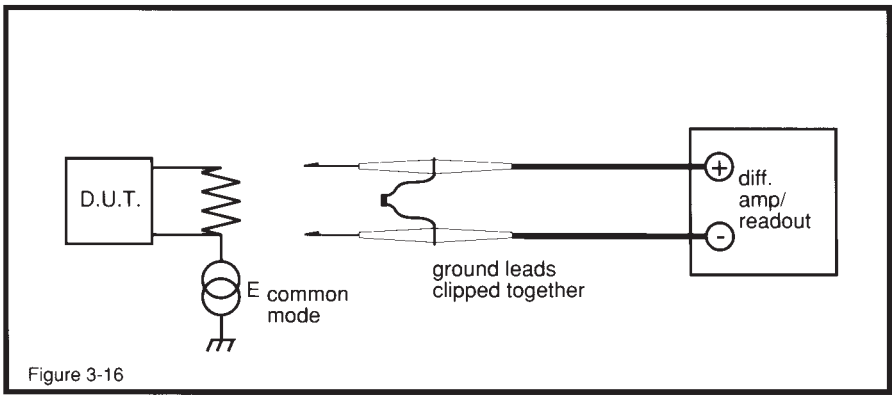


Figure 3-16. Basic connections to a device under test to make a differential measurement.

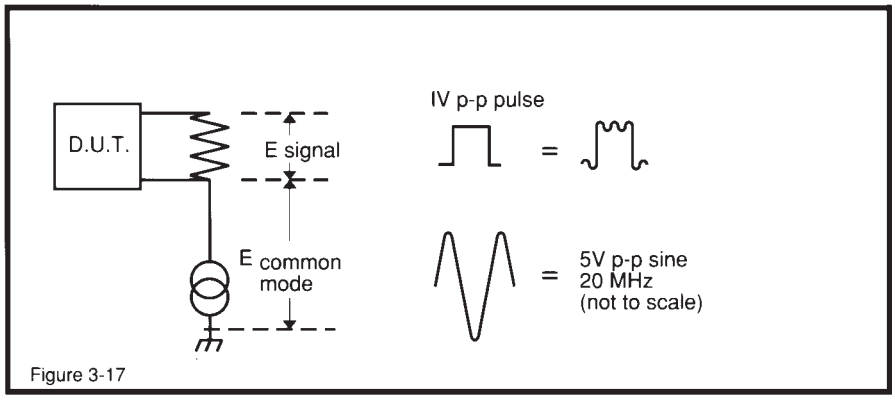
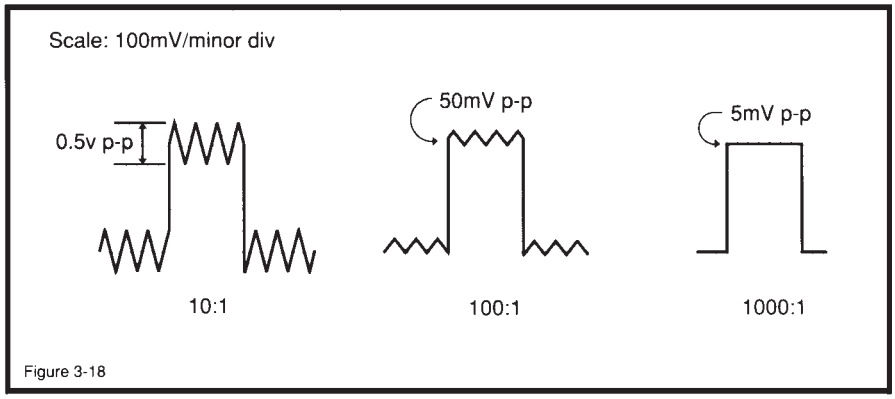


Figure 3-17. Simplified diagram. Elevated DUT. Common mode rejection is 10:1 at 20 MHz.



Figures 3-18, a, b and c. Displayed waveforms from the circuit shown in figure 3-17 at CMRR's of 10:1, 100:1 and 1000:1.

APPENDIX B

Measuring Amplifier Settling Time

High resolution measurement of amplifier settling at high speed is often necessary. Frequently, the amplifier is driven from a digital-to-analog converter (DAC). In particular, the time required for the DAC-amplifier combination to settle to final value after an input step is especially important. This specification allows setting a circuit's timing margins with confidence that the data produced is accurate. The settling time is the total length of time from input step application until the amplifier output remains within a specified error band around the final value.

Figure B1 shows one way to measure DAC amplifier settling time. The circuit uses the false sum node technique. The resistors and amplifier form a summing network. The amplifier output will step positive when the DAC moves. During slew, the oscilloscope probe is bounded by the diodes, limiting voltage excursion. When settling occurs, the summing node is arranged so the oscilloscope probe voltage should be zero. Note that the resistor divider's attenuation means the probe's output will be one-half the actual settled voltage.

In theory, this circuit allows settling to be observed to small amplitudes. In practice, it cannot be relied upon to produce useful measurements. Several flaws exist. The oscilloscope connection presents problems. As probe capacitance rises, AC loading of the resistor junction will influence observed settling waveforms. The 20pF probe shown alleviates this problem but its 10X attenuation sacrifices oscilloscope gain. 1X probes are not suitable because of their excessive input capacitance. An active 1X FET probe might work, but another issue remains.

The clamp diodes at the probe point are intended to reduce swing during amplifier slewing, preventing excessive oscilloscope overdrive. Unfortunately, oscilloscope overdrive recovery characteristics vary widely among different types and are not usually specified. The diodes' 600mV drop means the oscilloscope may see an unacceptable overload, bringing displayed results into question (for a discussion of oscilloscope overdrive considerations, see the Tutorial Section on Oscilloscopes). With the oscilloscope set at 1mV per division, the diode bound allows a 600:1 overdrive. Schottky diodes can cut this in half, but this is still much more than any real-time vertical amplifier is designed to accommodate.[1] The oscilloscope's overload recovery will completely dominate the observed waveform and all measurements will be meaningless.

One way to achieve reliable settling time measurements is to clip the incoming waveform in *time*, as well as amplitude. If the oscilloscope is prevented from seeing the waveform until settling is nearly complete, overload is avoided. Doing this requires placing a switch at the settle circuit's output and controlling it with an input-triggered, variable delay. FET switches are not suitable because of their gate-source capacitance. This capacitance will allow gate drive artifacts to corrupt the oscilloscope display,

Note 1: See Reference 3 for history and wisdom about vertical amplifiers.

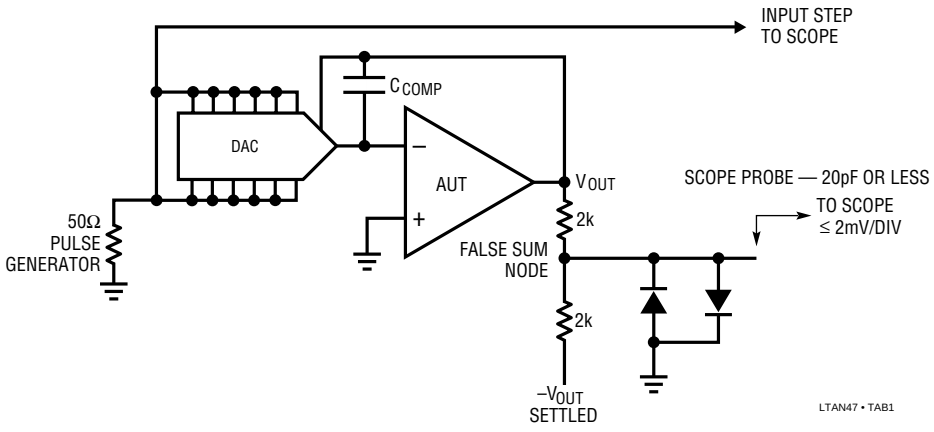


Figure B1. One (Not Very Good) Way to Measure DAC-Op Amp Settling Time

producing confusing readings. In the worst case, gate drive transients will be large enough to induce overload, defeating the switch's purpose.

Figure B2 shows a way to implement the switch which largely eliminates these problems. This circuit allows settling within 1mV to be observed. The Schottky sampling bridge is the actual switch. The bridge's inherent balance, combined with matched diodes and very high speed complementary bridge switching, yields a clean switched output. An output buffer stage unloads the settle node and drives the diode bridge.

The operation of the DAC-amplifier is as before. The additional circuitry provides the delayed switching function, eliminating oscilloscope overdrive. The settle node is buffered by A1, a unity gain broadband FET input buffer with 3pF input capacitance and 350MHz bandwidth. A1 drives the Schottky bridge. The pulse generator's output fires the 74123 one shot. The one shot is arranged to produce a delayed (controllable by the 20k potentiometer) pulse whose width (controllable by the 5k potentiometer) sets diode bridge on-time. If the delay is set appropriately, the oscilloscope will not see any input until settling is nearly complete, eliminating overdrive. The sample window width is adjusted so that all remaining settling activity is observable. In this way the oscilloscope's output is reliable and meaningful data may be taken. The one shot's output is level shifted by the Q1-Q4 transistors, providing complementary switching drive to the bridge. The actual switching transistors, Q1-Q2, are UHF types, permitting true differential bridge switching with less than 1ns of time skew.[2] The bridge's output may be observed directly (by oscilloscopes with adequate sensitivity) or A2 provides a times 10 amplified version. A2's gain of 20 (and the direct output's ÷ 2 scaling) derives from the 2k-2k settle node dividers attenuation. A third output, taken directly from A1, is also available. This output, which bypasses the entire switching circuitry, is designed to be monitored by a sampling oscilloscope. Sampling oscilloscopes are inherently immune to overload.[3] As such, a good test of this settling time test fixture (and the above statement) is to compare the signals displayed by the sampling 'scope and the Schottky-bridge-aided real time 'scope. As an *additional* test, a completely different method of measuring settling time (albeit considerably more complex) described by Harvey[4] was also employed. If all three approaches represent good measurement technique and are constructed properly, results should be identical.[5] If this is the case, the identical data produced by the three methods has a high probability of being valid. Figures B3, B4 and B5 show settling time details of an AD565A DAC and an LT1220 op amp. The photos represent the sampling bridge, sampling 'scope and Harvey methods, respectively. Photos B3 and B5 display the input step for convenience in ascertaining elapsed time. Photo B4, taken with a single trace sampling oscilloscope (Tektronix 1S1 with P6032 cathode follower probe in a 556 mainframe) uses the leftmost vertical graticule line as its zero time reference. All methods agree on 280ns to 0.01% settling (1mV on a 10V step). Note that Harvey's method inherently adds 30ns, which must be subtracted from the displayed 310ns to get the real number.[6] Additionally, the shape of the settling waveform, in every detail, is identical in all three photographs. This kind of agreement provides a high degree of credibility to the measured results.

Some poorly designed amplifiers exhibit a substantial thermal tail after responding to an input step. This phenomenon, due to die heating, can cause the output to wander outside desired limits long after settling has apparently occurred. After checking settling at high speed, it is always a good idea to slow the oscilloscope sweep down and look for thermal tails. Often the thermal tail's effect can be accentuated by loading the amplifier's output. Such a tail can make an amplifier appear to have settled in a much shorter time than it actually has.

To get the best possible settling time from any amplifier, the feedback capacitor, C_F, should be carefully chosen. C_F's purpose is to roll-off amplifier gain at the frequency which permits best dynamic response. The optimum value for C_F will depend on the feedback resistor's value and the characteristics of the source. DAC's are one of the most common sources and also one of the most difficult. DAC's current outputs must often be converted to a

Note 2: The Q1-Q4 bridge switching scheme, a variant of one described in Reference 14, was developed at LTC by George Feliz.
Note 3: See References 7, 8 and 18.
Note 4: See Reference 17.
Note 5: Construction details of the settling time fixture discussed here appear (literally) in Appendix F, "Additional Comments on Breadboarding". Also see the Tutorial Section on Breadboarding Techniques.
Note 6: See Reference 17.

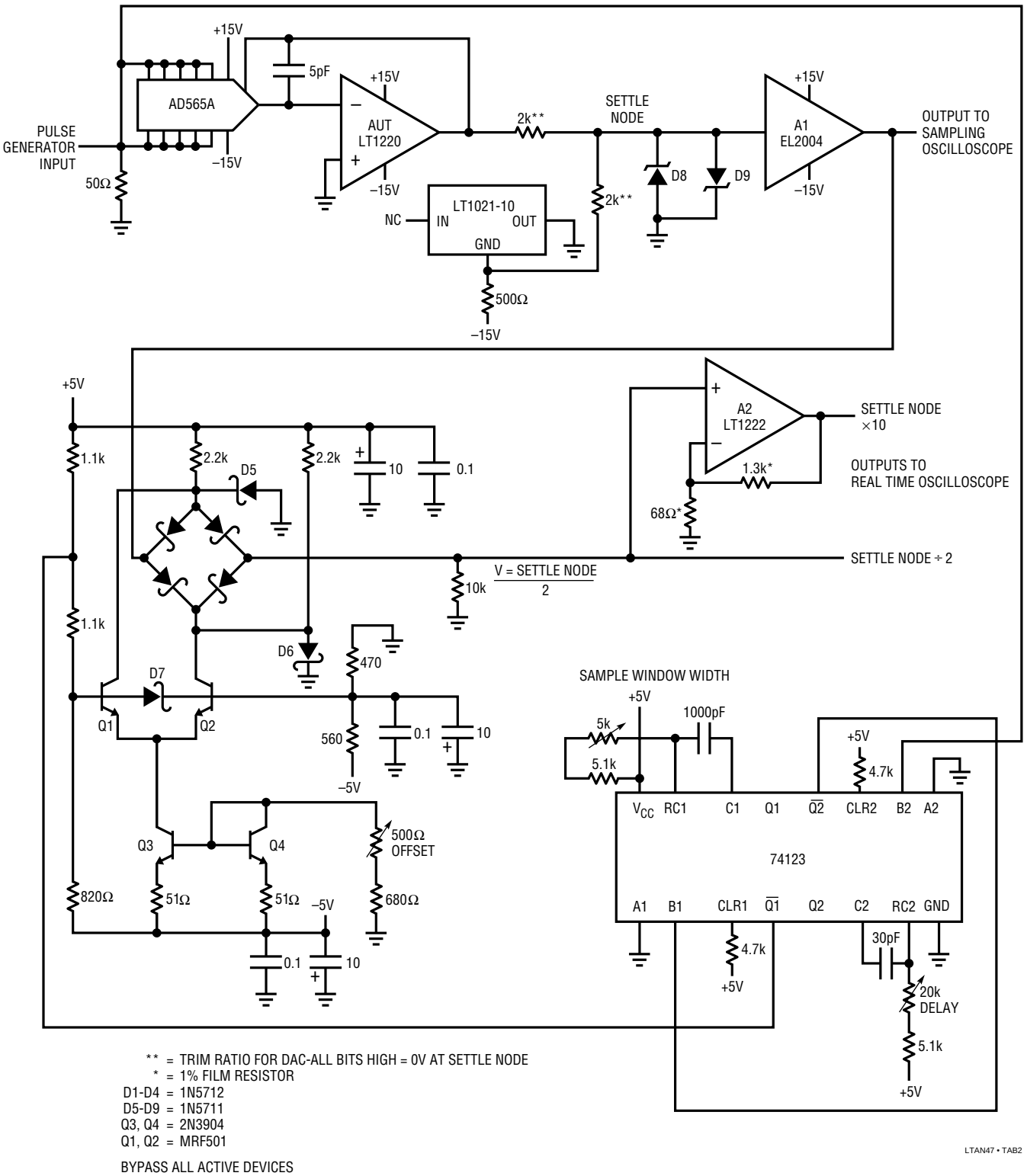


Figure B2. Settling Time Test Circuit Using a Sampling Bridge Eliminates Oscilloscope Overdrive

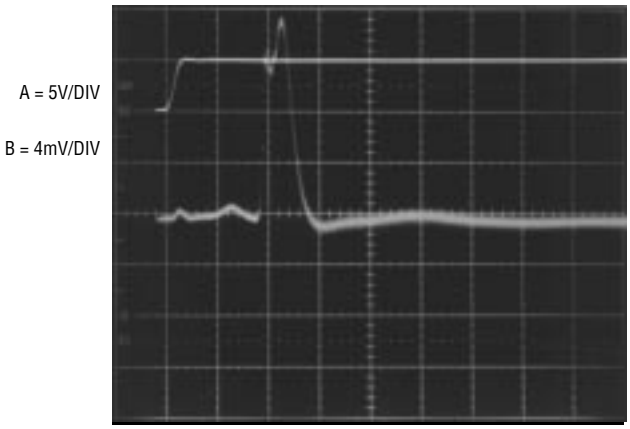


Figure B3. 280ns Settling Time as Measured by Figure B2's Circuit. Sampling Switch Closes Just Before Third Vertical Division, Allowing Settling Detail to be Observed Without Overdriving the Oscilloscope

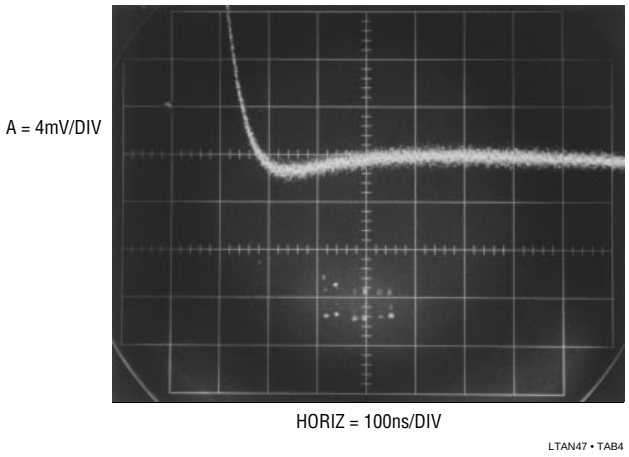


Figure B4. 280ns Settling Time as Measured at Figure B2's Sampling Oscilloscope Output by a Sampling 'Scope. Settling Time and Waveform Shape is Identical to Figure B3

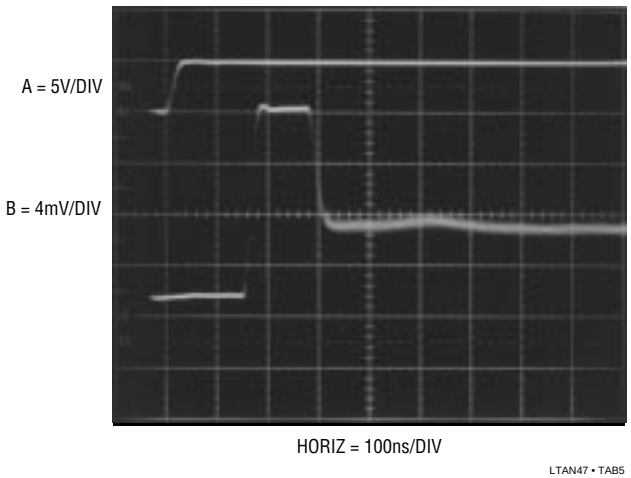


Figure B5. 280ns Settling Time as Measured by Harvey's Method. After Subtraction of this Method's Inherent 30ns Delay, Settling Time and Waveform Shape are Identical to Figures B3 and B4

voltage. Although an op amp can easily do this, care is required to obtain good dynamic performance. A fast DAC can settle to 0.01% in 200ns or less but its output also includes a parasitic capacitance term, making the amplifier's job more difficult. Normally, the DAC's current output is unloaded directly into the amplifier's summing junction, placing the parasitic capacitance from ground to the amplifier's input. The capacitance introduces feedback phase shift at high frequencies, forcing the amplifier to hunt and ring about the final value before settling. Different DACs have different values of output capacitance. CMOS DACs have the highest output capacitance and it varies with code. Bipolar DACs typically have 20pF-30pF of capacitance, stable over all codes. Because of their output capacitance, DAC's furnish an instructive example in amplifier compensation. Figure B6 shows the response of an industry standard DAC-80 type and a relatively slow (for this publication) op amp. Trace A is the input, while Traces B and C are the amplifier and settle outputs, respectively. In this example no compensation capacitor is used and the amplifier rings badly before settling. In Figure B7, an 82pF unit stops the ringing and settling time goes down to 4µs. The overdamped response means that C_F dominates the capacitance at the AUT's input and stability is assured. If fastest response is desired, C_F must be reduced. Figure B8 shows critically damped behavior obtained with a 22pF unit. The settling time of 2µs is the best obtainable for this DAC-amplifier combination. Higher speed is possible with faster amplifiers and DACs but the compensation issues remain the same.

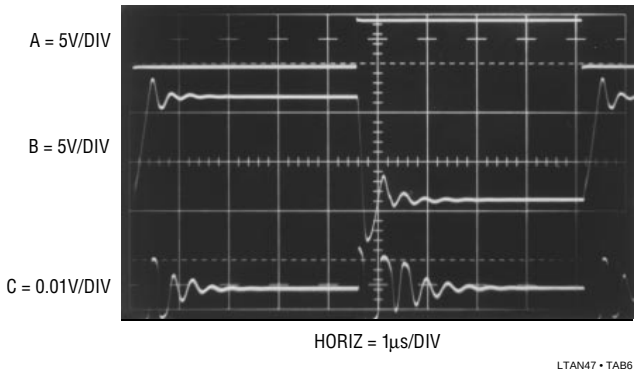


Figure B6. No Feedback Capacitor

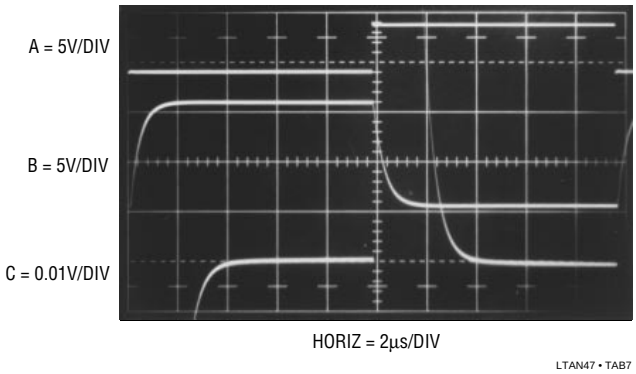


Figure B7. Relatively Large Feedback Capacitor

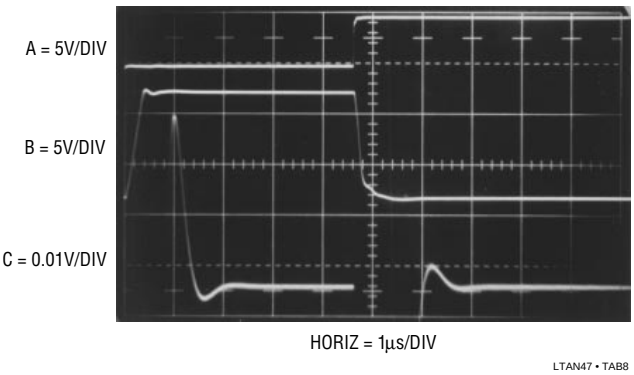


Figure B8. Reduced Feedback Capacitor Gives Fastest Settling

Figures B6-B8. Effects of Different Feedback Capacitors on a DAC-Op Amp Combination

APPENDIX C

The Oscillation Problem – Frequency Compensation Without Tears

All feedback systems have the propensity to oscillate. Basic theory tells us that gain and phase shift are required to build an oscillator. Unfortunately, feedback systems, such as operational amplifiers, have gain and phase shift. The close relationship between oscillators and feedback amplifiers requires careful attention when an op amp is designed. In particular, excessive input-to-output phase shift can cause the amplifier to oscillate when feedback is applied. Further, any time delay placed in the amplifier's feedback path introduces additional phase shift, increasing the likelihood of oscillation. This is why feedback loop enclosed stages can cause oscillation.

A large body of complex mathematics is available which describes stability criteria and can be used to predict stability characteristics of feedback amplifiers. For the most sophisticated applications, this approach is required to achieve optimum performance.

However, little has appeared which discusses, in practical terms, how to understand and address the issues of compensating feedback amplifiers. Specifically, a practical approach to stabilizing amplifier-power gain stage combinations is discussed here, although the considerations can be generalized to other feedback systems.

Oscillation problems in amplifier-power booster stage combinations fall into two broad categories; local and loop

oscillations. *Local* oscillations can occur in the boost stage, but should not appear in the IC op amp, which presumably was debugged prior to sale. These oscillations are due to transistor parasitics, layout and circuit configuration-caused instabilities. They are usually relatively high in frequency, typically in the 0.5MHz to 100MHz range. Usually, local booster stage oscillations do not cause loop disruption. The major loop continues to function, but contains artifacts of the local oscillation. Text Figure 101, repeated here as Figure C1 for reader convenience, furnishes an instructive example. The Q1, Q2 emitter follower pair has reasonably high f_t. These devices will oscillate if driven from a low impedance source (see insert, Figure C1 and References 43 and 44). The 100Ω resistor and the ferrite beads are included to make the op amps output look like a higher impedance to prevent problems. Q5 and Q6, also followers, have even higher f_t, but are driven from 330Ω sources, eliminating the problem.The photo in Figure C2 shows Figure C1 following an input with the 100Ω resistor and ferrite beads removed. Trace A is the input, while Trace B is the output. The resultant high frequency oscillation is typical of locally caused disturbances. Note that the major loop is functional, but the local oscillation corrupts the waveform.

Eliminating such local oscillations starts with device selection. Avoid high f_t transistors unless they are needed. When high frequency devices are in use, plan layout carefully. In very stubborn cases, it may be necessary to lightly bypass transistor junctions with small capacitors or RC networks. Circuits which use local feedback can sometimes require careful transistor selection and use. For example, transistors operating in a local loop may require different f_ts to achieve stability. Emitter followers are notorious sources of oscillation and should never be directly driven from low impedance sources (again, see References 43 and 44).

Loop oscillations are caused when the added gain stage supplies enough delay to force substantial phase shift. This causes the control amplifier to run too far out of phase with the gain stage. The control amplifier's gain combined with the added delay causes oscillation. Loop oscillations are usually relatively low in frequency, typically 10Hz-1MHz.

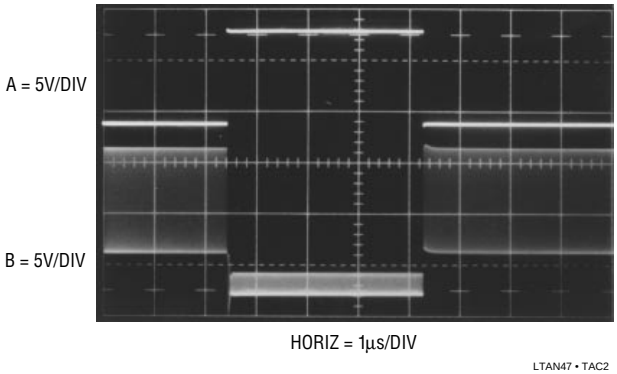


Figure C2. Local Oscillations Due to Booster Stage Instabilities

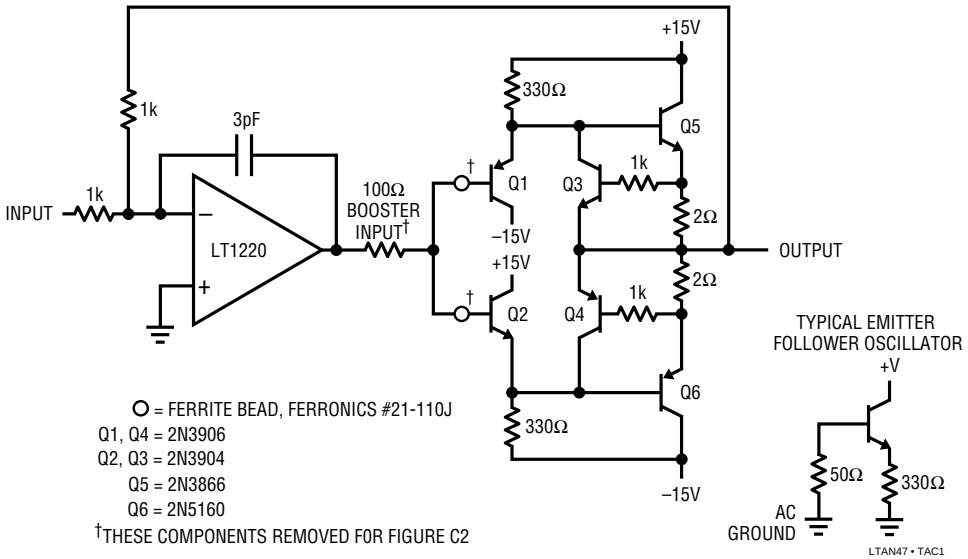


Figure C1. Figure 101's Booster Circuit with a Few Components Removed Begins Our Study of Loop Stability

A good way to eliminate loop-caused oscillations is to limit the gain-bandwidth of the control amplifier. If the booster stage has higher gain-bandwidth than the control amplifier, its phase delay is easily accommodated in the loop. When control amplifier gain-bandwidth dominates, oscillation is assured. Under these conditions, the control amplifier hopelessly tries to servo a feedback signal which consistently arrives too late. The servo action takes the form of an electronic tail chase with oscillation centered around the ideal servo point.

Frequency response roll-off of the control amplifier will almost always cure loop oscillations. In many situations it is preferable to brute force compensation using large capacitors in the major feedback loop. As a general rule, it is wise to stabilize the loop by rolling off control amplifier gain-bandwidth. The feedback capacitor serves only to trim step response and should not be relied on to stop outright oscillation.

Figures C3 and C4 illustrate these issues. The LT1006 amplifier used with the LT1010 current buffer produces the output shown in Figure C4. As before, Trace A is the input and Trace B the output. The LT1006 has less than

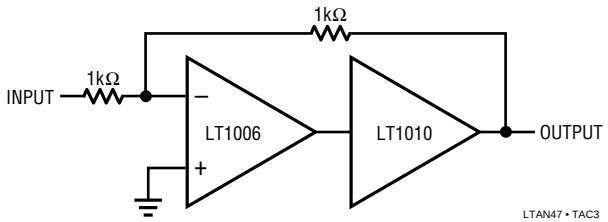


Figure C3. A Slow Op Amp and a Medium Speed Booster

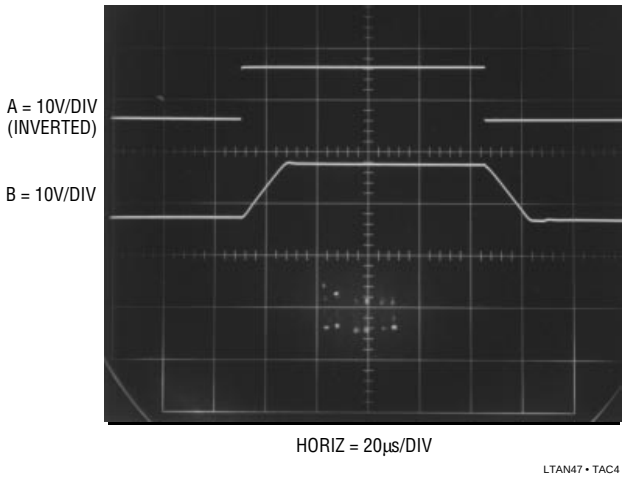


Figure C4. Loop Stability is "Free" When the Op Amp is Much Slower than the Booster

1MHz gain-bandwidth. The LT1010's 20MHz gain-bandwidth introduces negligible loop delay, and dynamics are clean. In this case, the LT1006's internal roll-off is well below that of the output stage and stability is achieved with no external compensation components. Figure C5 uses a 100MHz bandwidth LT1223 as the control amplifier. The associated photo (Figure C6) shows the results. Here, the control amplifier's roll-off is well beyond the output stage's, causing problems. The phase shift through the LT1010 is now appreciable and oscillations occur. Stabilizing this circuit requires degenerating the control amplifier's gain-bandwidth.

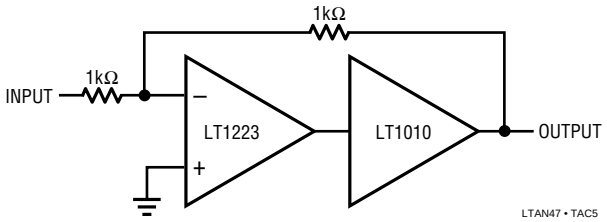


Figure C5. A Fast Op Amp and a Medium Speed Booster

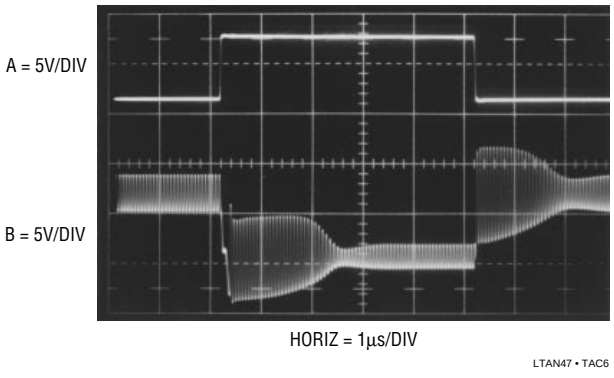


Figure C6. Loop Oscillation is "Free" When the Op Amp is Much Faster than the Booster

The fact that the slower op amp circuit doesn't oscillate is a key to understanding how to compensate booster loops. With the slow device, compensation is free. The faster amplifier makes the AC characteristics of the output stage become significant and requires roll-off components for stability. Practically, the LT1223's speed is simply too much for the LT1010. A somewhat slower amplifier is the way to go. Alternately, a faster booster may be employed. Figure C7 attempts this, but doesn't quite make it. Photo C8 is less corrupted, but 100MHz oscillation indicates the booster stage (borrowed from text Figure 101) is still too slow for the LT1223. Attempts to use another booster design in Figure C9 (similarly purloined from text Figure

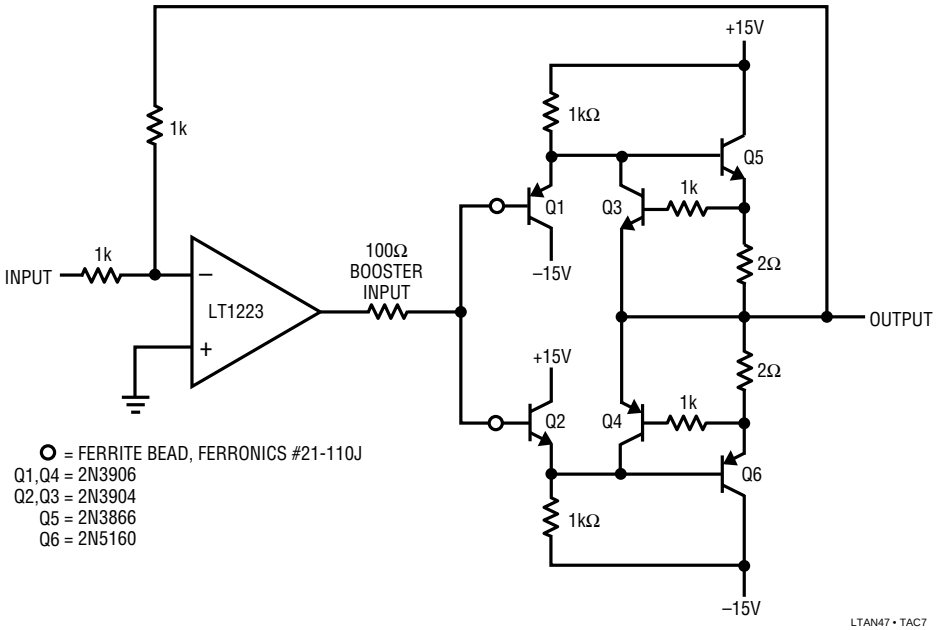


Figure C7. A Very Fast Amplifier with a Fast Booster

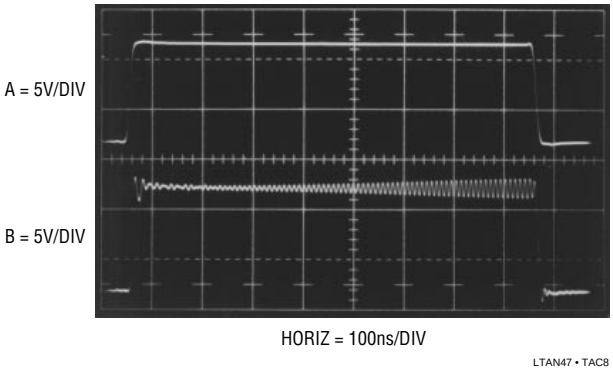


Figure C8. Figure C7's Booster is Not Quite Quick Enough to Prevent Loop Oscillation

104) fail for the same reason. Figure C10 shows 40MHz oscillation, indicative of this high power booster's slower speed.

Figure C11 has much more pleasant results. Here a 45MHz gain-bandwidth LT1220 has been substituted for the 100MHz LT1223 in Figure C7's circuit. The slower amplifier, combined with light local compensation, works well with the booster stage in its loop. Figure C12 shows a well controlled high speed output, nicely damped, with no sign of oscillations.

Power boosters are not the only things that can be placed within an amplifier's feedback loop. Text Figure 140's current source, reproduced here as Figure C13, is an interesting variation. There is no power booster in the loop, but rather a 40MHz differential amplifier with a gain of 10. To stabilize the circuit the slowest amplifier in the 1190 family, the 50MHz LT1190, is chosen. The local 100pF feedback slows it down a bit more and the loop is fast and stable (Figure C14). What happens if we remove the 100pF feedback path? Figure C15 shows that the loop is no longer stable under this condition because the LT1190 control amplifier cannot servo the phase shifted feedback at higher frequency. Put that 100pF capacitor back in!

It's worth mentioning that similar results to those obtained back in Figure C3 are obtainable by substituting a very slow control amplifier (e.g., an LT1006 which has less than 1MHz gain-bandwidth). The slower amplifier would give "free" compensation, eliminating the necessity for the 100pF unit. However, the circuit's frequency response would be severely degraded.

Text Figure 142's high power current source furnishes further instruction. This loop contains the differential amplifier *and* a booster, seemingly making things even more difficult. Figure C16, recognizable as text Figure 142's high power current source with the 100pF local compensation removed, oscillates above 10MHz. Replacing the compensation restores proper response. Figure

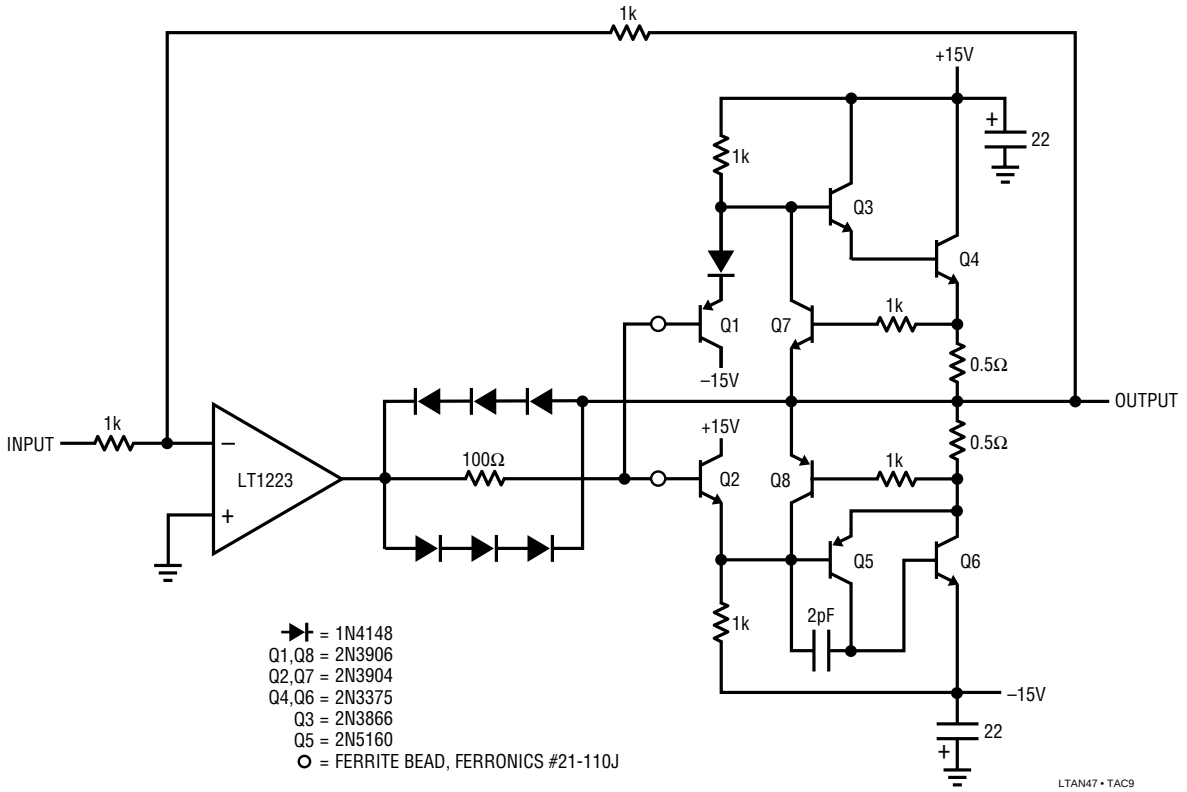


Figure C9. A Very Fast Amplifier with a Fast High Power Booster

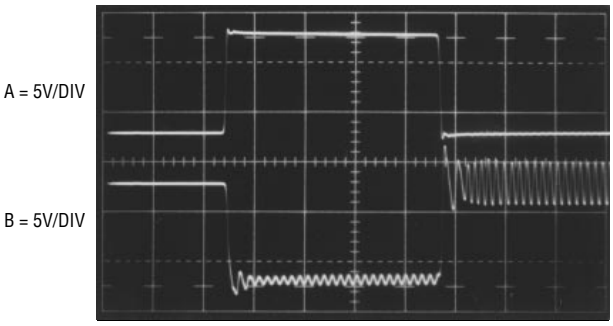


Figure C10. C9's High Power Booster is Fast But Causes Loop Oscillations

C17 shows the loop has no oscillations. What this tells us is that the control amplifier doesn't care just what generates the causal feedback between its input and output, so long as there isn't excessive delay. This circuit has a fairly busy feedback loop, but the control amplifier is oblivious to its bustling nature....unless you leave that 100pF feedback capacitor out!

When compensating loops like these, remember to investigate the effects of various loads and operating conditions. Sometimes a compensation scheme which appears fine gives bad results for some conditions. For this reason, check the completed circuit over as wide a variety of operating conditions as possible.

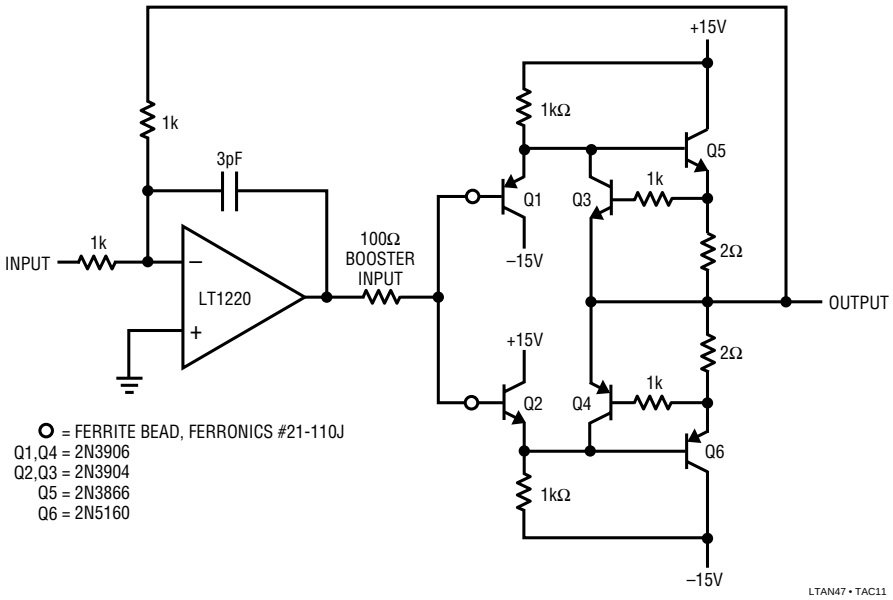


Figure C11. Figure 101 (Again) with 100Ω Resistor and Beads Reinstalled

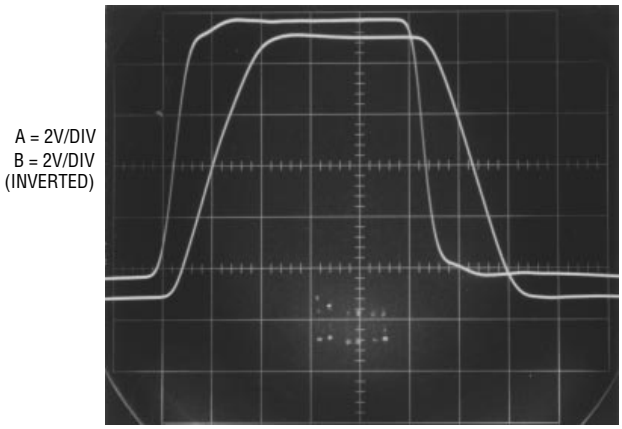


Figure C12. Lovely!

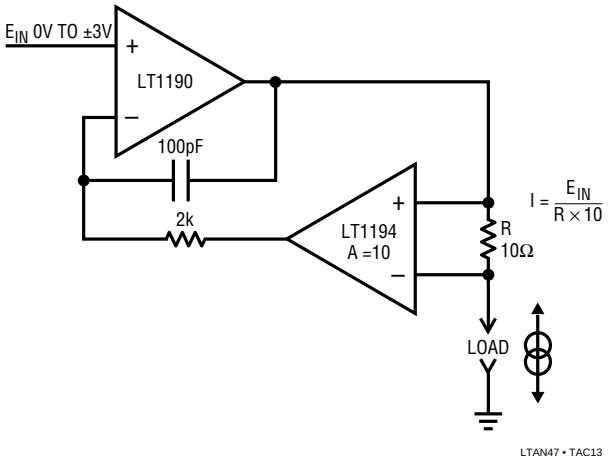


Figure C13. Figure 140's Current Source. What Do the RC Components Do?

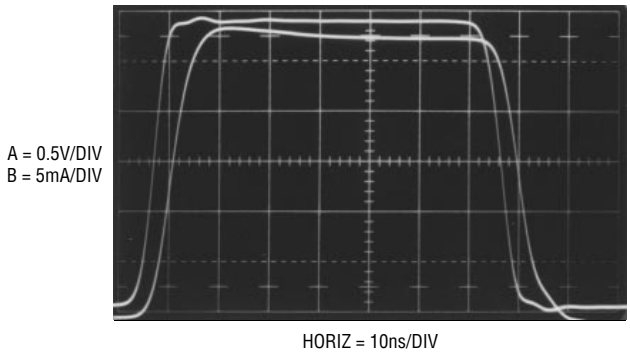


Figure C14. Response of the Current Source with the RC Components in Place

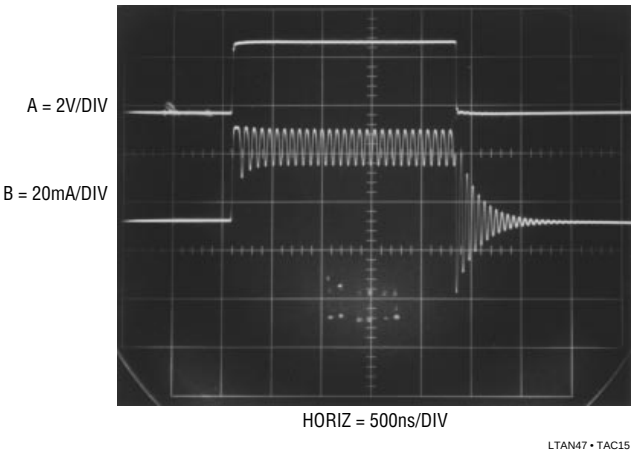


Figure C15. Removing the 100pF Capacitor Allows the Op Amp to See Phase Shifted Feedback, Causing Oscillation. Put that 100pF Back In!

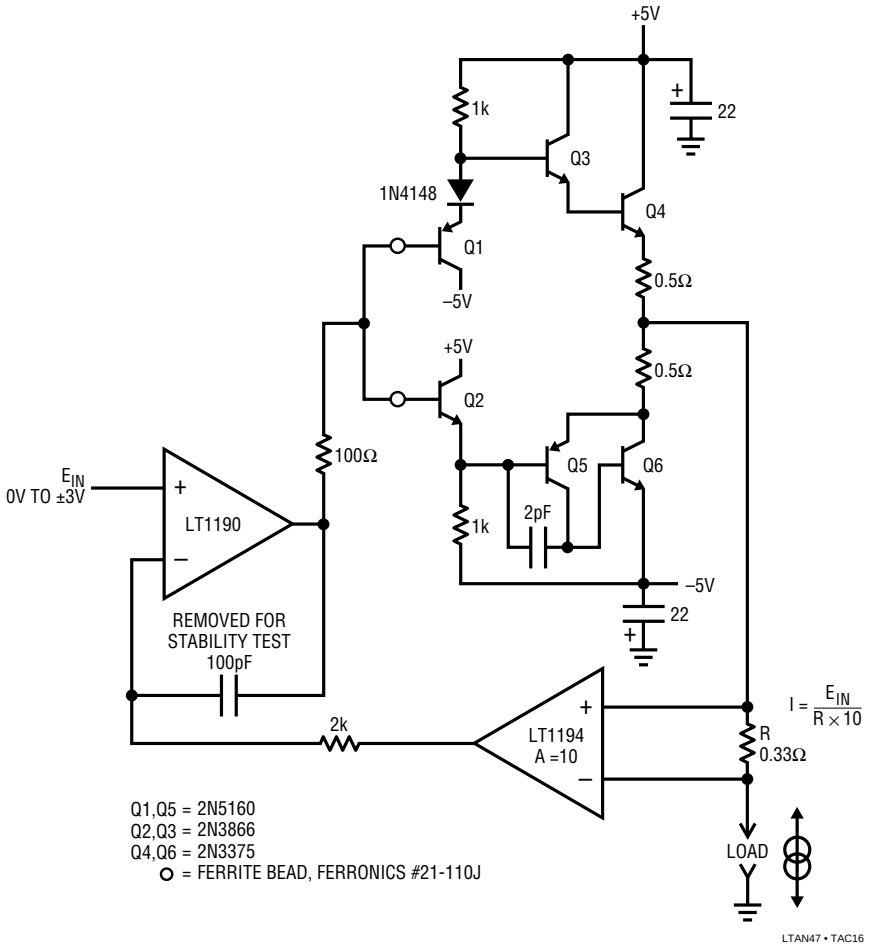


Figure C16. Text Figure 142's High Power Current Source. When the 100pF Capacitor is Removed, 10MHz Loop Oscillations Result

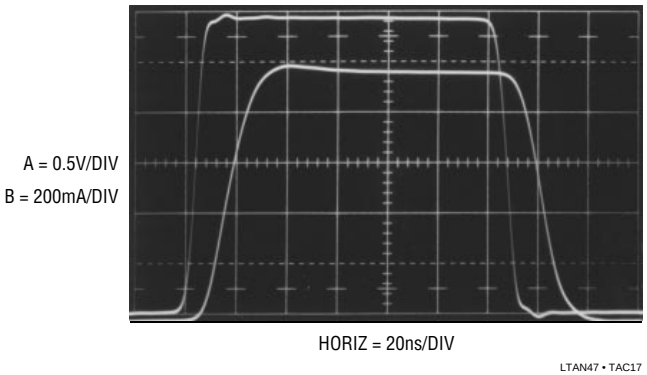


Figure C17. Much Better. Leave that 100pF Capacitor in There!

APPENDIX D

Measuring Probe-Oscilloscope Response

Verifying the rise time limit of wideband test equipment set-ups is a difficult task. In particular, the end-to-end rise time of oscilloscope-probe combinations is often required to assure measurement integrity. Conceptually, a pulse generator with rise times substantially faster than the oscilloscope-probe combination can provide this information. Figure D1's circuit does this, providing a 1ns pulse with rise and fall times inside 350ps. Pulse amplitude is 10V with a 50Ω source impedance. This circuit, built into a small box and powered by a 1.5V battery, provides a simple, convenient way to verify the rise time capability of almost any oscilloscope-probe combination.

The LT1073 switching regulator and associated components supply the necessary high voltage. The LT1073 forms a flyback voltage boost regulator. Further voltage step-up is obtained from a diode-capacitor voltage step-up network. L1 periodically receives charge and its flyback discharge delivers high voltage events to the step-up network. A portion of the step-up network's DC output is fed back to the LT1073 via the 10M, 24k divider, closing a control loop.

The regulator's 90V output is applied to Q1 via the 1M- 2pF combination. Q1, a 40V breakdown device, non-destructively avalanches when C1 charges high enough. The result is a quickly rising, very fast pulse across R4. C1 discharges, Q1's collector voltage falls and breakdown ceases. C1 then recharges until breakdown again occurs. This action causes free running oscillation at about 200kHz.[1,2] Figure D2 shows the output pulse. A 1GHz sampling oscilloscope (Tektronix 556 with 1S1 sampling plug-in) measures the pulse at 10V high with about a 1ns base. Rise time is 350ps, with fall time also indicating 350ps. There is a slight hint of ring after the falling edge, but it is well controlled. The figures may actually be faster, as the 1S1 is specified with a 350ps limit.[3]

Q1 may require selection to get avalanche behavior. Such behavior, while characteristic of the device specified, is not guaranteed by the manufacturer. A sample of 50 Motorola 2N2369s, spread over a 12 year date code span, yielded 82%. All good devices switched in less than 650ps. C1 is selected for a 10V amplitude output. Value spread is typically 2pF-4pF. Ground plane type construction with

Note 1: This method of generating fast pulses borrows heavily from the Tektronix type 111 Pretrigger Pulse Generator. See References 8 and 25.

Note 2: This circuit replaces the tunnel diode based arrangement shown in AN13, Appendix D. While AN13's circuit works well, it generates a smaller, more irregularly shaped pulse and the tunnel diodes have become quite expensive.

Note 3: Just before going to press the pulse was measured at Hewlett-Packard Laboratories with a HP-54120B 12GHz sampling oscilloscope. Rise and fall times were 216ps and 232ps, respectively. Photo available on request.

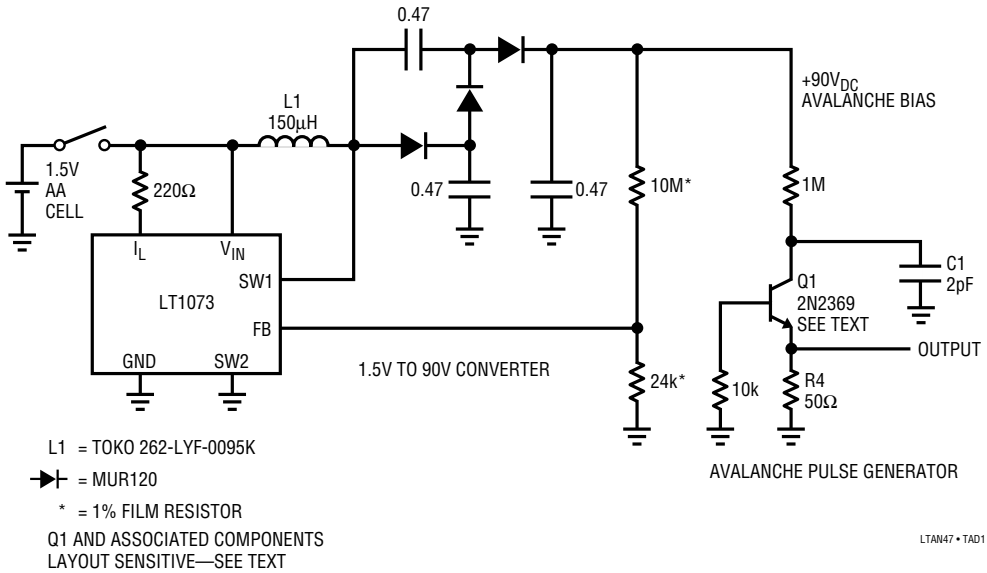


Figure D1. 350ps Rise/Fall Time Avalanche Pulse Generator

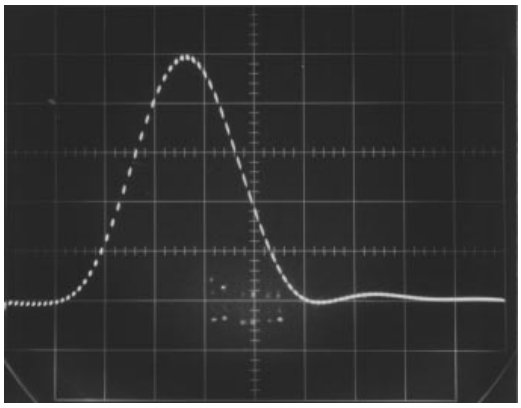


Figure D2. The Avalanche Pulse Generator's Output Monitored on a 1GHz Sampling Oscilloscope

high speed layout techniques are essential for good results from this circuit. Current drain from the 1.5V battery is about 5mA.

Figure D3 shows the physical construction of the actual generator. Power, supplied from a separate box, is fed into the generator's enclosure via a BNC connector. Q1 is mounted *directly* at the output BNC connector, with grounding and layout appropriate for wideband operation. Lead lengths, particularly Q1's and C1's, should be experimented with to get best output pulse purity. Figure D4 is the complete unit.

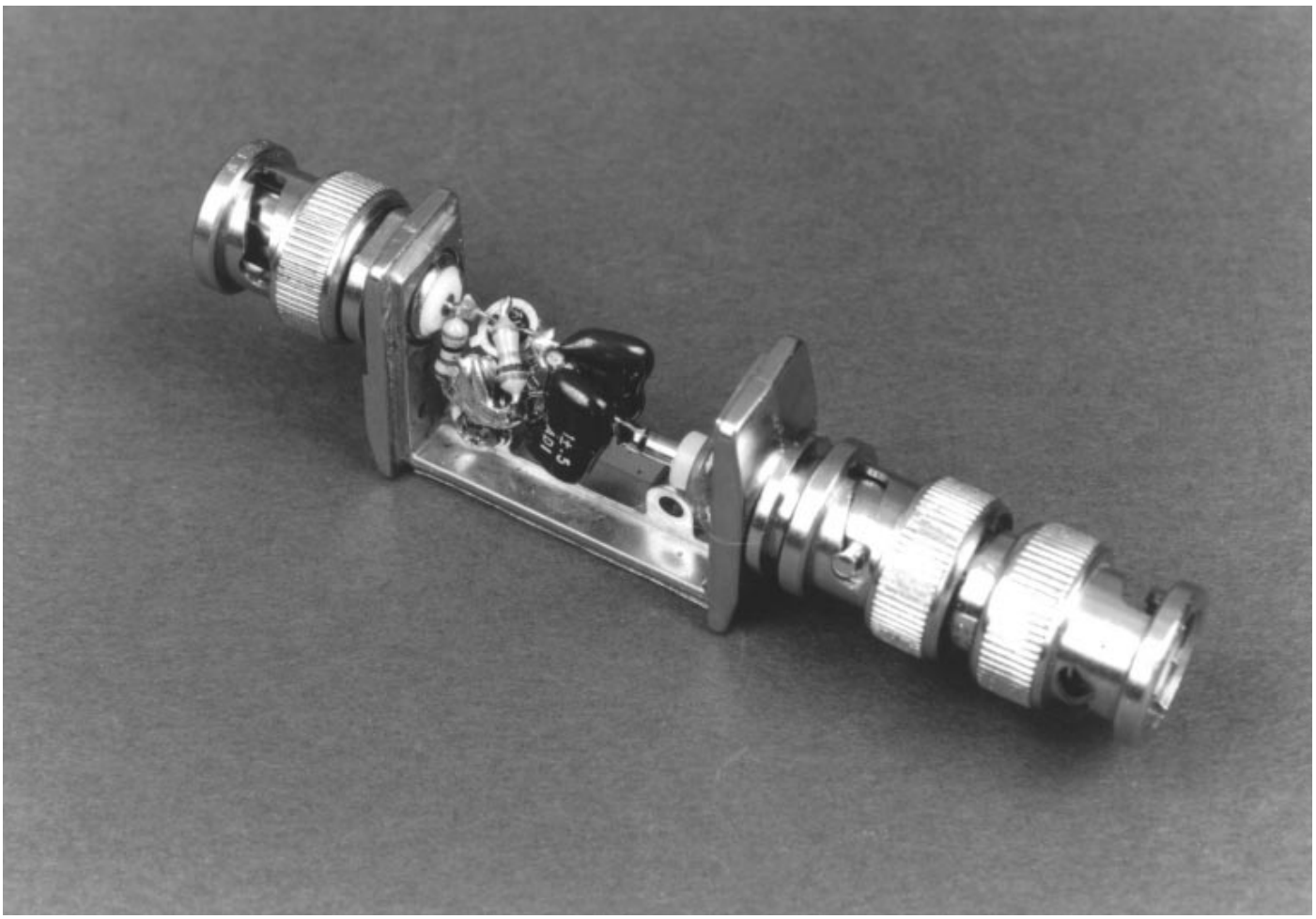


Figure D3. Details of the Avalanche Pulse Generator's Head. 90V_{DC} Enters at Lower Right BNC, Pulse Exits at Top Left BNC. Note Short Lead Lengths Associated with Output

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Figure D4. The Packaged Avalanche Pulser. 1.5V-90V Converter is in the Black Box. Avalanche Head is at Left

APPENDIX E

An Ultra-Fast High Impedance Probe

Under most circumstances the 1pF-2pF input capacitance and 10MΩ resistance of FET probes is more than adequate for difficult probing situations. Occasionally, however, very high input resistance with high speed is needed. At some sacrifice in speed and input capacitance compared to commercial probes, it is possible to construct such a probe. Figure E1 shows schematic details. A1, a 350MHz hybrid FET buffer, forms the electrical core of the probe. This device is a low input capacitance, wideband FET source follower driving a fast bipolar output stage. The input of the probe goes to this device via a 51Ω resistor, reducing the possibility of oscillations in the follower input stage when the probe sees low AC impedance. A1's output drives a guard shield around the probe's input line, reducing effective input capacitance to about 4pF. A ground referred shield encircles the guard shield, reducing pickup and making high quality ground connections to the circuit under test easy. A1 drives the output BNC cable to feed the oscilloscope. Normally, it is undesirable to back terminate the cable at A1 because the oscilloscope will see only half of A1's output. While a back termination provides the best signal dynamics, the resulting attenuation is a heavy penalty. The RC damper shown can be trimmed for best edge response while maintaining an unattenuated output.

What can't be seen in the schematic is the probe's physical construction. Very careful construction is required to maintain low input capacitance, low bias current and wide bandwidth. The probe head is particularly critical. Every effort should be made to minimize the length of wire between A1's input and the probe tip. In our lab, we have found that discarded pieces of broken 10X probes, particularly attenuator boxes and probe heads, provide an excellent packaging basis for this probe.[1] Figure E2 shows the probe head. Note the compact packaging. Additionally, A1's package is arranged so that it's (not insubstantial) dissipated heat is transferred to the probe case body when the snap-on cover (shown in photo) is in place. This reduces A1's substrate temperature, keeping bias current down. A1's input is directly connected to the probe head to minimize parasitic capacitance. The power supply for A1, located in a separate enclosure, is fed in through separate wires. A1's output is delivered to the oscilloscope via conventional BNC hardware.

Figure E3 shows the probe output (Trace B) responding to an input (Trace A) as monitored on a 350MHz oscilloscope (Tektronix 485). Measured specifications for our version of this probe include a rise time of 6ns, 6ns delay and 58MHz bandwidth. The delay time contribution is about evenly split between the amplifier and cable. Input capacitance is about 4pF without the probe hook tip and 7pF with the hook tip. Input bias current measured 400pA and gain error about 5%. (A1 is an open loop device.)

Note 1: This is not to encourage or even accept the breakage of probes. The author regards the breakage of oscilloscope probes as the lowest possible human activity. The sole exception to this condemnation is poor quality probes, which should be destroyed as soon as their deficiencies are discovered.

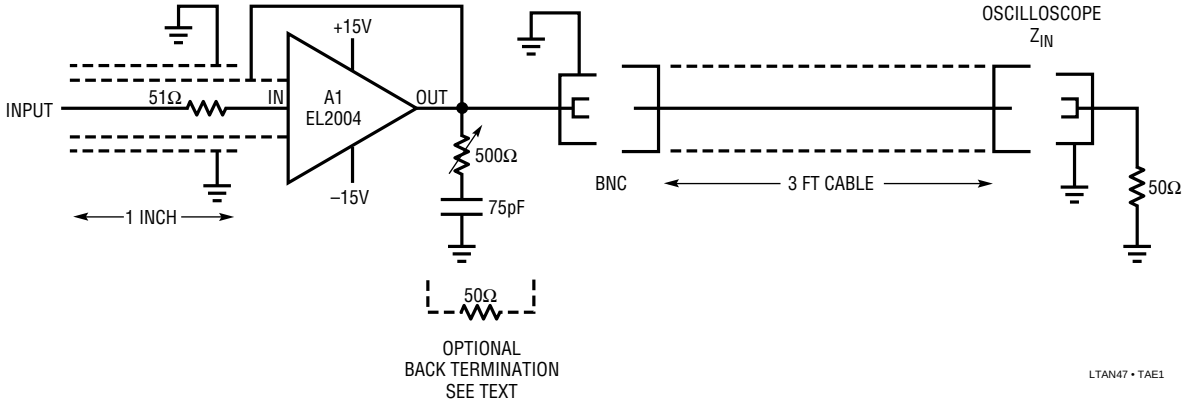

Figure E1. Ultra Fast Buffer Probe Schematic

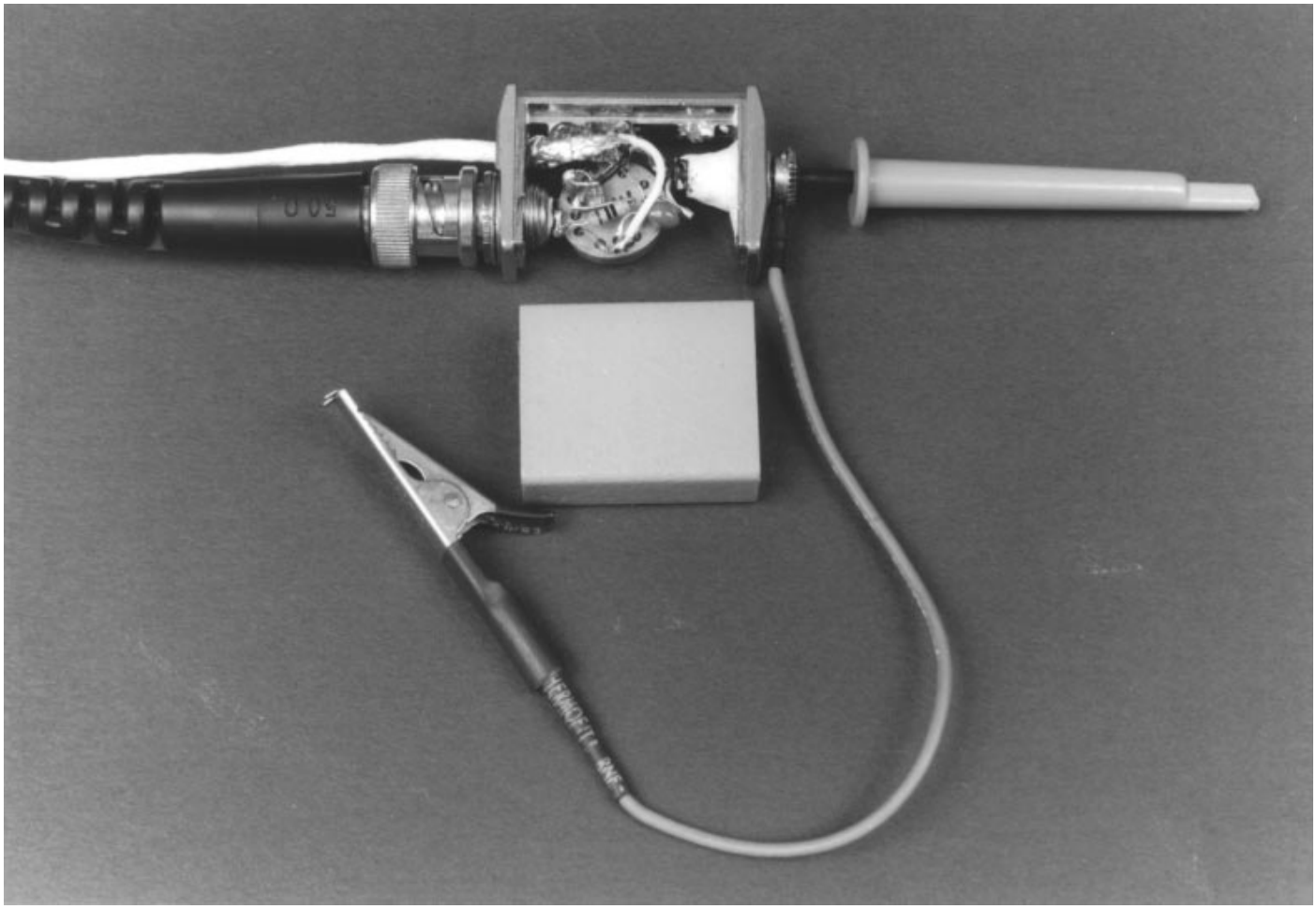

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Figure E2. Physical Layout of Ultra Fast Buffer Probe

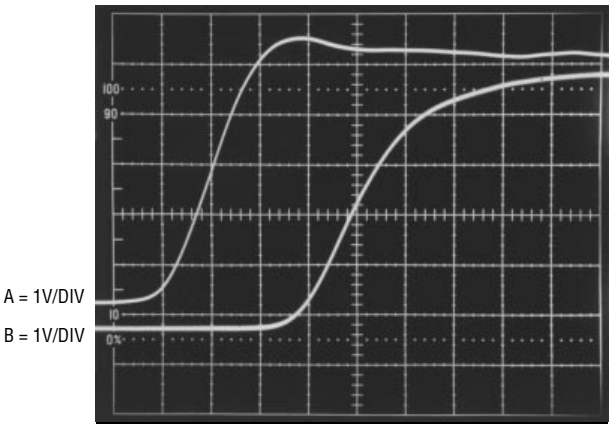

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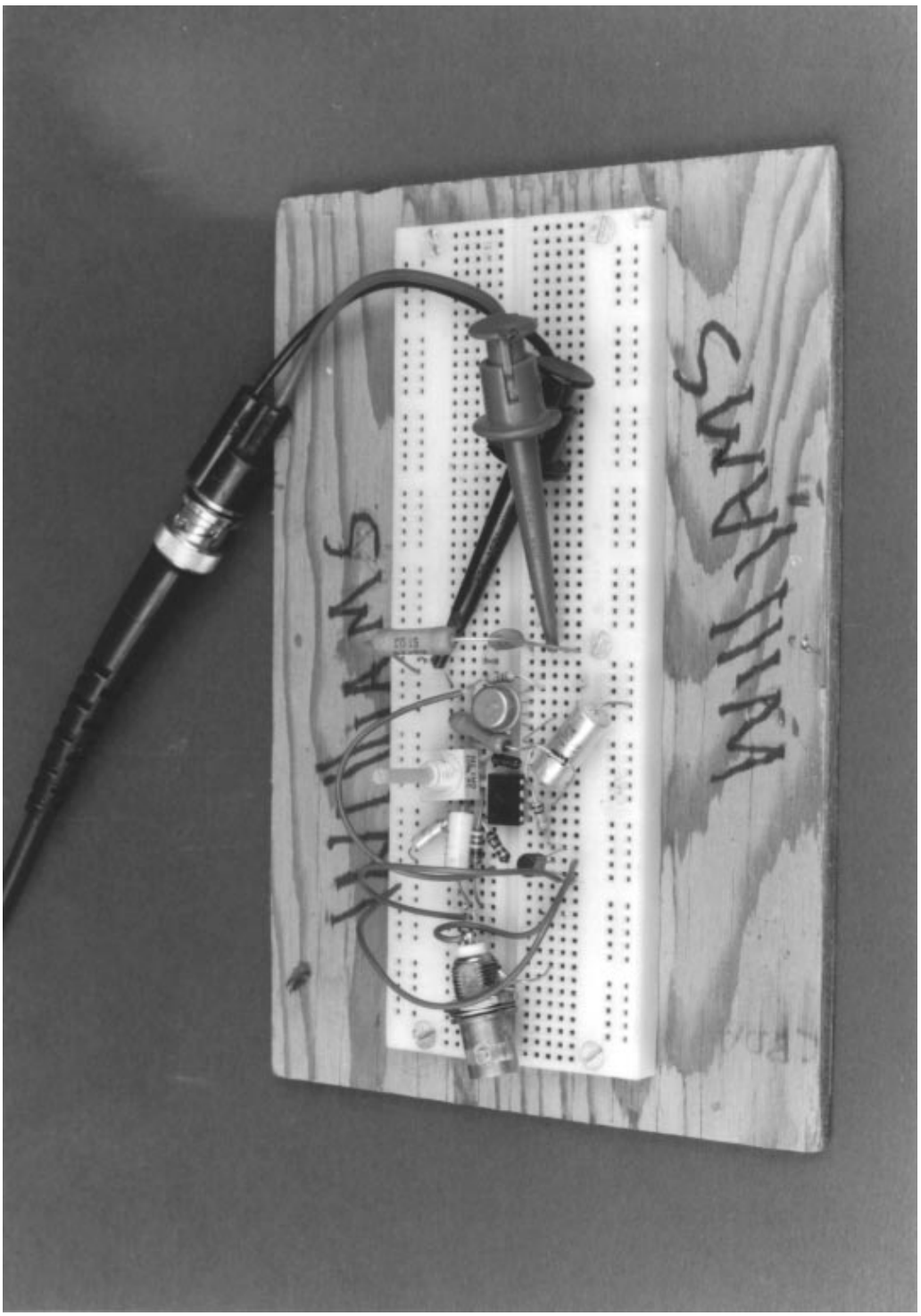
Figure E3. Probe Response (Trace B) to Input Pulse (Trace A)

APPENDIX F

Additional Comments on Breadboarding

This section contains, in visual form, commentary on some of the breadboards of the circuits described in the text. The breadboards appear in roughly corresponding order to their text presentation and comments are brief but hopefully helpful. The bit pushers have commented software; why not commented hardware?



LTAN47 • TAF1

Figure F1. No

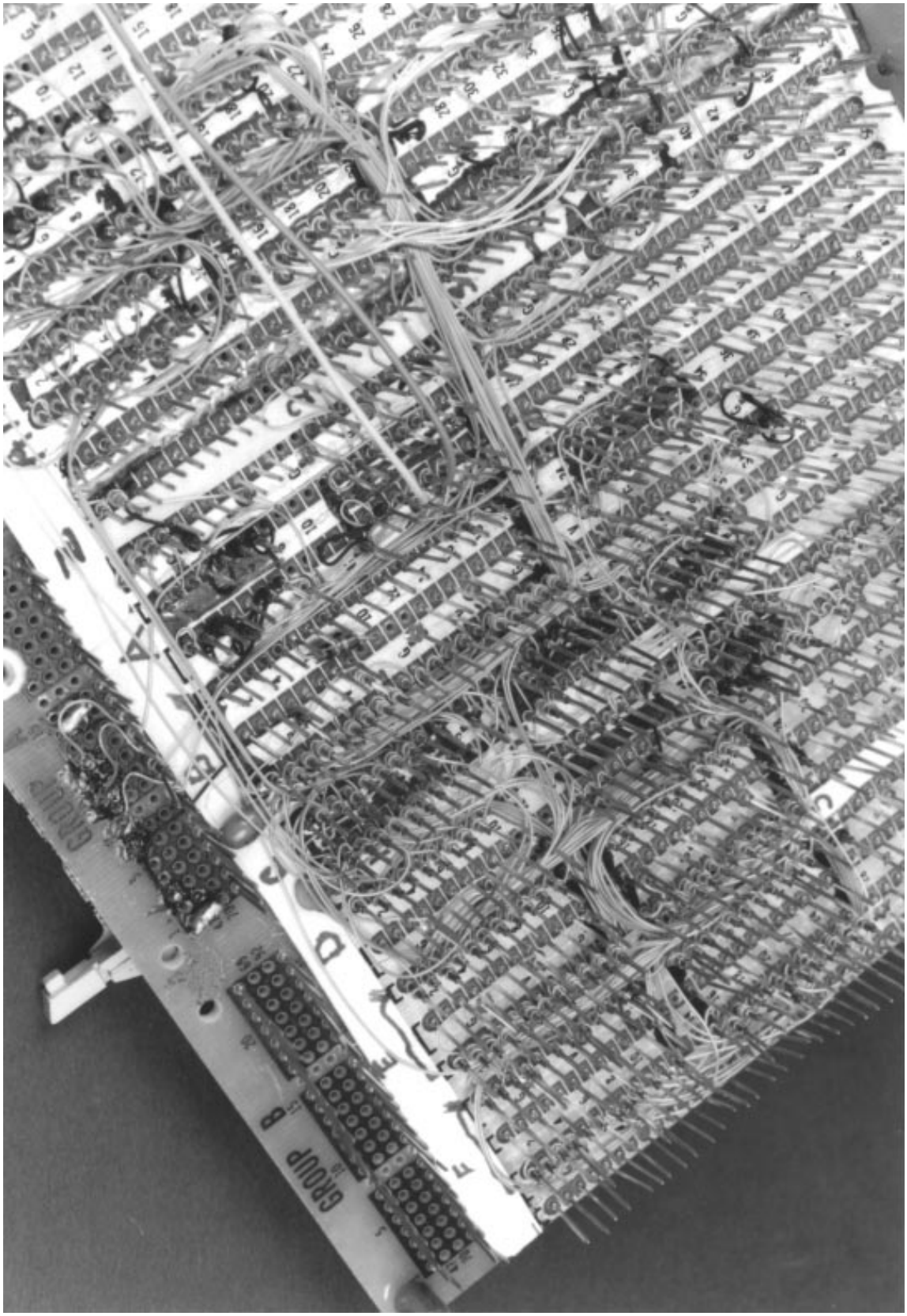
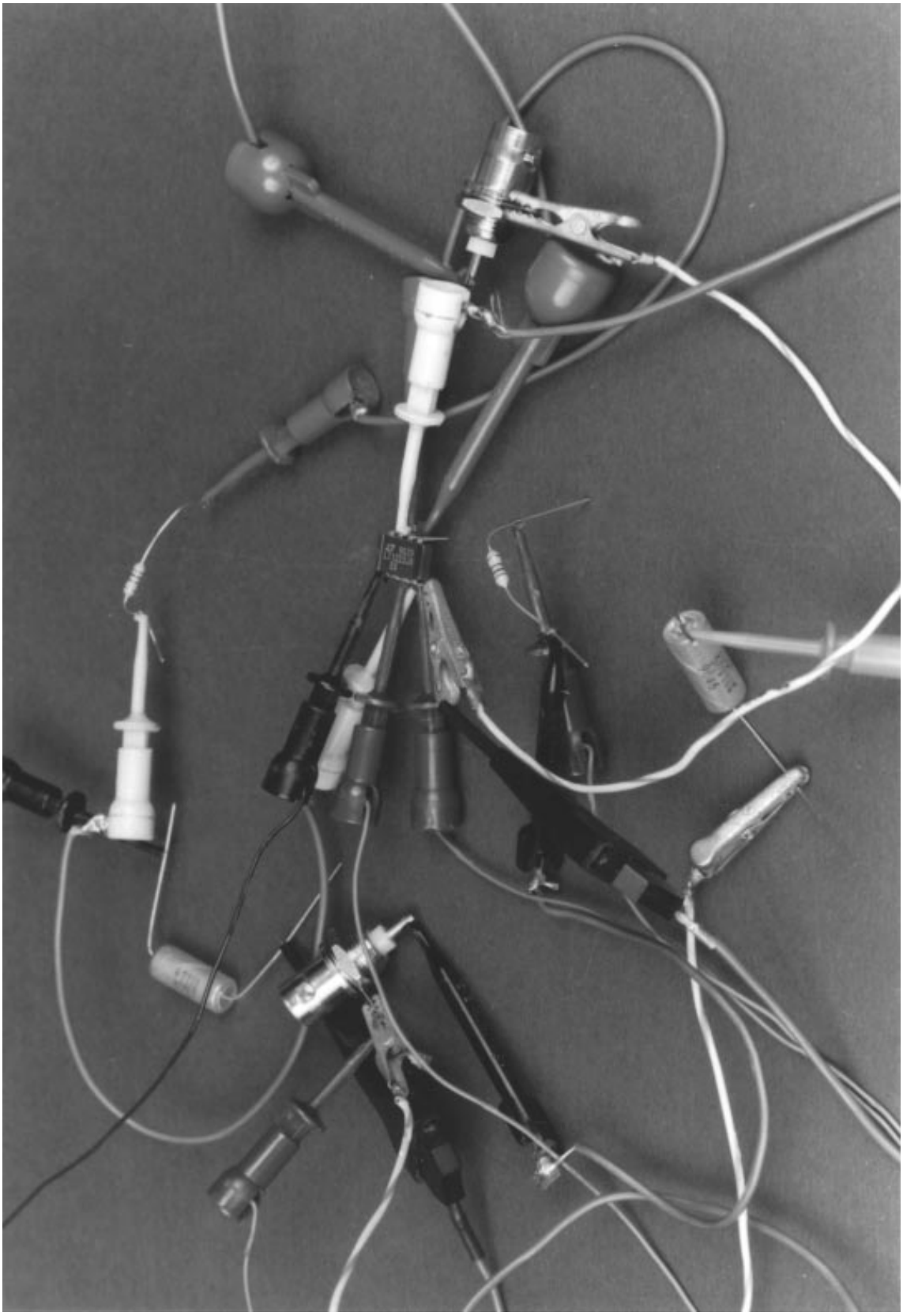


Figure F2. No



LT AN47 • TAF3

Figure F3. No

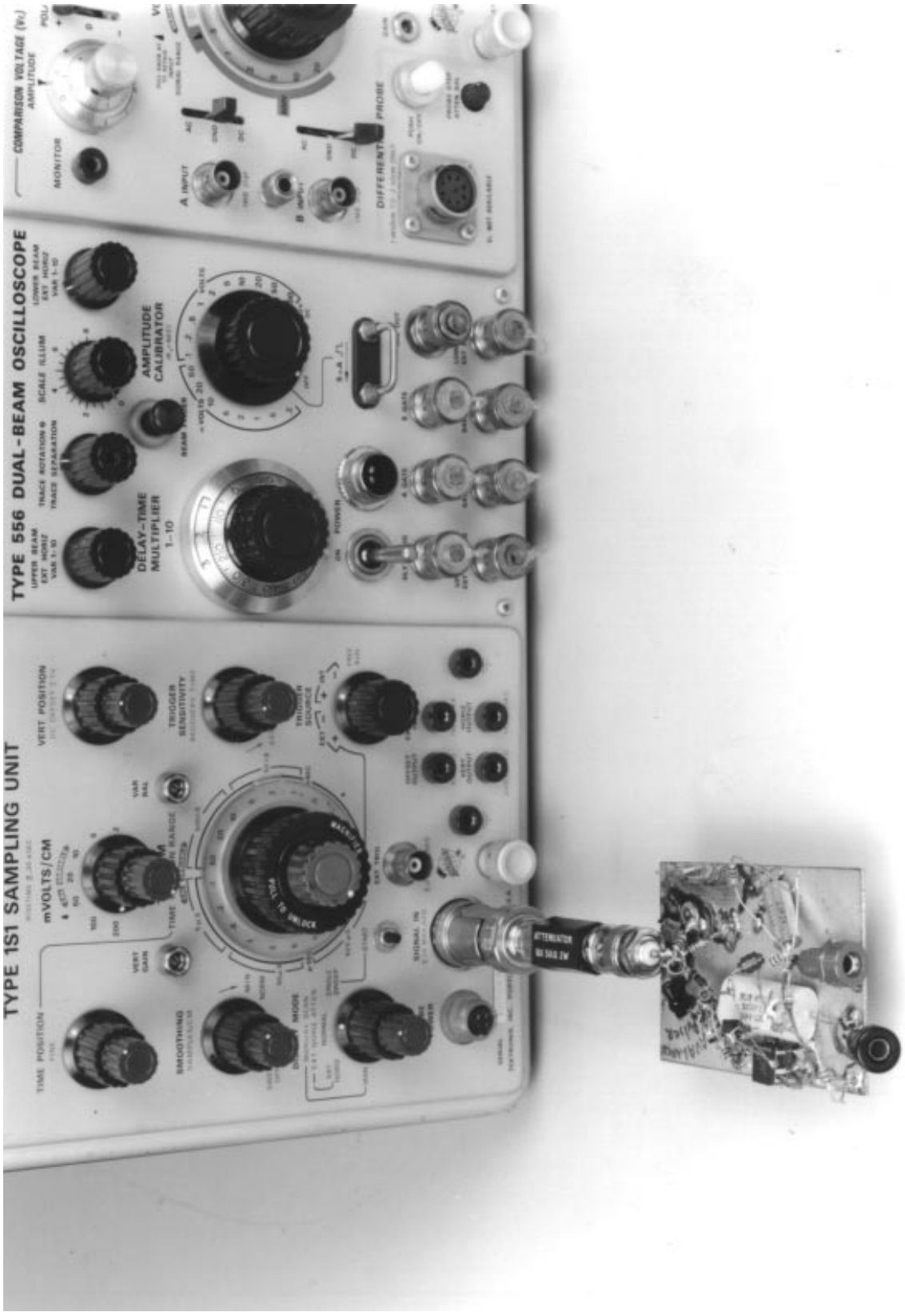
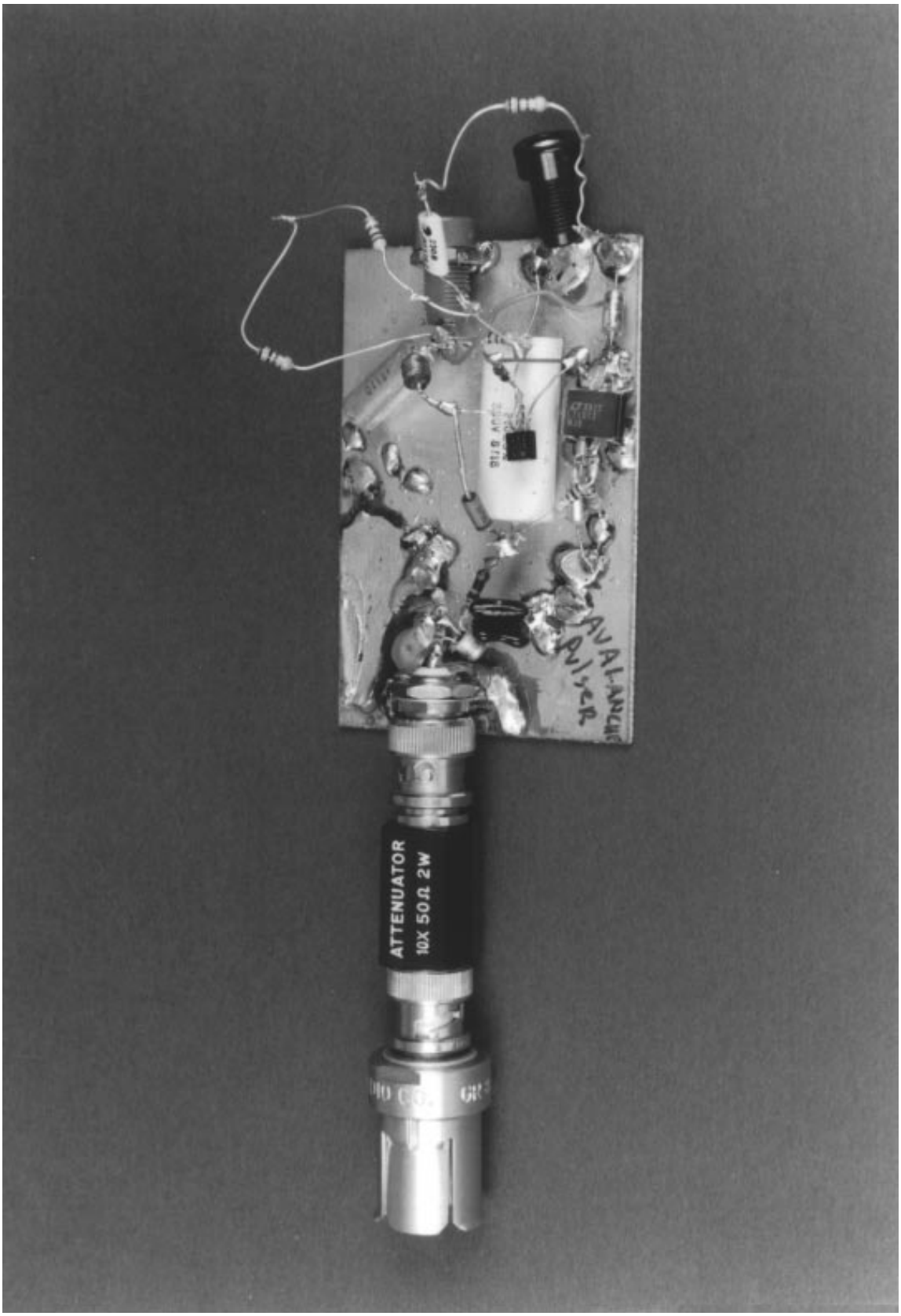
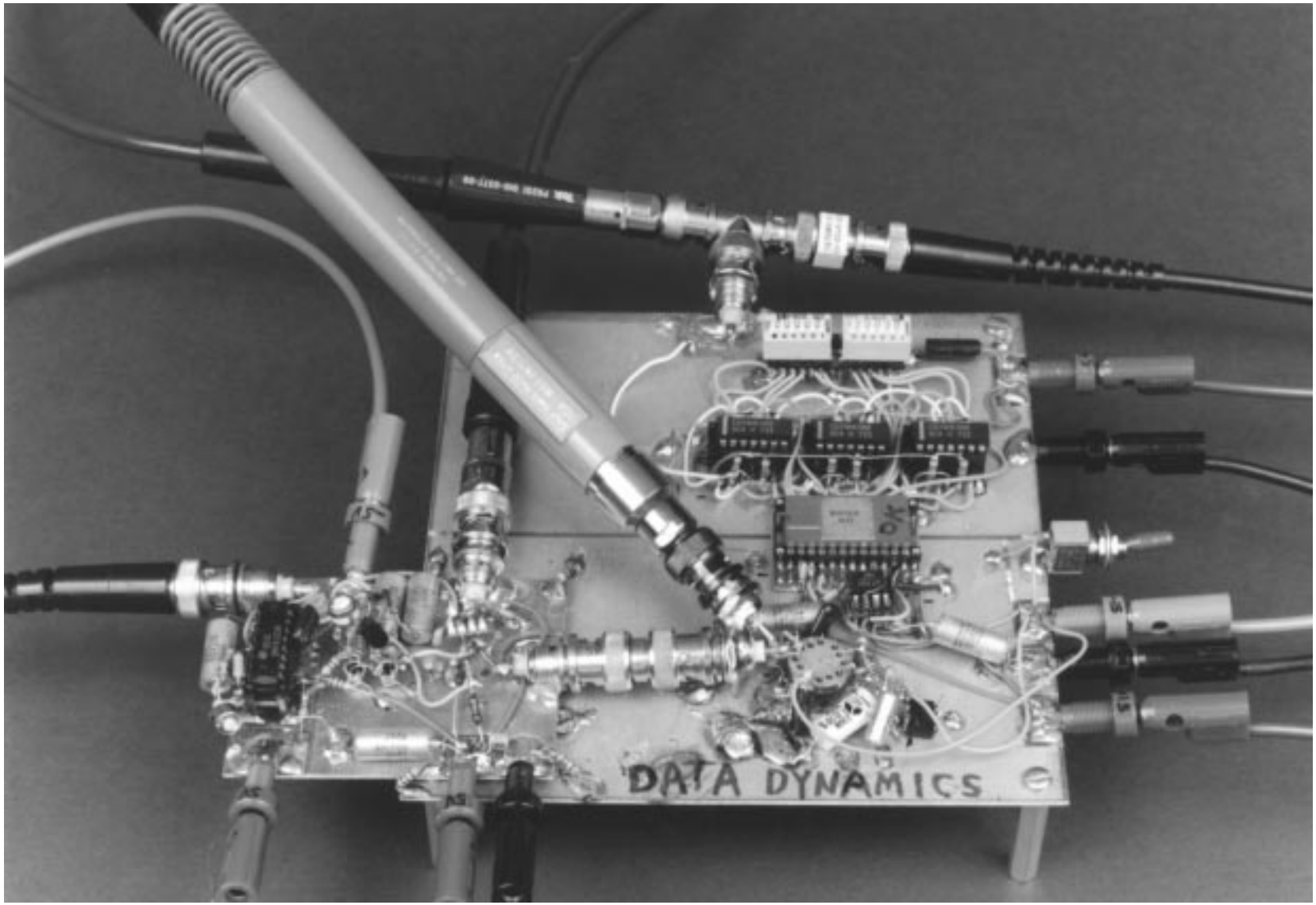


Figure F4. Prototype Avalanche Pulser Under Test. Direct Connection to Oscilloscope Eliminates Cable or Probe Effects



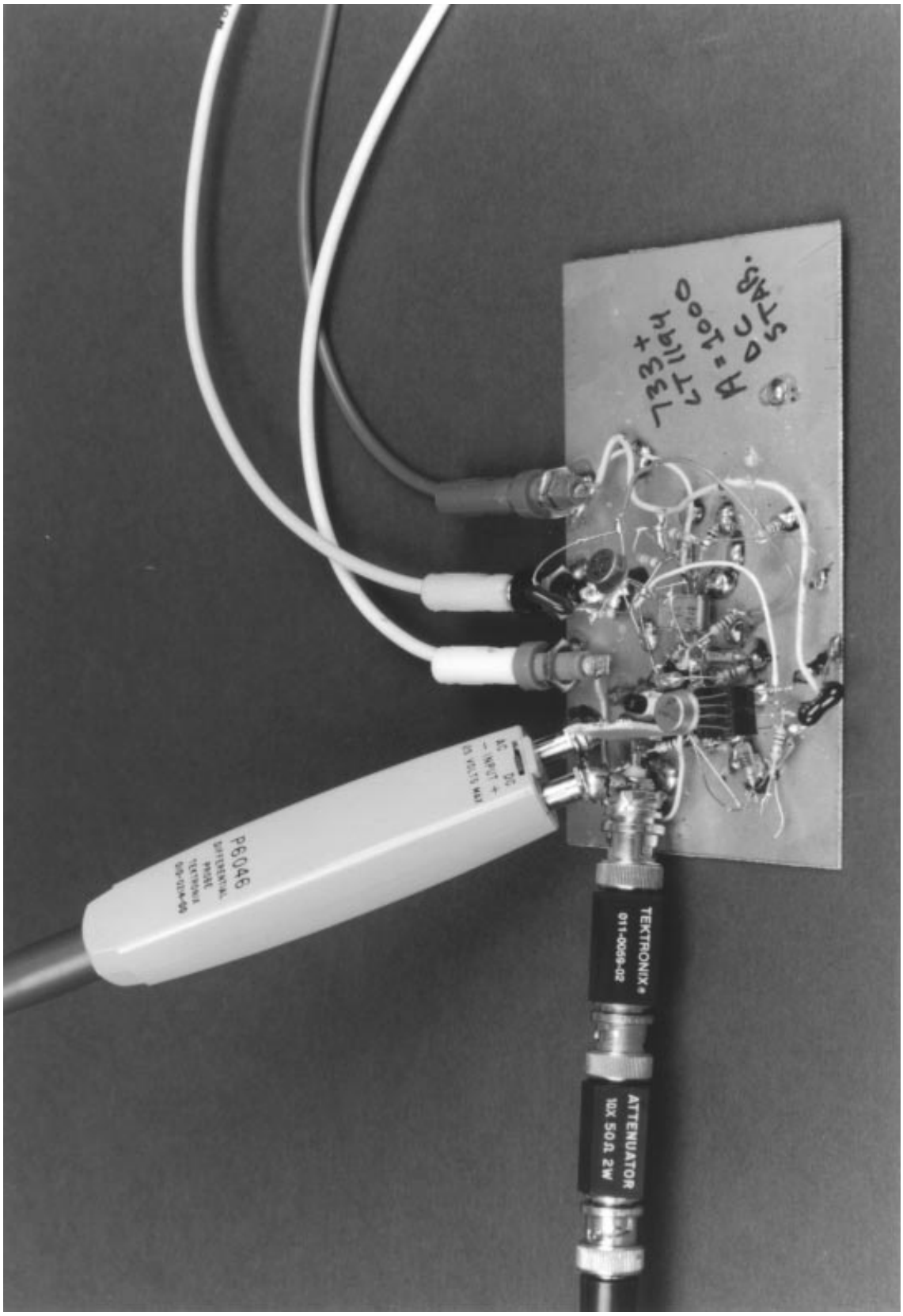
LTAN47 • TAF5

Figure F5. Close-Up of Prototype Avalanche Pulse Generator. DC Bias Generator (Right Side of Board) is Carelessly Wired, but Pulse Forming Circuitry (Left Side of Board, by BNC Connector) is Carefully and Tightly Wired



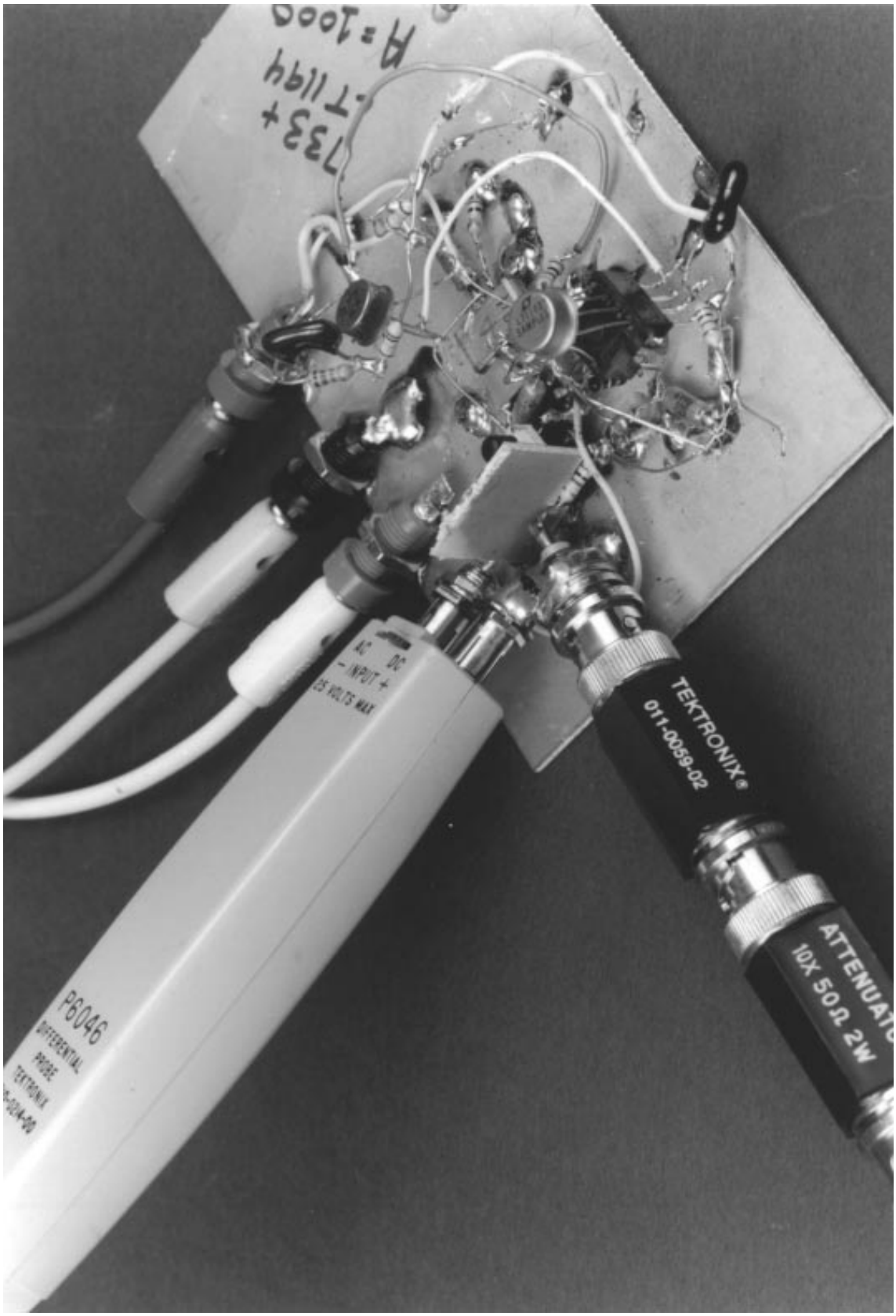
LTAN47 • TAF6

Figure F6. The Settling Time Test Fixture Described in Appendix B. DAC and Amplifier are in Center Right of Photo. Note Break in Clad Separating Analog and Digital Grounds and Attention to Layout in Switching Bridge (Lower Left). Switching Bridge is Returned Separately to Ground — Its Board is Mechanically Stood-Off From Main Board by 10MΩ Resistors. Output Section, Driving the Large P6032 Follower Probe, is at Lower Right



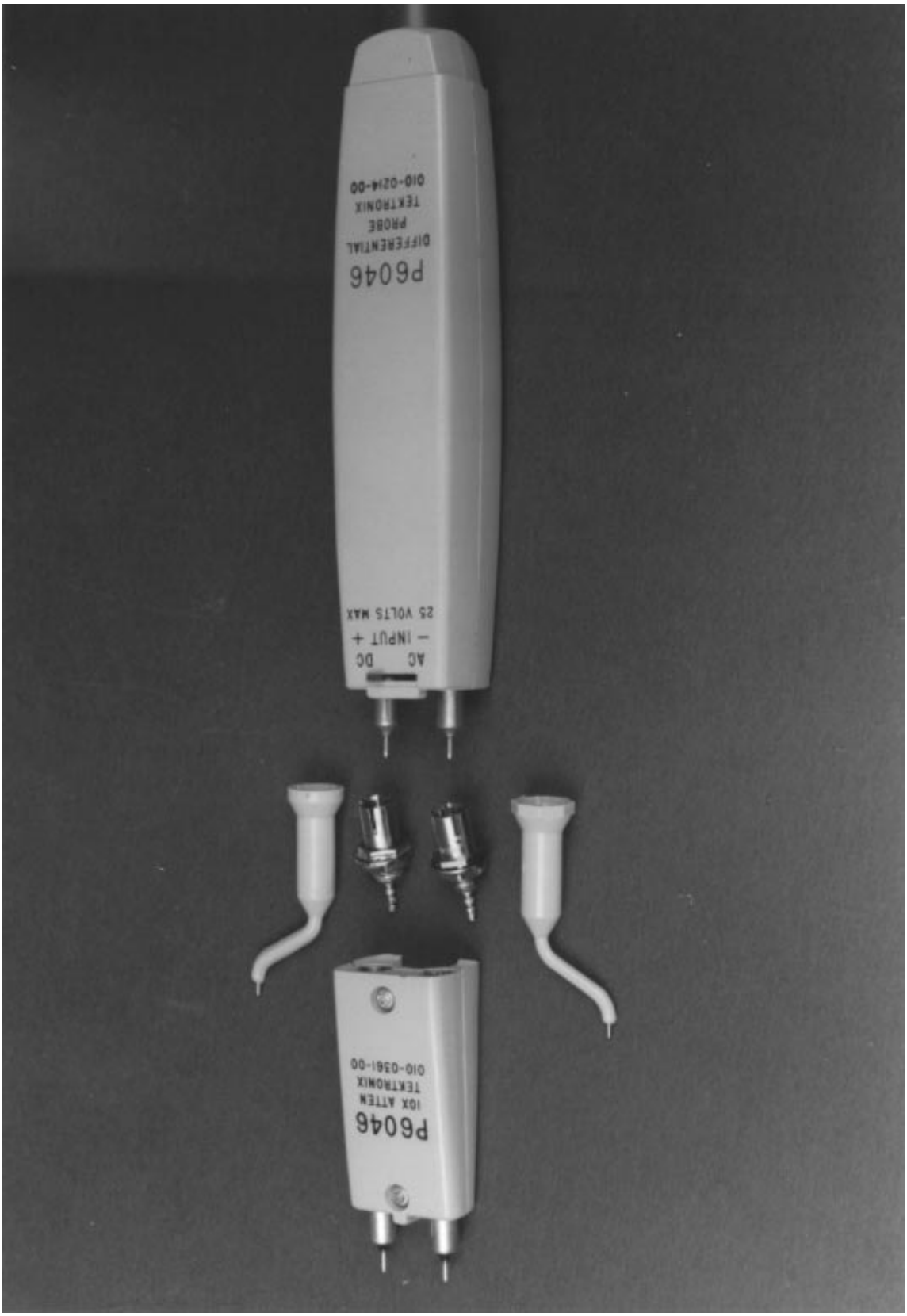
LTAN47 • TAF7

Figure F7. The X1000 38MHz Differential Amplifier. DC and Low Frequency Electronics use Sockets (Foreground) and Air Wire Techniques (Center Right) for Easy and Fast Breadboarding. Wideband Circuitry Hugs the Ground Plane, and is Clustered Near the Input BNC



LTAN47 • TAF8

Figure F8. Input Detail of X1000 Differential Amplifier. Clad Shield (Center Right) Prevents BNC Radiation from Corrupting Low Level Circuitry. Differential Probe Verifies Fidelity of 2.5mV Pulse Out of the X100 Attenuator Stacked Sections. Note DIP Packages Hugging Ground Plane, While Cans Operating at Low Frequency are Carelessly Wired

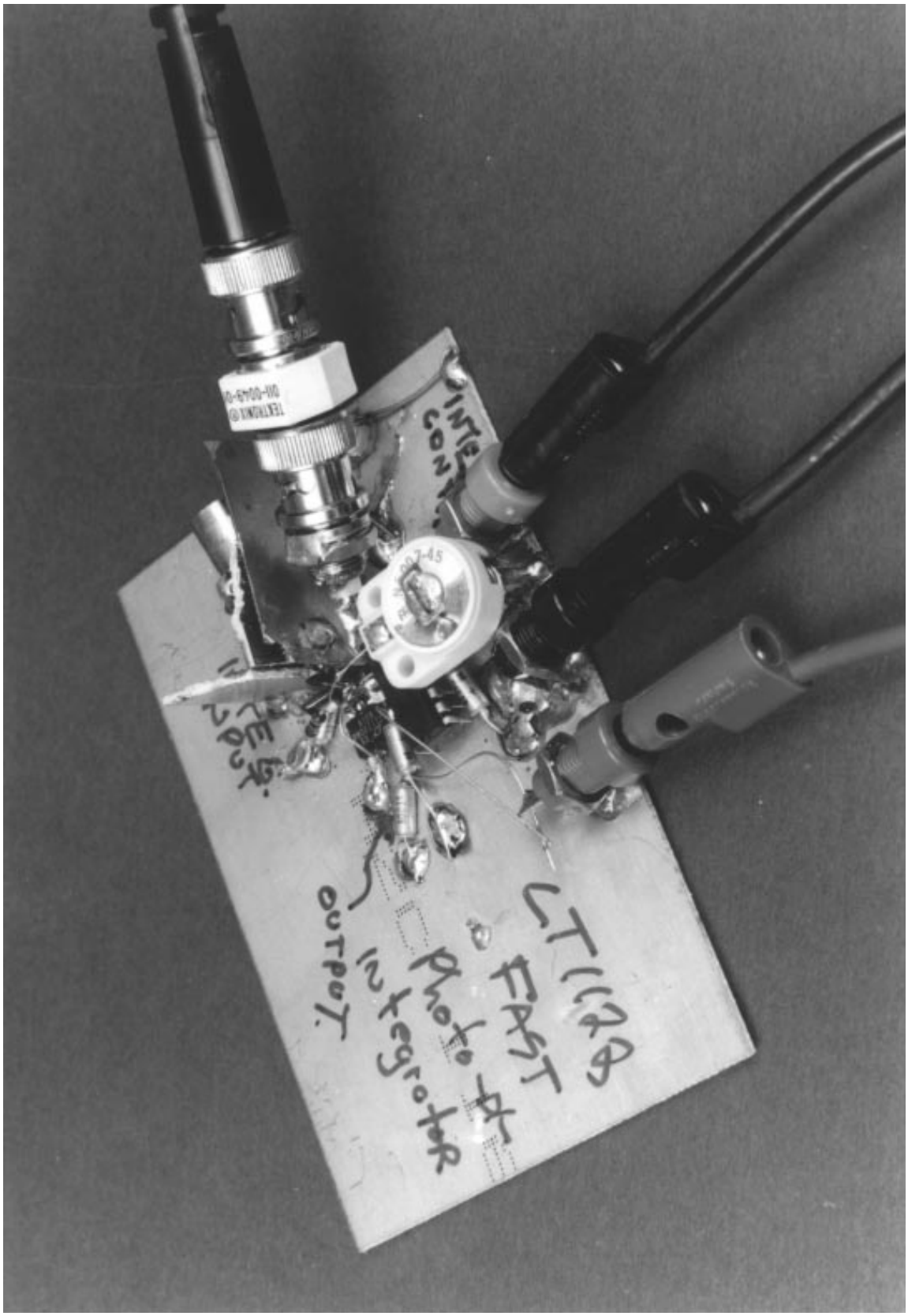


LTAN47 • TAF9

Figure F9. The Differential Probe and Its 10X Attenuator. Offset Probe Tips are Convenient for Making Differential Connections, but Sockets Maintain a True Coaxial Environment and are Preferred

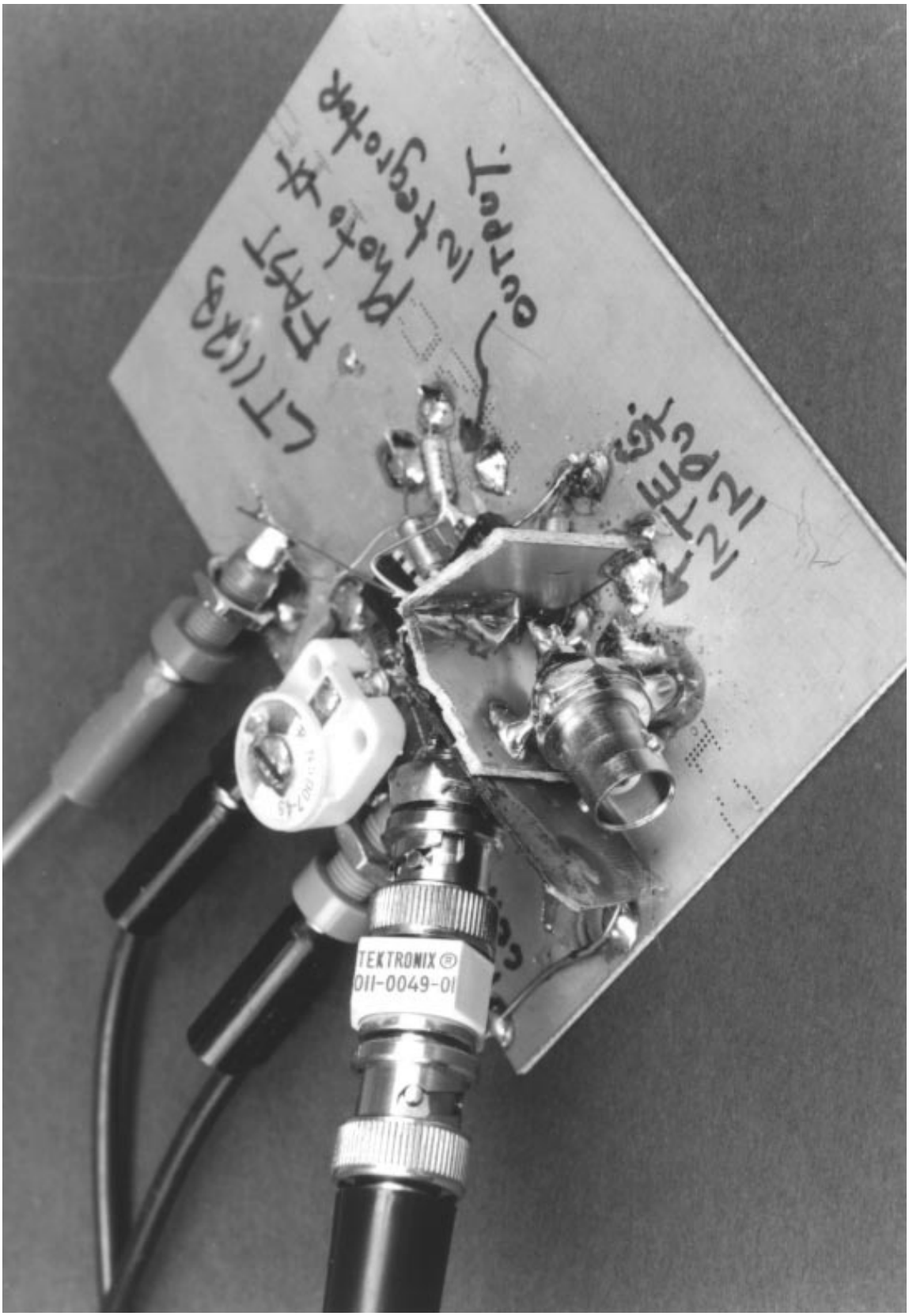
LTAN47 • TAF10

Figure F10. The Photodiode Amplifier Layout Emphasizes Low Capacitance at Amplifier (Located Below Trimmer Capacitor, Photo Center Upper Left). Vertical Guard Shield Breaks Up BNC Radiation; was Used When Photo Input was Simulated with a Pulse Generator



LTAN47 • TAF11

Figure F11. Fast Photo Integrator Under Test with Pulse Generator Simulating a Photo Input. BNC Radiation is Controlled with Extensive Shielding at Integrator Input (Just Visible Upper Center). Control Input (Cable Connected BNC) is Less Critical; Does Not Require Shielding



LTAN47 • TAF12

Figure F12. Photo Integrator Details. Integrator Input BNC is Fully Shielded From Integrator Amp — 1pF Coupling From BNC Output to Summing Point will Cause Excessive Peaking. Amplifier and Switch ICs are Just Visible

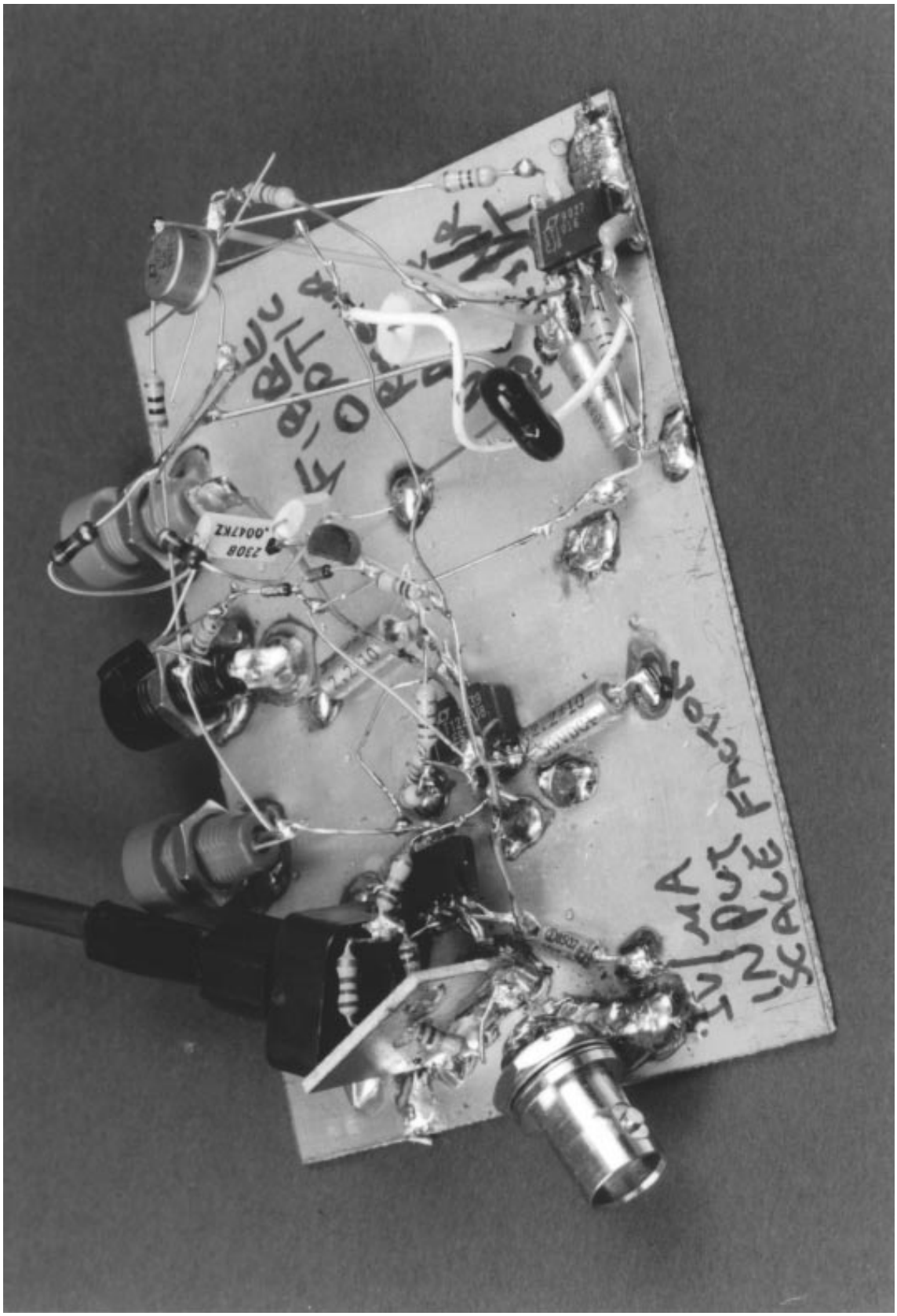
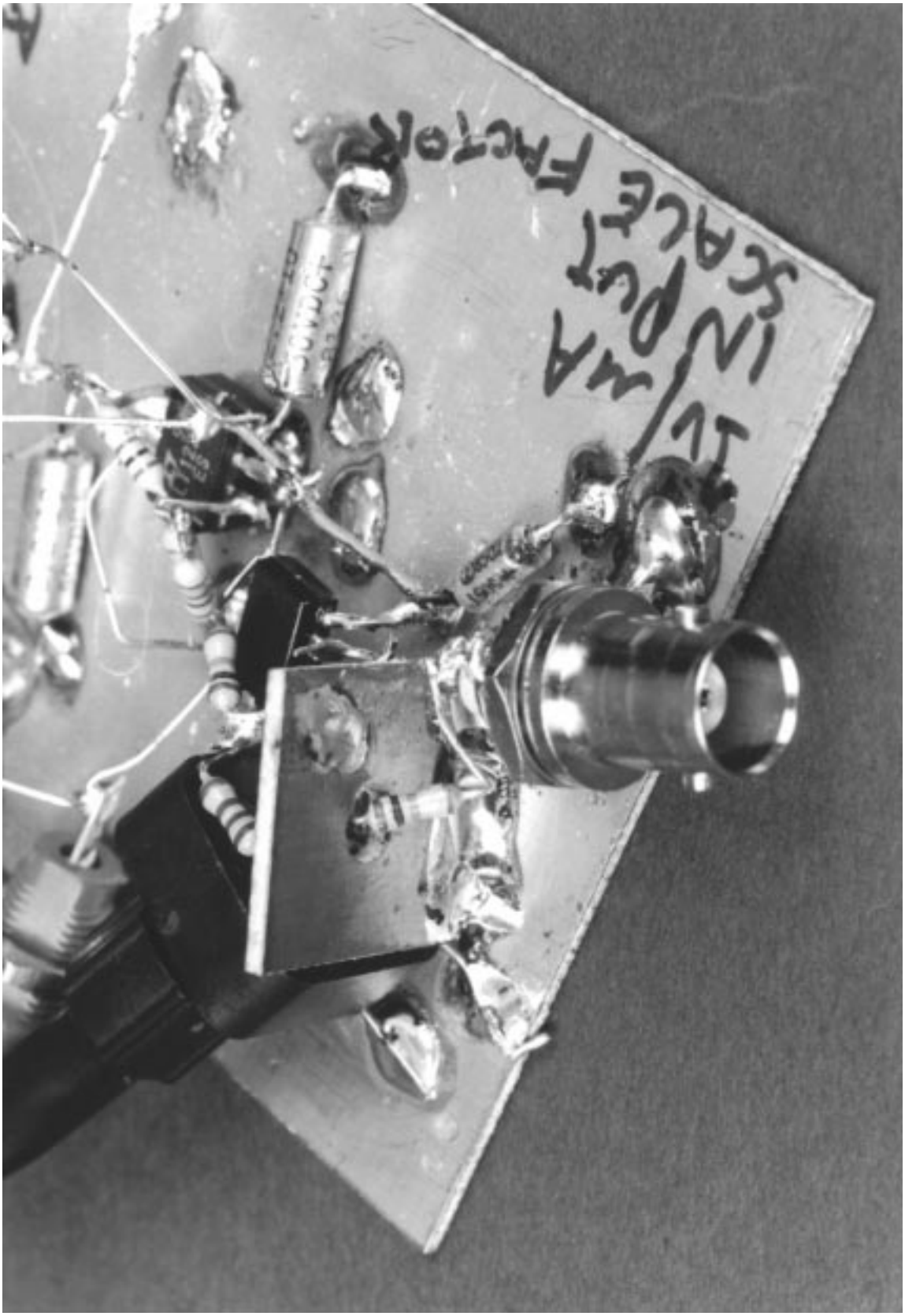
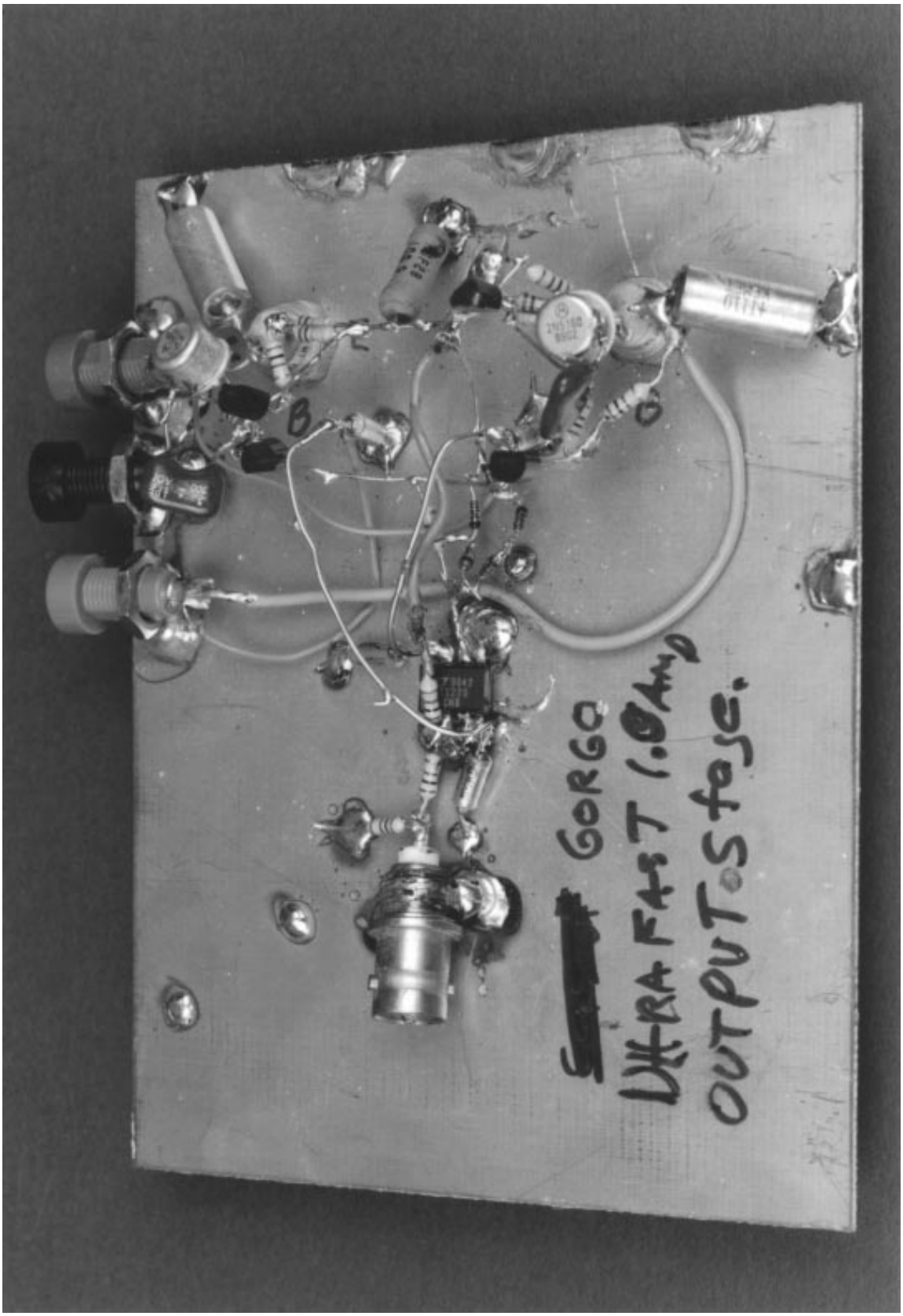


Figure F13. The Adaptive Trigger Fiber Optic Receiver. BNC Photo-Simulation Input and Fiber Optic Line Both Connected. Low Frequency Wiring is Haphazardly Constructed While High Frequency Sections are Tight and Hug the Ground Plane. Note Vertical Shield at Photo-Simulation Input BNC



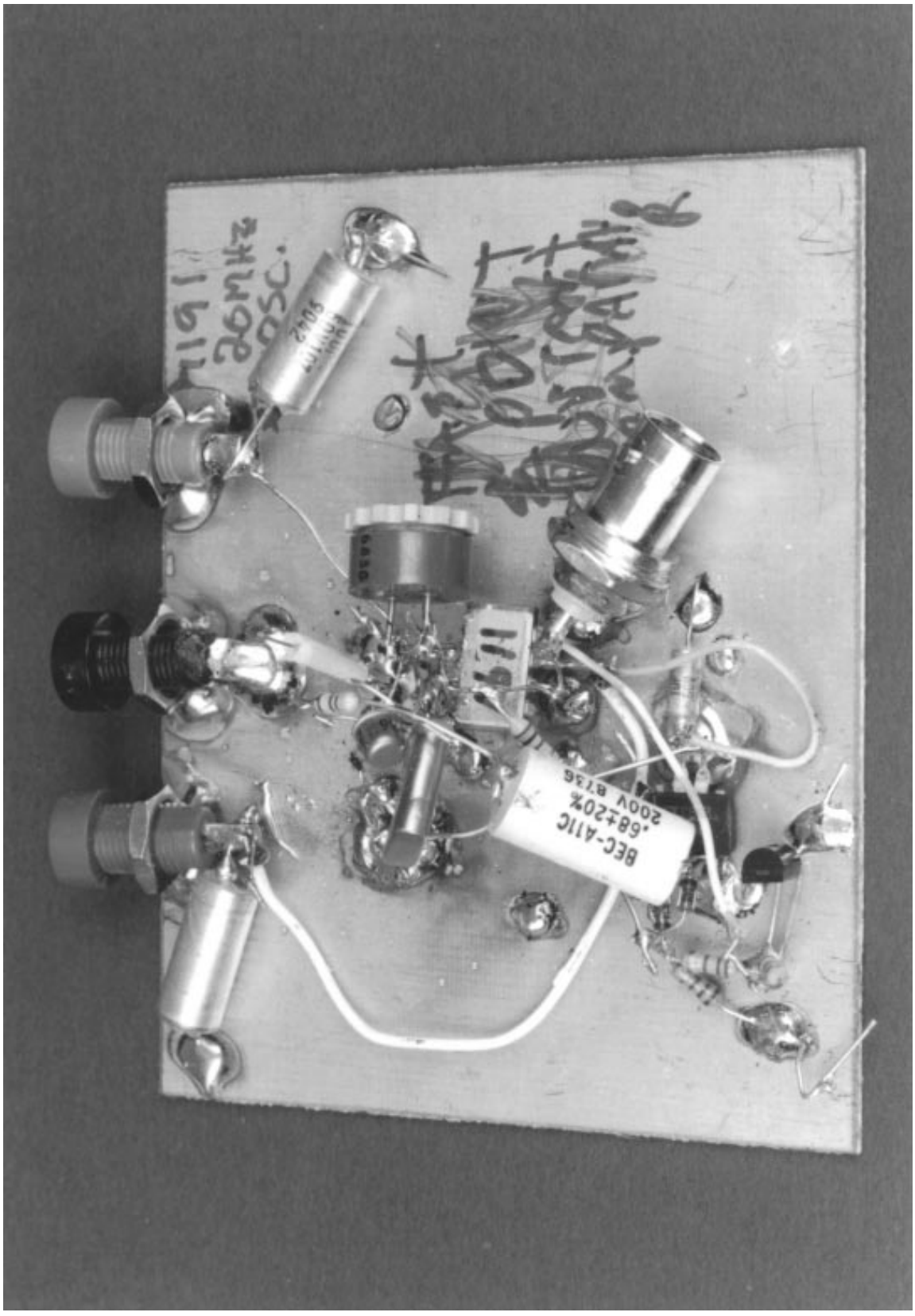
LTAN47 • TAF14

Figure F14. Detail of the Fiber Optic Receiver's Photo-Simulation BNC Input. Resistor From BNC is Routed Through a Small Hole in Vertical Shield, Minimizing Capacitance. Another Resistor on the Shield's Other Side Divides Effects of Residual Capacitance to Keep Summing Point Clean



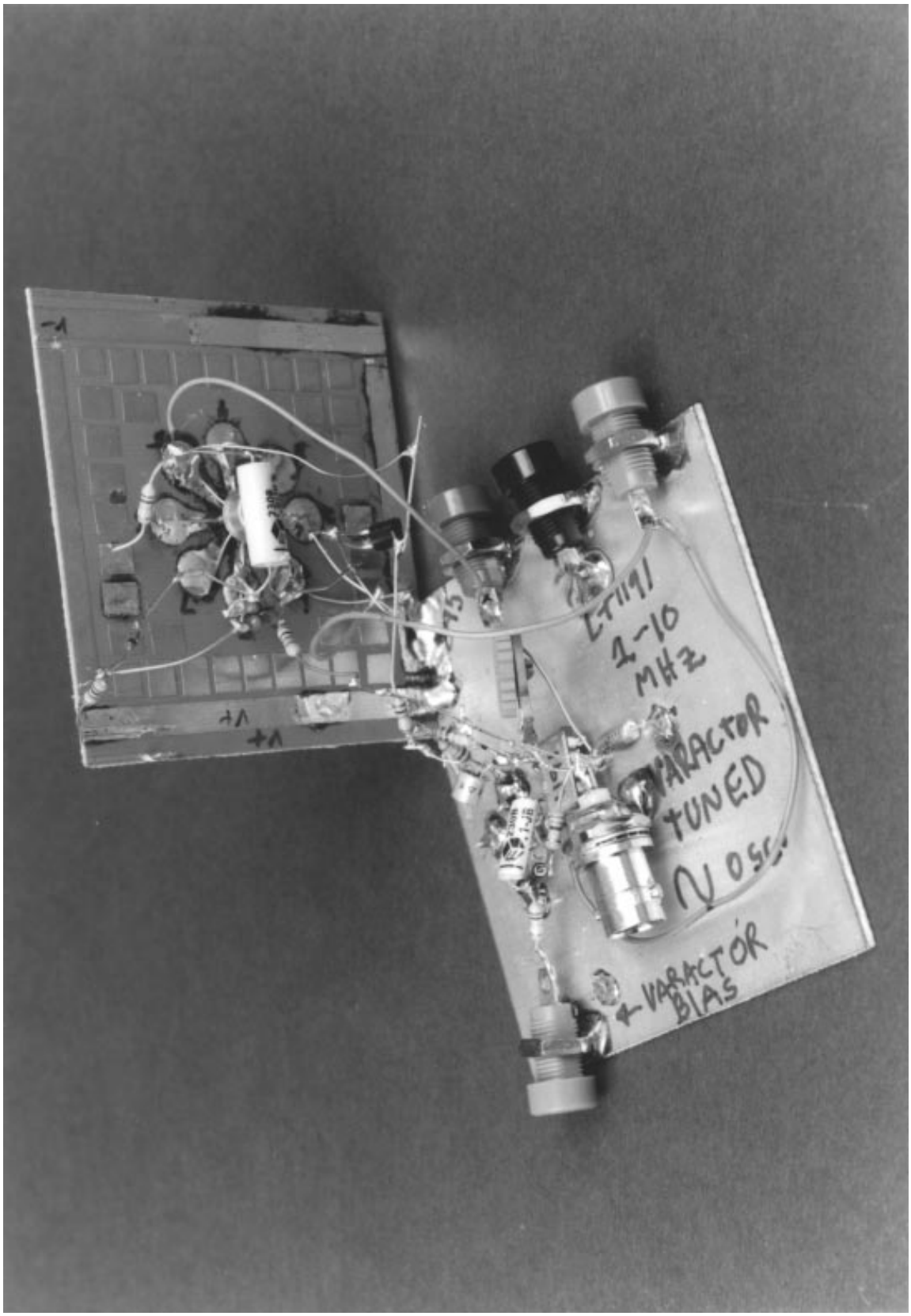
LTAN47 • TAF15

Figure F15. The 1A Booster. Note Heavy Bypassing Right at the Output Power Transistors (Both Stud-Mounted to Clad). Local Compensation Capacitors (Right Side Upper and Lower) Have Short Leads



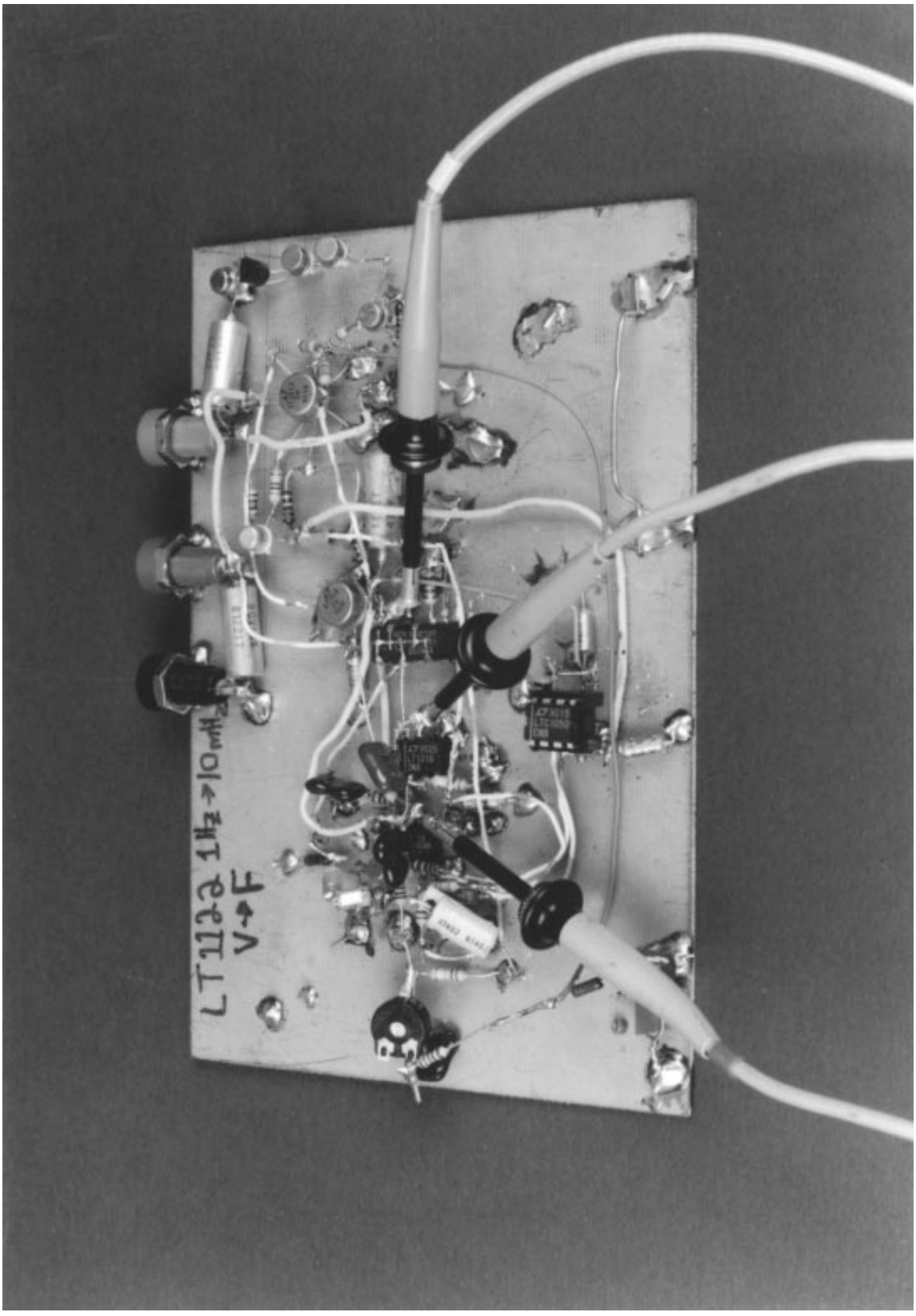
LTAN47 • TAF16

Figure F16. 20MHz Sine Wave Crystal Oscillator. DC-AGC Section is at Lower Left, Oscillator is in Center. Control FET is Located at Oscillator Amplifier. Slow Gate Control Signal Arrives via Long-Leaded Resistor, (Photo Center Upper Left)



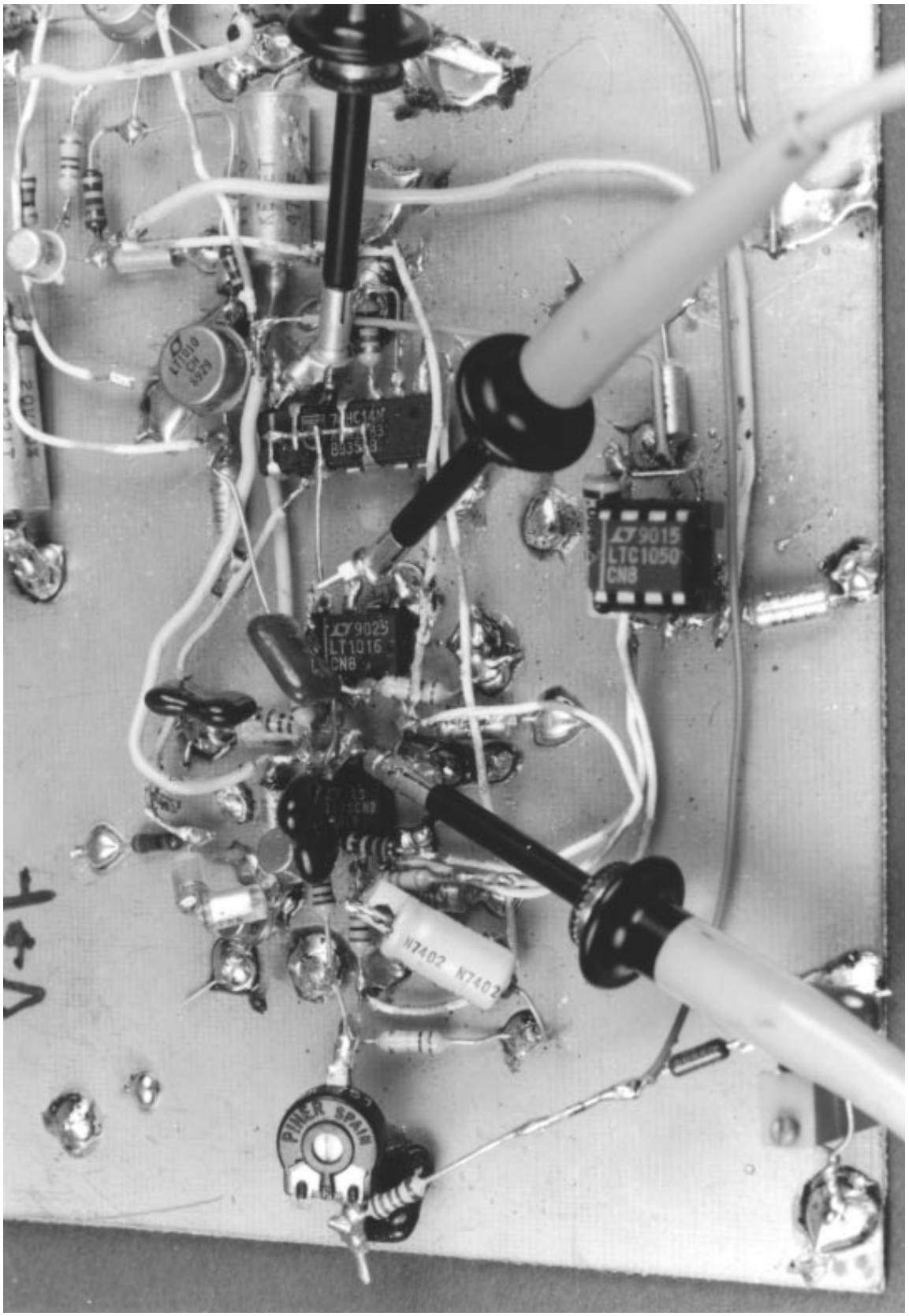
LTAN47 • TAF17

Figure F17. The Varactor Tuned Wien Bridge. DC-AGC Section is on Vertical Board — High Frequency Section Hugs the Ground Plane. Control FET (Center Left), Located at Oscillator, is Biased From a Long Line Originating on AGC Board. Note FET Gate Resistor is Located at FET, Not DC Board. Oscillator Output Receives Reverse Treatment



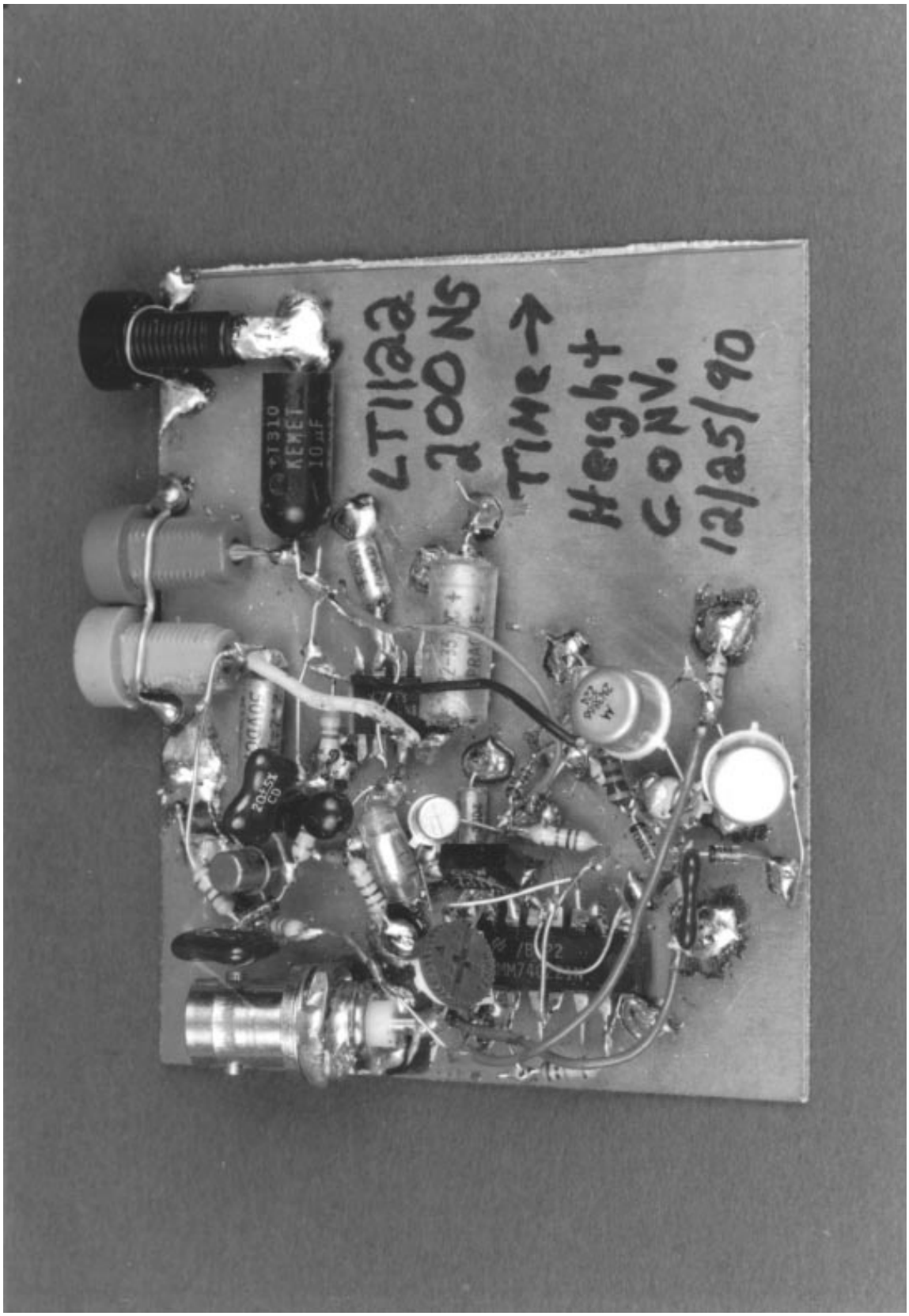
LTAN47 • TAF18

Figure F18. The 1Hz-10MHz V to F Breadboard with Probes Attached. DC Servo Amplifier is Socketed, with Long Leads. Reference Section, Starting at Breadboard (Upper Right), Works Toward Reference Switch (Large DIP at Board Center). Note Very Tight Layout in Amplifier-Comparator Region (Board Left Center)



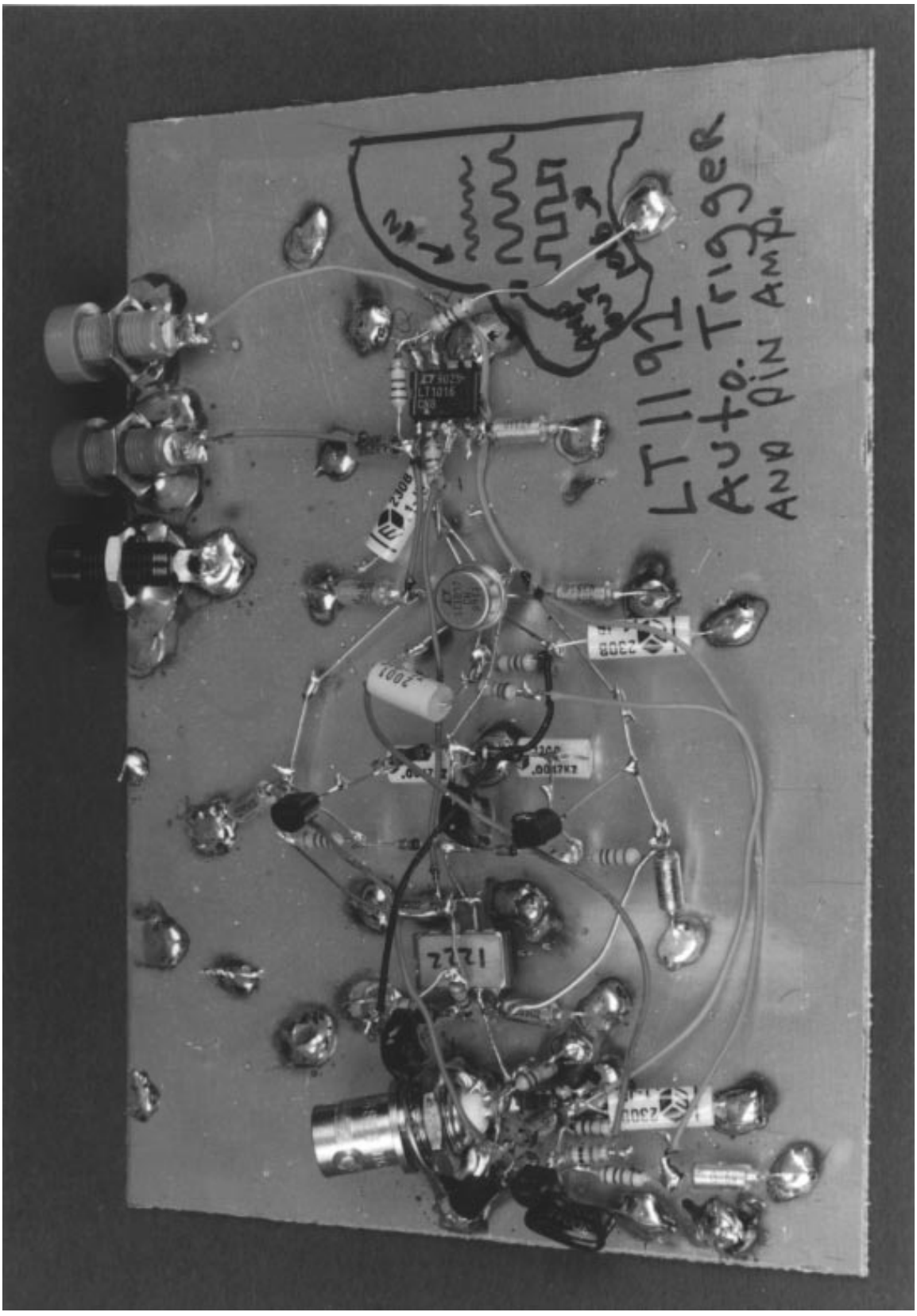
LTAN47 • TAF19

Figure F19. Details of 1Hz-10Mhz V to F High Speed Section. LT1122 Integrator is Just Visible Under its Associated Discrete Components. Summing Point (Left Side of Amplifier) is Layout's Electrical Center. LT1016 Wiring is Also Very Tight Except for its Output Which Goes to Reference Switch. DC Servo Amplifier Sleeps in its Socket. Note Probe Tip Connectors



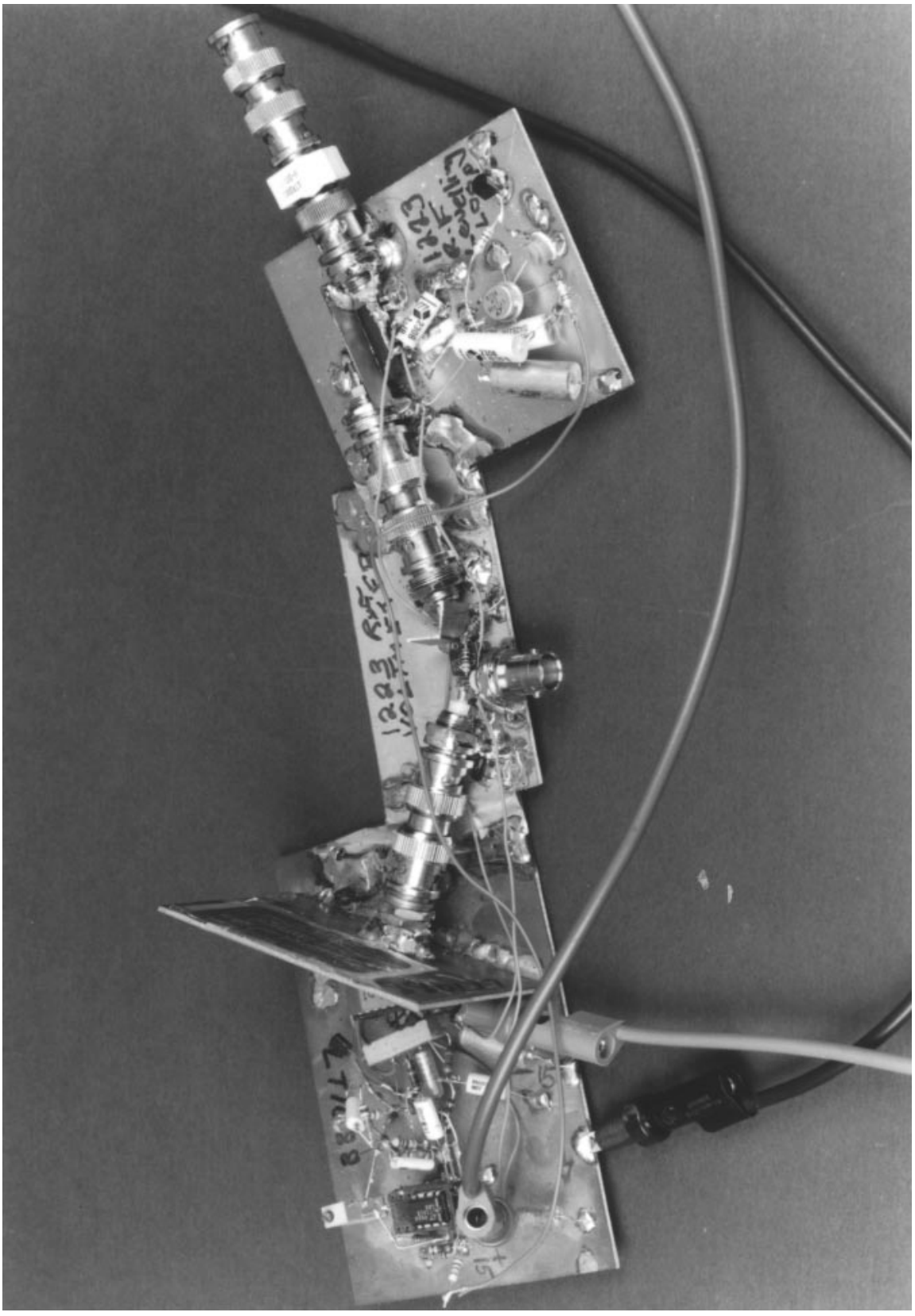
LTAN47 • TAF20

Figure F20. The Time-to-Height Converter. Switched Current Source, (Board Center Left), has Very Tight Layout. Follower Amplifier is at Board Upper Center. Major Components (in Order from Top to Bottom), Include Current Source Switch Transistor, Current Source Transistor (Black Case), Integrator Capacitor (Silver) and Reset Transistor. Note Short Connection to Amplifier Input Pin



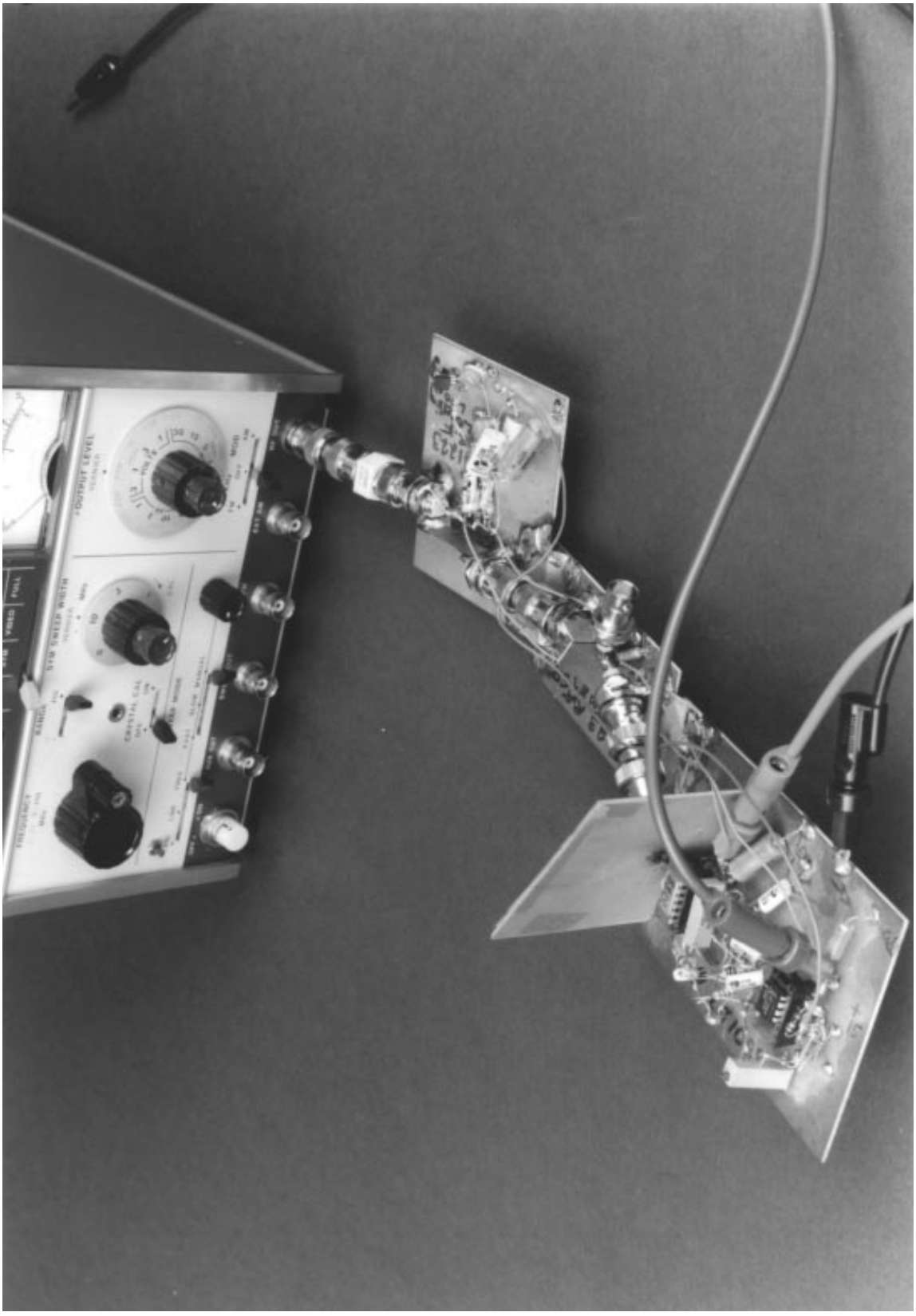
LTAN47 • TAF21

Figure F21. The Automatic Trigger. Low Frequency Automatic Level Section is Spread Out, (Right Side of Board). Wideband Circuitry Hugs Ground Plane and is Located Near Input BNC. Amplifier's Low Impedance, Fast Output Feeds LT1016 Output Comparator Over a Relatively Long Wire Run, Routed Through Insensitive Section of DC Circuitry



LTAN47 • TAF22

Figure F22. The RF Leveling Loop. The RMS to DC Converter (Left Board) was Built First, Then the RF Pre-Amp (Center Board) and Finally the Multiplier-Servo Board. Each Board's Performance was Verified Before Joining Them. Note Copper Tape Maintaining Ground Plane Integrity Between Boards

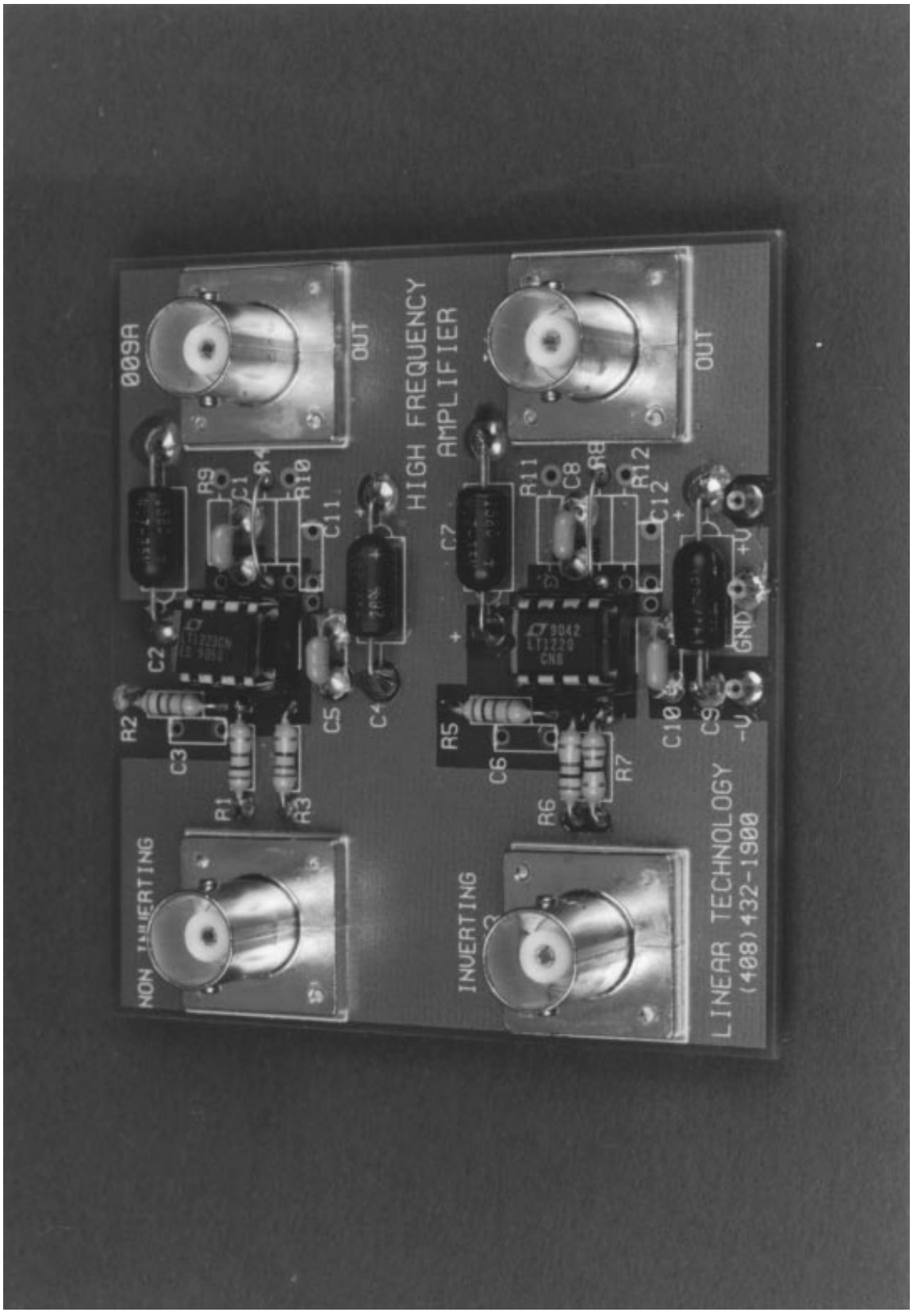


LTAN47 • TAF23

Figure F23. RF Leveling Loop Attached Directly to the Test Generator. Cable Uncertainties are Eliminated Because There is No Cable

LTAN47 • TAF24

Figure F24. The Voltage Controlled Current Source. Vertical Shield (Upper Left) Absorbs Input BNC Radiation. Amplifier-Loop Compensation Components are Located Directly at Amplifier (Behind Shield)



LTAN47 • TAF25

Figure F25. The Good Life. The High Frequency Amplifier Demonstration Board Discussed in Appendix I. Sockets are a Compromise Between Best Performance and Flexibility

APPENDIX G

FCC Licensing and Construction Permit Applications for Commerical AM Broadcasting Stations

In accordance with the application for Figure 116's circuit, and our law-abiding nature, find facsimiles of the appropriate FCC applications below. The complete forms are available by writing to:

Federal Communications Commission
Washington, D.C. 20554

Federal Communications Commission
Washington, D. C. 20554

FCC 301

Approved by OMB
3060-0027
Expires 2/28/92
See Page 25 for information regarding public burden estimate

APPLICATION FOR CONSTRUCTION PERMIT FOR COMMERCIAL BROADCAST STATION

For COMMISSION Fee Use Only

FEE NO:

FEE TYPE:

FEE AMT:

ID SEQ:

For APPLICANT Fee Use Only

Is a fee submitted with this application? ☐ Yes ☐ No

If fee exempt (see 47 C.F.R. Section 1.1112), indicate reason therefor (check one box):

☐ Noncommercial educational licensee
☐ Governmental entity

FOR COMMISSION USE ONLY

FILE NO.

Section I – GENERAL INFORMATION

1. Name of Applicant

Street Address or P.O. Box

City | State | ZIP Code

Telephone No. (Include Area Code)

Send notices and communications to the following person at the address below:

Name

Street Address or P.O. Box

City | State | ZIP Code

Telephone No. (Include Area Code)

2. This application is for: ☐ AM ☐ FM ☐ TV

(a) Channel No. or Frequency

(b) Principal Community | City | State

(c) Check one of the following boxes:

☐ Application for NEW station

☐ MAJOR change in licensed facilities; call sign: _____

☐ MINOR change in licensed facilities; call sign: _____

☐ MAJOR modification of construction permit; call sign: _____

File No. of construction permit: _____

☐ MINOR modification of construction permit; call sign: _____

File No. of construction permit: _____

☐ AMENDMENT to pending application; Application file number: _____

NOTE: It is not necessary to use this form to amend a previously filed application. Should you do so, however, please submit only Section I and those other portions of the form that contain the amended information.

6. Is this application mutually exclusive with a renewal application? ☐ Yes ☐ No

If Yes, state: Call letters | Community of License: City | State

Figure G1

Federal Communications Commission
Washington, D.C. 20554

APPLICATION FOR NEW BROADCAST STATION LICENSE
(Carefully read instructions before filling out Form)
RETURN ONLY FORM TO FCC

Approved by OMB
3060-0029
Expires 9/30/90

For Commission Fee Use Only

FEE NO:

FEE TYPE:

FEE AMT:

ID SEQ:

For Applicant Fee Use Only

Is a fee submitted with this application? ☐ Yes ☐ No

If No, indicate reason therefor (check one box):

☐ Nonfeeable application
Fee Exempt (See 47 C.F.R. Section 1.1112)
☐ Noncommercial educational licensee
☐ Governmental entity

SECTION I – GENERAL DATA

For Commission Use Only

File No.

Legal Name of Applicant

Mailing Address

City | State | Zip Code

Telephone No. (include area code)

1. Facilities authorized by construction permit

This application is for: ☐ Commercial ☐ Noncommercial

☐ AM Directional ☐ AM Non-Directional ☐ FM Directional ☐ FM Non-Directional ☐ TV

Call Letters	Community of License	Construction Permit File No.	Modification of Construction Permit File No(s).	Expiration Date of Last Construction Permit

2. Is the station now operating pursuant to automatic program test authority in accordance with 47 C.F.R. Section 73.1620? ☐ Yes ☐ No

If No, explain.

3. Have all the terms, conditions, and obligations set forth in the above described construction permit been fully met? ☐ Yes ☐ No

If No, state exceptions.

4. Apart from the changes already reported, has any cause or circumstance arisen since the grant of the underlying construction permit which would result in any statement or representation contained in the construction permit application to be now incorrect? ☐ Yes ☐ No

If Yes, explain.

5. Has the permittee filed its Ownership Report (FCC Form 323) or ownership certification in accordance with 47 C.F.R. Section 73.3615(b)? ☐ Yes ☐ No ☐ Does not apply

If No, explain.

Figure G2

Figure G1-G2. The FCC Forms Appropriate for Figure 116's Circuit

APPENDIX H

About Current Feedback

Contrary to some enthusiastic marketing claims, current feedback isn't new. In fact, it is much older than "normal" voltage feedback, which has been so popularized by op amps. The current feedback connection is *at least* 50 years old, and probably much older. William R. Hewlett used it in 1939 to construct his now famous sine wave oscillator.[1] "Cathode feedback" was widely applied in RF and wideband instrument design throughout the 30's, 40's and 50's. It was a favorite form of feedback, if for no other reason than there wasn't any place else left to feed back to!

In the early 1950's G.A. Philbrick Researches introduced the K2-W, the first commercially available packaged operational amplifier. This device, with its high impedance differential inputs, permitted the voltage type feedback so common today. Although low frequency instrumentation types were quick to utilize the increased utility afforded by high impedance feedback nodes, RF and wideband designers hardly noticed. They continued to use cathode feedback, called (what else?) emitter feedback in the new transistor form.

Numerous examples of the continued use of current feedback in RF and wideband instruments are found in designs dating from the 1950's to the present.[2] With ostensibly easier to use voltage type feedback a reality during this period, particularly as monolithic devices became cheaper, why did discrete current feedback continue to be used? The reason for the continued popularity of current techniques was (and is) bandwidth. Current feedback is simply much faster. Additionally, within limits, a current feedback based amplifier's bandwidth does not degrade as closed loop gain is increased. This is a significant advantage over voltage feedback amplifiers, where bandwidth falls as closed loop gain is increased.

Note 1: See Appendix C, "The Wien Bridge and Mr. Hewlett", in Reference 19. See also References 20 through 24 and 46.

Note 2: See the "General Electric Transistor Manual", published by G.E. in 1964. See also operating and service manuals for the Hewlett-Packard 3400A RMS Voltmeter, 1120A FET probe, and the Tektronix P6042 current probe.

Relatively recently, current based designs have become available as general purpose, easy to use monolithic and hybrid devices. This brings high speed capability to a much wider audience, hopefully opening up new applications. So, while the technique is not new, marketing claims notwithstanding, the opportunity is. Although current based designs have poorer DC performance than voltage amplifiers, their bandwidth advantage is undeniable. What's the magic?

Current Feedback Basics

William H. Gross

The distinctions of how current feedback amplifiers differ from voltage feedback amplifiers are not obvious at first, because, from the outside, the differences can be subtle. Both amplifier types use a similar symbol, and can be applied on a first order basis using the same equations. However, their behavior in terms of gain bandwidth tradeoffs and large signal response is another story.

Unlike voltage feedback amplifiers, small signal bandwidth in a current feedback amplifier isn't a straight inverse function of closed loop gain, and large signal response is closer to ideal. Both benefits are because the feedback resistors determine the amount of current driving the amplifier's internal compensation capacitor. In fact, the amplifier's feedback resistor (R_f) from output to inverting input works with internal junction capacitances to set the closed loop bandwidth. Even though the gain set resistor (R_g) from inverting input to ground works with the R_f to set the voltage gain, just as in a voltage feedback op amp, the closed loop bandwidth does not change. The explanation of this is fairly straightforward. The equivalent gain bandwidth product of the CFA is set by the Thevenin equivalent resistance at the inverting input and the internal compensation capacitor. If R_f is held constant and gain changed with R_g, the Thevenin resistance changes by the same amount as the gain. From an overall loop standpoint, this change in feedback attenuation will produce a change in noise gain, and a proportionate reduction of open loop bandwidth (as in a conventional op amp). With current feedback, however, the key point is that changes in Thevenin resistance also produce compensatory changes

in open loop bandwidth, unlike a conventional fixed gain bandwidth amplifier. As a result, the net closed loop bandwidth of a current-fed-back amplifier remains the same for various closed loop gains.

Figure H1 shows the LT1223 voltage gain vs frequency for five gain settings driving 100Ω. Shown for comparison is a plot of the fixed 100MHz gain bandwidth limitation that a voltage feedback amplifier would have. It is obvious that for gains greater than one, the LT1223 provides 3-20 times more bandwidth.

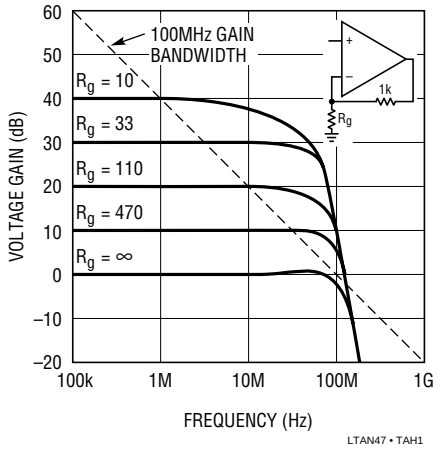


Figure H1. Voltage Gain vs Frequency for Current Feedback Amplifier (Family of Curves) and a Conventional Voltage Amplifier (Straight Line)

Because the feedback resistor determines the compensation of the LT1223, bandwidth and transient response can be optimized for almost every application. When operating on ±15V supplies, R_f should be 1kΩ or more for stability, but on ±5V, the minimum value is 680Ω, because the junction capacitors increase with lower voltage. For either case, larger feedback resistors can also be used, but will slow down the LT1223 (which may be desirable in some applications).

The LT1223 delivers excellent slew rate and bandwidth with better DC performance than previous current feedback amplifiers (CFAs). On ±15V supplies with a 1k feedback resistor, the small signal bandwidth is 100MHz into a 400Ω load and 75MHz into 100Ω. The input will follow slew rates of 250V/μs with the output generating over 500V/μs, and output slew rate is well over 1000V/μs for large input overdrive. Input offset voltage is 3mV (max), and input bias current is 3μA (max). A 10kΩ pot, connected to pins 1 and 5 with wiper to V^+, provides optional offset trimming. This trim shifts inverting input current about ±10μA, effectively producing input voltage offset.

The LT1223 also has shutdown control, available at pin 8. Pulling more than 200μA from pin 8 drops the supply current to less than 3mA, and puts the output into a high impedance state. The easy way to force shutdown is to ground pin 8 using an open collector (drain) logic stage. An internal resistor limits current, allowing direct interfacing with no additional parts. When pin 8 is open, the LT1223 operates normally.

The difference in operating characteristics between op amps and CFAs result in slight differences in common circuit configurations. Figure H2 summarizes some popular circuit types, showing differences between op amps and CFAs. Gain can be set with either R_{IN} or R_f in an op amp, while a CFA's feedback resistor (R_f) is fixed. Op amp bandwidth is controllable with a feedback capacitor; for a CFA, bandwidth must be limited at the input. A feedback capacitor is never used. In an integrator, the 1k resistor must be included in the CFA so its negative input sees the optimal impedance. Finally, (not shown) there is no correlation between bias currents of a CFA's inputs. Because of this, source impedance matching will not improve DC accuracy. Matching input source impedances aids offset performance in op amps that do not have internal bias current cancellation.

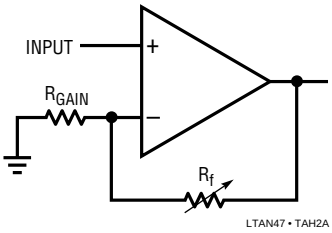
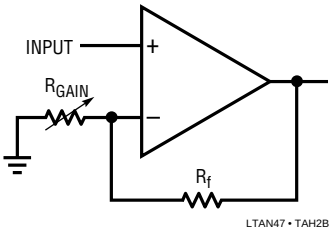
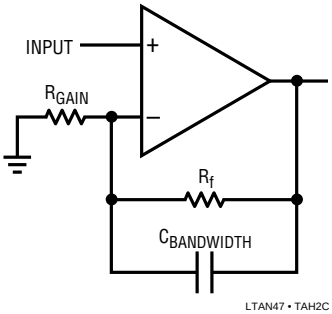
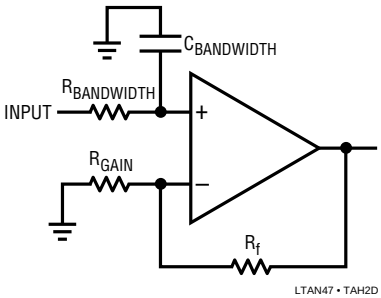
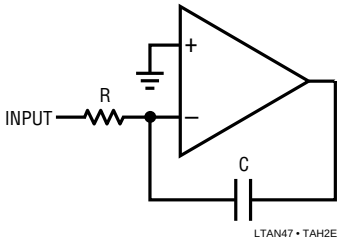
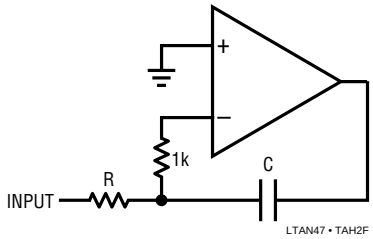
CIRCUIT TYPE	VOLTAGE FEEDBACK OP AMP	CURRENT FEEDBACK AMPLIFIER
SETTING GAIN		
LIMITING BANDWIDTH		
INTEGRATOR		

Figure H2. Some Practical Differences in Applying Current and Voltage Amplifiers

APPENDIX I

High Frequency Amplifier Evaluation Board

LTC demo board 009 (photo, Figure I1, schematic, Figure I2) is designed to simplify the evaluation of high speed operational amplifiers. It includes both an inverting and non-inverting circuit, and extra holes are provided to allow the use of board-mounted BNC or SMA connectors. The two circuits are independent with the exception of shared power supply and ground connections.

Layout is a primary contributor to the performance of any high speed amplifier. Poor layout techniques adversely affect the behavior of a finished circuit. Several important layout techniques, all used in demo board 009, are described below:

1. Top side ground plane. The primary task of a ground plane is to lower the impedance of ground connections. The inductance between any two points on a uniform sheet of copper is less than the inductance of a thin, straight trace of copper connecting the same two points. The ground plane approximates the characteristics of a copper sheet and lowers the impedance at key points in the circuit, such as the grounds of connectors and supply bypass capacitors.

2. Ground plane voids. Certain components and circuit nodes are very sensitive to stray capacitance. Two good examples are the summing node of the op amp and the feedback resistor. Voids are put in the ground plane in these areas to reduce stray ground capacitance.

3. Input/output matching. The width of the input and output traces is adjusted to a stripline impedance of 50Ω. Note that the terminating resistors (R3 and R7) are connected to the end of the input lines, not at the connector. While stripline techniques aren't absolutely necessary for the demo board, they are important on larger layouts where line lengths are longer. The short lines on the demo board can be terminated in 50Ω, 75Ω, or 93Ω without adversely affecting performance.

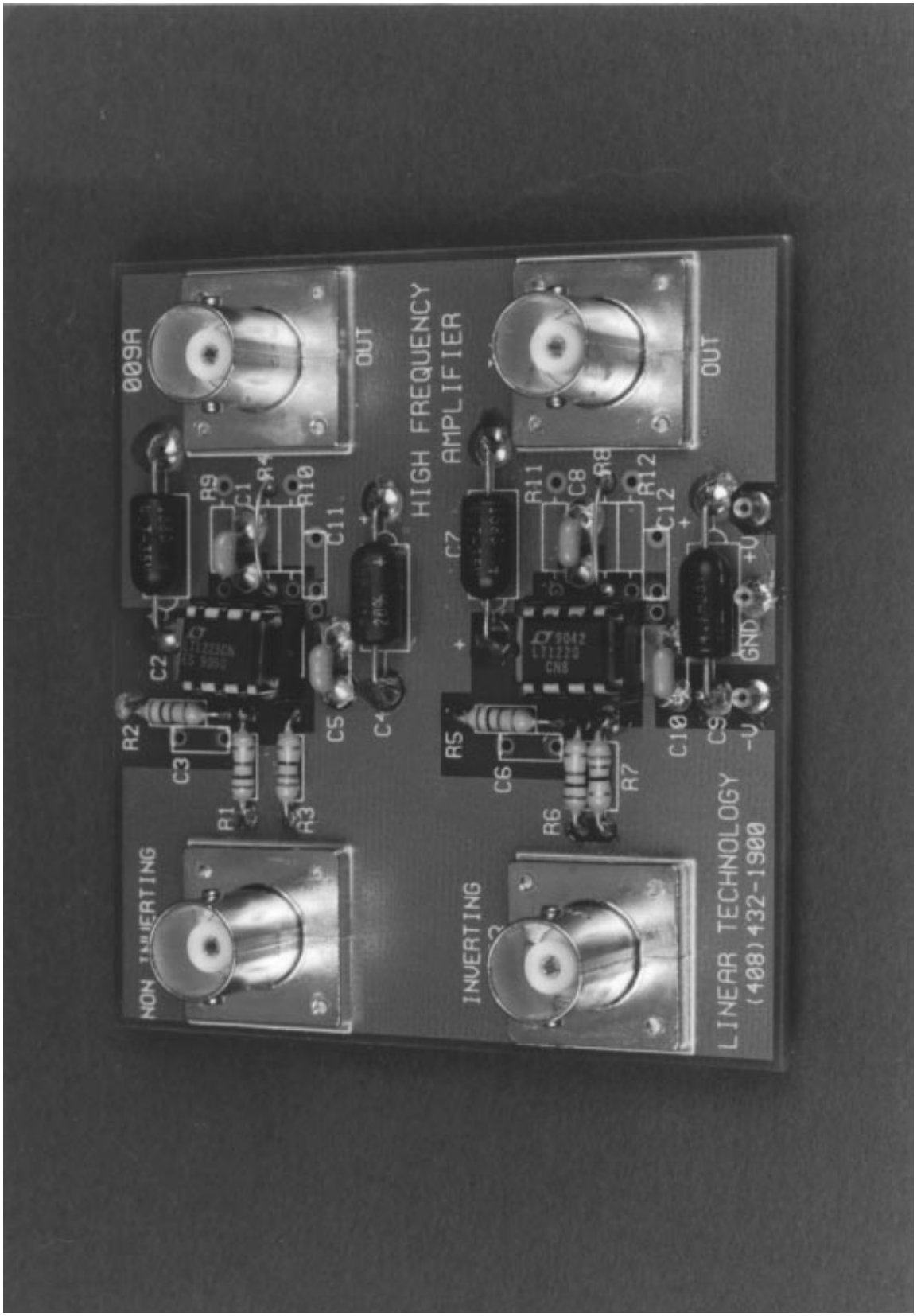
4. Separation of input and output grounds. Even though the ground plane exhibits a low impedance, input and output grounds are still separated. For example, the termination resistors (R3 and R7) and the gain-setting resistor (R1) are grounded in the vicinity of the input connector. Supply bypass capacitors (C1, C2, C4, C5, C7, C8, C9 and C10) are returned to ground in the vicinity of the output connectors.

The circuit board is designed to accommodate standard 8-pin miniDIP, single operational amplifiers such as the LT1190 and LT1220 families. Both voltage and current feedback types can be used. Pins 1, 5 and 8 are outfitted with extra holes for use in adjusting DC offsets, compensation, or, in the case of the LT1223 and LT1190/1/2, for shutting down the amplifier.

If a current feedback amplifier such as the LT1223 is being evaluated, omit C3/C6. R4 and R6 are included for impedance matching when driving low impedance lines. If the amplifier is supposed to drive the line directly, or if the load impedance is high, R4 and R8 can be replaced by jumpers. Similarly R10 and R12 can be used to establish a load at the output of the amplifier.

Low profile sockets may be used for the op amps to facilitate changing parts, but performance may be affected above 100MHz.

High speed operational amplifiers work best when their supply pins are bypassed with R_f-quality capacitors. C1, C5, C8 and C10 should be 10nF disc ceramic or other capacitors with a self-resonant frequency greater than 10MHz. The polarized capacitors (C2, C4, C7, and C9) should be 1μF to 10μF tantalums. Most 10nF ceramics are self-resonant well above 10MHz and 4.7μF solid tantalums (axial leaded) are self-resonant at 1MHz or below. Lead lengths are critical; the self-resonant frequency of a 4.7μF tantalum drops by a factor of 2 when measured through 2" leads. Although a capacitor may become inductive at high frequencies, it is still an effective bypass component above resonance because the impedance is low.



LTAN47 • TA1

Figure 11. The Enticing LTC High Frequency Amplifier Demonstration Board. Sockets are Not Optimal, but Allow Trying Different Amplifiers

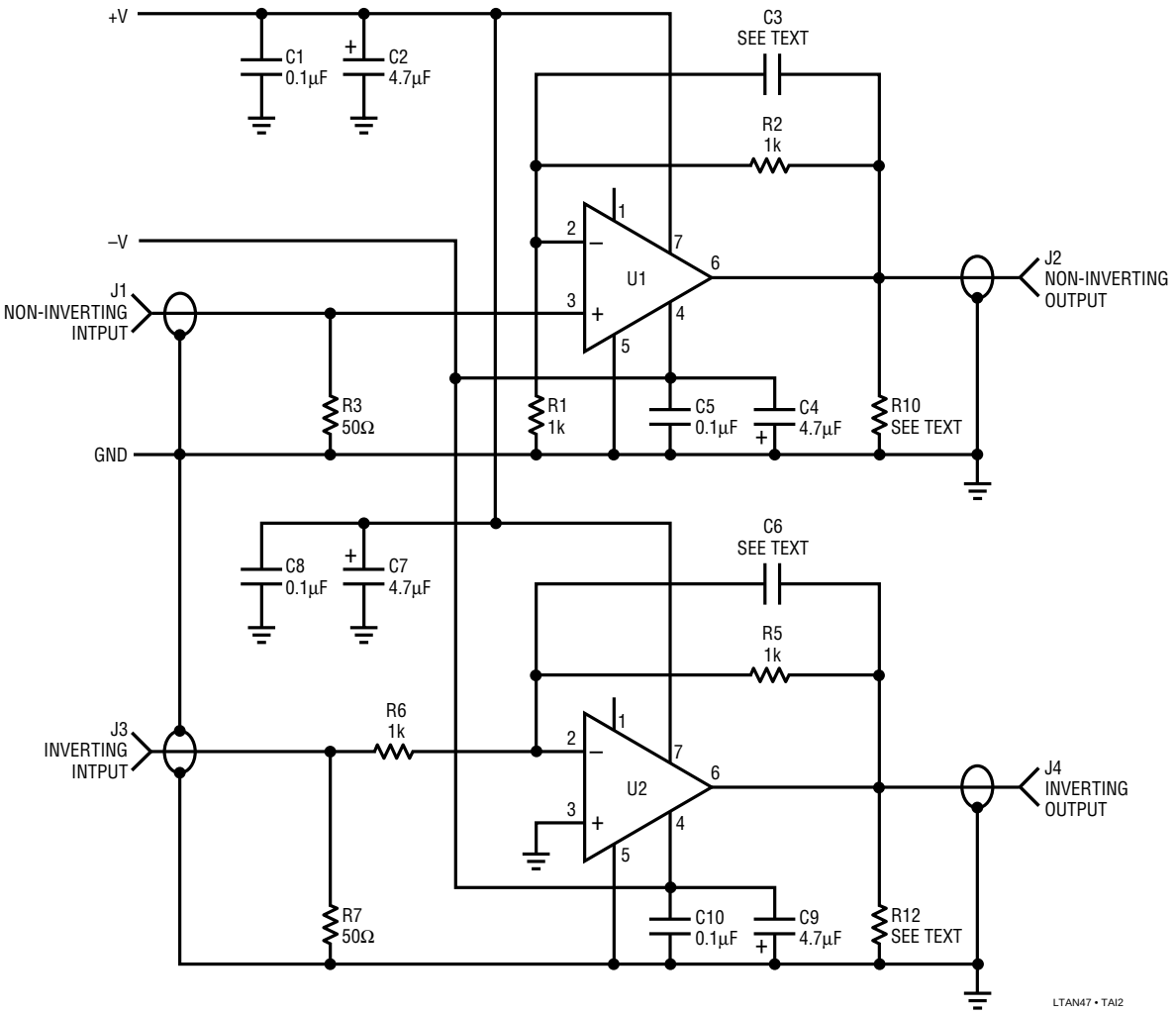


Figure I2. High Frequency Amplifier Demonstration Board Schematic

APPENDIX J

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The Contributions of Edsel Murphy to the Understanding of the Behavior of Inanimate Objects

D. L. KLIPSTEIN

Abstract—**Consideration is given to the effects of the contributions of Edsel Murphy to the discipline of electronics engineering. His law is stated in both general and special form. Examples are presented to corroborate the author's thesis that the law is universally applicable.**

I. Introduction

IT HAS LONG BEEN the consideration of the author that the contributions of Edsel Murphy, specifically his general and special laws delineating the behavior of inanimate objects, have not been fully appreciated. It is deemed that this is, in large part, due to the inherent simplicity of the law itself.

It is the intent of the author to show, by references drawn from the literature, that the law of Murphy has produced numerous corollaries. It is hoped that by noting these examples, the reader may obtain a greater appreciation of Edsel Murphy, his law, and its ramifications in engineering and science.

As is well known to those versed in the state-of-the-art, Murphy's Law states that "If anything can go wrong, it will." Or, to state it in more exact mathematical form:

$$1 + 1 \neq 2 \qquad (1)$$

where $\neq$ is the mathematical symbol for hardly ever.

Some authorities have held that Murphy's Law was first expounded by H. Cohen[1] when he stated that "If anything can go wrong, it will — during the demonstration." However, Cohen has made it clear that the broader scope of Murphy's general law obviously takes precedence.

To show the all-pervasive nature of Murphy's work, the author offers a small sample of the application of the law in electronics engineering.

II. General Engineering

II.1. A patent application will be preceded by one week by a similar application made by an independent worker.

II.2. The more innocuous a design change appears, the further its influence will extend.

II.3. All warranty and guarantee clauses become void upon payment of invoice.

II.4. The necessity of making a major design change increases as the fabrication of the system approaches completion.

II.5. Firmness of delivery dates is inversely proportional to the tightness of the schedule.

II.6. Dimensions will always be expressed in the least usable term. Velocity, for example, will be expressed in furlongs per fortnight.[2]

II.7. An important Instruction Manual or Operating Manual will have been discarded by the Receiving Department.

II.8. Suggestions made by the Value Analysis group will increase costs and reduce capabilities.

II.9. Original drawings will be mangled by the copying machine.[3]

III. Mathematics

III.1. In any given miscalculation, the fault will never be placed if more than one person is involved.

III.2. Any error that can creep in, will. It will be in the direction that will do the most damage to the calculation.

III.3. All constants are variables.

III.4. In any given computation, the figure that is most obviously correct will be the source of error.

III.5. A decimal will always be misplaced.

III.6. In a complex calculation, one factor from the numerator will always move into the denominator.

IV. Prototyping and Production

IV.1. Any wire cut to length will be too short.

IV.2. Tolerances will accumulate unidirectionally toward maximum difficulty of assembly.

IV.3. Identical units tested under identical conditions will not be identical in the field.

IV.4. The availability of a component is inversely proportional to the need for that component.

IV.5. If a project requires n components, there will be n-1 units in stock.[4]

IV.6. If a particular resistance is needed, that value will not be available. Further, it cannot be developed with any available series or parallel combination.[5]

IV.7. A dropped tool will land where it can do the most damage. (Also known as the law of selective gravitation.)

IV.8. A device selected at random from a group having 99% reliability, will be a member of the 1% group.

IV.9. When one connects a 3-phase line, the phase

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sequence will be wrong.[6]

IV.10. A motor will rotate in the wrong direction.[7]

IV.11. The probability of a dimension being omitted from a plan or drawing is directly proportional to its importance.

IV.12. Interchangeable parts won't.

IV.13. Probability of failure of a component, assembly, subsystem or system is inversely proportional to ease of repair or replacement.

IV.14. If a protoype functions perfectly, subsequent production units will malfunction.

IV.15. Components that must not and cannot be assembled improperly will be.

IV.16. A dc meter will be used on an overly sensitive range and will be wired in backwards.[8]

IV.17. The most delicate component will drop.[9]

IV.18. Graphic recorders will deposit more ink on humans than on paper.[10]

IV.19. If a circuit cannot fail, it will.[11]

IV.20. A fail-safe circuit will destroy others.[12]

IV.21. An instantaneous power-supply crowbar circuit will operate too late.[13]

IV.22. A transistor protected by a fast-acting fuse will protect the fuse by blowing first.[14]

IV.23. A self-starting oscillator won't.

IV.24. A crystal oscillator will oscillate at the wrong frequency — if it oscillates.

IV.25. A pnp transistor will be an npn.[15]

IV.26. A zero-temperature-coefficient capacitor used in a critical circuit will have a TC of –750 ppm/°C.

IV.27. A failure will not appear till a unit has passed Final Inspection.[16]

IV.28. A purchased component or instrument will meet its specs long enough, and only long enough, to pass Incoming Inspection.[17]

IV.29. If an obviously defective component is replaced in an instrument with an intermittent fault, the fault will reappear after the instrument is returned to service.[18]

IV.30. After the last of 16 mounting screws has been removed from an access cover, it will be discovered that the wrong access cover has been removed.[19]

IV.31. After an access cover has been secured by 16 hold-down screws, it will be discovered that the gasket has been omitted.[20]

IV.32. After an instrument has been fully assembled, extra components will be found on the bench.

IV.33. Hermetic seals will leak.

V. Specifying

V.1. Specified environmental conditions will always be exceeded.

V.2. Any safety factor set as a result of practical experience will be exceeded.

V.3. Manufacturers' spec sheets will be incorrect by a factor of 0.5 or 2.0, depending on which multiplier gives the most optimistic value. For salesmen's claims these factors will be 0.1 or 10.0.

V.4. In an instrument or device characterized by a number of plus-or-minus errors, the total error will be the sum of all errors adding in the same direction.

V.5. In any given price estimate, cost of equipment will exceed estimate by a factor of 3.[21]

V.6. In specifications, Murphy's Law supersedes Ohm's.

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[5] — — — —, *loc cit.*
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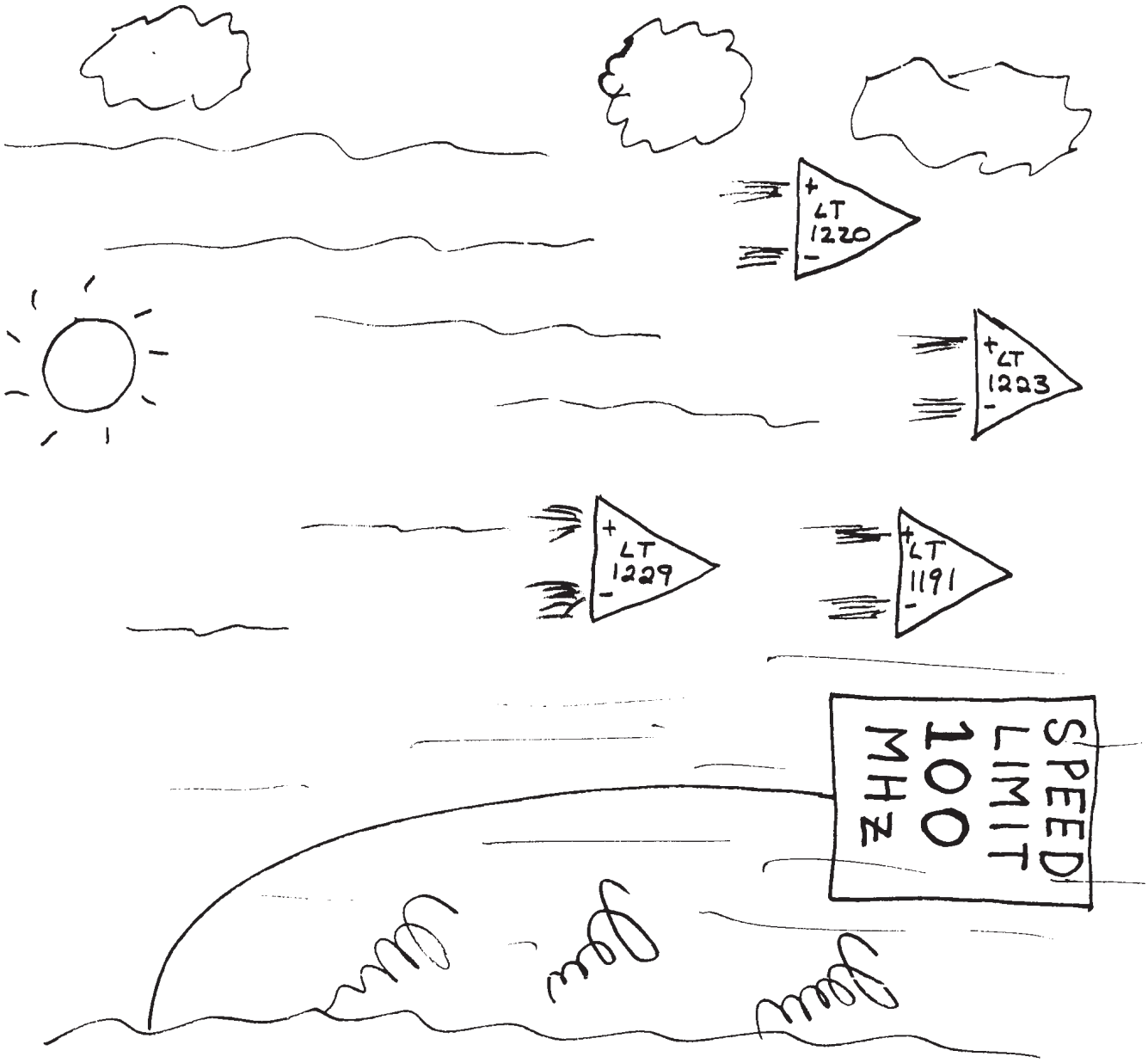
[20] — — — —, *loc cit.*
[21] P. Dietz, Data Technology, private communication.

*In some cases where no reference is given, the source material was misplaced during preparation of this paper (another example of Murphy's Law). In accordance with the law, these misplaced documents will turn up on the date of publication of this paper.

The man who developed one of the most profound concepts of the twentieth century is practically unknown to most engineers. He is a victim of his own law. Destined for a secure place in the engineering hall of fame, something went wrong.

His real contribution lay not merely in the discovery of the law but more in its universality and in its impact. The law itself, though inherently simple, has formed a foundation on which future generations will build.

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.



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