Isolated Flyback Switching Regulator

FEATURES

- **No Transformer "Third Winding" or Optoisolator Required**
- **±5% Accurate Output Voltage Without User Trims (See Circuit Below)**
- Resistor Programmable Output Voltage
- **Regulation Maintained Well Into Discontinuous Mode (Light Load)**
- Optional Load Compensation
- Operating Frequency: 285kHz
- Easily Synchronized to External Clock
- Available in 16-Pin Narrow SO Package

APPLICATIONS

- Isolated Flyback Switching Regulators
- Ethernet Isolated 5V to –9V Converters
- Medical Instruments
- Isolated Telecom Supplies

DESCRIPTION

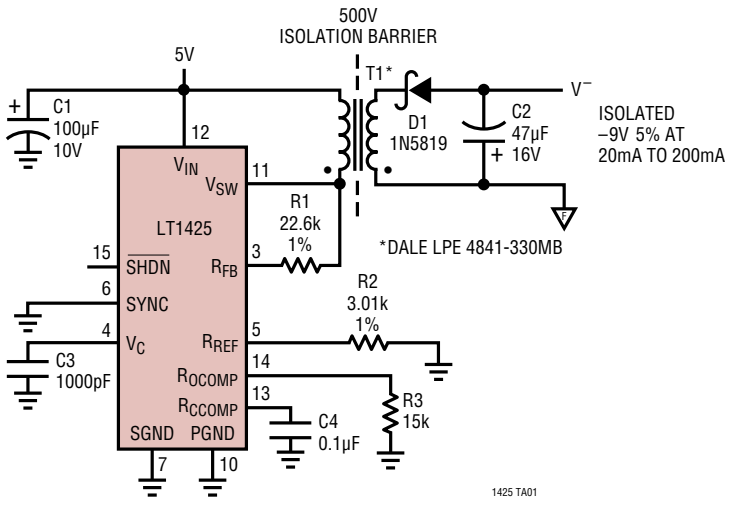
The LT®1425 is a monolithic high power switching regulator specifically designed for the isolated flyback topology. No "third winding" or optoisolator is required; the integrated circuit senses the isolated output voltage directly from the primary side flyback waveform. A high current, high efficiency switch is included on the die along with all oscillator, control and protection circuitry.

The LT1425 operates with input supply voltages from 3V to 20V and draws only 7mA quiescent current. It can deliver output power up to 6W with no external power devices. By utilizing current mode switching techniques, it provides excellent AC and DC line regulation.

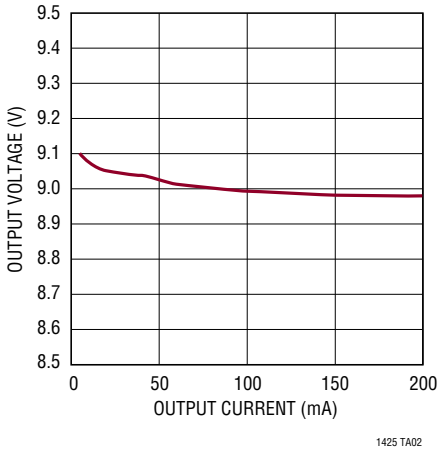
The LT1425 has a number of features not found on other switching regulator ICs. Its unique control circuitry can maintain regulation well into discontinuous mode in most applications. Optional load compensation circuitry allows for improved load regulation. An externally activated shutdown mode reduces total supply current to 15µA for standby operation.

TYPICAL APPLICATION

5V to Isolated –9V$_{OUT}$



Load Regulation

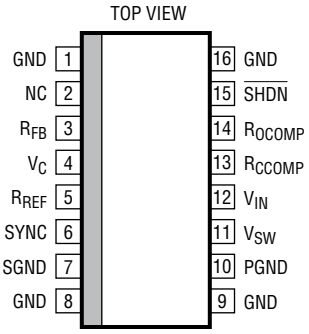


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 20V
Switch Voltage 35V
$\overline{SHDN}$, SYNC Pin Voltage 7V
R_{FB} Pin Current 2mA
Operating Junction Temperature Range
LT1425C ..... 0°C to 125°C
LT1425I ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



S PACKAGE
16-LEAD PLASTIC SO

T_{JMAX} = 145°C, θ_{JA} = 75°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT1425CS#PBF	LT1425CS#TRPBF	1425	16-Lead Plastic SOIC	0°C to 125°C
LT1425IS#PBF	LT1425IS#TRPBF	1425	16-Lead Plastic SOIC	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, T_J = 25°C, V_{SW} Open, V_C = 1.4V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Feedback Amplifier							
I_{REF}	Reference Current	Measured at R_{FB} Pin with R_{REF} = 3.000k	 ●	402 396	408	414 420	µA µA
I_{IN}	R_{REF} Pin Input Curren				500		nA
g_m	Feedback Amplifier Transconductance	Δ_{IC} = ±10µA (Note 2)	●	400	1000	1600	µmho
I_{SOURCE}, I_{SINK}	Feedback Amplifier Source or Sink Current		●	30	50	80	µA
V_{CL}	Feedback Amplifier Clamp Voltage				1.9		V
	Reference Voltage/Current Line Regulation	5V ≤ V_{IN} ≤ 18V	●		0.01	0.04	%/V
	Voltage Gain	(Note 3)			500		V/V
	V_{IN} Sense Error		●		10	25	mV
Output Switch							
BV	Output Switch Breakdown Voltage	I_C = 5mA	●	35	50		V
$V(V_{SW})$	Output Switch On-Voltage	I_{SW} = 1A	●		0.55	0.85	V
I_{LIM}	Switch Current Limit	Duty Cycle = 50%, 0°C ≤ T_J ≤ 125°C Duty Cycle = 50%, –40°C ≤ T_J ≤ 125°C Duty Cycle = 80%	●	1.35 1.2	1.60 1.60 1.30	1.95 1.95	A A A
Current Amplifier							
	Control Pin Threshold	Duty Cycle = Minimum	 ●	0.95 0.85	1.2	1.3 1.4	V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, T_J = 25°C, V_{SW} Open, V_C = 1.4V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Control Voltage to Switch Transconductance				2		A/V
Timing							
f_{SW}	Switching Frequency		 ●	260 240	285	300 320	kHz kHz
t_{ON}	Minimum Switch ON Time			170	210	260	ns
t_{ED}	Flyback Enable Delay Time				150		ns
t_{EN}	Minimum Flyback Enable Time				180		ns
	Maximum Switch Duty Cycle		●	85	90	96	%
Load Compensation							
	$\Delta V_{RCCOMP}/\Delta I_{SW}$				0.45		Ω
SYNC Function							
	Minimum SYNC Amplitude		●		1.5	2.2	V
	Synchronization Range			320		450	kHz
	SYNC Pin Input Resistance				40		kΩ
Power Supply							
$V_{IN(MIN)}$	Minimum Input Voltage		●		2.8	3.1	V
I_{CC}	Supply Current		●		7.0	9.5	mA
	Shutdown Mode Supply Current		●		15	40	µA
	Shutdown Mode Threshold		●	0.3	0.9	1.3	V

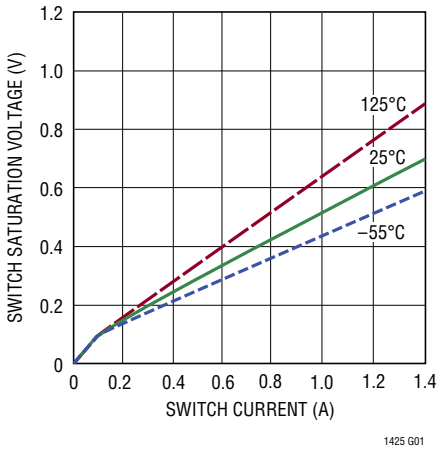
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Feedback amplifier transconductance is R_{REF} referred.

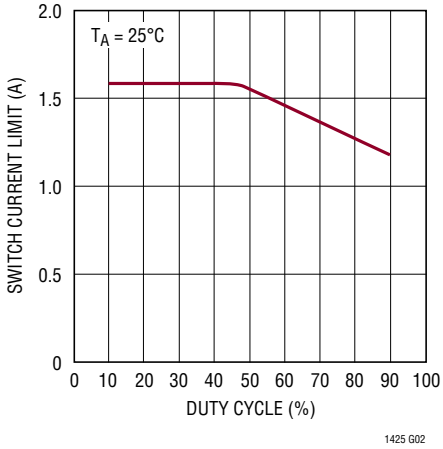
Note 3: Voltage gain is R_{REF} referred.

TYPICAL PERFORMANCE CHARACTERISTICS

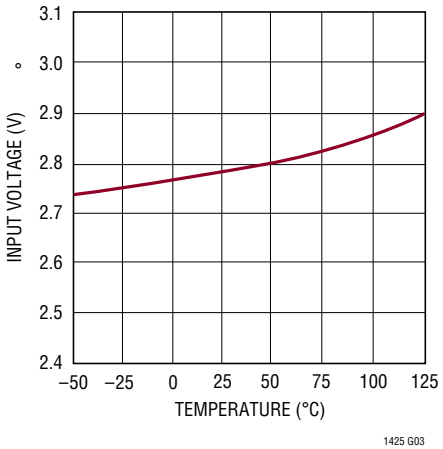
Switch Saturation Voltage vs Switch Current



Switch Current Limit vs Duty Cycle

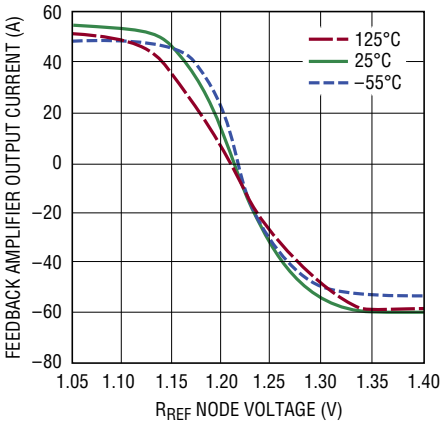


Minimum Input Voltage vs Temperature

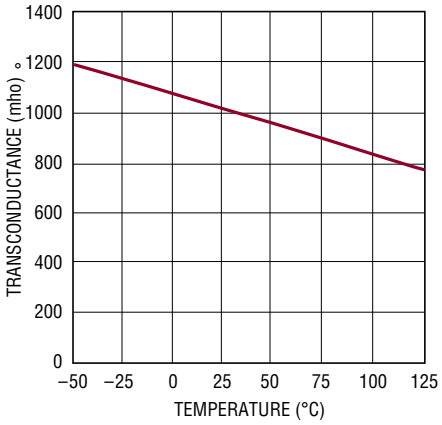


TYPICAL PERFORMANCE CHARACTERISTICS

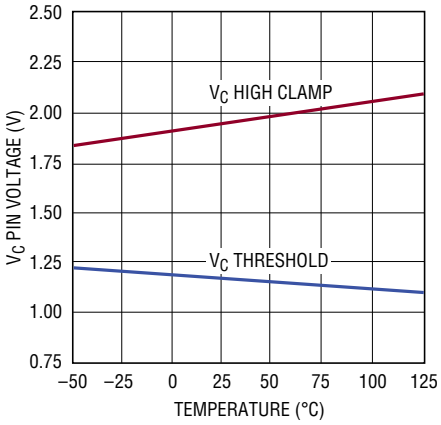
Feedback Amplifier Output Current vs R_{REF} Pin Voltage



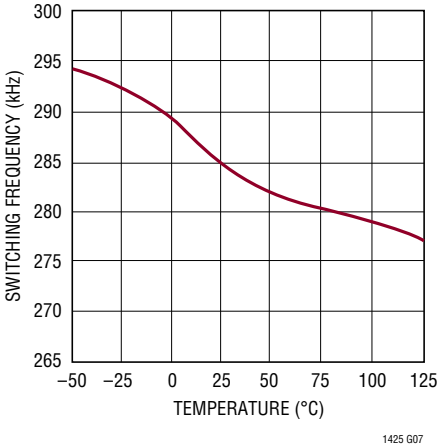
Error Amplifier Transconductance vs Temperature (R_{REF} Referred)



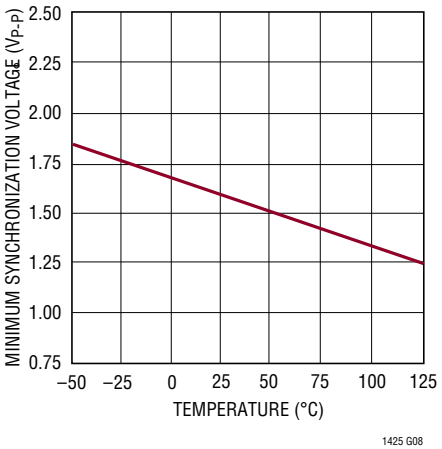
V_C Pin Threshold and High Clamp Voltage vs Temperature



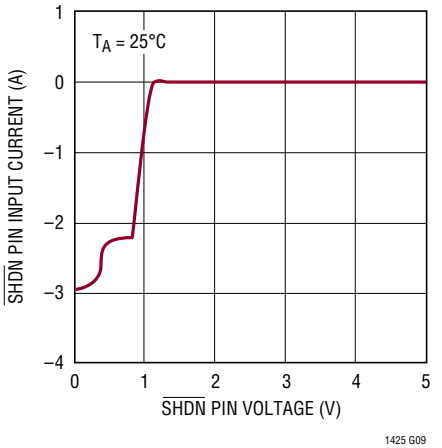
Switching Frequency vs Temperature



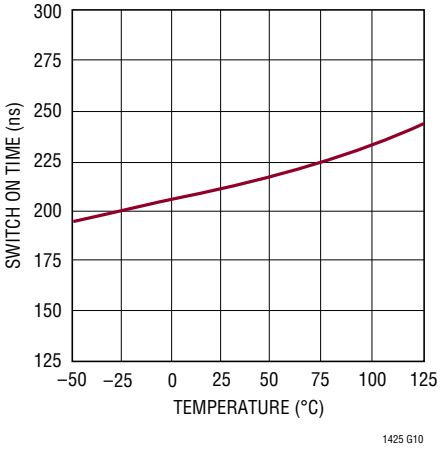
Minimum Synchronization Voltage vs Temperature



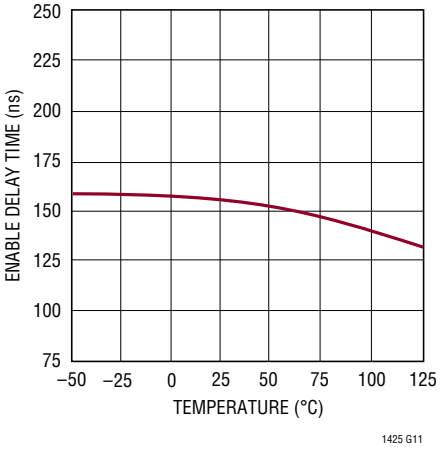
$\overline{SHDN}$ Pin Input Current vs Voltage



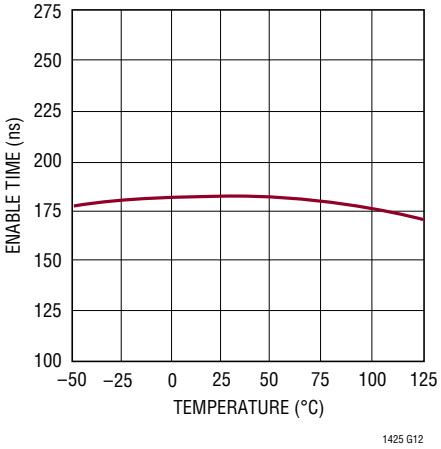
Minimum Switch ON Time vs Temperature



Flyback Enable Delay Time vs Temperature



Minimum Flyback Enable Time vs Temperature



PIN FUNCTIONS

GND (Pins 1, 8, 9, 16): Ground. These pins connect to the substrate of the die and are separate from the power ground and signal ground. They should connect directly to a good quality ground plane.

R_{FB} (Pin 3): Input Pin for External "Feedback" Resistor Connected to Transformer Primary (V_{SW}). The ratio of this resistor to the R_{REF} resistor, times the internal bandgap (V_{BG}) reference, is the primary determinant of the output voltage (plus the effect of any nonunity transformer turns ratio). The average current through this resistor during the flyback period should be approximately 400µA. See Applications Information for more details.

V_C (Pin 4): Control Voltage. This pin is the output of the feedback amplifier and the input of the current comparator. Frequency compensation of the overall loop is effected by placing a capacitor between this node and ground.

R_{REF} (Pin 5): Input Pin for External Ground-Referred "Reference" Resistor. This resistor should be in the range of 3k, but for convenience, need not be this value precisely. See Applications Information for more details.

SYNC (Pin 6): Pin to Synchronize Internal Oscillator to External Frequency Reference. It is directly logic compatible and can be driven with any signal between 10% and 90% duty cycle. If unused, this pin can be left floating; however, for best noise immunity the pin should be grounded.

SGND (Pin 7): Signal Ground. This pin is a clean ground. The internal reference and feedback amplifier are referred to it. Keep the ground path connection to R_{REF} and the V_C compensation capacitor free of large ground currents.

PGND (Pin 10): Power Ground. This pin is the emitter of the power switch device and has large currents flowing through it. It should be connected directly to a good quality ground plane.

V_{SW} (Pin 11): This is the collector node of the output switch and has large currents flowing through it. Keep the traces to the switching components as short as possible to minimize electromagnetic radiation and voltage spikes.

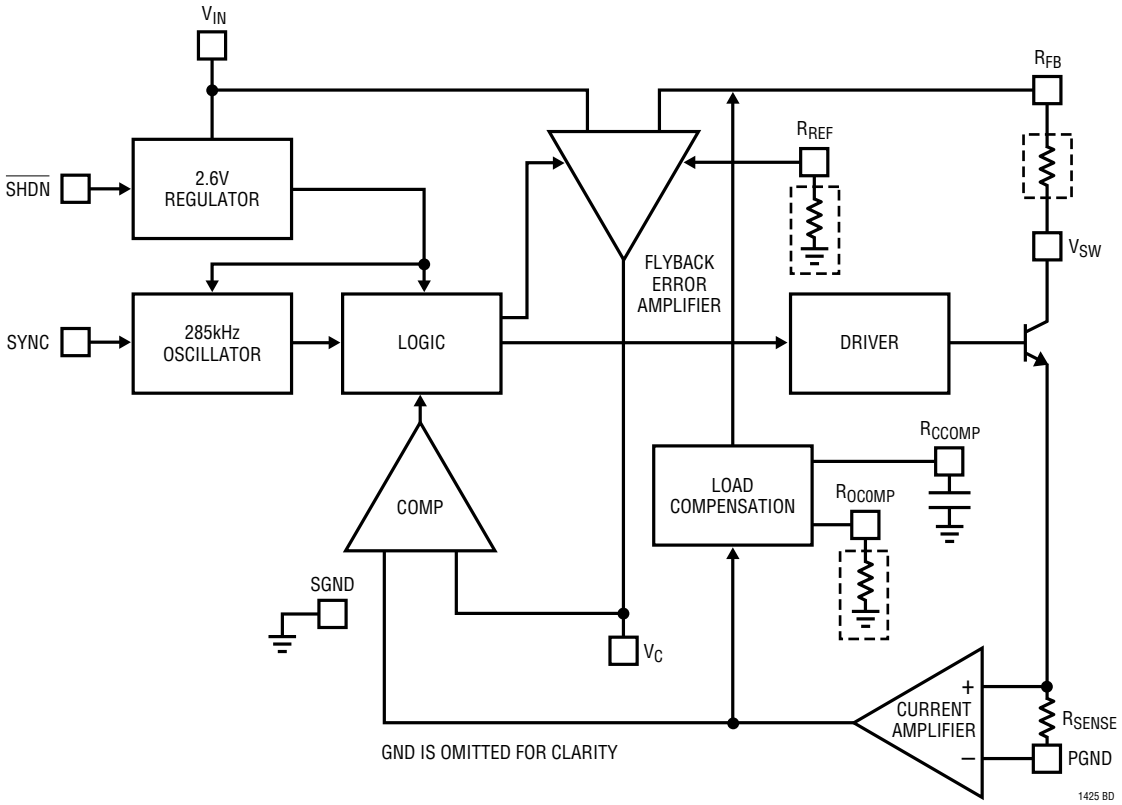
V_{IN} (Pin 12): Supply Voltage. Bypass input supply pin with 10µF or more. The part goes into undervoltage lockout when VIN drops below 2.8V. Undervoltage lockout stops switching and pulls the V_C pin low.

R_{CCOMP} (Pin 13): Pin for the External Filter Capacitor for Load Compensation Function. A common 0.1µF ceramic capacitor will suffice for most applications. See Applications Information for further details.

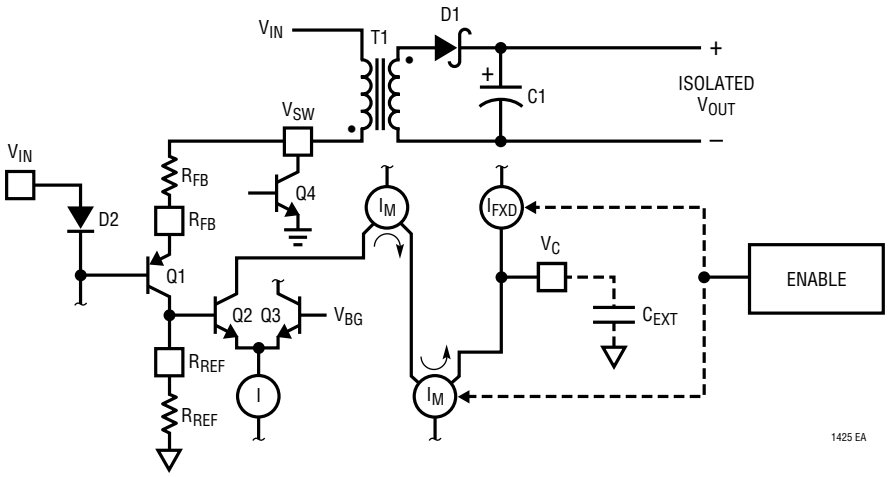
R_{OCOMP} (Pin 14): Input Pin for Optional External Load Compensation Resistor. Use of this pin allows nominal compensation for nonzero output impedance in the power transformer secondary circuit, including secondary winding impedance, output Schottky diode impedance and output capacitor ESR. In less demanding applications this resistor is not needed. See Applications Information for more details.

$\overline{SHDN}$ (Pin 15): Shutdown. This pin is used to turn off the regulator and reduce V_{IN} input current to a few tens of microamperes. The $\overline{SHDN}$ pin can be left floating when unused.

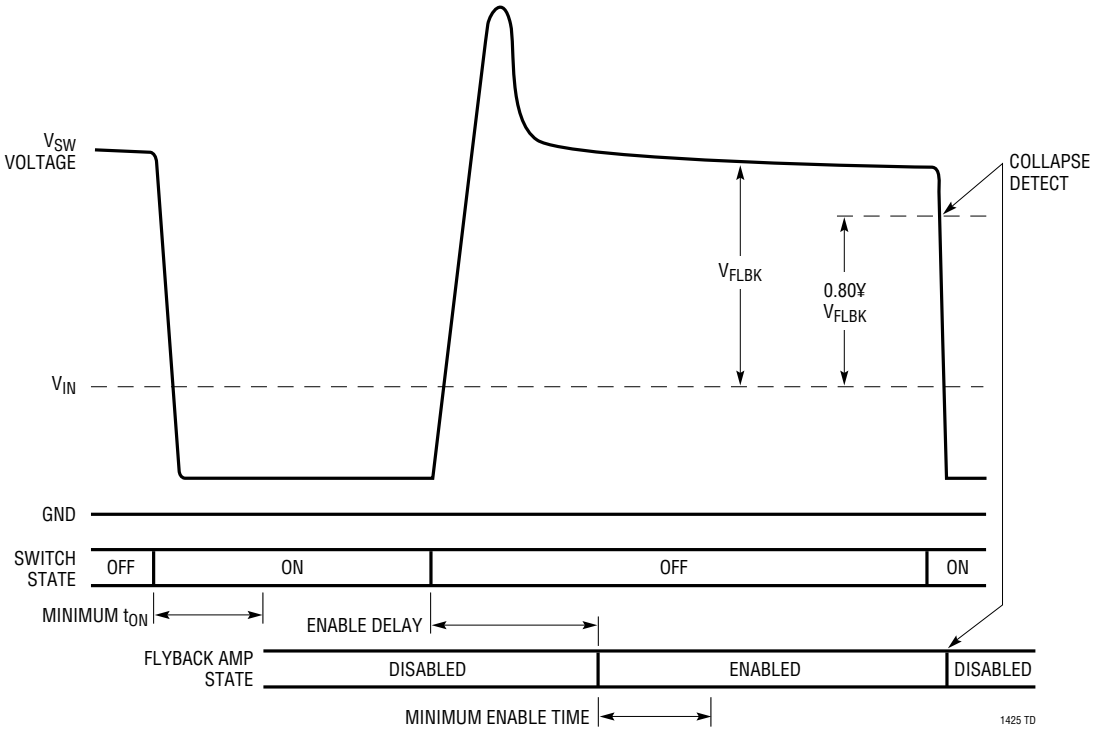
BLOCK DIAGRAM



FLYBACK ERROR A PLIFIER DIAGRAM



TIMING DIAGRAM



OPERATION

The LT1425 is a current mode switching regulator IC that has been designed specifically for the isolated flyback topology. The special problem normally encountered in such circuits is that information relating to the output voltage on the isolated secondary side of the transformer must be communicated to the primary side in order to maintain regulation. Historically, this has been done with optoisolators or extra transformer windings. Optoisolator circuits waste output power and the extra components they require increase the cost and physical volume of the power supply. Optoisolators can also exhibit trouble due to limited dynamic response (temporal), nonlinearity, unit-to-unit variation and aging over life. Circuits employing extra transformer windings also exhibit deficiencies. The extra winding adds to the transformer's physical size and cost. Dynamic response is often mediocre. There is usually no method for maintaining load regulation versus load.

The LT1425 derives its information about the isolated output voltage by examining the primary side flyback pulse waveform. In this manner no optoisolator nor extra transformer winding is required. This IC is a quantum improvement over previous approaches because: target output voltage is directly resistor-programmable, regulation is maintained well into discontinuous mode and optional load compensation is available.

The Block Diagram shows an overall view of the system. Many of the blocks are similar to those found in traditional designs including: internal bias regulator, oscillator, logic, current amplifier and comparator, driver and output switch. The novel sections include a special flyback error amplifier and a load compensation mechanism. Also, due to the special dynamic requirements of flyback control, the logic system contains additional functionality not found in conventional designs.

OPERATION

Within the dashed lines in the Block Diagram can be found the R_{REF}, R_{FB} and R_{OCOMP} resistors. They are external resistors on the user-programmable LT1425. The capacitor connected to the R_{CCOMP} pin is also external.

The LT1425 operates much the same as traditional current mode switchers, the major difference being a different type of error amplifier which derives its feedback information from the flyback pulse. Due to space constraints, this discussion will not reiterate the basics of current mode switcher/controllers and isolated flyback converters. A good source of information on these topics is ADI's Application Note 19.

ERROR AMPLIFIER—PSEUDO DC THEORY

Please refer to the simplified diagram of the Flyback Error Amplifier. Operation is as follows: when output switch Q4 turns off, its collector voltage rises above the V_{IN} rail. The amplitude of this flyback pulse, i.e., the difference between it and V_{IN}, is given as:

$$V_{FLBK} = \frac{V_{OUT} + V_F + (I_{SEC})(ESR)}{N_{SP}}$$

V_F = D1 forward voltage
I_{SEC} = Transformer secondary current
ESR = Total impedance of secondary circuit
N_{SP} = Transformer effective secondary-to-primary turns ratio

The flyback voltage is then converted to a current by the action of R_{FB} and Q1. Nearly all of this current flows through resistor R_{REF} to form a ground-referred voltage. This is then compared to the internal bandgap reference by the differential transistor pair Q2/Q3. The collector current from Q2 is mirrored around and subtracted from fixed current source I_{FXD} at the V_C pin. An external capacitor integrates this net current to provide the control voltage to set the current mode trip point.

The relatively high gain in the overall loop will then cause the voltage at the R_{REF} resistor to be nearly equal to the bandgap reference V_{BG}. (V_{BG} is not present in final output voltage setting equation. See Applications Information section.) The relationship between V_{FLBK} and V_{BG} may then be expressed as:

$$\alpha \frac{V_{FLBK}}{R_{FB}} = \frac{V_{BG}}{R_{REF}} \text{ or,}$$

$$V_{FLBK} = V_{BG}\left(\frac{R_{FB}}{R_{REF}}\right)\left(\frac{1}{\alpha}\right)$$

α = Ratio of Q1 I_C to I_E
V_{BG} = Internal bandgap reference

Combination with the previous V_{FLBK} expression yields an expression for V_{OUT}, in terms of the internal reference, programming resistors, transformer turns ratio and diode forward voltage drop:

$$V_{OUT} = V_{BG}\left(\frac{R_{FB}}{R_{REF}}\right)\left(\frac{N_{SP}}{\alpha}\right) - V_F - I_{SEC}\,(ESR)$$

Additionally, it includes the effect of nonzero secondary output impedance. See Load Compensation for details. The practical aspects of applying this equation for V_{OUT} are found in the Applications Information section.

So far, this has been a pseudo-DC treatment of flyback error amplifier operation. But the flyback signal is a pulse, not a DC level. Provision must be made to enable the flyback amplifier only when the flyback pulse is present. This is accomplished by the dashed line connections to the block labeled "ENABLE." Timing signals are then required to enable and disable the flyback amplifier.

ERROR AMPLIFIER—DYNAMIC THEORY

There are several timing signals that are required for proper LT1425 operation. Please refer to the Timing Diagram.

Minimum Output Switch ON Time

The LT1425 effects output voltage regulation via flyback pulse action. If the output switch is not turned on at all, there will be no flyback pulse, and output voltage information is no longer available. This would cause irregular loop response and start-up/latchup problems. The solution chosen is to require the output switch to be on for an absolute minimum time per each oscillator cycle. This in turn establishes a minimum load requirement to

OPERATION

maintain regulation. See Applications Information section for further details.

Enable Delay

When the output switch shuts off, the flyback pulse appears. However, it takes a finite time until the transformer primary side voltage waveform approximately represents the output voltage. This is partly due to rise time on the V_{SW} node, but more importantly due to transformer leakage inductance. The latter causes a voltage spike on the primary side not directly related to output voltage. (Some time is also required for internal settling of the feedback amplifier circuitry.)

In order to maintain immunity to these phenomena, a fixed delay is introduced between the switch turn-off command and the enabling of the feedback amplifier. This is termed "enable delay." In certain cases where the leakage spike is not sufficiently settled by the end of the enable delay period, regulation error may result. See Applications Information section for further details.

Collapse Detect

Once the feedback amplifier is enabled, some mechanism is then required to disable it. This is accomplished by a collapse detect comparator, that compares the flyback voltage (R_{REF} referred) to a fixed reference, nominally 80% of V_{BG}. When the flyback waveform drops below this level, the feedback amplifier is disabled. This action accommodates both continuous and discontinuous mode operation.

Minimum Enable Time

The feedback amplifier, once enabled, stays enabled for a fixed minimum time period termed "minimum enable time." This prevents lock-up, especially when the output voltage is abnormally low, e.g., during start-up. The minimum enable time period ensures that the V_C node is able to "pump up" and increase the current mode trip point to the level where the collapse detect system exhibits proper operation. The "minimum enable time" often determines the low load level at which output voltage regulation is lost. See Applications Information section for details.

Effects of Variable Enable Period

It should now be clear that the flyback amplifier is enabled only during a portion of the cycle time. This can vary from the fixed "minimum enable time" described to a maximum of roughly the OFF switch time minus the enable delay time. Certain parameters of flyback amp behavior will then be directly affected by the variable enable period. These include effective transconductance and V_C node slew rate.

Load Compensation Theory

The LT1425 uses the flyback pulse to obtain information about the isolated output voltage. A potential error source is caused by transformer secondary current flow through the real life nonzero impedances of the output rectifier, transformer secondary and output capacitor. This has been represented previously by the expression (I_{SEC} (ESR). However, it is generally more useful to convert this expression to an effective output impedance. Because the secondary current only flows during the off portion of the duty cycle, the effective output impedance equals the lumped secondary impedance times the inverse of the OFF duty cycle. That is,

$$R_{OUT} = ESR\left(\frac{1}{DC\ OFF}\right)$$

where,

R_{OUT} = Effective supply output impedance

ESR = Lumped secondary impedance

DC OFF = OFF duty cycle

Expressing this in terms of the ON duty cycle, remembering DC OFF = 1 – DC,

$$R_{OUT} = ESR\left(\frac{1}{1 - DC}\right)$$

DC = ON duty cycle

In less critical applications, or if output load current remains relatively constant, this output impedance error may be judged acceptable and the external R_{FB} resistor value adjusted to compensate for nominal expected error. In more demanding applications, output

OPERATION

impedance error may be minimized by the use of the load compensation function.

To implement the load compensation function, a voltage is developed that is proportional to average output switch current. This voltage is then impressed across the external R_{OCOMP} resistor and the resulting current is then subtracted from the R_{FB} node. As output loading increases, average switch current increases to maintain rough output voltage regulation. This causes an increase in R_{OCOMP} resistor current subtracted from the R_{FB} node, through which feedback loop action causes a corresponding increase in target output voltage.

Assuming a relatively fixed power supply efficiency, Eff,

Power Out = (Eff)(Power In)

$(V_{OUT})(I_{OUT}) = (Eff)(V_{IN})(I_{IN})$

Average primary side current may be expressed in terms of output current as follows:

$$I_{IN} = \left(\frac{V_{OUT}}{(V_{IN})(Eff)}\right) I_{OUT}$$

Combining the efficiency and voltage terms in a single variable,

$I_{IN} = K1(I_{OUT})$

where,

$$K1 = \left(\frac{V_{OUT}}{(V_{IN})(Eff)}\right)$$

Switch current is converted to voltage by a sense resistor and amplified by the current sense amplifier with associated gain G. This voltage is then impressed across the external R_{OCOMP} resistor to form a current that is subtracted from the R_{FB} node. So the effective change in V_{OUT} target is:

$$\Delta V_{OUT} = K1(\Delta I_{OUT})\left(\frac{(R_{SENSE})(G)}{R_{OCOMP}}\right) R_{FB}$$

Expressing the product of R_{SENSE} and G as the data sheet value of $\Delta V_{RCCOMP}/\Delta I_{SW}$,

$$R_{OUT} = K1\left(\frac{\Delta V_{RCCOMP}}{\Delta I_{SW}}\right)\left(\frac{R_{FB}}{R_{OCOMP}}\right) \text{ and,}$$

$$R_{OCOMP} = K1\left(\frac{\Delta V_{RCCOMP}}{\Delta I_{SW}}\right)\left(\frac{R_{FB}}{R_{OUT}}\right)$$

where,

K1 = Dimensionless variable related to V_{IN}, V_{OUT} and efficiency as above

$\left(\frac{\Delta V_{RCCOMP}}{\Delta I_{SW}}\right)$ = Data sheet value for R_{CCOMP} pin action vs switch current

R_{FB} = External “feedback” resistor value

R_{OUT} = Uncompensated output impedance

$$\frac{\Delta V_{OUT}}{\Delta I_{OUT}} = K1\left(\frac{\Delta V_{RCCOMP}}{\Delta I_{SW}}\right)\left(\frac{R_{FB}}{R_{OCOMP}}\right)$$

Nominal output impedance cancellation is obtained by equating this expression with R_{OUT}. The practical aspects of applying this equation to determine an appropriate value for the R_{OCOMP} resistor are found in the Applications Information section.

APPLICATIONS INFORMATION

SELECTING R_{FB} AND R_{REF} RESISTOR VALUES

The expression for V_{OUT} developed in the Operation section can be rearranged to yield the following expression for R_{FB}:

$$R_{FB} = R_{REF}\left(\frac{V_{OUT} + V_F + I_{SEC}(ESR)}{V_{BG}}\right)\left(\frac{\alpha}{N_{SP}}\right)$$

The unknown parameter α, which represents the fraction of R_{FB} current flowing into the R_{REF} node, can be represented instead by specified data sheet values as follows:

$$(I_{REF})(\alpha)(3k) = V_{BG}$$

$$\alpha = \left(\frac{V_{BG}}{(I_{REF})(3k)}\right)$$

Allowing the expression for R_{FB} to be rewritten as:

$$R_{FB} = R_{REF}\left(\frac{V_{OUT} + V_F + I_{SEC}(ESR)}{I_{REF}(3k)N_{SP}}\right)$$

where,

V_{OUT} = Desired output voltage

V_F = Switching diode forward voltage

$(I_{SEC})(ESR)$ = Secondary resistive losses

I_{REF} = Data sheet reference current value

N_{SP} = Effective secondary-to-primary turns ratio

Strictly speaking, the above equation defines R_{FB} not as an absolute value, but as a ratio of R_{REF}. So the next question is, "What is the proper value for R_{REF}?" The answer is that R_{REF} should be approximately 3k. This is because the LT1425 is trimmed and specified using this value of R_{REF}. If the impedance of R_{REF} varies considerably from 3k, additional errors will result. However, a variation in R_{REF} of several percent or so is perfectly acceptable. This yields a bit of freedom in selecting standard 1% resistor values to yield nominal R_{FB}/R_{REF} ratios.

SELECTING R_{OCOMP} RESISTOR VALUE

The Operation section previously derived the following expressions for R_{OUT}, i.e., effective output impedance and R_{OCOMP}, the external resistor value required for its nominal compensation:

$$R_{OUT} = ESR\left(\frac{1}{1 - DC}\right)$$

$$R_{OCOMP} = K1\left(\frac{\Delta V_{RCCOMP}}{\Delta I_{SW}}\right)\left(\frac{R_{FB}}{R_{OUT}}\right)$$

While the value for R_{OCOMP} may therefore be theoretically determined, it is usually better in practice to employ empirical methods. This is because several of the required input variables are difficult to estimate precisely. For instance, the ESR term above includes that of the transformer secondary, but its effective ESR value depends on high frequency behavior, not simply DC winding resistance. Similarly, K1 appears to be a simple ratio of V_{IN} to V_{OUT} times (differential) efficiency, but theoretically estimating efficiency is not a simple calculation. The suggested empirical method is as follows:

Build a prototype of the desired supply using the eventual secondary components. Temporarily ground the R_{CCOMP} pin to disable the load compensation function. Operate the supply over the expected range of output current loading while measuring the output voltage deviation. Approximate this variation as a single value of R_{OUT} (straight line approximation). Calculate a value for the K1 constant based on V_{IN}, V_{OUT} and the measured (differential) efficiency. They are then combined with the data sheet typical value for $(\Delta V_{RCCOMP}/\Delta I_{SW})$ to yield a value for R_{OCOMP}.

Verify this result by connecting a resistor of roughly this value from the R_{OCOMP} pin to ground. (Disconnect the ground short to R_{CCOMP} and connect the requisite 0.1µF filter capacitor to ground.) Measure the output impedance with the new compensation in place. Modify the original R_{OCOMP} value if necessary to increase or decrease the effective compensation.

Once the proper load compensation resistor has been chosen, it may be necessary to adjust the value of the R_{FB} resistor. This is because the load compensation system exhibits some nonlinearity. In particular, the circuit can shift the reference current by a noticeable

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amount when output switch current is zero. Please refer to Figure 1 which shows nominal reference current shift at zero load for a range of R_{OCOMP} values. Example: for a load compensation resistor of 12k, the graph indicates a 1.0% shift in reference current. The R_{FB} resistor value should be adjusted down by about 1.0% to restore the original target output voltage.

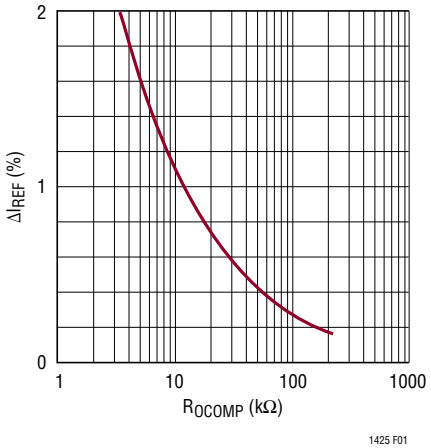

Figure 1.

In less critical applications, or when output current remains relatively constant, the load compensation function may be deemed unnecessary. In such cases, a reduced component solution may be obtained as follows: Leave the R_{OCOMP} node open ($R_{OCOMP} = \infty$), and replace the filter capacitor normally on the R_{CCOMP} node with a short to ground.

TRANSFORMER DESIGN CONSIDERATIONS

Transformer specification and design is perhaps the most critical part of applying the LT1425 successfully. In addition to the usual list of caveats dealing with high frequency isolated power supply transformer design, the following information should prove useful.

Turns Ratio

Note that due to the use of an R_{FB}/R_{REF} resistor ratio to set output voltage, the user has relative freedom in selecting transformer turns ratio to suit a given application. In other words, "screwball" turns ratios like "1.736:1.0" can scrupulously be avoided! In contrast, simpler ratios of small integers, e.g., 1:1, 2:1, 3:2, etc. can be employed which yield more freedom in setting total turns and mutual inductance. Turns ratio can then be chosen on the basis of desired duty cycle. However, remember that the input supply voltage plus the secondary-to-primary referred version of the flyback pulse (including leakage spike) must not exceed the allowed output switch breakdown rating.

Leakage Inductance

Transformer leakage inductance (on either the primary or secondary) causes a spike after output switch turn-off. This is increasingly prominent at higher load currents where more stored energy must be dissipated. In many cases a "snubber" circuit will be required to avoid overvoltage breakdown at the output switch node. ADI's Application Note 19 is a good reference on snubber design.

In situations where the flyback pulse extends beyond the enable delay time, the output voltage regulation will be affected to some degree. It is important to realize that the feedback system has a deliberately limited input range, roughly ±50mV referred to the R_{REF} node, and this works to the user's advantage in rejecting large, i.e., higher voltage leakage spikes. In other words, once a leakage spike is several volts in amplitude, a further increase in amplitude has little effect on the feedback system. So the user is generally advised to arrange the snubber circuit to clamp at as high a voltage as comfortably possible, observing switch breakdown, such that leakage spike duration is as short as possible.

As a rough guide, total leakage inductances of several percent (of mutual inductance) or less may require a snubber, but exhibit little to no regulation error due to leakage spike behavior. Inductances from several percent up to perhaps ten percent cause increasing regulation error.

Severe leakage inductances in the double digit percentage range should be avoided if at all possible as there is a potential for abrupt loss of control at high load current. This curious condition potentially occurs when the leakage spike becomes such a large portion of the flyback waveform that the processing circuitry is fooled into thinking that the leakage spike itself is the real flyback signal! It then reverts to a potentially stable state whereby

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the top of the leakage spike is the control point, and the trailing edge of the leakage spike triggers the collapse detect circuitry. This will typically reduce the output voltage abruptly to a fraction, perhaps between one-third to two-thirds of its correct value. If load current is reduced sufficiently, the system will snap back to normal operation. When using transformers with considerable leakage inductance, it is important to exercise this worst-case check for potential bistability:

1. Operate the prototype supply at maximum expected load current.
2. Temporarily short circuit the output.
3. Observe that normal operation is restored.

If the output voltage is found to hang up at an abnormally low value, the system has a problem. This will usually be evident by simultaneously monitoring the V_{SW} waveform on an oscilloscope to observe leakage spike behavior firsthand. A final note, the susceptibility of the system to bistable behavior is somewhat a function of the load I/V characteristics. A load with resistive, i.e., I = V/R behavior is the most susceptible to bistability. Loads which exhibit "CMOSsy", i.e., $I = V^2/R$ behavior are less susceptible.

Secondary Leakage Inductance

In addition to the previously described effects of leakage inductance in general, leakage inductance on the secondary in particular exhibits an additional phenomenon. It forms an inductive divider on the transformer secondary, that reduces the size of the primary-referred flyback pulse used for feedback. This will increase the output voltage target by a similar percentage. Note that unlike leakage spike behavior, this phenomenon is load independent. To the extent that the secondary leakage inductance is a constant percentage of mutual inductance (over manufacturing variations), this can be accommodated by adjusting the R_{FB}/R_{REF} resistor ratio.

Winding Resistance Effects

Resistance in either the primary or secondary will act to reduce overall efficiency (P_{OUT}/P_{IN}). Resistance in the secondary increases effective output impedance which degrades load regulation (at least before load compensation is employed).

Bifilar Winding

A bifilar or similar winding technique is a good way to minimize troublesome leakage inductances. However, remember that this will increase primary-to-secondary capacitance and limit the primary-to-secondary breakdown voltage, so bifilar winding is not always practical.

Finally, the ADI Applications group is available to assist in the choice and/or design of the transformer. Happy Winding!

Output Voltage Error Sources

Conventional nonisolated switching power supply ICs typically have only two substantial sources of output voltage error—the internal or external resistor divider network that connects to V_{OUT} and the internal IC reference. The LT1425, which senses the output voltage in both a dynamic and an isolated manner, exhibits additional potential error sources to contend with. Some of these errors are proportional to output voltage, others are fixed in an absolute millivolt sense. Here is a list of possible error sources and their effective contribution:

Internal Voltage Reference

The internal bandgap voltage reference is, of course, imperfect. Its error, both at 25°C and over temperature is already included in the specifications for Reference Current.

User Programming Resistors

Output voltage is controlled by the ratio of R_{FB} to R_{REF}. Both are user supplied external resistors. To the extent that the resistor ratio differs from the ideal value, the output voltage will be proportionally affected.

Schottky Diode Drop

The LT1425 senses the output voltage from the transformer primary side during the flyback portion of the cycle. This sensed voltage therefore includes the forward drop, V_F, of the rectifier (usually a Schottky diode). The nominal V_F of this diode should therefore be included

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in R_{FB} calculations. Lot-to-lot and ambient temperature variations will show up as output voltage shift/drift.

Secondary Leakage Inductance

Leakage inductance on the transformer secondary reduces the effective primary-to-secondary turns ratio (NP/NS) from its ideal value. This will increase the output voltage target by a similar percentage. To the extent that secondary leakage inductance is constant from part-to-part, this can be accommodated by adjusting the R_{FB} to R_{REF} resistor ratio.

Output Impedatnce Error

An additional error source is caused by transformer secondary current flow through the real life nonzero impedances of the output rectifier, transformer secondary and output capacitor. Because the secondary current only flows during the off portion of the duty cycle, the effective output impedance equals the "DC" lumped secondary impedance times the inverse of the off duty cycle. If the output load current remains relatively constant, or, in less critical applications, the error may be judged acceptable and the R_{FB} value adjusted for nominal expected error. In more demanding applications, output impedance error may be minimized by the use of the load compensation function (see Load Compensation).

V_{IN} Sense Error

The LT1425 determines the size of the flyback pulse by comparing the V_{SW} signal to V_{IN}, through R_{FB}. This comparison is not perfect, in the sense that an offset exists between the sensing mechanism and the actual V_{IN}. This is expressed in the data sheet as V_{IN} sense error. This error is fixed in absolute millivolt terms relative to V_{OUT} (with the exception that it is reflected to V_{OUT} by any non-unity secondary-to-primary turns ratio).

MINIMUM LOAD CONSIDERATIONS

The LT1425 generally provides better low load performance than previous generation switcher/controllers utilizing indirect output voltage sensing techniques. Specifically, it contains circuitry to detect flyback pulse "collapse," thereby supporting operation well into discontinuous mode. Nevertheless, there still remain constraints to ultimate low load operation. They relate to the minimum switch ON time and the minimum enable time. Discontinuous mode operation will be assumed in the following theoretical derivations.

As outlined in the Operation section, the LT1425 utilizes a minimum output switch ON time, t_{ON}. This value can be combined with expected V_{IN} and switching frequency to yield an expression for minimum delivered power.

$$\text{Min Power} = \left(\frac{1}{2}\right)\left(\frac{f}{L_{PRI}}\right)(V_{IN} \bullet t_{ON})^2$$
$$= (V_{OUT})(I_{OUT})$$

This expression then yields a minimum output current constraint:

$$I_{OUT(MIN)} = \left(\frac{1}{2}\right)\left(\frac{f}{(L_{PRI})(V_{OUT})}\right)(V_{IN} \bullet t_{ON})^2$$

where,

f = Switching frequency (nominally 285kHz)

L_{PRI} = Transformer primary side inductance

V_{IN} = Input voltage

V_{OUT} = Output voltage

t_{ON} = Output switch minimum ON time

An additional constraint has to do with the minimum enable time. The LT1425 derives its output voltage information from the flyback pulse. If the internal minimum enable time pulse extends beyond the flyback pulse, loss of regulation will occur. The onset of this condition can be determined by setting the width of the flyback pulse equal to the sum of the flyback enable delay, t_{ED}, plus the minimum enable time, t_{EN}. Minimum power delivered to the load is then:

$$\text{Min Power} = \left(\frac{1}{2}\right)\left(\frac{f}{L_{SEC}}\right)[V_{OUT} \bullet (t_{EN} + t_{ED})]^2$$
$$= (V_{OUT})(I_{OUT})$$

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which yields a minimum output constraint:

$$I_{OUT(MIN)} = \left(\frac{1}{2}\right)\left(\frac{f(V_{OUT})}{L_{SEC}}\right)(t_{ED} + t_{EN})^2$$

where,

f = Switching frequency (nominally 285kHz)

L_{SEC} = Transformer secondary side inductance

V_{OUT} = Output voltage

t_{ED} = Enable delay time

t_{EN} = Minimum enable time

Note that generally, depending on the particulars of input and output voltages and transformer inductance, one of the above constraints will prove more restrictive. In other words, the minimum load current in a particular application will be either "output switch minimum ON time" constrained, or "minimum flyback pulse time" constrained. (A final note—L_{PRI} and L_{SEC} refer to transformer inductance as seen from the primary or secondary side respectively. This general treatment allows these expressions to be used when the transformer turns ratio is nonunity.)

MAXIMUM LOAD/SHORT-CIRCUIT CONSIDERATIONS

The LT1425 is a current mode controller. It uses the V_C node voltage as an input to a current comparator which turns off the output switch on a cycle-by-cycle basis as this peak current is reached. The internal clamp on the V_C node, nominally 1.9V, then acts as an output switch peak current limit. This action becomes the switch current limit specification. The maximum available output power is then determined by the switch current limit, which is somewhat duty cycle dependent due to internal slope compensation action.

Short-circuit conditions are handled by the same mechanism. The output switch turns on, peak current is quickly reached and the switch is turned off. Because the output switch is only on for a small fraction of the available period, internal power dissipation is controlled. (The LT1425 contains an internal overtemperature shutdown circuit, that disables switch action, just in case.)

While the majority of users will not experience a problem, there is however, a possibility of loss of current limit under certain conditions. Remember that the LT1425 exhibits a minimum switch ON time, irrespective of current trip point. If the duty cycle exhibited by this minimum ON time is greater than the ratio of secondary winding voltage (referred-to-primary) divided by input voltage, then peak current will not be controlled at the nominal value, and will cycle-by-cycle ratchet up to some higher level. Expressed mathematically, the requirement to maintain short-circuit control is:

$$(t_{ON})(f) < \left(\frac{V_F + (I_{SC})(R_{SEC})}{(V_{IN})(N_{SP})}\right)$$

where,

t_{ON} = Output switch minimum ON time

f = Switching frequency

I_{SC} = Short-circuit output current

V_F = Output diode forward voltage at I_{SC}

R_{SEC} = Resistance of transformer secondary

V_{IN} = Input voltage

N_{SP} = Secondary-to-primary turns ratio (N_{SEC}/N_{PRI})

Trouble will typically only be encountered in applications with a relatively high product of input voltage times secondary-to-primary turns ratio. Additionally, several real world effects such as transformer leakage inductance, AC winding losses and output switch voltage drop combine to make this simple theoretical calculation a conservative estimate. In cases where short-circuit protection is mandatory and this theoretical calculation indicates cause for concern, the prototype should be observed directly as follows: short the output while observing the V_{SW} signal with an oscilloscope. The measured output switch ON time can then be compared against the specifications for minimum t_{ON}.

Thermal Considerations

Care should be taken to ensure that the worst-case input voltage and load current conditions do not cause excessive die temperatures. The narrow 16-pin package is rated at 75°C/W.

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Average supply current (including driver current) is:

$$I_{IN} = 7mA + DC\left(\frac{I_{SW}}{35}\right)$$

where,
I_{SW} = Switch current
DC = On switch duty cycle

Switch power dissipation is given by:

$$P_{SW} = (I_{SW})2(R_{SW})(DC)$$

R_{SW} = Output switch ON resistance

Total power dissipation of the die is the sum of supply current times supply voltage plus switch power:

$$P_{D(TOTAL)} = (I_{IN} \bullet V_{IN}) + P_{SW}$$

FREQUENCY COMPENSATION

Loop frequency compensation is performed by connecting a capacitor from the output of the error amplifier (V_C pin) to ground. An additional series resistor, often required in traditional current mode switcher controllers is usually not required, and can even prove detrimental. The phase margin improvement traditionally offered by this extra resistor will usually be already accomplished by the nonzero secondary circuit impedance, which adds a "zero" to the loop response.

In further contrast to traditional current mode switchers, V_C pin ripple is generally not an issue with the LT1425. The dynamic nature of the clamped feedback amplifier forms an effective track/hold type response, whereby the V_C voltage changes during the flyback pulse, but is then "held" during the subsequent "switch ON" portion of the next cycle. This action naturally holds the V_C voltage stable during the current comparator sense action (current mode switching).

PCB LAYOUT CONSIDERATIONS

For maximum efficiency, switch rise and fall times are made as short as practical. To prevent radiation and high frequency resonance problems, proper layout of the components connected to the IC is essential, especially the power paths (primary and secondary). B field (magnetic) radiation is minimized by keeping output diode, switch pin and output bypass capacitor leads as short as possible. E field radiation is kept low by minimizing the length and area of all traces connected to the switch pin. A ground plane should always be used under the switcher circuitry to prevent interplane coupling.

The high speed switching current paths are shown schematically in Figure 2. Minimum lead length in these paths are essential to ensure clean switching and minimal EMI. The path containing the input capacitor, transformer primary, output switch, the path containing the transformer secondary, output diode and output capacitor are the only ones containing nanosecond rise and fall times. Keep these paths as short as possible.

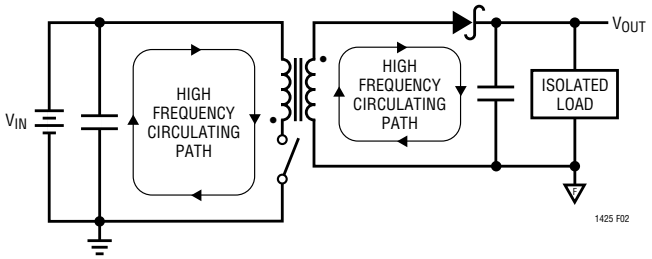


Figure 2.

TYPICAL APPLICATIONS

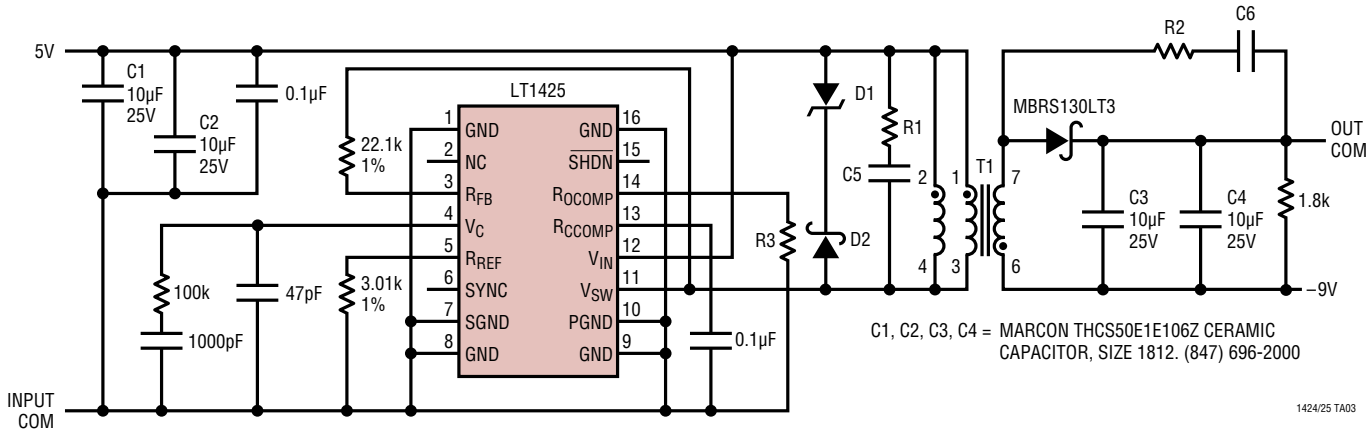
The following are several application examples of the LT1425. The first shows an isolated LAN supply which provides –9V with ±1% load regulation for output currents of 0mA to 250mA. An alternate transformer, the Coiltronics part, provides a complete PCMCIA Type II height solution. The LT1425 offers excellent load regulation and fast dynamic response not found in similar isolated flyback schemes.

The next example shows a ±15V supply with 1.5kV of isolation. The sum of line/load/cross regulation is better than ±3%. Full load efficiency is between 72% (V_{IN} = 5V) and 80% (V_{IN} = 15V). The isolation is ultimately limited only by bobbin selection and transformer construction.

The "–48V to 5V Isolated Telecom Supply" uses an external cascoded 200V MOSFET to extend the LT1425's 35V maximum switch voltage limit. The input voltage range (–36V to –72V) also exceeds the LT1425's 20V maximum input voltage, so a bootstrap winding is used. D1, D2, Q2 and Q3 and associated components for the necessary start-up circuitry with hysteresis. When C1 charges to 15V, switching begins and the bootstrap winding begins to supply power before C1 has a chance to discharge to 11V. Feedback voltage is fed directly through a resistor divider to the R_{REF} pin. The load compensation circuitry is bypassed, resulting in ±5% load regulation.

Finally, the "12V to 5V Isolated Converter" is similar to the previous example in that a cascoded MOSFET is used to prevent voltage breakdown of the output switch. But because the nominal 12V input is well within the range of the V_{IN} pin, no bootstrap winding is required and normal load compensation function is provided. Diode D1, transistor Q1 and associated components provide an undervoltage lockout function via the $\overline{SHDN}$ pin. The off-the-shelf transformer provides up to 5W of isolated regulated power.

–9V Isolated LAN Supply

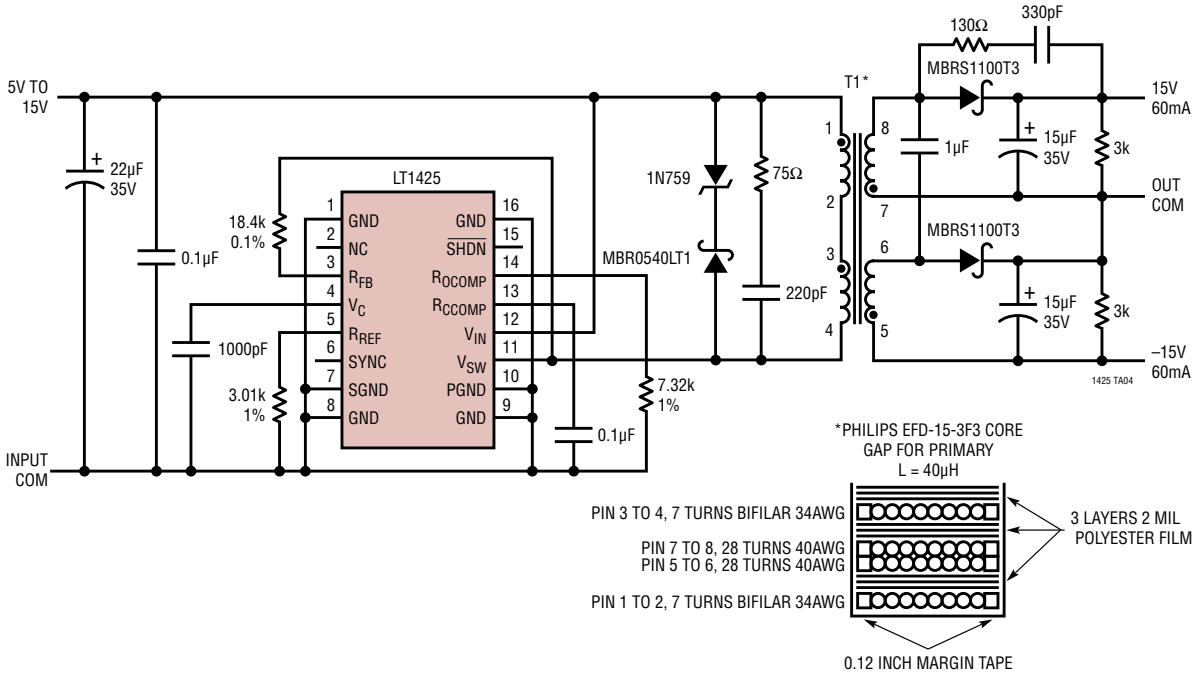


Transformer T1

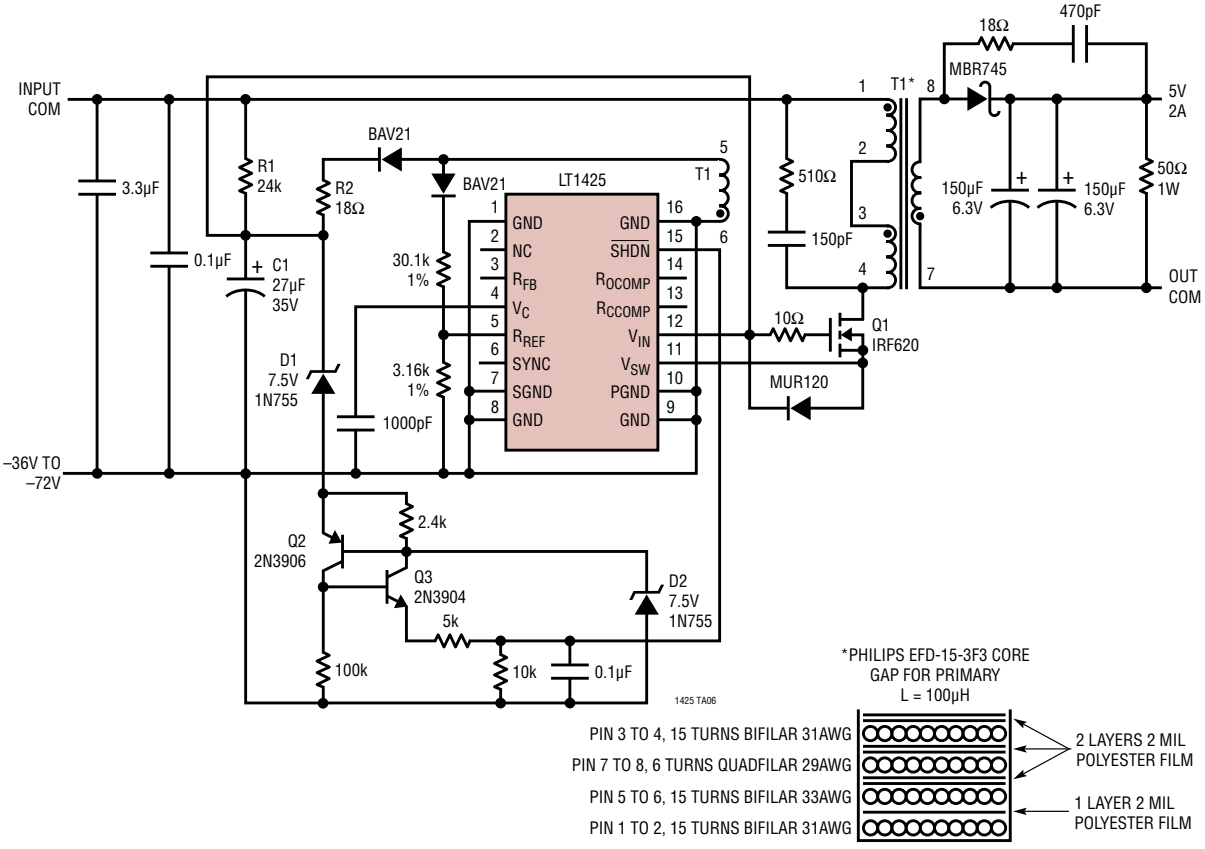
	LPRI	RATIO	ISOLATION	(L × W × H)	I_{OUT}	EFFICIENCY	D1	D2	R1, R2	C5, C6	R3
DALE LPE-4841-A307	36µH	1:1:1	500VAC	10.7 × 11.5 × 6.3mm	250mA	76%	NOT USED	NOT USED	47Ω	330pF	13.3k
COILTRONICS CTX02-13483	27µH	1:1	500VAC	14 × 14 × 2.2mm	200mA	70%	1N5248	MBR0540TL1	75Ω	220pF	5.9k

TYPICAL APPLICATIONS

±15V Isolated Power Supply



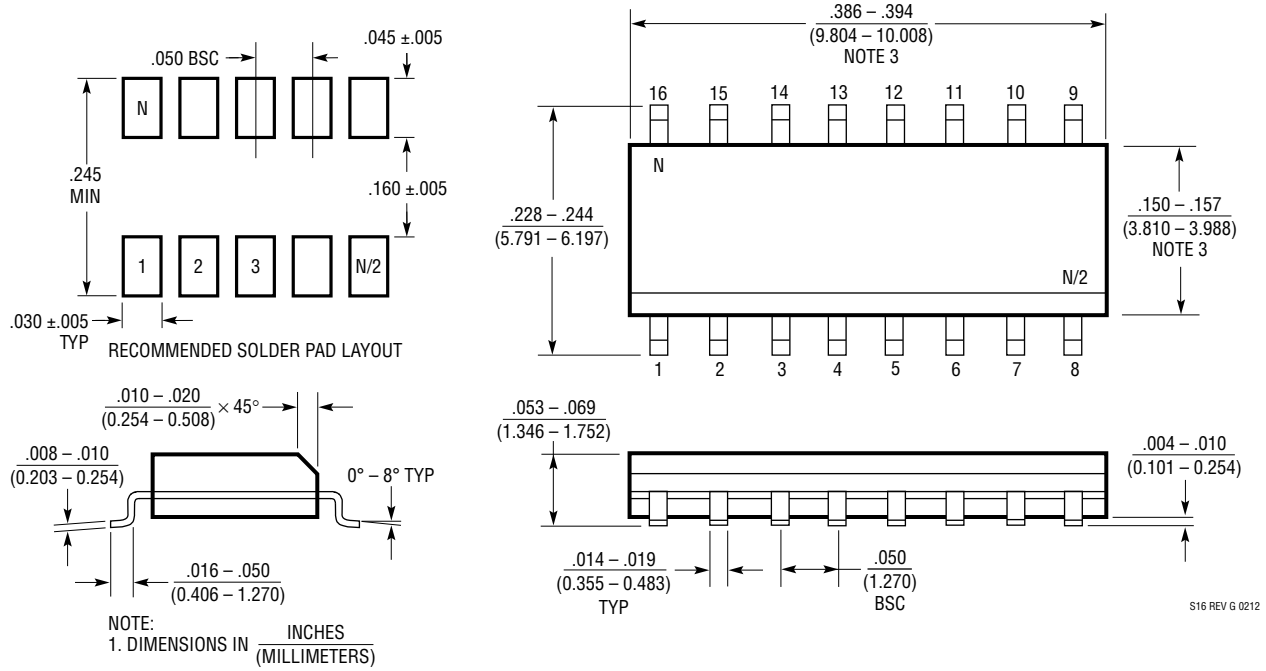
–48V to 5V Isolated Telecom Supply



Rev. B

PACKAGE DESCRIPTION

S Package
16-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)



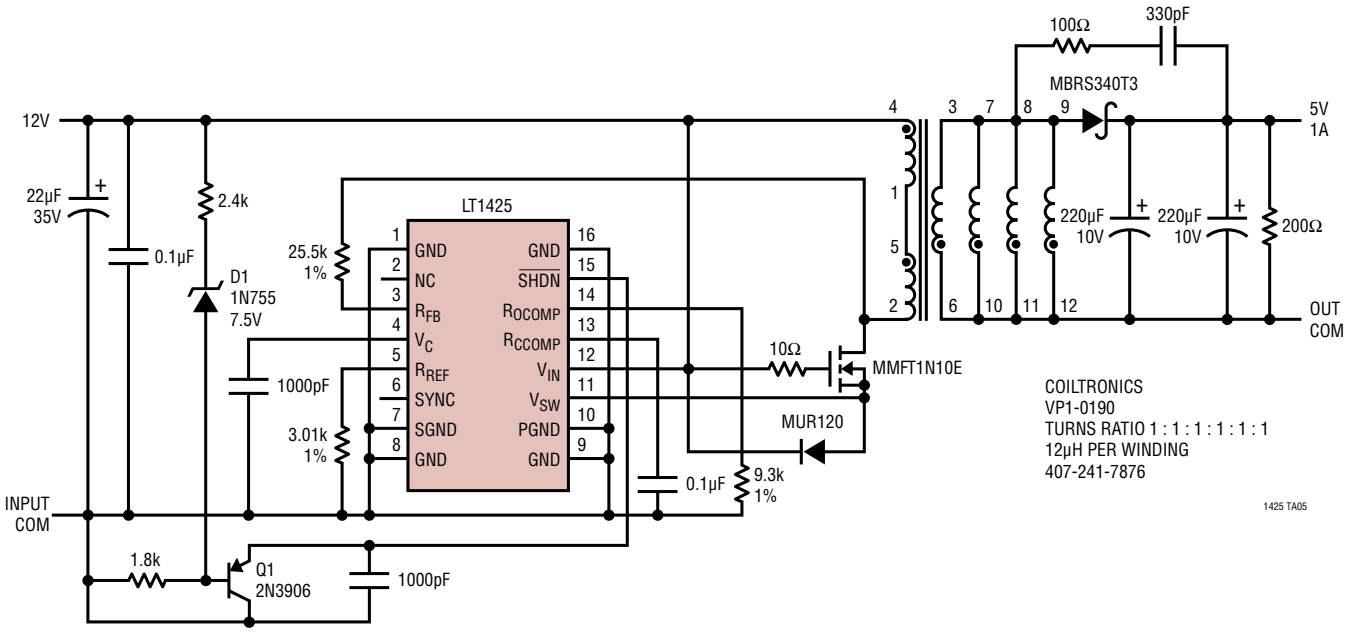
NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	07/21	Changed commercial and industrial Operating Junction Temperature Range Abs Max rating to 125°C.	2
		Changed I_{LIM} conditions and limits.	2
		Changed Maximum Switch Duty Cycle limit to 96%.	2
		Changed I_{CC} Shutdown Mode Threshold limits.	3

TYPICAL APPLICATION

12V to 5V Isolated Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1105	Off-Line Switching Regulator	Built-In Isolated Regulation Without Optoisolator
LT1170/LT1171/LT1172	5A/3A/1.25A Flyback Regulators	Isolated Flyback Mode for Higher Currents
LT1372/LT1377	500kHz/1MHz Boost/Flyback Regulators	Uses Ultrasmall Magnetics
LT1424-5/LT1424-9	Application Specific Isolated Regulator	8-Pin Fixed Voltage Version of LT1425