Application Note 87

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Data Conversion, Interface and Signal Conditioning Products

Richard Markell, Editor

INTRODUCTION

Application Note 87 is the fifth in a series that excerpts useful circuits from Linear Technology magazine to preserve them for posterity. This application note highlights data conversion, interface and signal conditioning circuits from issue VI:1 (February 1996) through issue VIII:4 (November 1998). Like its predecessor, AN67, this Application Note includes circuits for high speed video, interface and hot swap circuits, active RC and switched capacitor filter circuitry and a variety of data conversion and instrumentation circuits. There are also several circuits that cannot be so neatly categorized. So, without further ado, I'll let the authors describe their circuits.

Note: Article Titles appear in this application note exactly as they originally appeared in *Linear Technology* magazine. This may result in some inconsistency in the usage of terminology.

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Data Converters

THE LTC1446 AND LTC1446L: WORLD'S FIRST DUAL 12-BIT DACS IN SO-8 PACKAGES
by Hassan Malik and Jim Brubaker

Dual 12-Bit Rail-to-Rail Performance in a Tiny SO-8

The LTC1446 and LTC1446L are dual 12-bit, single-supply, rail-to-rail voltage output digital-to-analog converters. Both of these parts include an internal reference and two DACs with rail-to-rail output buffer amplifiers, packed in a small, space-saving 8-pin SO or PDIP package. A power-on reset initializes the outputs to zero-scale at power-up.

The LTC1446 has an output swing of 0V to 4.095V, making each LSB equal to 1mV. It operates from a single 4.5V to 5.5V supply, dissipating 3.5mW (I_{CC} typical = 700μA). The LTC1446L has an output swing of 0V to 2.5V. It can operate on a single supply with a wide range of 2.7V to 5.5V. It dissipates 1.35mW (I_{CC} typical = 450μA) at a 3V supply.

An Autoranging 8-Channel ADC with Shutdown

Figure 1 shows how to use an LTC1446 to make an autoranging ADC. The microprocessor sets the reference span and the common pin for the analog input by loading the appropriate digital code into the LTC1446. V_{OUTA} controls the common pin for the analog inputs to the LTC1296 and V_{OUTB} controls the reference span by setting the REF+ pin on the LTC1296. The LTC1296 has a shutdown pin that goes low in shutdown mode. This will turn off the PNP transistor supplying power to the LTC1446. The resistor and capacitor on the LTC1446 outputs act as a lowpass filter for noise.
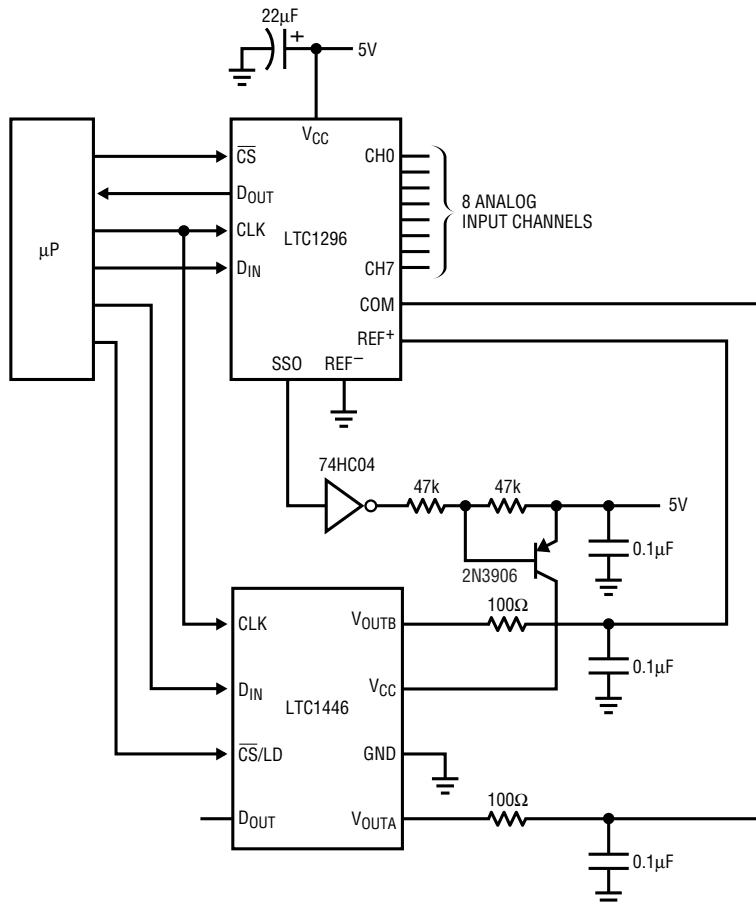
Figure 1. An Autoranging 8-Channel ADC with Shutdown

A Wide-Swing, Bipolar-Output DAC with Digitally Controlled Offset

Figure 2 shows how to use an LTC1446 and an LT1077 to make a wide bipolar-output-swing 12-bit DAC with an offset that can be digitally programmed. V_{OUTA}, which can be set by loading the appropriate digital code for DAC A, sets the offset. As this value changes, the transfer curve for the output moves up and down, as shown in the figure.
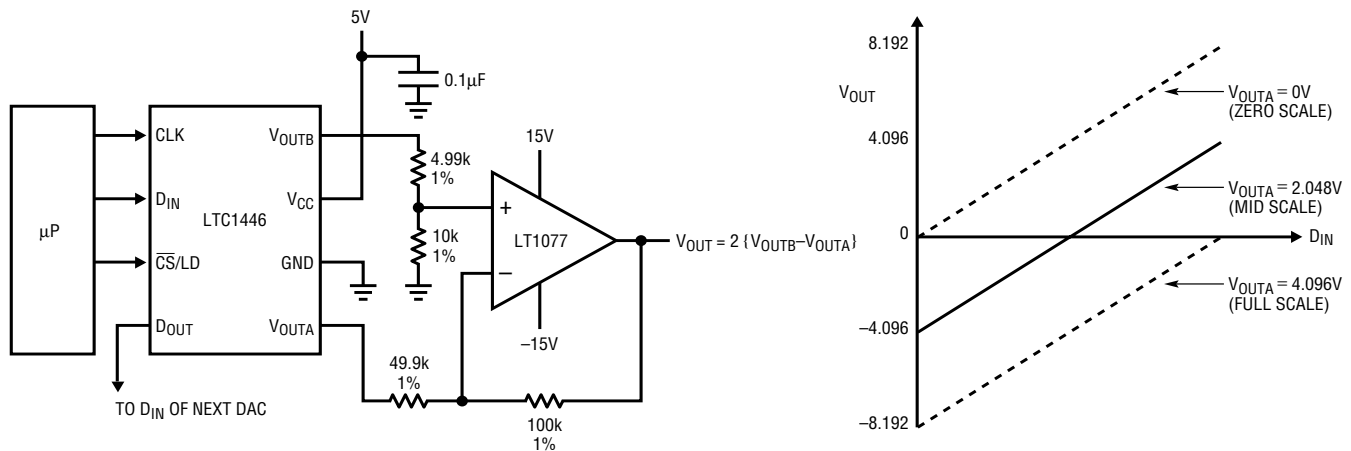
Figure 2. A Wide-Swing, Bipolar Output DAC with Digitally Controlled Offset

MULTICHANNEL A/D USES A SINGLE ANTIALIASING FILTER
by LTC Applications Staff

The circuit in Figure 3 demonstrates how the LTC1594's independent analog multiplexer can simplify the design of a 12-bit data acquisition system. All four channels are MUXed into a single 1kHz, fourth-order Sallen-Key anti-aliasing filter, which is designed for single-supply operation. Since the LTC1594's data converter accepts inputs from ground to the positive supply, rail-to-rail op amps were chosen for the filter to maximize dynamic range. The LT1368 dual rail-to-rail op amp is compensated for the 0.1µF load capacitors (C1 and C2) that help reduce the amplifier's output impedance and improve supply rejection at high frequencies. The filter contributes less than 1LSB of error due to offsets and bias currents. The filter's noise and distortion are less than –72dB for a 100Hz, 2V_{P-P} offset sine input.

The combined MUX and A/D errors result in an integral nonlinearity error of ±3LSB (maximum) and a differential nonlinearity error of ±0.75LSB (maximum). The typical signal-to-noise plus distortion ratio is 68dB, with approximately –78dB of total harmonic distortion. The LTC1594 is programmed through a 4-wire serial interface that allows efficient data transfer to a wide variety of microprocessors and microcontrollers. Maximum serial clock speed is 200kHz, which corresponds to a 10.5kHz sampling rate.

The complete circuit consumes approximately 800µA from a single 5V supply. For ratiometric measurements, the A/D's reference can also be taken from the 5V supply. Otherwise, an external reference should be used.
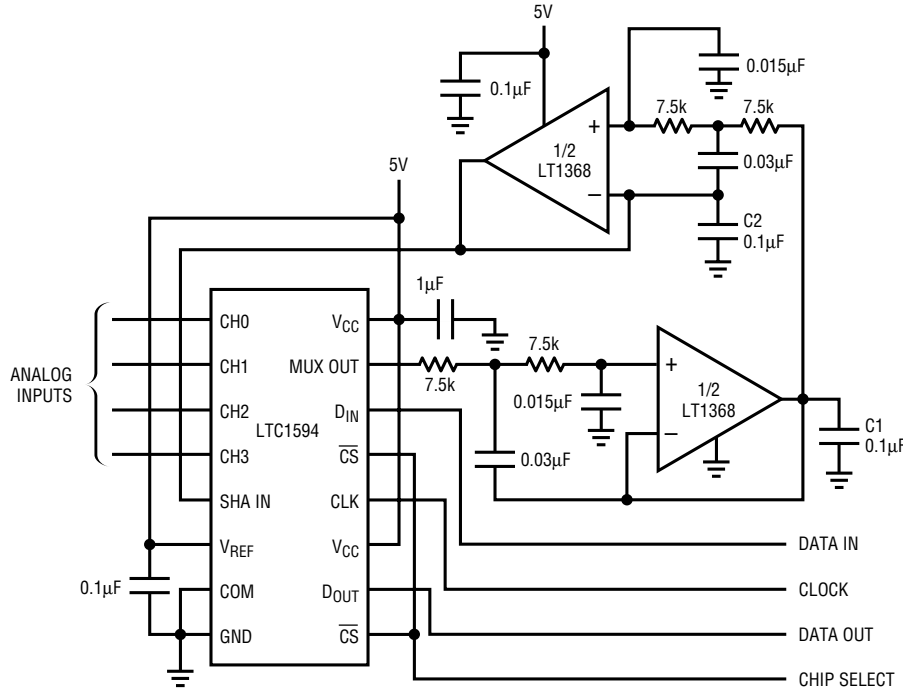
Figure 3. Simple Data Acquisition System Takes Advantage of the LTC1594's MUX OUT/SHA IN Loop to Filter Analog Signals Prior to A/D Conversion

LTC1454/54L AND LTC1458/58L: DUAL AND QUAD 12-BIT, RAIL-TO-RAIL, MICROPOWER DACS
by Hassan Malik and Jim Brubaker

Dual and Quad Rail-to-Rail DACs Offer Flexibility and Performance

The LTC1454 and LTC1454L are dual 12-bit, single supply, rail-to-rail voltage-output digital-to-analog converters. The LTC1458 and LTC1458L are quad versions of this family. These DACs have an easy-to-use, SPI-compatible interface. A CLR pin and power-on-reset both reset the DAC outputs to zero scale. DNL is guaranteed to be less than 0.5LSB. Each DAC has its own rail-to-rail voltage output buffer amplifier. The onboard reference is brought out to a separate pin and can be connected to the REFHI pins of the DACs. There is also a REFLO pin that can be used to offset the DAC range. For further flexibility the ×1/×2 pin for each DAC allows the user to select a gain of either 1 or 2. The LTC1454/54L are available in 16-pin PDIP and SO packages, and the LTC1458/58L are available in 28-pin SO or SSOP packages.

5V and 3V Single Supply and Micropower

The LTC1454 and LTC1458 operate from a single 4.5V to 5.5V supply. The LTC1454 dissipates 3.5mW (I_{CC} typical = 700μA), whereas the LTC1458 dissipates 6.5mW (I_{CC} typical = 1.3mA). There is an onboard reference of 2.048V and a nominal full scale of 4.095V when using the onboard reference and a gain-of-2 configuration.

The LTC1454L and LTC1458L operate on a single supply with a wide range of 2.7V to 5.5V. The LTC1454L dissipates 1.35mW (I_{CC} typical = 450μA), whereas the LTC1458L dissipates 2.4mW (I_{CC} typical = 800μA) from a 3V supply. There is a 1.22V onboard reference and a convenient full scale of 2.5V when using the onboard reference and a gain-of-2 configuration.

Flexibility Allows a Host of Applications

These products can be used in a wide range of applications, including digital calibration, industrial process control, automatic test equipment, cellular telephones and portable, battery-powered systems.

A 12-Bit DAC with Digitally Programmable Full Scale and Offset

Figure 4 shows how to use one LTC1458 to make a 12-bit DAC with a digitally programmable full scale and offset. DAC A and DAC B are used to control the offset and full scale of DAC C. DAC A is connected in a ×1 configuration and controls the offset of DAC C by moving REFLO_C above ground. The minimum value to which this offset can be programmed is 10mV. DAC B is connected in a ×2 configuration and controls the full scale of DAC-C by driving REFHI_C. Note that the voltage at REFHI_C must be less than or equal to $V_{CC}/2$, corresponding to DAC B's code $\leq 2,500$ for $V_{CC} = 5V$, since DAC-C is being operated in ×2 mode for full rail-to-rail output swing.

The transfer characteristic is:

$$V_{OUTC} = 2 \times [D_C \times (2 \times D_B - D_A) + D_A] \times REFOUT$$

where REFOUT = The reference output

D_A = (DAC A digital code)/4096 this sets the offset

D_B = (DAC B digital code)/4096 this sets the full scale

D_C = (DAC C digital code)/4096

A Single-Supply, 4-Quadrant Multiplying DAC

The LTC1454L can also be used for four-quadrant multiplying with an offset signal ground of 1.22V. This application is shown in Figure 5. The inputs are connected to REFHI_B or REFHI_A and have a 1.22V amplitude around a signal ground of 1.22V. The outputs will swing from 0V to 2.44V, as shown by the equation with the figure.

Figure 4. A 12-Bit DAC with Digitally Controlled Zero Scale and Full Scale

$$V_O_{A/B} = (V_{IN} - V_{REF}) \left[GAIN \left(\frac{D_{IN}}{4096} - 1 \right) + 1 \right] + V_{REF}$$

$$= \left(V_{IN} - 1.22 \right) \left(2.05 \frac{D_{IN}}{4096} - 1.05 \right) + 1.22V$$
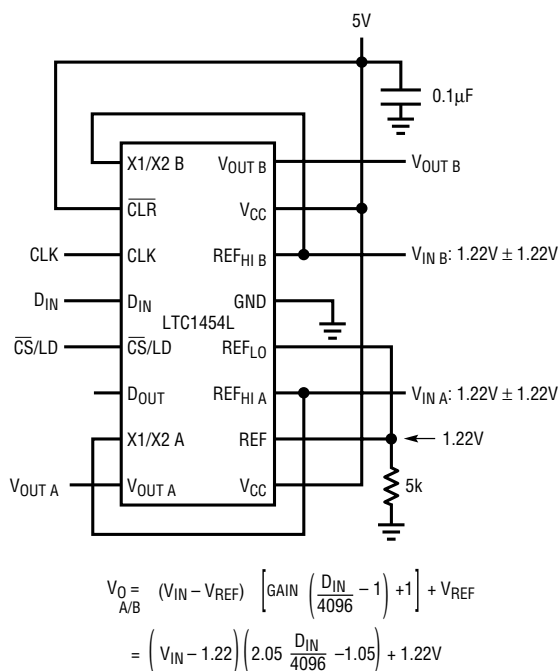
Figure 5. Single-Supply, 4-Quadrant Multiplying DAC

MICROPOWER ADC AND DAC IN SO-8
GIVE PC 12-BIT ANALOG INTERFACE
by LTC Applications Staff

Needing to add two channels of simple, inexpensive, low powered, compact analog input/output to a PC computer, The LTC1298 ADC and LTC1446 DAC were chosen. The LTC1298 and the LTC1446 are the first SO-8 packaged 2-channel devices of their kind. The LTC1298 draws just 340μA. A built-in auto shutdown feature further reduces power dissipation at reduced sampling rates (to 30μA at 1ksps). Operating on a 5V supply, the LTC1446 draws just 1mA (typ). Although the application shown is for PC data acquisition, these two converters provide the smallest, lowest power solutions for many other analog I/O applications.

The circuit shown in Figure 6 connects to a PC's serial interface using four interface lines: DTR, RTS, CTS and TX. DTR is used to transmit the serial clock signal, RTS is used to transfer data to the DAC and ADC, CTS is used to receive conversion results from the LTC1298 and the signal on TX selects either the LTC1446 or the LTC1298 to receive input data. The LTC1298's and LTC1446's low power dissipation allows the circuit to be powered from the serial port. The TX and RTS lines charge capacitor C4 through diodes D3 and D4. An LT1021-5 regulates the voltage to 5V. Returning the TX and RTS lines to a logic high after sending data to the DAC or completion of an ADC conversion provides constant power to the LT1021-5.

Using a 486-33 PC, the throughput was 3.3ksps for the LTC1298 and 2.2ksps for the LTC1446. Your mileage may vary.

Listing 1 is C code that prompts the user to either read a conversion result from the ADC's CH0 or write a data word to both DAC channels.
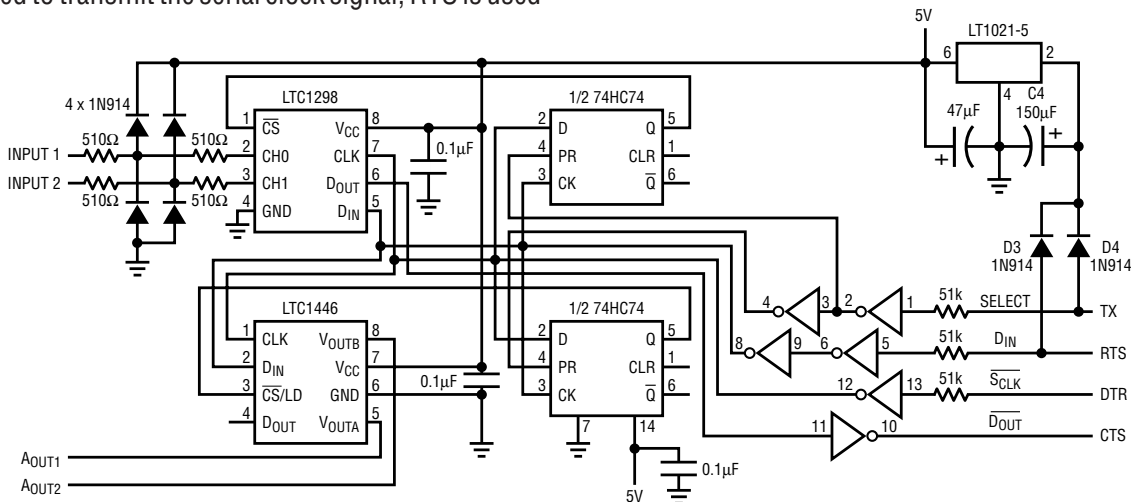
Figure 6. Communicating Over the Serial Port, the LTC1298 and LTC1446 in SO-8 Create a Simple, Low Power, 2-Channel Analog Interface for PCs

Listing 1. C Code to Configure the Analog Interface

```
#define port 0x3FC        /* Control register, RS232 */
#define inprt 0x3FE        /* Status reg. RS232 */
#define LCR  0x3FB         /* Line Control Register */
#define high 1
#define low 0
#define Clock 0x01         /* pin 4, DTR */
#define Din 0x02           /* pin 7, RTS */
```

```
#define Dout 0x10          /* pin 8, CTS input */
#include<stdio.h>
#include<dos.h>
#include<conio.h>
/* Function module sets bit to high or low */
void set_control(int Port,char bitnum,int flag)
{
    char temp;
    temp = inportb(Port);
    if (flag==high)
      temp |= bitnum;           /* set output bit to high */
        else
            temp &= ~bitnum;    /* set output bit to low */
    outportb(Port,temp);
}
            /* This function brings CS high or low (consult the schematic) */
void CS_Control(direction)
{
if (direction)
    {
    set_control(port,Clock,low);        /* set clock high for Din to be read */
    set_control(port,Din,low);          /* set Din low */
set_control(port,Din,low);              /* set Din high to make CS goes high */
    }
    else  {
        outportb(port, 0x01);           /* set Din & clock low */
      Delay(10);
      outportb(port, 0x03);             /* Din goes high to make CS go low */
        }
}
        /* This function outputs a 24-bit (2x12) digital code to LTC1446L */
void Din_(long code,int clock)
{
    int x;
    for(x = 0; x<clock; ++x)
    {
    code <<= 1;                             /* align the Din bit */
    if (code & 0x1000000)
        {
        set_control(port,Clock,high);       /* set Clock low */
        set_control(port,Din,high);         /* set Din bit high */
        }
    else  {
        set_control(port,Clock,high);       /* set Clock low  */
        set_control(port,Din,low);          /* set Din low */
        }
    set_control(port,Clock,low);            /* set Clock high for DAC to latch */
    }
```

```
}
                                                /* Read bit from ADC to PC */
Dout_()
{
int temp, x, volt =0;
for(x = 0; x<13; ++x)
     {
     set_control(port,Clock,high);
     set_control(port,Clock,low);
     temp = inportb(inprt);                /* read status reg. */
     volt <<= 1;                           /* shift left one bit for serial transmission
*/
     if(temp & Dout)
     volt += 1;                            /* add 1 if input bit is high */
     }
return(volt & 0xfff);
}
/* menu for the mode selection */
char menu()
{
printf("Please select one of the following:\na: ADC\nd: DAC\nq: quit\n\n");
return (getchar());
}
void main()
{
long code;
char mode_select;
int temp,volt=0;
  /* Chip select for DAC & ADC is controlled by RS232 pin 3 TX line.  When LCR's bit 6 is set,
              the DAC is selected and the reverse is true for the ADC. */
outportb(LCR,0x0);             /* initialize DAC */
outportb(LCR,0x64);            /* initialize ADC */
while((mode_select = menu()) != 'q')
     {
     switch(mode_select)
          {
          case 'a':
               {
               outportb(LCR,0x0);              /* selecting ADC */
               CS_Control(low);                /* enabling the ADC CS */
               Din_(0x680000, 0x5);            /* channel selection */
               volt = Dout_();
               outportb(LCR,0x64);             /* bring CS high */
               set_control(port,Din,high);     /* bring Din signal high */
               printf("\ncode: %d\n",volt);
               }
          break;
          case 'd':
```

```
                {
                printf("Enter DAC input code (0 – 4095):\n");
                scanf("%d", &temp);
                code = temp;
                code += (long)temp << 12; /* converting 12-bit to 24-bit word */
                outportb(LCR,0x64);          /* selecting DAC */
                CS_Control(low);             /* CS enable */
                Din_(code,24);               /* loading digital data to DAC */
                outportb(LCR,0x0);           /* bring CS high */
                outportb(LCR,0x64);          /* disabling ADC */
                set_control(port,Din,high);  /* bring Din signal high */
                }
        break;
        }
    }
}
```

THE LTC1594 AND LTC1598: MICROPOWER 4- AND 8-CHANNEL 12-BIT ADCS
by Marco Pan

Micropower ADCs in Small Packages

The LTC1594 and LTC1598 are micropower 12-bit ADCs that feature a 4- and 8-channel multiplexer, respectively. The LTC1594 is available in a 16-pin SO package and the LTC1598 is available in a 24-pin SSOP package. Each ADC includes a simple, efficient serial interface that reduces interconnects and, thereby, possible sources of corrupting digital noise. Reduced interconnections also reduce board size and allow the use of processors having fewer I/O pins, both of which help reduce system costs.

The LTC1594 and LTC1598 include an auto shutdown feature that reduces power dissipation when the converter is inactive (whenever the CS signal is a logic high).
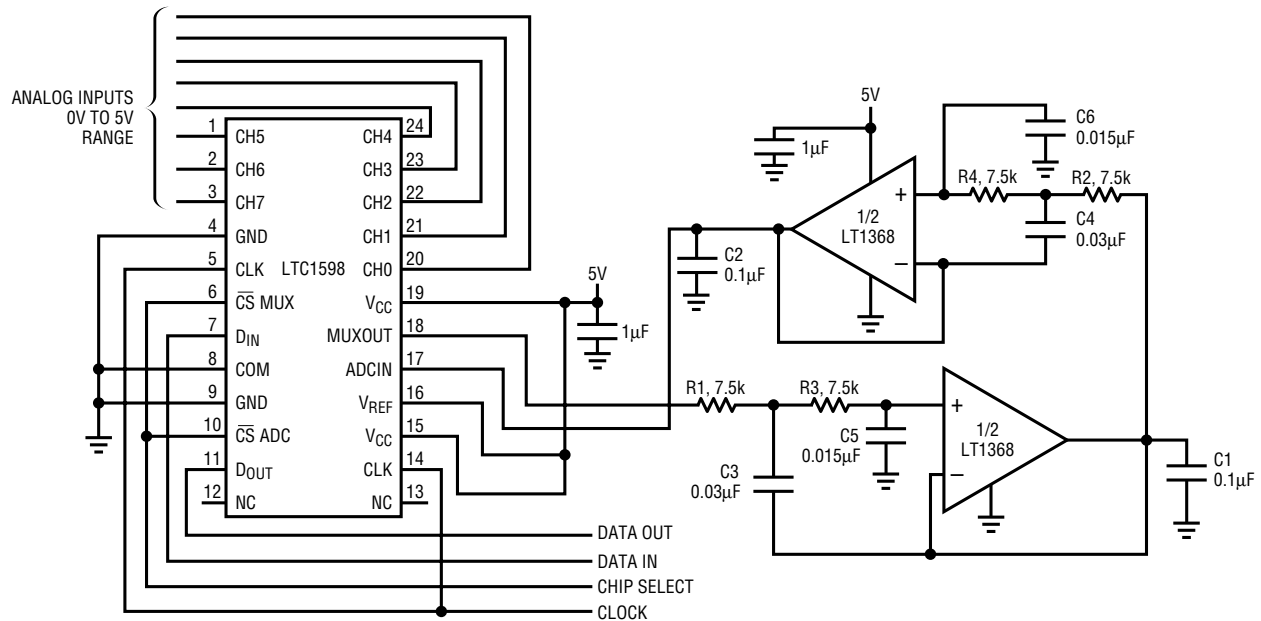

Figure 7. Simple Data Acquisition System Takes Advantage of the LTC1598's MUX OUT/ADCIN Pins to Filter Analog Signals Prior to A/D Conversion
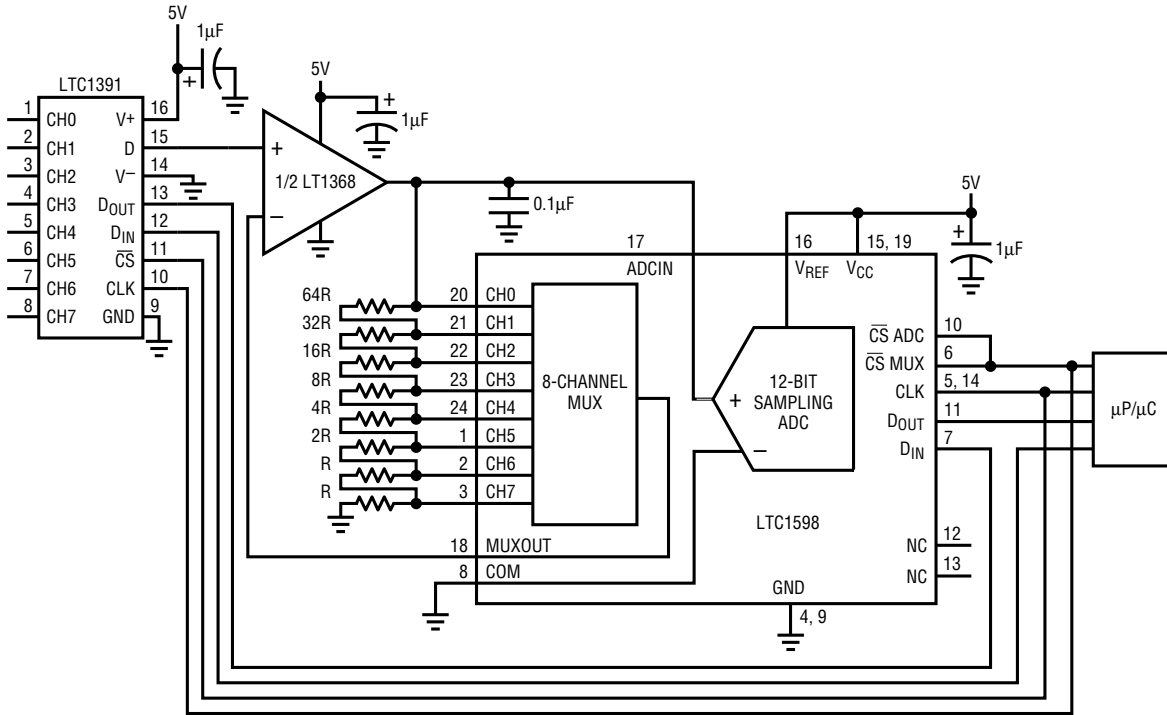
Figure 8. Using the MUXOUT/ADCIN Loop of the LTC1598 to Form a PGA with Eight Gains in a Noninverting Configuration

MUXOUT/ADCIN Loop
Economizes Signal Conditioning

The MUXOUT and ADCIN pins form a very flexible external loop that allows PGA and/or processing analog input signals prior to conversion. This loop is also a cost effective way to perform the conditioning, because only one circuit is needed instead of one for each channel. Figure 7 shows the loop being used to antialias filter several analog inputs. The output signal of the selected MUX channel, present on the MUXOUT pin, is applied to R1 of the Sallen-Key filter. The filter bandlimits the analog

Table 1. PGA Gain for Each MUX Channel of Figures 8 and 9

Mux Channel	Noninverting Gain	Inverting Gain
0	1	−1
1	2	−2
2	4	−4
3	8	−8
4	16	−16
5	32	−32
6	64	−64
7	128	−128

signal and its output is applied to ADCIN. The LT1368 rail-to-rail op amps used in the filter will, when lightly loaded as in this application, swing to within 8mV of the positive supply voltage. Since only one circuit is used for all channels, each channel sees the same filter characteristics.

Using MUXOUT/ADCIN Loop as PGA

Combined with the LTC1391 (as shown in Figure 8) the LTC1598's MUXOUT/ADCIN loop and an LT1368 can be used to create an 8-channel PGA with eight noninverting gains for each channel. The output of the LT1368 drives the ADCIN and the resistor ladder. The resistors above the selected MUX channel form the feedback for the LT1368. The loop gain for this amplifier is $(R_{S1}/R_{S2}) + 1$. R_{S1} is the summation of the resistors above the selected MUX channel and R_{S2} is the summation of the resistors below the selected MUX channel. If CH0 is selected, the loop gain is 1 since R_{S1} is 0. Table 1 shows the gain for each MUX channel. The LT1368 dual rail-to-rail op amp is designed to operate with 0.1μF load capacitors. These capacitors provide frequency compensation for the amplifiers, help reduce the amplifiers' output impedance and improve

supply rejection at high frequencies. Because the LT1368's I_B is low, the R_{ON} of the selected channel will not affect the loop gain given by the formula above. In the case of the inverting configuration of Figure 9, the selected channel's R_{ON} will be added to the resistor that sets the loop gain.

8-Channel, Differential, 12-Bit A/D System Using the LTC1391 and LTC1598

The LTC1598 can be combined with the LTC1391 8-channel, serial-interface analog multiplexer to create a differential A/D system. Figure 10 shows the complete 8-channel, differential A/D circuit. The system uses the LTC1598's MUX as the noninverting input multiplexer and the LTC1391 as inverting input multiplexer. The LTC1598's MUXOUT drives the ADCIN directly. The inverting multiplexer's output is applied to the LTC1598's COM input. The LTC1598 and LTC1391 share the CS, D_{IN}, and CLK control signals. This arrangement simultaneously selects the same channel on each multiplexer and maximizes the system's throughput. The dotted-line connection daisy-chains the MUXes of the LTC1391 and LTC1598 together. This configuration provides the flexibility to select any channel in the noninverting input MUX with respect to any channel in the inverting input MUX. This allows any combination of signals applied to the inverting and noninverting MUX inputs to be routed to the ADC for conversion.
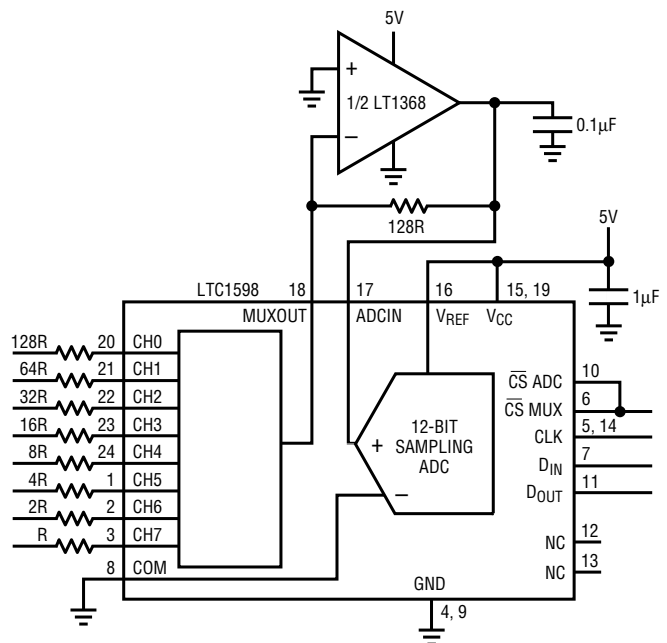

Figure 9. Using the MUXOUT/ADCIN Loop of the LTC1598 to Form a PGA with Eight Inverting Gains
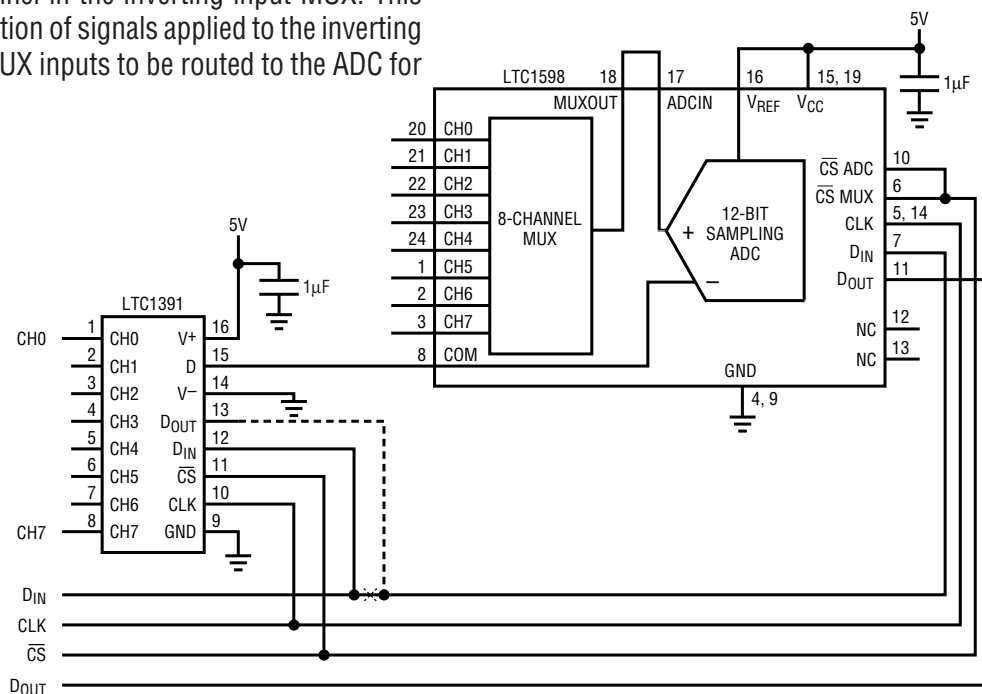

Figure 10. Using the LTC1598 and LTC1391 as an 8-Channel, Differential 12-Bit ADC System: Opening the Indicated Connection and Shorting the Dashed Connection Daisy-Chains the External and Internal MUXes, Increasing Channel-Selection Flexibility.

MUX THE LTC1419 WITHOUT SOFTWARE
by LTC Applications Staff

The circuit shown in Figure 11 uses hardware instead of software routines to select multiplexer channels in a data acquisition system. The circuit features the LTC1419 800ksps 14-bit ADC. It receives and converts signals from a 74HC4051 8-channel multiplexer. Three of the four output bits from an additional circuit, a 74HC4520 dual 4-bit binary counter, are used to select a multiplexer channel. A logic high power-on or processor-generated reset is applied to the counter's pin 7.

After the counter is cleared, the multiplexer's channel selection input is 000 and the input to channel 0 is applied to the LTC1419's S/H input. The channel-selection counter is clocked by the rising edge of the convert start (CONVST) signal that initiates a conversion. As each CONVST pulse increments the counter from 000 to 111, each multiplexer channel is individually selected and its input signal is applied to the LTC1419. After each of the eight channels has been selected, the counter rolls over to zero and the

process repeats. At any time, the input multiplexer channel can be reset to 0 by applying a logic-high pulse to pin 7 of the counter.

This data acquisition circuit has a throughput of 800ksps or 100ksps/channel. As shown in Figure 12, the SINAD is 76.6dB for a full-scale ±2.5V, 1.19kHz sine wave input signal.
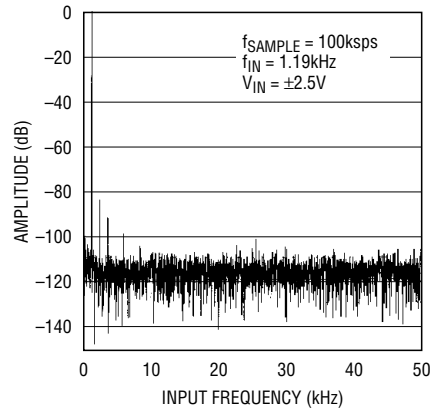

Figure 12. FFT of the MUXed LTC1419's Conversion of a Full-Scale 1.19kHz Sine Wave
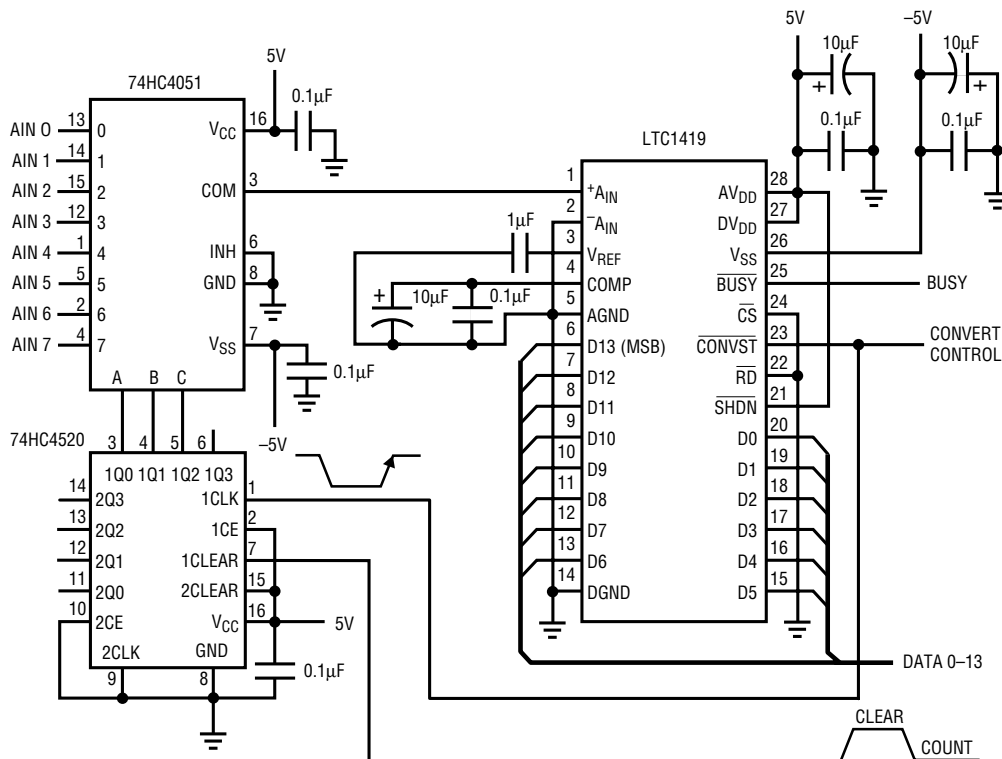

Figure 11. This Simple Stand-Alone Circuit Requires no Software to Sequentially Sample and Convert Eight Analog Signal Channels at 14-bit Resolution and 100ksps/Channel.

THE LTC1590 DUAL 12-BIT DAC IS EXTREMELY VERSATILE
by LTC Applications Staff

CMOS multiplying DACs make versatile building blocks that go beyond their basic function of converting digital data into analog signals. This article details some of the other circuits that are possible when using the LTC1590 dual, serially interfaced 12-bit DAC.

The circuit shown in Figure 13 uses the LTC1590 to create a digitally controlled attenuator using DAC_A and a programmable gain amplifier (PGA) using DAC_B. The attenuator's gain is set using the following equation:

$$V_{OUT} = -V_{IN} \frac{D}{2^n}$$

where V_{OUT} = output voltage
         V_{IN} = input voltage
         n = DAC resolution in bits
         D = value of code applied to DAC
            (min code = 000_H)

The attenuator's gain varies from 4095/4096 to 1/4096. A code of 0 can be used to completely attenuate the input signal.

The PGA's gain is set using the following equation:

$$V_{OUT} = -V_{IN} \frac{2^n}{D}$$

where V_{OUT} = output voltage
         V_{IN} = input voltage
         n = DAC resolution in bits
         D = value of code applied to DAC
            (min code = 001_H)

The gain is adjustable from 4096/4095 to 4096/1. A code of 0 is meaningless, since this results in infinite gain and the amplifier operates open loop. With either configuration, the attenuator's and PGA's gain are set with 12 bits accuracy.

A further modification to the basic attenuator and PGA is shown in Figure 14. In this circuit, DAC_A's attenuator circuit is modified to give the output amplifier a gain set by the ratio of resistors R3 and R4. The equation for this attenuator with output gain is

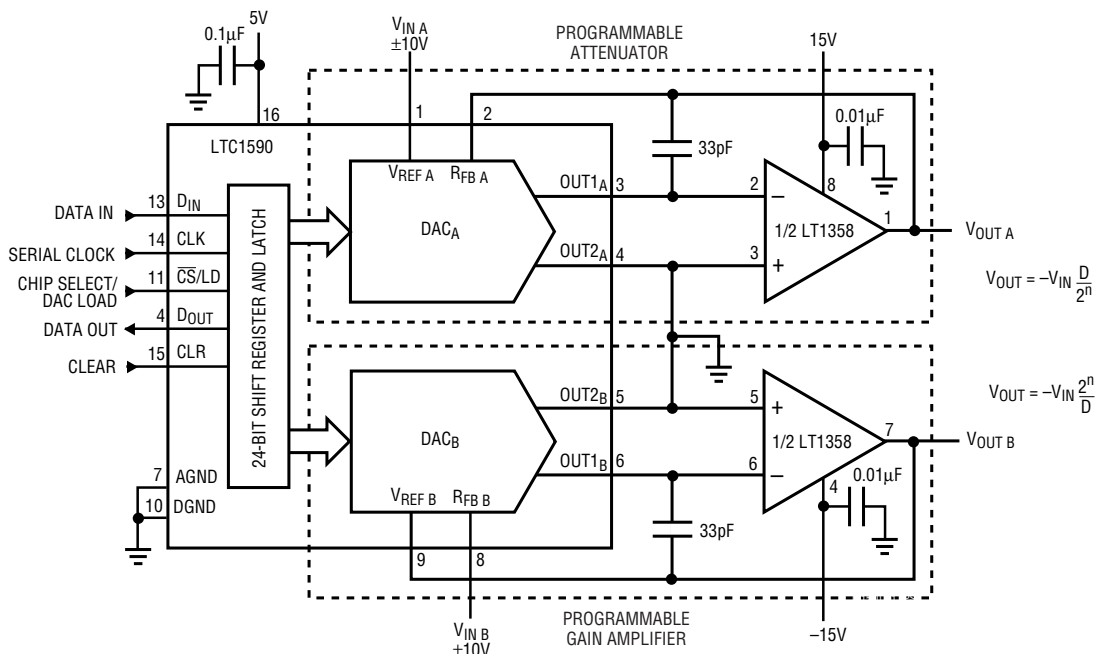$$V_{OUT} = -V_{IN} \frac{16D}{2^n}$$

Figure 13. Driving DAC$_A$'s Reference Input (V$_{REF}$) and Tying the Feedback Resistor (R$_{FB}$) to the Op Amp's Output Creates a 12-Bit- Accurate Attenuator. Reversing the V$_{REF}$ and R$_{FB}$ Connections Configures DAC$_B$ as a Programmable-Gain Amplifier.
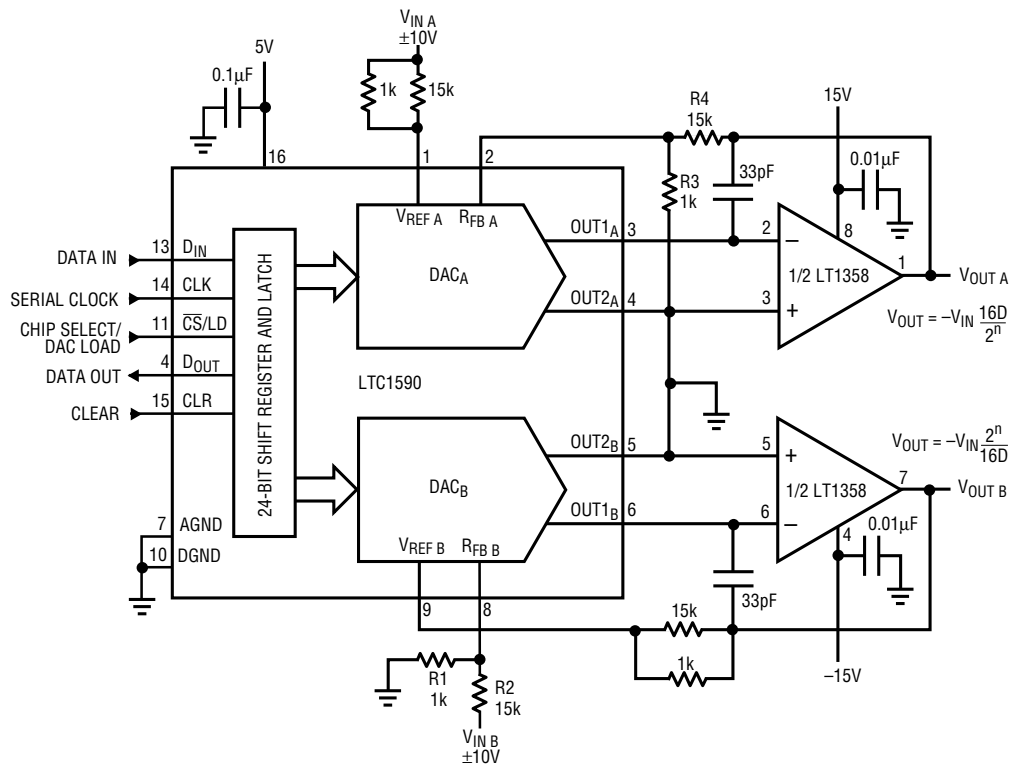
**Figure 14. Modifying the Basic Attenuator and PGA Creates Gain for the
Attenuator (R3 and R4) and Attenuation at the PGA's Input (R1 and R2).**

With the values shown, the attenuator's gain has a range of $-1/256$ to -16. This range is easily modified by changing the ratio of R3 and R4. In the other half of the circuit, an attenuator has been added to the input of DAC_B, configured as a PGA. The equation for this PGA with input attenuation is

$$V_{OUT} = -V_{IN}\frac{2^n}{16D}$$

This sets the gain range from effectively $-1/16$ to -256. Again, this range can be modified by changing the ratio of R1 and R2.

The LTC1590 can also be used as the control element that sets a lowpass filter's cutoff frequency. This is shown in Figure 15. The DAC becomes an adjustable resistor that sets the time constant of the integrator formed by U4 and C_I. With the integrator enclosed within a feedback loop, a lowpass filter is created.

The cutoff frequency range is a function of the DAC's resolution and the digital data that sets the effective resistance. The effective resistance is

$$R_{REF} = R_I \frac{2^n}{D}$$

Using this effective resistance, the cutoff frequency is

$$f_C = \frac{D}{2^{n+1} \bullet \pi \bullet R_I \bullet C_I}$$

The cutoff frequency range varies from 0.0000389/RC to 0.159/RC. As an example, to set the minimum cutoff frequency to 10Hz, make $R_I = 8.25k$ and $C_I = 470pF$. At an input code of 1, the cutoff frequency is 10Hz. The cutoff frequency increases linearly with increasing code, becoming 40.95kHz at a code of 4095. Generally, as the code changes by ±1 bit, the cutoff frequency changes by an amount equal to the frequency at $D = 1$. In this example, the cutoff frequency changes in 10Hz steps.
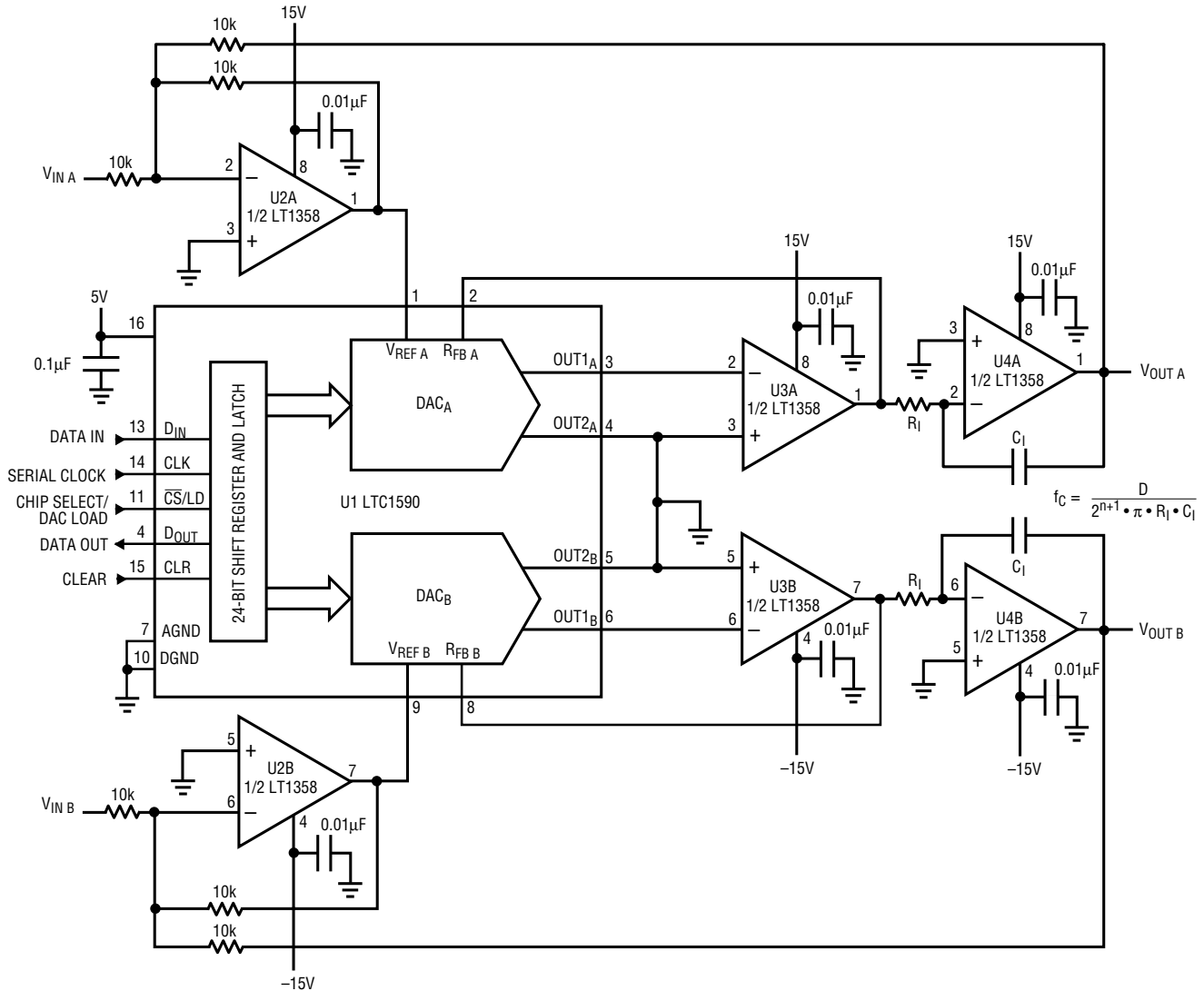
Figure 15. This LTC1590-Controlled Dual Single-Pole Lowpass Filter Uses R_I and the DAC's Input Code to Create an Effective Resistance that Sets the Integrator's Time Constant and, Therefore, the Circuit's Cutoff Frequency.

$$f_C = \frac{D}{2^{n+1} \cdot \pi \cdot R_I \cdot C_I}$$

NEW 16-BIT SO-8 DAC HAS 1LSB MAX INL AND DNL OVER INDUSTRIAL TEMPERATURE

by Jim Brubaker and William C. Rempfer

New generations of industrial systems are moving to 16 bits and hence require high performance 16-bit data converters. The new LTC1595/LTC1596 16-bit DACs provide the easiest to use, most cost effective, highest performance solution for industrial and instrumentation applications. The LTC1595/LTC1596 are serial input, 16-bit, multiplying current output DACs. Features of the new DACs include:

❏ ±1LSB maximum INL and DNL over the industrial temperature range

❏ Ultralow, 1nV-s glitch impulse

❏ ±10V output capability

❏ Small SO-8 package (LTC1595)

❏ Pin-compatible upgrade for industry-standard 12-bit DACs (DAC8043/8143 and AD7543)

0V–10V and ±10V Output Capability

Precision 0V–10V Outputs with One Op Amp

Figure 16 shows the circuit for a 0V–10V output range. The DAC uses an external reference and a single op amp in this configuration. This circuit can also perform 2-quadrant multiplication where the reference input is driven by a ±10V input signal and V_{OUT} swings from 0V to $-V_{REF}$. The full-scale accuracy of the circuit is very precise because it is determined by precision-trimmed internal resistors. The power dissipation of the circuit is set by the op amp dissipation and the current drawn from the DAC reference input (7k nominal). The supply current of the DAC itself is less than 10µA.

An advantage of the LTC1595/LTC1596 is the ability to choose the output op amp to optimize the accuracy, speed, power and cost of the application. Using an LT1001 provides excellent DC precision, low noise and low power dissipation (90mW total for Figure 16's circuit). For higher speed, an LT1007, LT1468 or LT1122 can be used. The LT1122 will provide settling to 1LSB in 3µs for a full-scale transition. Figure 17 shows the 3µs settling performance obtained with the LT1122. The feedback capacitor in Figure 16 ensures stability. In higher speed applications, it can be used to optimize transient response. In slower applications, the capacitor can be increased to reduce glitch energy and provide filtering.
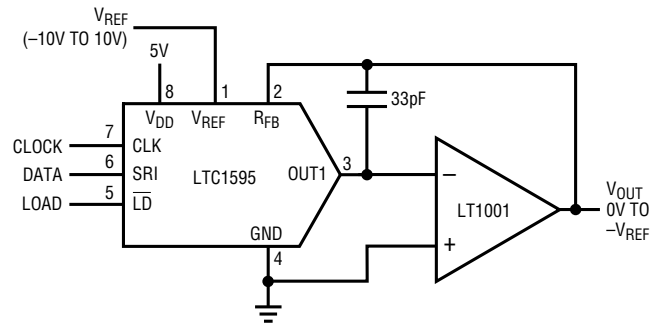
Figure 16. With a Single External Op Amp, the DAC Performs 2-Quadrant Multiplication with ±10V Input and 0V to $-V_{REF}$ Output. With a Fixed –10V Reference, it Provides a Precision 0V–10V Unipolar Output.

Figure 17. When Used with an LT1122 (in the Circuit of Figure 16), the LTC1595/LTC1596 Can Settle in 3µs to a Full-Scale Step. The Top Trace Shows the Output Swinging from 0V to 10V. The Bottom Trace Shows the Gated Settling Waveform Settling to 1LSB (1/3 of a Division) in 3µs.
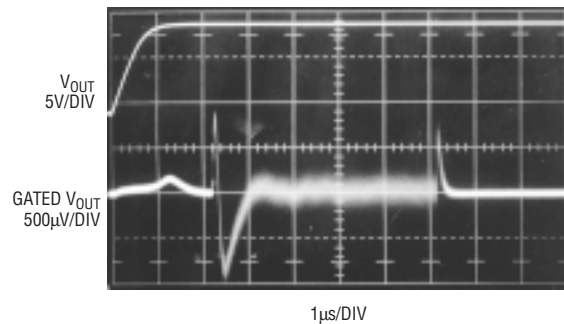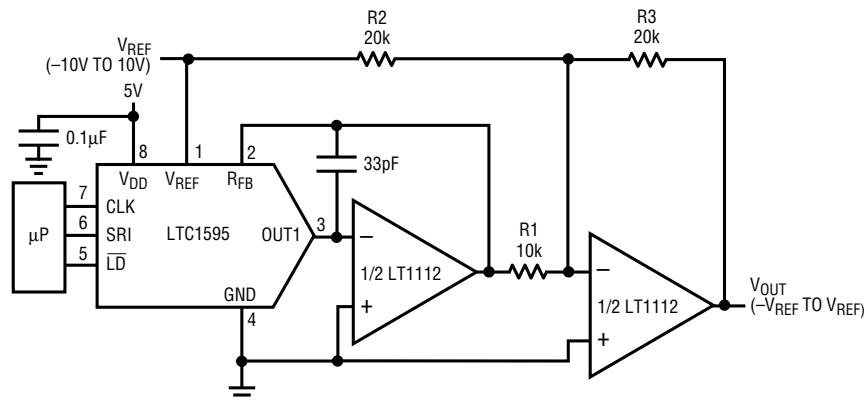

Figure 18. With a Dual Op Amp, the DAC Performs 4-Quadrant Multiplication. With a Fixed 10V Reference, it Provides a ±10V Bipolar Output.

Precision ±10V Outputs with a Dual Op Amp

Figure 18 shows a bipolar, 4-quadrant multiplying application. The reference input can vary from –10V to 10V and V_{OUT} swings from –V_{REF} to +V_{REF}. If a fixed 10V reference is used, a precision ±10V bipolar output will result.

Unlike the unipolar circuit of Figure 16, the bipolar gain and offset will depend on the matching of the external resistors. A good way to provide good matching and save board space is to use a pack of matched 20k resistors (the 10k unit is formed by placing two 20k resistors in parallel).

The LT1112 dual op amp is an excellent choice for high precision, low power applications that do not require high speed. The LT1469 or LT1124 will provide faster settling. Again, with op amp selection the user can optimize the speed, power, accuracy and cost of the application.

LTC1659, LTC1448: SMALLEST RAIL-TO-RAIL 12-BIT DACS HAVE LOWEST POWER
by Hassan Malik

In this age of portable electronics, power and size are the primary concerns of most designers. The LTC1659 and the LTC1448 are rail-to-rail, 12-bit, voltage output DACs that address both of these concerns. The LTC1659 is a single DAC in an MSOP-8 package that draws only 250µA from a 3V or 5V supply, whereas the LTC1448 is a dual DAC in an SO-8 package that draws 450µA from a 3V or 5V supply.

Figure 19 shows a convenient way to use the LTC1659 in a digital control loop where 12-bit resolution is required. The output of the LTC1659 will swing from 0V to V_{REF}, because there is a gain of one from the REF pin to V_{OUT} at full-scale. Because the output can only swing up to V_{CC}, V_{REF} should be less than or equal to V_{CC} to prevent the loss of codes and degradation of PSRR near full-scale.

To obtain full dynamic range, the REF pin can be connected to the supply pin, which can be driven from a reference to guarantee absolute accuracy (see Figure 20). The LT1236 is a precision 5V reference with an input range of 7.2V to 40V. In this configuration, the LTC1659 has a wide output swing of 0V to 5V. The LTC1448 can be used in a similar configuration where dual DACs are needed.
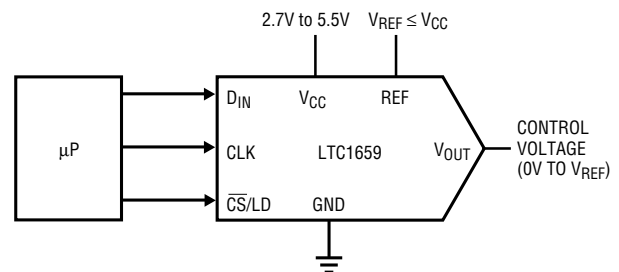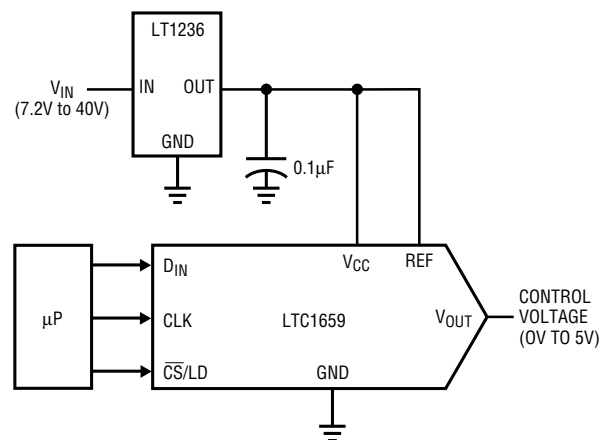

Figure 19. 12-Bit DAC for Digital Control Loop

Figure 20. 12-Bit DAC with Wide Output Swing

AN SMBus-CONTROLLED 10-BIT, CURRENT OUTPUT, 50μA FULL-SCALE DAC
by Ricky Chow

The LTC1427-50 is a 10-bit, current-output DAC with an SMBus interface. This device provides precision, full-scale current of 50μA ±1.5% at room temperature (±2.5% over temperature), wide output voltage DC compliance (from –15V to (V_{CC} – 1.3V)) and guaranteed monotonicity over a wide supply-voltage range. It is an ideal part for applications in contrast/brightness control or voltage adjustment in feedback loops.

Digitally Controlled LCD Bias Generator

Figure 21 is a schematic of a digitally controlled LCD bias generator using a standard SMBus 2-wire interface. The LT1317 is configured as a boost converter, with the output voltage (V_{OUT}) determined by the values of the feedback resistors, R1 and R2. The LTC1427-50's DAC current output is connected to the feedback node of the LT1317. The LTC1427-50's DAC current output increases or decreases according to the data sent via the SMBus. As the DAC output current varies from 0μA to 50μA, the output voltage is controlled over the range of 12.7V to 24V. A 1LSB change in the DAC output current corresponds to an 11mV change in the output voltage.

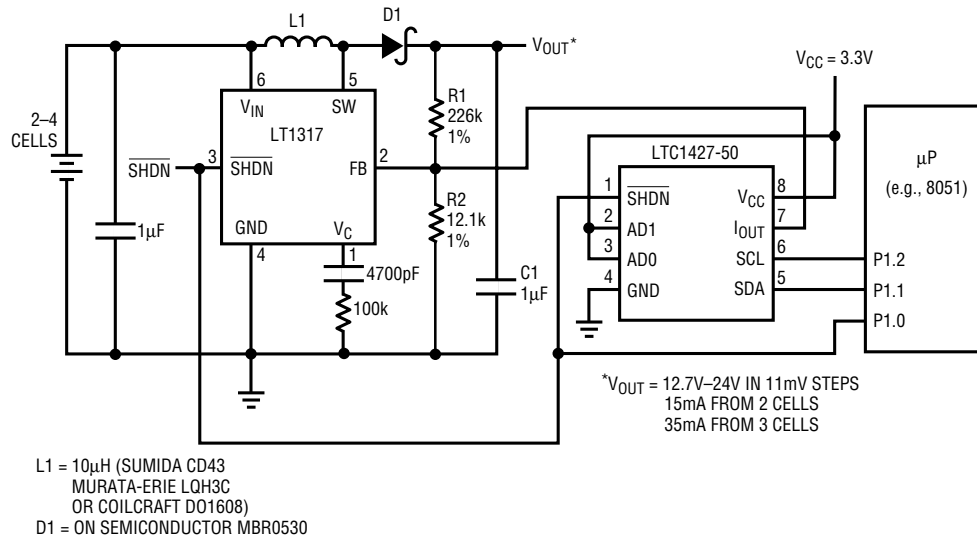L1 = 10μH (SUMIDA CD43
        MURATA-ERIE LQH3C
        OR COILCRAFT DO1608)
D1 = ON SEMICONDUCTOR MBR0530

*V_{OUT} = 12.7V–24V IN 11mV STEPS
        15mA FROM 2 CELLS
        35mA FROM 3 CELLS

Figure 21. Digitally Controlled LCD Bias Generator

Interface Circuits

SIMPLE RESISTIVE SURGE PROTECTION FOR INTERFACE CIRCUITS
by LTC Applications Staff

Surges and Circuits

Many interface circuits must survive surge voltages such as those created by lightning strikes. These high voltages cause the devices within the IC to break down and conduct large currents, causing irreversible damage to the IC. Engineers must design circuits that tolerate the surges expected in their environments. They can quantify the surge tolerance of circuitry by using a surge standard. Standards differ mainly in their voltage levels and wave forms. At LTC, we test surge resistance using the circuit of Figure 22. We describe the voltage wave form (Figure 23) by its peak value V_P, the "front time" T_F (roughly, the rise time), and the "time to half-value" $T_{1/2}$ (roughly, the time from the beginning of the pulse to when the pulse decays to half of V_P). Surges are similar to ESD, but challenge circuits in a different way. A surge may rise to 1kV in 10ms, whereas an ESD pulse might rise to 15kV in only a few ns. However, the surge lasts for more than 100ms, whereas the ESD pulse decays in about 50ns. Thus, the surge challenges the power dissipation ability of the protection circuitry, whereas the ESD challenges the turn-on time and peak current handling. The Linear Technology LT1137A has on-chip circuitry to withstand ESD pulses up to 15kV (IEC 801-2). This circuitry also increases the surge tolerance of the LT1137A relative to a standard 1488/1489.
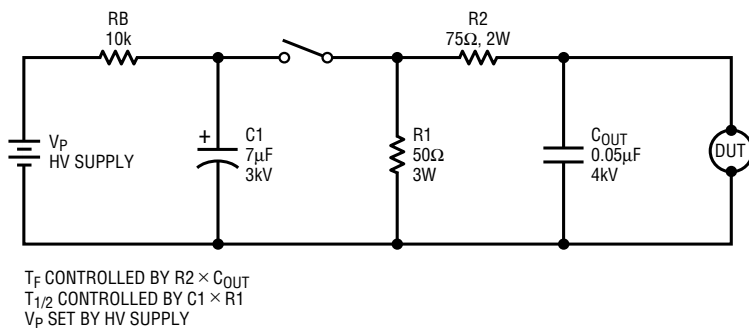

T_F CONTROLLED BY R2 × C_{OUT}
$T_{1/2}$ CONTROLLED BY C1 × R1
V_P SET BY HV SUPPLY

Figure 23. LTC Surge-Test Waveform

Designing for Surge Tolerance

Many designers enhance the surge tolerance of a circuit by placing a transient voltage suppressor (TVS) in parallel with the vulnerable IC pins, as shown in Figure 24. The TVS contains Zener diodes, which break down at a certain voltage and shunt the surge current to ground. Thus, the TVS clamps the voltage at a level safe for the IC. The TVS, like any protection circuitry, increases the manufacturing cost and complexity of the circuit. Alternately, designers can use a series resistor to protect the vulnerable pins, as shown in Figure 25. The resistor reduces the current

T_F CONTROLLED BY R2 × C_{OUT}
$T_{1/2}$ CONTROLLED BY C1 × R1
V_P SET BY HV SUPPLY

Figure 22. LTC Surge-Test Circuit: T_F Controlled by R2 • C_{OUT}; $T_{1/2}$ Controlled by C1 •R1; V_P Set by HV Supply

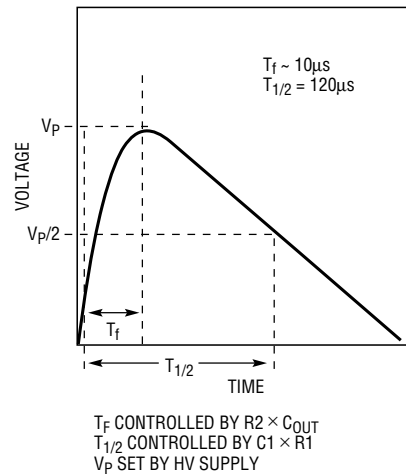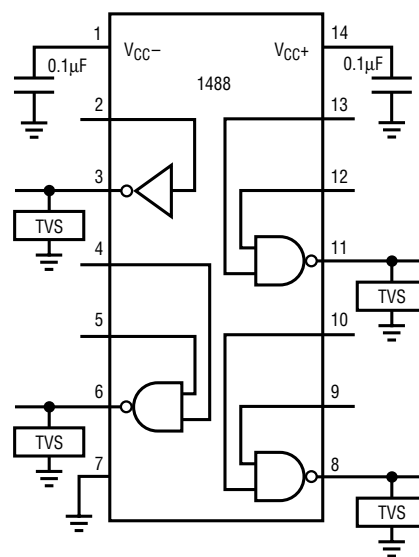**Figure 24. 1488 Line Driver with TVS Surge Protection**
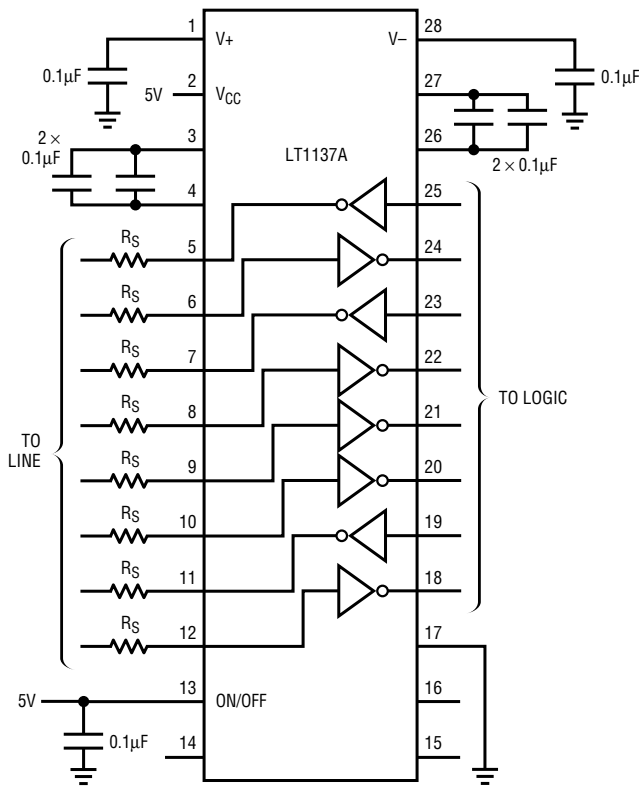
Figure 25. LT1137A with Resistive Surge Protection

flowing into the IC to a safe level. Resistive protection simplifies design and inventory and may offer lower cost. The resistance must be large enough to protect the IC, but not so large that it degrades the frequency performance of the circuit. Larger surge amplitudes require increased resistance to protect the IC. More robust ICs need less
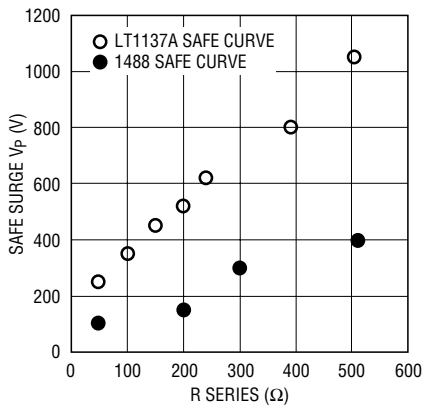
Figure 26. Safe Curves for 1488 (SN75188N) and LT1137A. Safe Curves Represent the Highest V_P for Which No IC Damage Occurred After 10 Surges
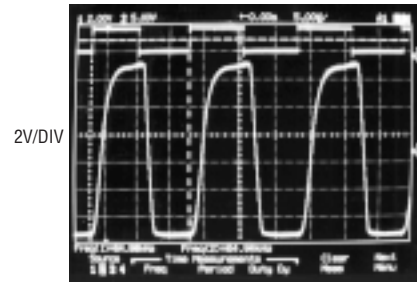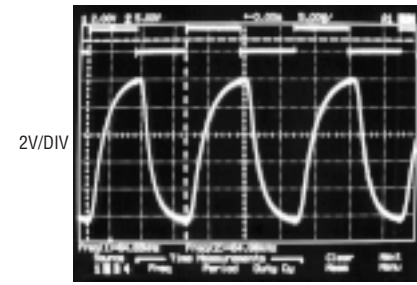
Figure 27. Output Waveforms with Series Resistor

Figure 28. Testing Line Driver Output Waveform

resistance for protection against a given surge amplitude. Linear's LT1137A is protected by a much smaller resistor than a 1488, as shown in Figure 26. These curves are empirical "rules of thumb." You should test actual circuits.

The series resistor may have an adverse effect on the frequency performance of the circuit. When protecting a receiver, the resistor has little effect. Figures 27a and 27b show the effect of a 600Ω resistor on the driver-output wave form. These waveforms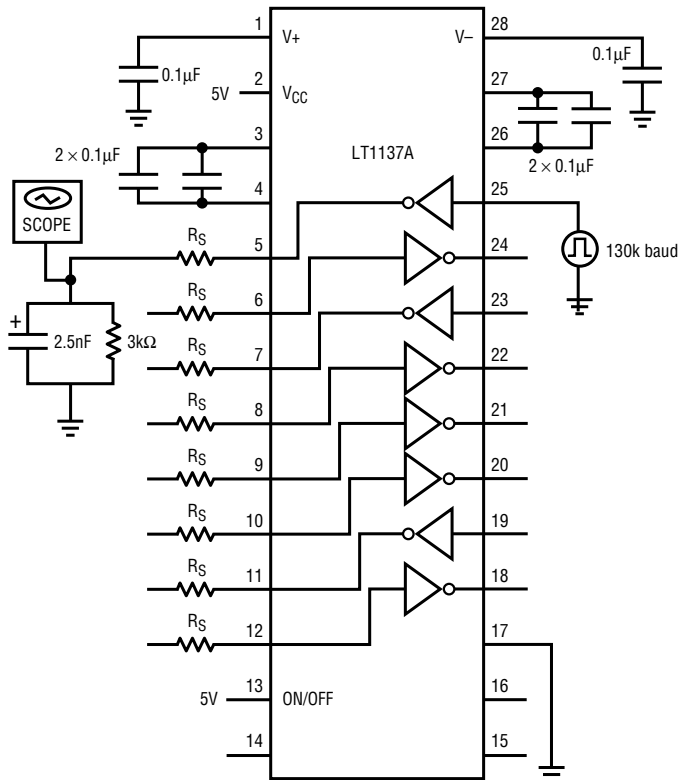 were obtained with the test circuit of Figure 28. A 600Ω resistor is adequate for 1kV surges, but has minimal effect on the driver wave form up to 130kbaud, even with a worst-case load of 3kΩ||2.5nF.

You must choose the series resistor carefully to withstand the surge. Unfortunately, neither voltage ratings nor power ratings provide an adequate basis for choosing surge-tolerant resistors. Usually, through-hole resistors will withstand much larger surges than surface mount resistors of the same value and power rating. Typical 1/8 Watt

surface mount resistors are not suitable for protecting the LT1137A. If you use surface mount components, you may need ratings of 1W or more. With the LT1137A, you can use carbon film 1/4W through-hole resistors against surges up to about 900V, and 1/2W carbon film resistors against surges up to about 1200V. Unfortunately, using series or parallel combinations of resistors *does not* increase the surge handling as one would expect.

Resistive Surge Protection

The LT1137A has proprietary circuitry that makes it more robust against ESD and surges than the standard 1488/1489. The greater surge tolerance of the LT1137A makes it practical to use resistive surge protection, reducing inventory and component cost relative to TVS surge protection. The major considerations are the surge tolerance required, the resulting resistor value needed, resistor robustness and frequency performance.

THE LTC1343 AND LTC1344 FORM A SOFTWARE-SELECTABLE MULTIPLE-PROTOCOL INTERFACE PORT USING A DB-25 CONNECTOR
by Robert Reay

Introduction

With the explosive growth in data networking equipment has come the need to support many different serial protocols using only one connector. The problem facing interface designers is to make the circuitry for each serial protocol share the same connector pins without introducing conflicts. The main source of frustration is that each serial protocol requires a different line termination that is not easily or cheaply switched.

With the introduction of the LTC1343 and LTC1344, a complete software-selectable serial interface port using an inexpensive DB-25 connector becomes possible. The chips form a serial interface port that supports the V.28 (RS232), V.35, V.36, RS449, EIA-530, EIA-530A or X.21 protocols in either DTE or DCE mode and is both NET1 and NET2 compliant. The port runs from a single 5V supply and

supports an echoed clock and loop-back configuration that helps eliminate glue logic between the serial controller and the line transceivers.

A typical application is shown in Figure 29. Two LTC1343s and one LTC1344 form the interface port using a DB-25 connector, shown here in DTE mode.

Each LTC1343 contains four drivers and four receivers and the LTC1344 contains six switchable resistive terminators. The first LTC1343 is connected to the clock and data signal lines along with the diagnostic LL (local loop-back) and TM (test mode) signals. The second LTC1343 is connected to the control-signal lines along with the diagnostic RL (remote loop-back) signal. The single-ended driver and receiver could be separated to support the RI (ring-indicate) signal. The switchable line terminators in the LTC1344 are connected only to the high speed clock and data signals. When the interface protocol is changed via the digital mode selection pins (not shown), the drivers and receivers are automatically reconfigured and the appropriate line terminators are connected.
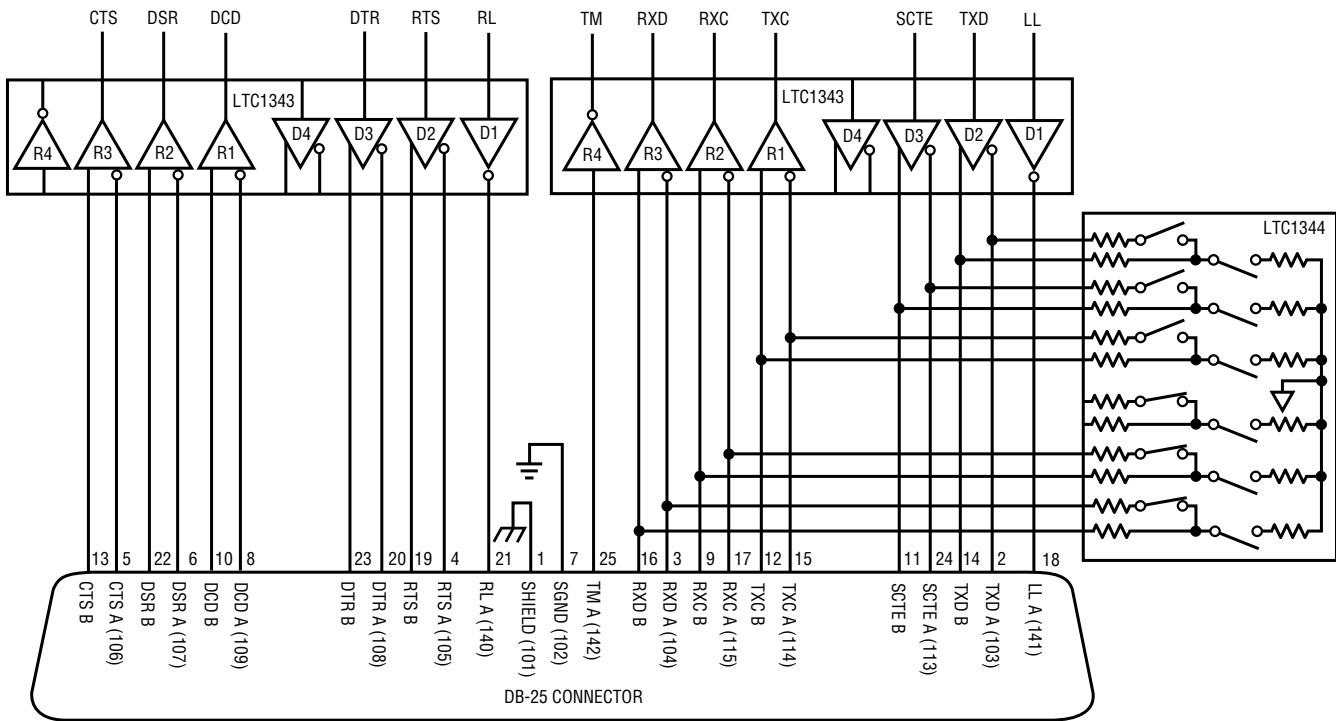
Figure 29. LTC1343/LTC1344 Typical Application

Review of Interface Standards

The serial interface standards RS232, EIA-530, EIA-530A, RS449, V.35, V.36 and X.21 specify the function of each signal line, the electrical characteristics of each signal, the connector type, the transmission rate and the data exchange protocols. The RS422 (V.11) and RS423 (V.10) standards merely define electrical characteristics. The RS232 (V.28) and V.35 standards also specify their own electrical characteristics. In general, the US standards start with RS or EIA, and the equivalent European standards start with V or X. The characteristics of each interface are summarized in Table 2.

Table 2 shows only the most commonly used signal lines. Note that each signal line must conform to only one of four electrical standards, V.10, V.11, V.28 or V.35.

V.10 (RS423) Interface

A typical V.10 unbalanced interface is shown in Figure 30. A V.10 single-ended generator (output A with ground C)

Figure 30. Typical V.10 Interface

Figure 31. V.10 Receiver Configuration

Table 2. Interface Summary

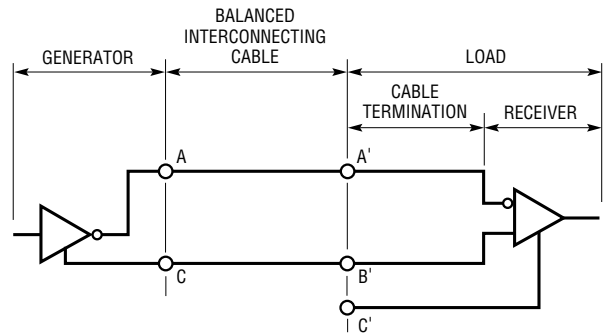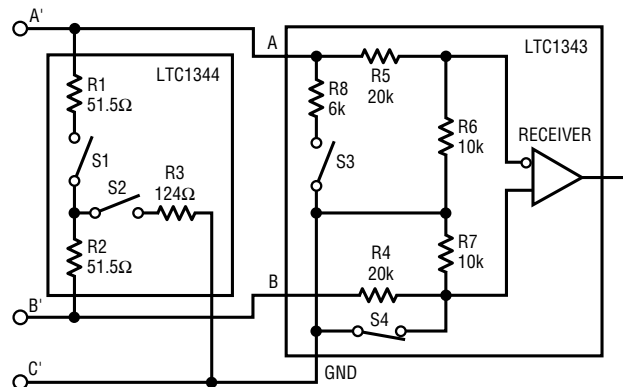|	Clock and Data Signals					Control Signals					Test Signals			
	TXD	SCTE	TXC	RXC	RXD	RTS	DTR	DSR	DCD	CTS	RI	LL	RL	TM
CCITT#	(103)	(113)	(114)	(115)	(104)	(105)	(108)	(107)	(109)	(106)	(125)	(141)	(140)	(142)
RS232	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28
EIA-530	V.11	V.11	V.11	V.11	V.11	V.11	V.11	V.11	V.11	V.11	__	V.10	V.10	V.10
EIA-530A	V.11	V.11	V.11	V.11	V.11	V.11	V.10	V.10	V.11	V.11	V.10	V.10	V.10	V.10
RS449	V.11	V.11	V.11	V.11	V.11	V.11	V.11	V.11	V.11	V.11	V.10	V.10	V.10	V.10
V.35	V.35	V.35	V.35	V.35	V.35	V.28	__	V.28	V.28	V.28	__	__	__	__
V.36	V.11	V.11	V.11	V.11	V.11	V.11	__	V.11	V.11	V.11	__	V.10	V.10	V.10
X.21	V.11	V.11	V.11	V.11	V.11	V.11	__	__	V.11		__	__	__	__	__

is connected to a differential receiver with input A' connected to A and input B' connected to the signal-return ground C. The receiver's ground C' is separate from the signal return. Usually, no cable termination between A' and B' is required for V.10 interfaces. The V.10 receiver configuration for the LTC1343 and LTC1344 is shown in Figure 31.

In V.10 mode, switches S1 and S2 inside the LTC1344 and S3 inside the LTC1343 are turned off. Switch S4 inside the LTC1343 shorts the noninverting receiver input to ground so the B input at the connector can be left floating. The cable termination is then the 30k input impedance to the ground of the LTC1343 V.10 receiver.

V.11 (RS422) Interface

A typical V.11 balanced interface is shown in Figure 32. A V.11 differential generator with outputs A and B and ground C is connected to a differential receiver with ground C', input A' connected to A and input B' connected to B. The V.11 in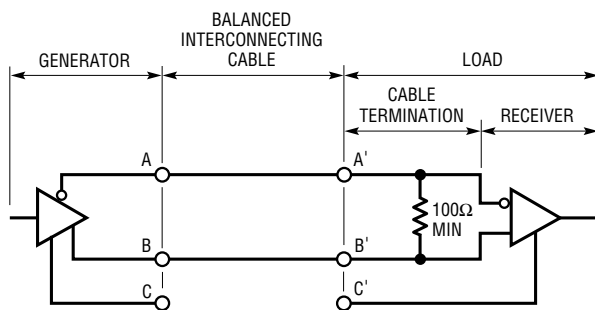terface has a differential termination at the receiver end with a minimum value of 100Ω. The termination resistor is optional in the V.11 specification, but for the high speed clock and data lines, the termination is required to prevent reflections from corrupting the data. In V.11 mode, all switches are off except S1 inside the LTC1344, which connects a 103Ω differential termination impedance to the cable, as shown in Figure 33.

V.28 (RS232) Interface

A typical V.28 unbalanced interface is shown in Figure 34. A V.28 single-ended generator (output A with ground C) is connected to a single-ended receiver with input A' connected to A and ground C' connected via the signal return ground to C. In V.28 mode, all switches are off except S3 inside the LTC1343, which connects a 6k impedance (R8) to ground in parallel with 20k (R5) plus 10k (R6), for an combined impedance of 5k, as shown in Figure 35. The noninverting input is disconnected inside the LTC1343 receiver and connected to a TTL level reference voltage for a 1.4V receiver trip point.
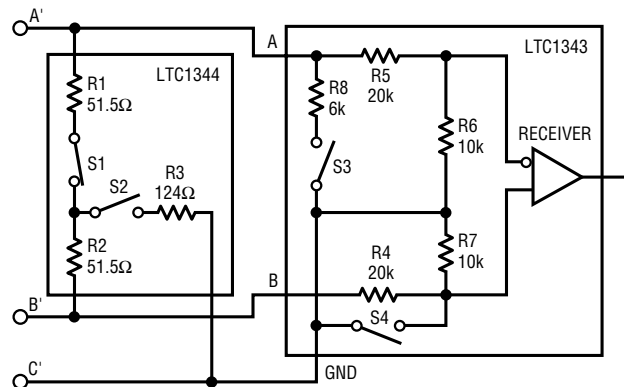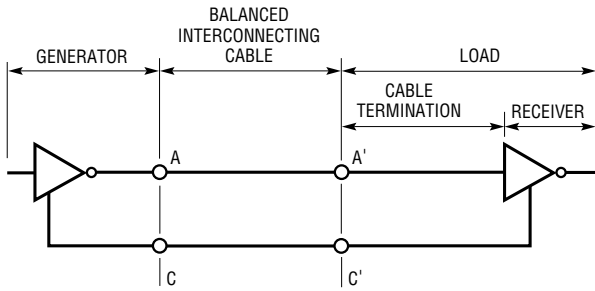

Figure 32. Typical V.11 Interface

Figure 33. V.11 Receiver Configuration
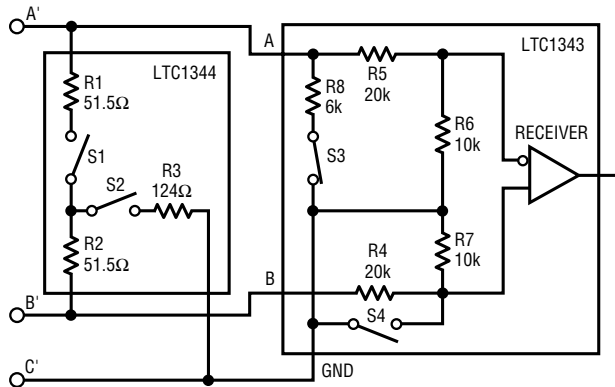
Figure 34. Typical V.28 Interface
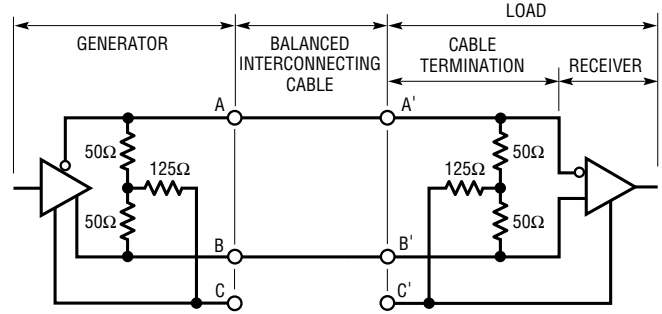
Figure 36. Typical V.35 Interface

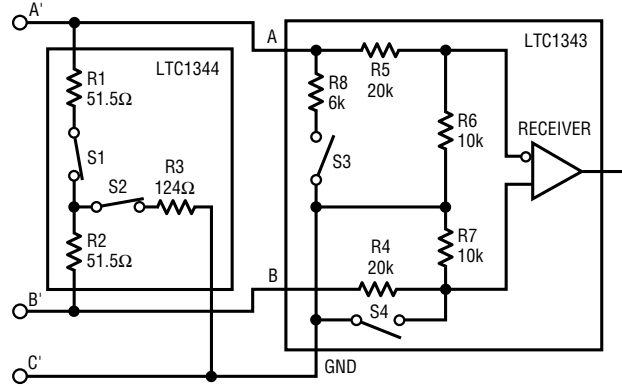Figure 35. V.28 Receiver Configuration

Figure 37. V.35 Receiver Configuration

V.35 Interface

A typical V.35 balanced interface is shown in Figure 36. A V.35 differential generator with outputs A and B and ground C is connected to a differential receiver with ground C', input A' connected to A and input B' connected to B. The V.35 interface requires T or delta network termination at the receiver end and the generator end. The receiver differential impedance measured at the connector must be 100 ±10Ω, and the impedance between shorted terminals (A' and B') and ground (C') is 150 ±15Ω.

In V.35 mode, both switches S1 and S2 inside the LTC1344 are on, connecting the T-network impedance, as shown in Figure 37. Both switches in the LTC1343 are off. The 30k input impedance of the receiver is placed in parallel with the T-network termination, but does not affect the overall input impedance significantly.

The generator differential impedance must be 50Ω to 150Ω, and the impedance between shorted terminals (A and B) and ground (C) is 150Ω ±15Ω. For the generator termination, switches S1 and S2 are both on and the top

side of the center resistor is brought out to a pin so it can be bypassed with an external capacitor to reduce common mode noise, as shown in Figure 38.

Any mismatch in the driver rise and fall times or skew in driver propagation delays will force current through the center termination resistor to ground, causing a high frequency common mode spike on the A and B terminals. This spike can cause EMI problems that are reduced by capacitor C1, which shunts much of the common mode energy to ground rather than down the cable.
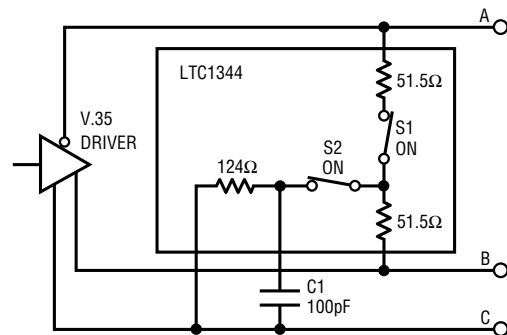
Figure 38. V.35 Driver Using the LTC1344

Table 3. LTC1343/LTC1344 Mode Selection

LTC1343 Mode Name	M2	M1	M0	CTRL/CLK	D1	D 2	D 3	D 4	R1	R 2	R 3	R 4
V.10/RS423	0	0	0	X	V.10	V.10	V.10	V.10	V.10	V.10	V.10	V.10
RS530A clock & data	0	0	1	0	V.10	V.11	V.11	V.11	V.11	V.11	V.11	V.10
RS530A control	0	0	1	1	V.10	V.11	V.10	V.11	V.11	V.10	V.11	V.10
Reserved	0	1	0	X	V.10	V.11	V.11	V.11	V.11	V.11	V.11	V.10
X.21	0	1	1	X	V.10	V.11	V.11	V.11	V.11	V.11	V.11	V.10
V.35 clock & data	1	0	0	0	V.28	V.35	V.35	V.35	V.35	V.35	V.35	V.28
V.35 control	1	0	0	1	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28
RS530/RS449/V.36	1	0	1	X	V.10	V.11	V.11	V.11	V.11	V.11	V.11	V.10
V.28/RS232	1	1	0	X	V.28	V.28	V.28	V.28	V.28	V.28	V.28	V.28
No Cable	1	1	1	X	Z	Z	Z	Z	Z	Z	Z	Z

Figure 39. Mode Selection by Cable

Figure 40. Mode Selection by Controller

LTC1343/LTC1344 Mode Selection

The interface protocol is selected using the mode select pins M0, M1, M2 and CTRL/$\overline{\text{CLK}}$, as summarized in Table 3. The CTRL/$\ove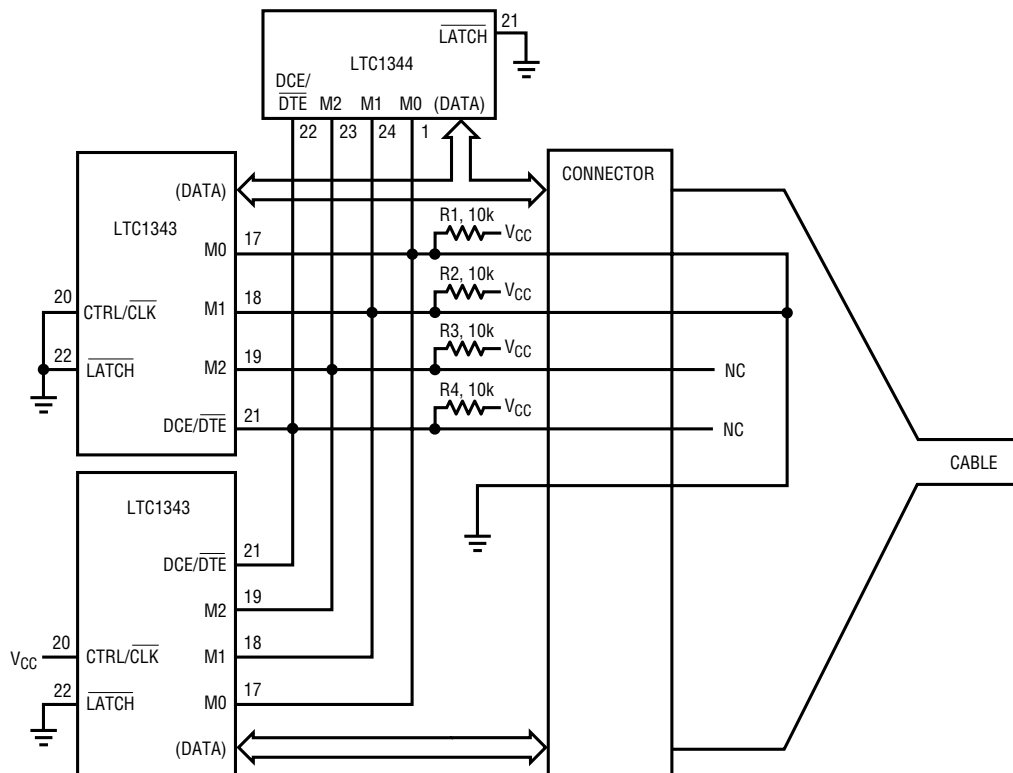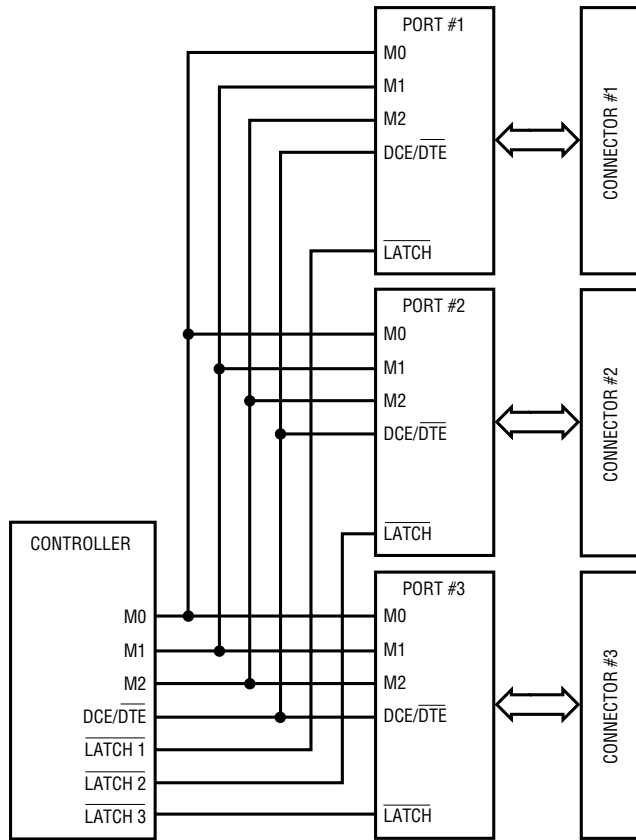rline{\text{CLK}}$ pin should be pulled high if the LTC1343 is being used to generate control signals and pulled low if used to generate clock and data signals.

For example, if the port is configured as a V.35 interface, the mode selection pins should be M2 = 1, M1 = 0, M0 = 0. For the control signals, CTRL/$\overline{\text{CLK}}$ = 1 and the drivers and receivers will operate in RS232 (V.28) electrical mode. For the clock and data signals, CTRL/$\overline{\text{CLK}}$ = 0 and the drivers and receivers will operate in V.35 electrical mode, except for the single-ended driver and receiver, which will operate in the RS232 (V.28) electrical mode. The DCE/$\overline{\text{DTE}}$ pin will configure the port for DCE mode when high, and DTE when low.

The interface protocol may be selected by simply plugging the appropriate interface cable into the connector. The mode pins are routed to the connector and are left unconnected (1) or wired to ground (0) in the cable, as shown in Figure 39.

The pull-up resistors R1–R4 ensure a binary 1 when a pin is left unconnected and also ensure that the two LTC1343s and the LTC1344 enter the no-cable mode when the cable is removed. In the no-cable mode, the LTC1343 power supply current drops to less than 200µA and all LTC1343 driver outputs and LTC1344 resistive terminators are forced into a high impedance state. Note that the data latch pin, $\overline{\text{LATCH}}$, is shorted to ground for all chips.

The interface protocol may also be selected by the serial controller or host microprocessor, as shown in Figure 40.

The mode selection pins M0, M1, M2 and DCE/$\overline{\text{DTE}}$ can be shared among multiple interface ports, while each port has a unique data-latch signal that acts as a write enable. When the $\overline{\text{LATCH}}$ pin is low, the buffers on the M0, M1, M2, CTRL/$\overline{\text{CLK}}$, DCE/$\overline{\text{DTE}}$, LB and $\overline{\text{EC}}$ pins are transparent. When the $\overline{\text{LATCH}}$ pin is pulled high, the buffers latch the data, and changes on the input pins will no longer affect the chip.

The mode selection may also be accomplished by using jumpers to connect the mode pins to ground or V_{CC}.

Loop-Back

The LTC1343 contains logic for placing the interface into a loop-back configuration for testing. Both DTE and DCE loop-back configurations are supported. Figure 41 shows a complete DTE interface in the loop-back configuration and Figure 42 the DCE loop-back configuration. The loop-back configuration is selected by pulling the LB pin low.

Enabling the Single-Ended Driver and Receiver

When the LTC1343 is being used to generate the control signals (CTRL/$\overline{\text{CLK}}$ = high) and the $\overline{\text{EC}}$ pin is pulled low, the DCE/$\overline{\text{DTE}}$ pin becomes an enable for driver 1 and receiver 4 so their inputs and outputs can be tied together, as shown in Figure 43.
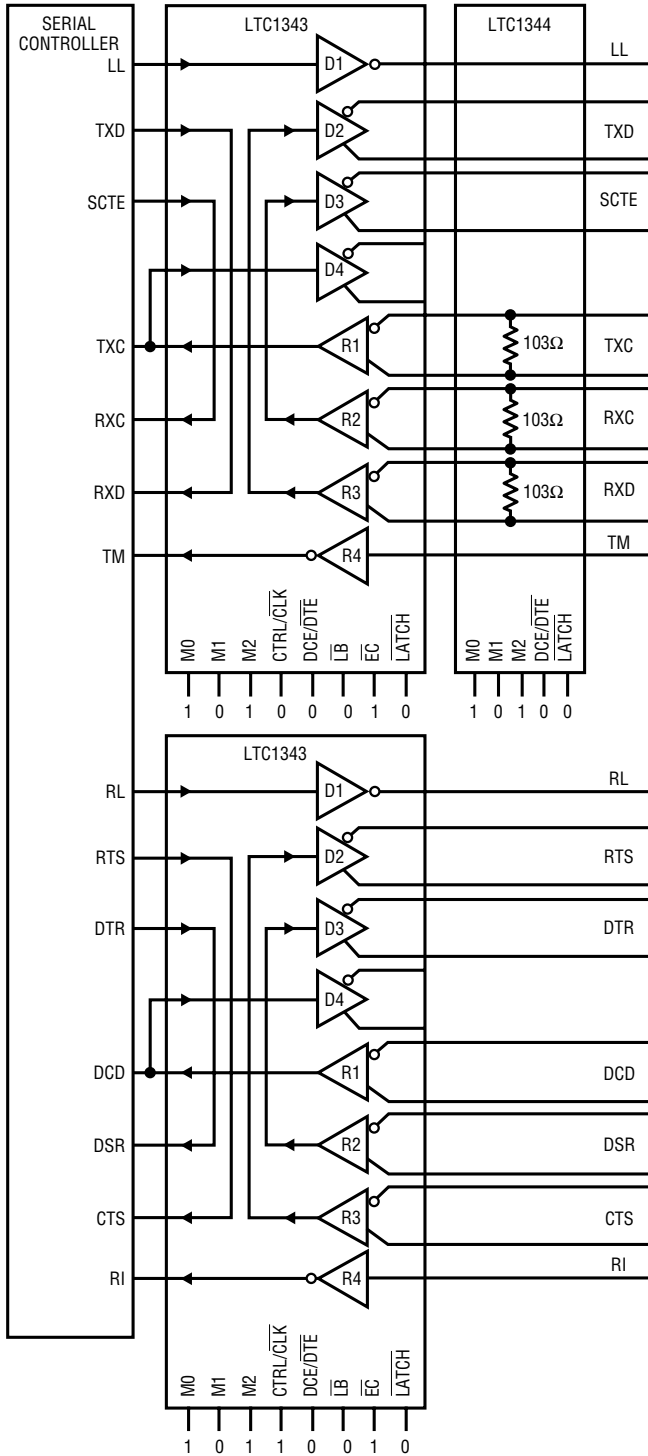
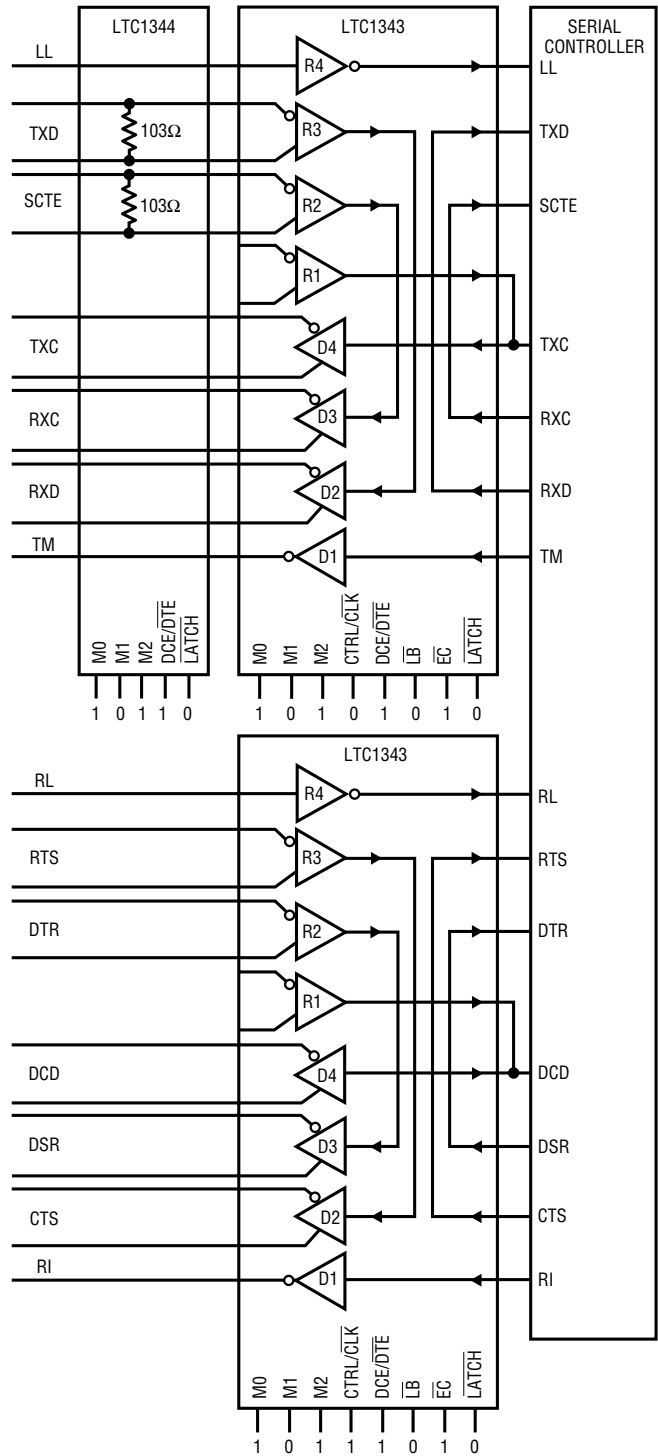**Figure 41. Normal DTE Loop-Back**

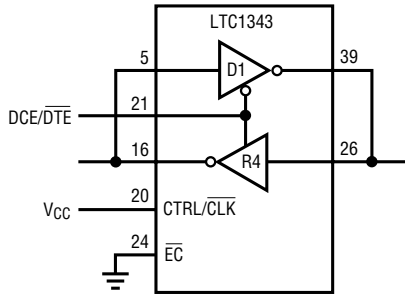

Figure 42. Normal DCE Loop-Back

Figure 43. Single-Ended Driver and Receiver Enable

The EC pin has no affect on the configuration when CTRL/CLK is high except to allow the DCE/DTE pin to become an enable. When DCE/DTE is low, the driver 1 output is enabled. The receiver 4 output goes into three-state, and the input presents a 30k load to ground.

When DCE/DTE is high, the driver 1 output goes into three-state, and the receiver 4 output is enabled. The receiver 4 input presents a 30k load to ground in all modes except when configured for RS232 operation, when the input impedance is 5k to ground.

Multiprotocol Interface with DB-25 or μDB-26 Connectors

A multiprotocol serial interface with a standard DB-25 connector EIA-530 pin configuration is shown in Figure 44. (Figures 44–47 follow on pp. 30–33). The signal lines must be reversed in the cable when switching between DTE and DCE using the same connector. For example, in DTE mode, the RXD signal is routed to receiver 3, but in DCE mode, the TXD signal is routed to receiver 3. The interface mode is selected by logic outputs from the controller or from jumpers to either V_{CC} or GND on the mode-select pins. The single-ended driver 1 and receiver

4 of the control chip share the RL signal on connector pin 21. With EC low and CTRL/CLK high, the DCE/DTE pin becomes an enable signal.

Single-ended receiver 4 can be connected to pin 22 to implement the RI (ring indicate) signal in RS232 mode (see Figure 45). In all other modes, pin 22 carries the DSR(B) signal.

A cable selectable multiprotocol interface is shown in Figure 46. Control signals LL, RL and TM are not implemented. The V_{CC} supply and select lines M0 and M1 are brought out to the connector. The mode is selected in the cable by wiring M0 (connector pin 18) and M1 (connector pin 21) and DCE/DTE (connector pin 25) to ground (connector pin 7) or letting them float. If M0, M1 or DCE/DTE are floating, pull-up resistors R3, R4 and R5 will pull the signals to V_{CC}. The select bit M1 is hard wired to V_{CC}. When the cable is pulled out, the interface goes into the no-cable mode.

A cable-selectable multiprotocol interface found in many popular data routers is shown in Figure 47. The entire interface, including the LL signal, can be implemented using the tiny μDB-26 connector.

Conclusion

The LTC1343 and LTC1344 allow the designer of a multiprotocol serial interface to spend all of his time on the software rather than the hardware. Simply drop the chips down on the board, hook them up to the connector and a serial controller, apply the 5V supply voltage and you're off and running. In addition, the chip set's small size and unique termination topology allow many ports to be placed on a board using inexpensive connectors and cables.
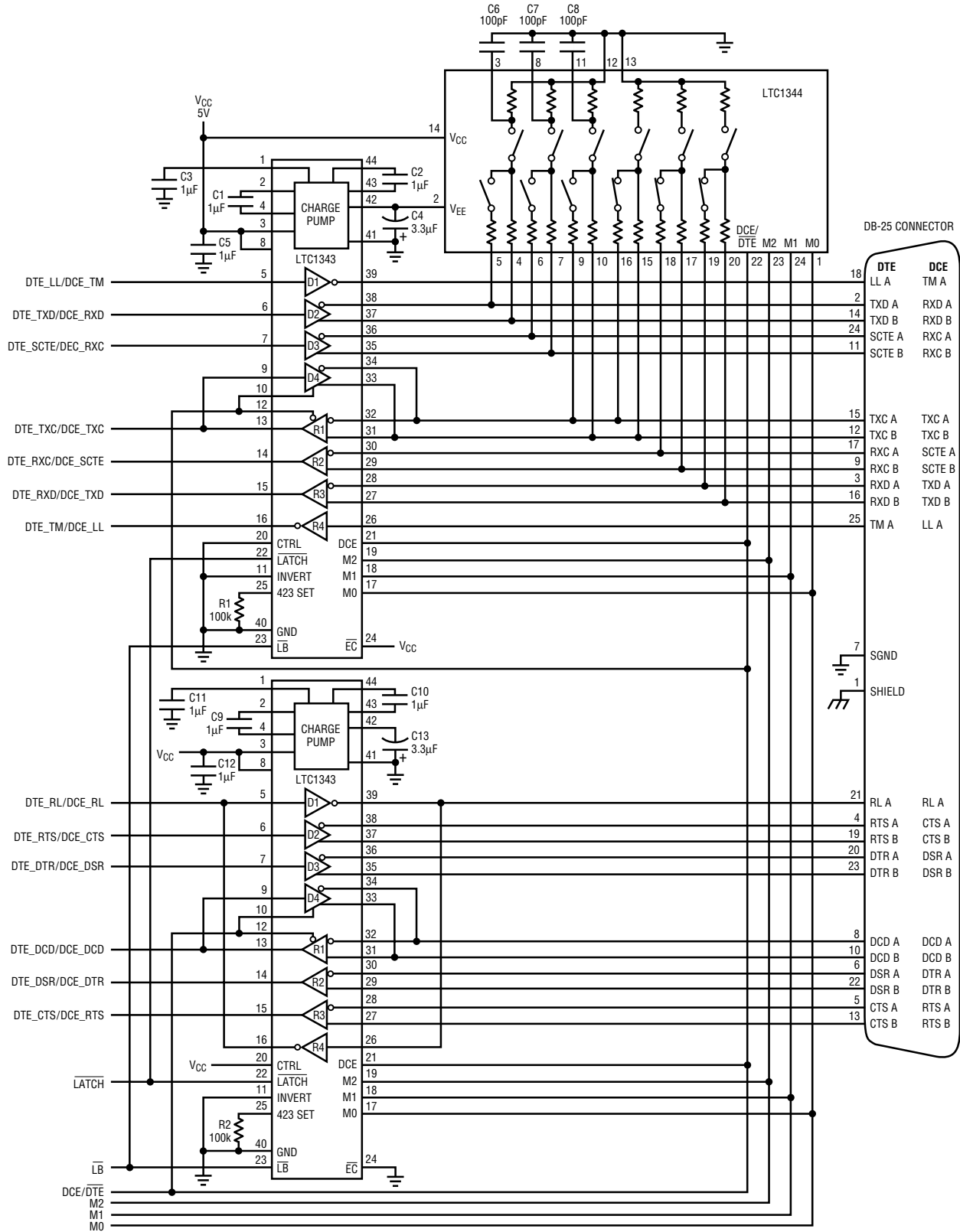
Figure 44. Controller-Selectable Multiprotocol DTE/DCE Port with DB-25 Connector
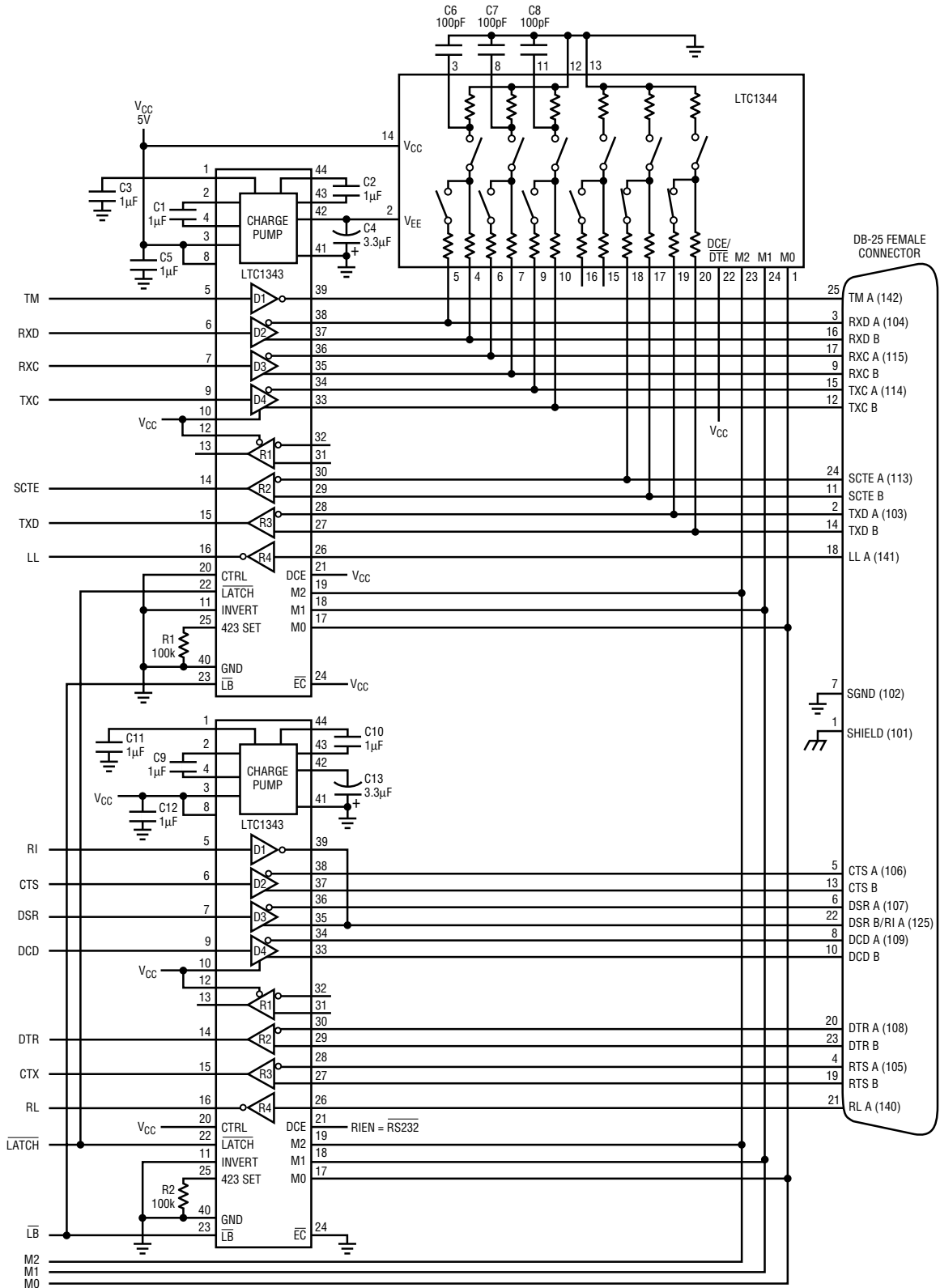
Figure 45. Controller-Selectable Multiprotocol DCE Port with Ring-Indicate and DB-25 Connector
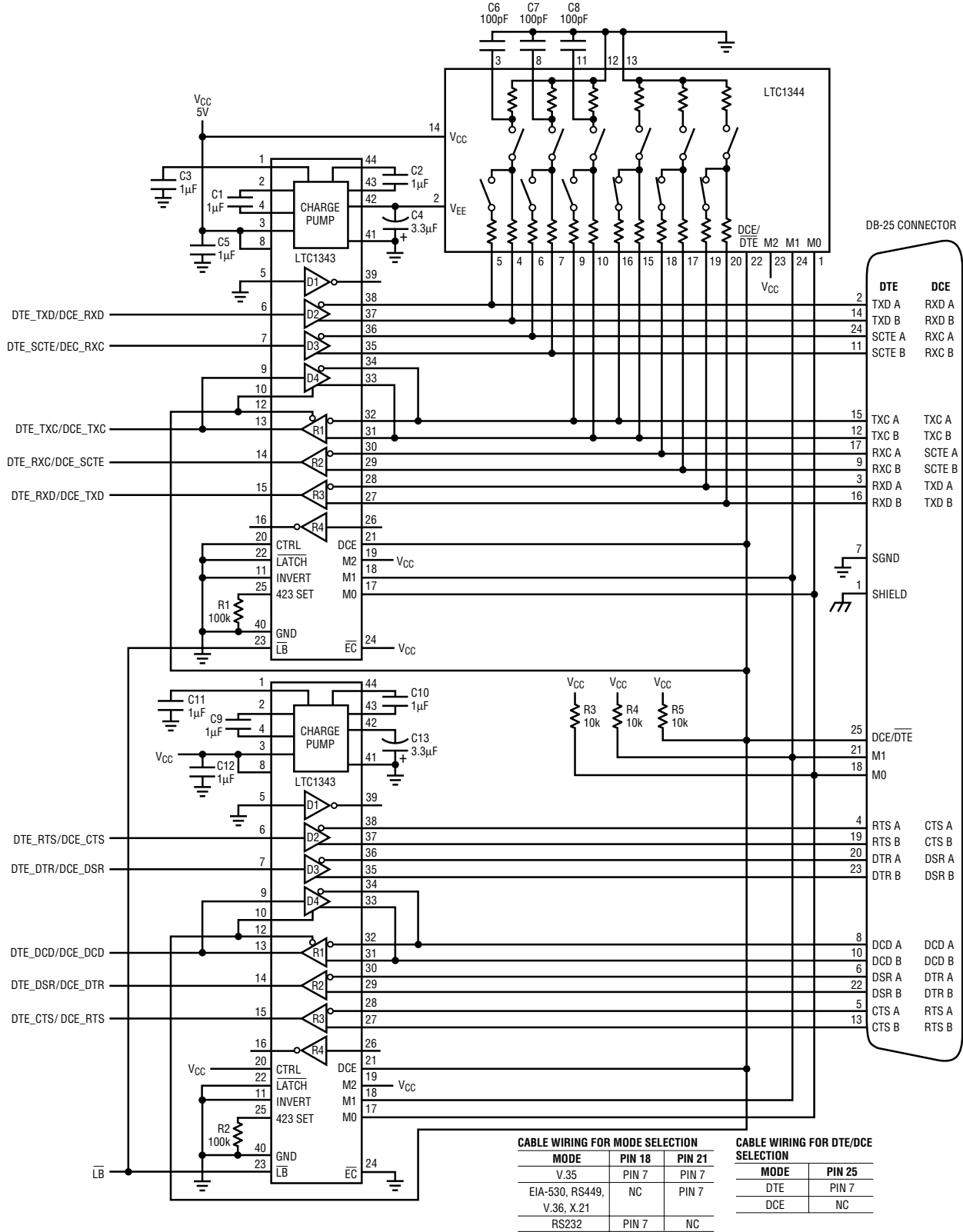
Figure 46. Cable-Selectable Multiprotocol DTE/DCE Port with DB-25 Connector

CABLE WIRING FOR MODE SELECTION		
MODE	PIN 18	PIN 21
V.35	PIN 7	PIN 7
EIA-530, RS449, V.36, X.21	NC	PIN 7
RS232	PIN 7	NC

CABLE WIRING FOR DTE/DCE SELECTION	
MODE	PIN 25
DTE	PIN 7
DCE	NC
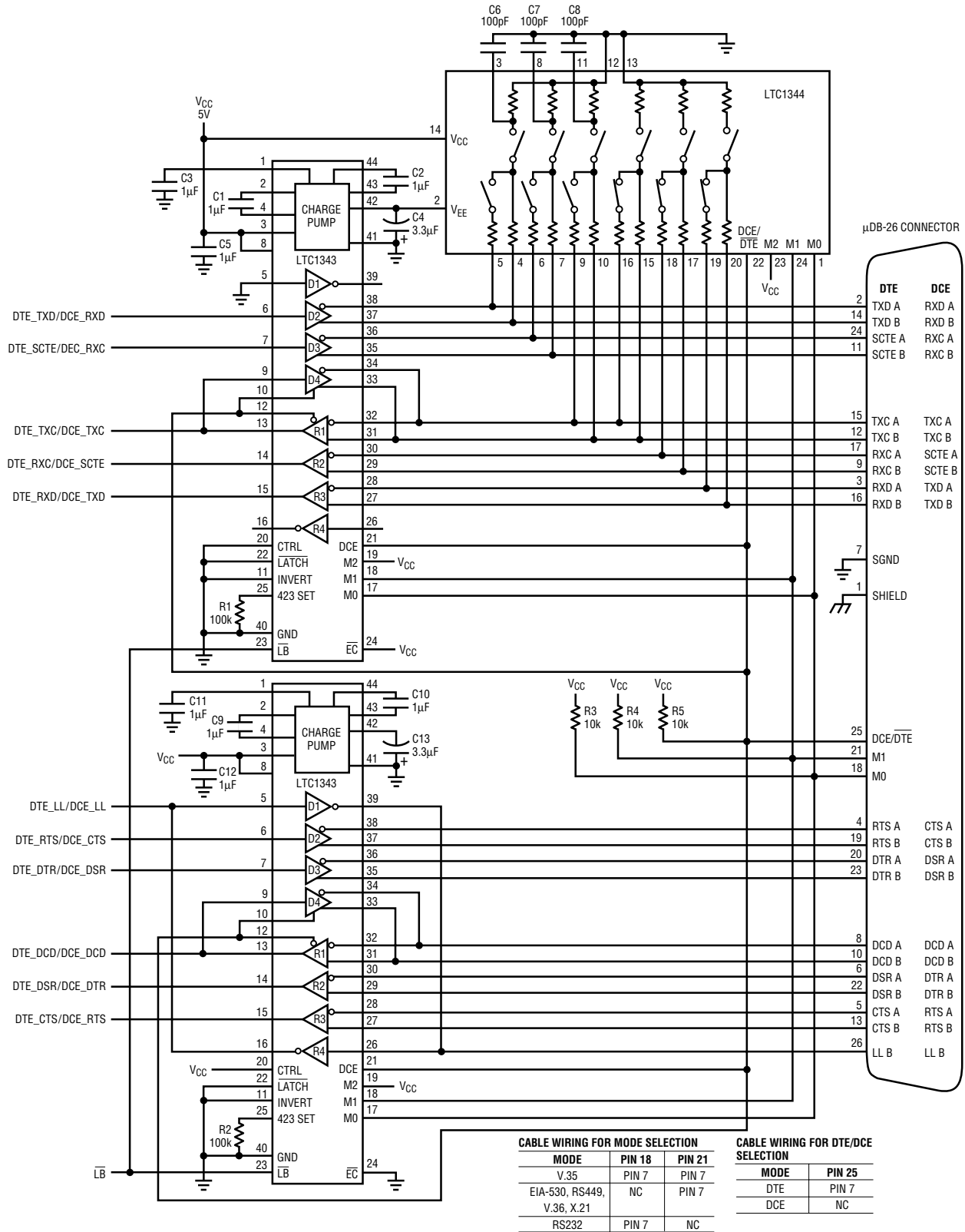
Figure 47. Cable-Selectable Multiprotocol DTE/DCE Port with μDB-26 Connector

CABLE WIRING FOR MODE SELECTION		
MODE	PIN 18	PIN 21
V.35	PIN 7	PIN 7
EIA-530, RS449, V.36, X.21	NC	PIN 7
RS232	PIN 7	NC

CABLE WIRING FOR DTE/DCE SELECTION	
MODE	PIN 25
DTE	PIN 7
DCE	NC

THE LT1328: A LOW COST IRDA RECEIVER SOLUTION FOR DATA RATES UP TO 4MBPS

by Alexander Strong

IrDA SIR

The LT1328 circuit in Figure 48 operates over the full 1cm to 1 meter range of the IrDA standard at the stipulated light levels. For IrDA data rates of 115kbps and below, a 1.6µs pulse width is used for a zero and no pulse for a one. Light levels are 40mW/sr (milliwatts per steradian) to 500mW/sr. Figure 49 shows a scope photo for a transmitter input (top trace) and the LT1328 output (bottom trace). Note that the input to the transmitter is inverted; that is, transmitted light produces a high at the input, which results in a zero at the output of the transmitter. The Mode pin (pin 7) should be high for these data rates.

An IrDA- compatible transmitter can also be implemented with only six components, as shown in Figure 50. Power requirements for the LT1328 are minimal: a single 5V supply and 2mA of quiescent current.
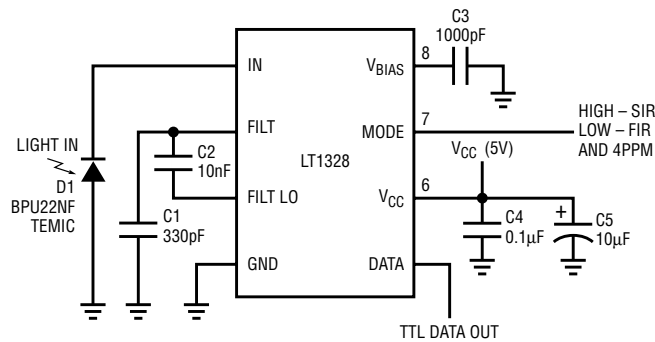

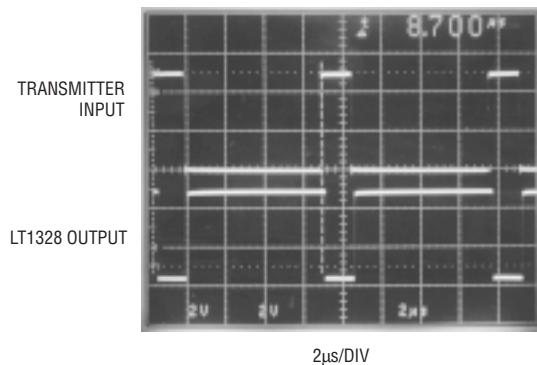Figure 48. LT1328 IrDA Receiver—Typical Application

2µs/DIV

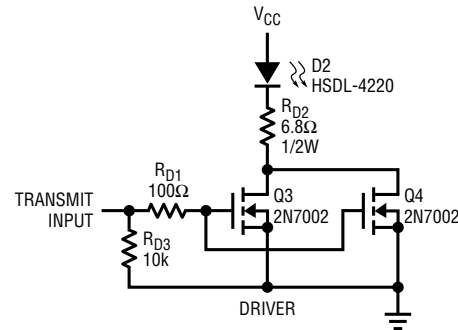**Figure 49. IrDA 115kbps Modulation**

Figure 50. IrDA Transmitter

IrDA FIR

The second fastest tier of the IrDA standard addresses 576kbps and 1.152Mbps data rates, with pulse widths of 1/4 of the bit interval for zero and no pulse for one. The 1.152Mbps rate, for example, uses a pulse width of 217ns; the total bit time is 870ns. Light levels are 100mW/sr to 500mW/sr over the 1cm to 1 meter range. A photo of a transmitted input and LT1328 output is shown in Figure 51. The LT1328 output pulse width will be less than 800ns wide over all of the above conditions at 1.152Mbps. Pin 7 should be held low for these data rates and above.

4ppm

The last IrDA encoding method is for 4Mbps and uses pulse position modulation, thus its name: 4ppm. Two bits are encoded by the location of a 125ns wide pulse at one of the four positions within a 500ns interval (2 bits • 1/500ns = 4Mbps). Range and input levels are the same as for 1.152Mbps. Figure 52 shows the LT1328 reproduction of this modulation.

200ns/DIV

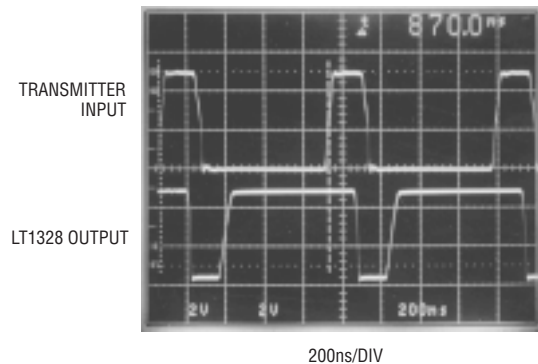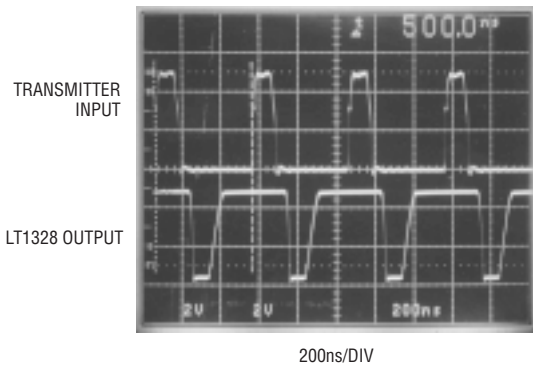**Figure 51. IrDA 1.152Mbps Modulation**

Figure 52. IrDA 4ppm Modulation

LT1328 Functional Description

Figure 53 is a block diagram of the LT1328. Photodiode current from D1 is transformed into a voltage by feedback resistor R_{FB}. The DC level of the preamp is held at V_{BIAS} by the servo action of the transconductance amplifier's g_m. The servo action only suppresses frequencies below the R_{g_m}/C_{FILT} pole. This highpass filtering attenuates interfering signals, such as sunlight or incandescent or fluorescent lamps, and is selectable at pin 7 for low or high data rates. For high data rates, pin 7 should be held low. The highpass filter breakpoint is set by the capacitor C1 at $f = 25/(2\pi \cdot R_{g_m} \cdot C)$, where $R_{g_m} = 60k$. The 330pF capacitor (C1) sets a 200kHz corner frequency and is used for data rates above 115kbps. For low data rates (115kbps and below), the capacitance at pin 2 is increased by taking pin 7 to a TTL high. This switches C2 in parallel with C1, lowering the highpass filter breakpoint. A 10nF cap (C2) produces a 6.6kHz corner. Signals processed by the preamp/g_m amplifier combination cause the comparator output to swing low.
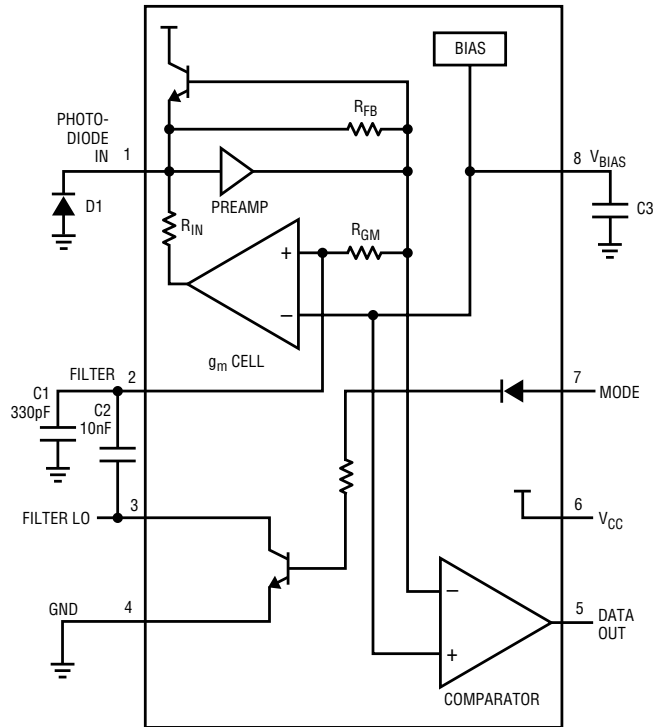

Figure 53. LT1328 Block Diagram

Conclusion

In summary, the LT1328 can be used to build a low cost receiver compatible with IrDA standards. Its ease of use and flexibility also allow it to provide solutions to numerous other photodiode receiver applications. The tiny MSOP package saves on PC board area.

LTC1387 SINGLE 5V RS232/RS485 MULTIPROTOCOL TRANSCEIVER
by Y.K. Sim

Introduction

The LTC1387 is a single 5V supply, logic-configurable, single-port RS232 or RS485 transceiver. The LTC1387 offers a flexible combination of two RS232 drivers, two RS232 receivers, an RS485 driver, an RS485 receiver and an onboard charge pump to generate boosted voltages for true RS232 levels from a single 5V supply. The RS232 transceivers and RS485 transceiver are designed to share the same port I/O pins for both single-ended and differential signal communication modes. The RS232 transceiver supports both RS232 and EIA562 standards, whereas the RS485 transceiver supports both RS485 and RS422 standards. Both half-duplex and full-duplex communication are supported.

RS232 MODE	RS485 TRANSMIT MODE	RS485 RECEIVE MODE	SHUTDOWN MODE
RXEN = 1	RXEN = 0	RXEN = 1	RXEN = 0
DXEN = 0	DXEN = 1	DXEN = 0	DXEN = 0
MODE = 0	MODE = 1	MODE = 1	MODE = X
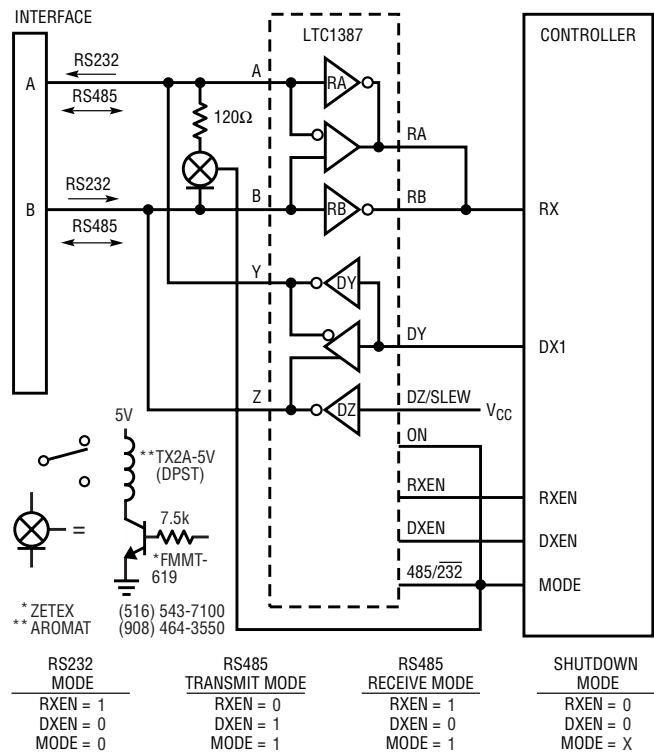
Figure 55. Full-Duplex RS232, Half-Duplex RS485

RS232 TRANSMIT MODE	RS232 RECEIVE MODE	RS485 TRANSMIT MODE	RS485 RECEIVE MODE	SHUTDOWN MODE
RXEN = 0	RXEN = 1	RXEN = 0	RXEN = 1	RXEN = 0
DXEN = 1	DXEN = 0	DXEN = 1	DXEN = 0	DXEN = 0
MODE = 0	MODE = 0	MODE = 1	MODE = 1	MODE = X
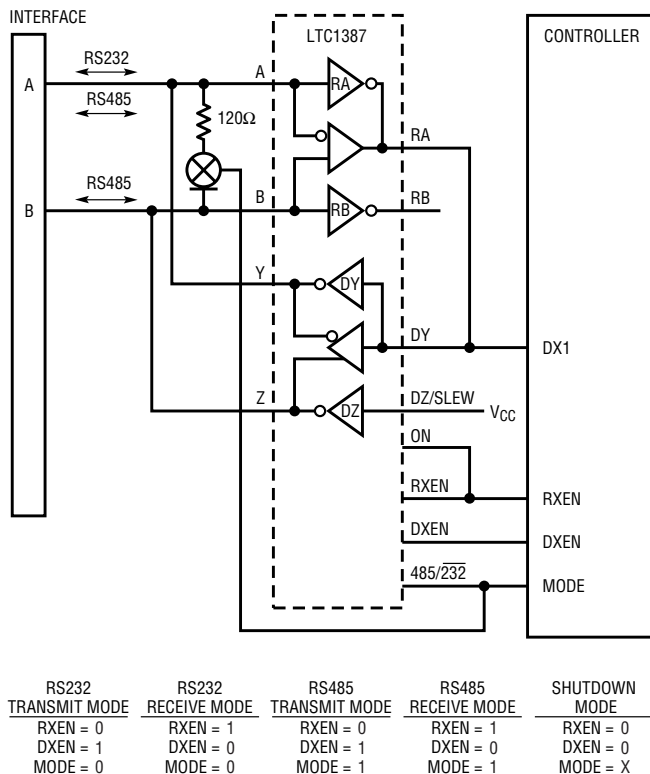
Figure 54. Half-Duplex RS232, Half-Duplex RS485

RS232 MODE	RS485 MODE	SHUTDOWN MODE
RXEN = 1	RXEN = 1	RXEN = 0
DXEN = 1	DXEN = 1	DXEN = 0
MODE = 0	MODE = 1	MODE = X

Figure 56. Full-Duplex RS232 (1-Channel), Full-Duplex RS422

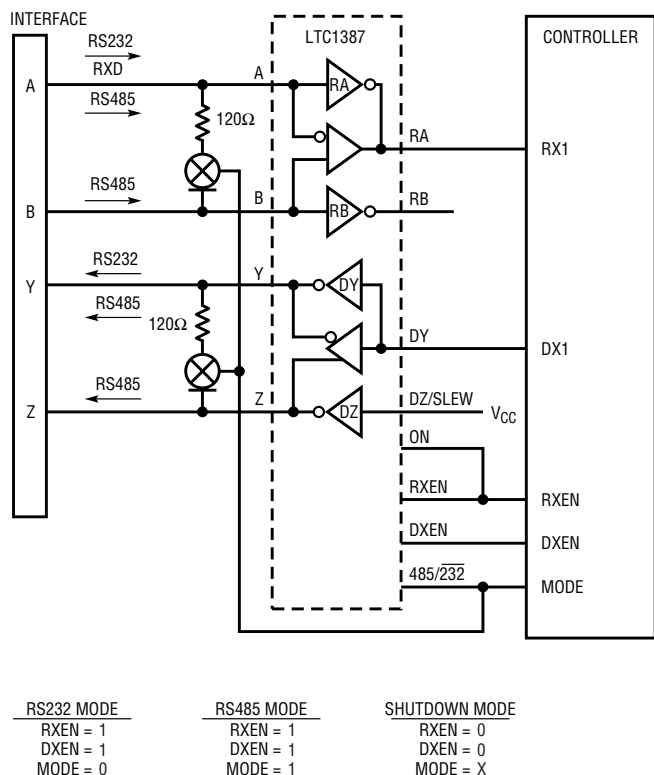A logic input selects between RS485 and RS232 modes. Three additional control inputs allow the LTC1387 to be reconfigured easily via software to adapt to various communication needs, including a one-signal line RS232 I/O mode (see function tables in figures). Four examples of interface port connections are shown in Figures 54–57.

A SLEW input pin, active in RS485 mode, changes the driver transition between normal and slow slew-rate modes. In normal RS485 slew mode, the twisted pair cable must be terminated at both ends to minimized signal reflection. In slow-slew mode, the maximum signal bandwidth is reduced, minimizing EMI and signal reflection problems. Slow-slew-rate systems can often use improperly terminated or even unterminated cables with acceptable results. If cable termination is required, external termination resistors can be connected through switches or relays.

The LTC1387 features micropower shutdown mode, loopback mode for self-test, high data rates (120kbaud for RS232 and 5Mbaud for RS485) and 7kV ESD protection at the driver outputs and receiver inputs.
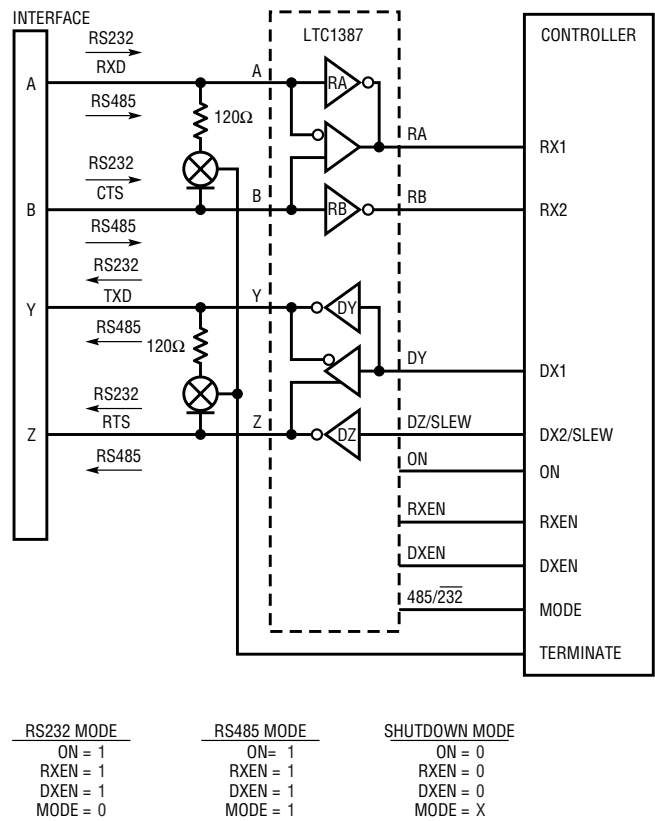

RS232 MODE	RS485 MODE	SHUTDOWN MODE
ON = 1	ON= 1	ON = 0
RXEN = 1	RXEN = 1	RXEN = 0
DXEN = 1	DXEN = 1	DXEN = 0
MODE = 0	MODE = 1	MODE = X

Figure 57. Full-Duplex RS232 (2-Channel), Full-Duplex RS485 with Slew and Termination Control

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A 10MB/s MULTIPLE-PROTOCOL CHIP SET SUPPORTS NET1 AND NET2 STANDARDS

by David Soo

Introduction

Typical Application

Like the LTC1343 software-selectable multiprotocol transceiver, introduced in the August, 1996 issue of *Linear Technology* , the LTC1543/LTC1544/LTC1344A chip set creates a complete software-selectable serial interface using an inexpensive DB-25 connector. The main difference between these parts is the division of functions: the LTC1343 can be configured as a data/clock chip or as a control-signal chip using the CTRL/$\overline{CLK}$ pin, whereas the

LTC1543 is a dedicated data/clock chip and the LTC1544 is a control-signal chip. The chip set supports the V.28 (RS232), V.35, V.36, RS449, EIA-530, EIA-530A and X.21 protocols in either DTE or DCE mode.

Figure 58 shows a typical application using the LTC1543, LTC1544 and LTC1344A. By just mapping the chip pins to the connector, the design of the interface port is complete. The figure shows a DCE mode connection to a DB-25 connector.

The LTC1543 contains three drivers and three receivers, whereas the LTC1544 contains four drivers and four receivers. The LTC1344A contains six switchable resistive terminators that are connected only to the high speed clock and data signals. When the interface protocol is changed via the mode selection pins, M2, M1 and M0, the

Table 4. Mode-Pin Functions

LTC1543/LTC1544 Mode Name	M2	M1	M0
Not Used	0	0	0
EIA-530A	0	0	1
EIA-530	0	1	0
X.21	0	1	1
V.35	1	0	0
RS449/V.36	1	0	1
RS232/V.28	1	1	0
No Cable	1	1	1

drivers, receivers and line terminators are placed in their proper configuration. The mode pin functions are summarized in Table 4. There are internal 50μA pull-up current sources on the mode select pins, DCE/$\overline{\text{DTE}}$ and the INVERT pins.

DTE vs DCE Operation

The LTC1543/LTC1544/LTC1344A chip set can be configured for either DTE or DCE operation in one of two ways. The first way is when the chip set is a dedicated DTE or DCE port with a connector of appropriate gender. The second way is when the port has one connector that can be configured for DTE or DCE operation by rerouting the signals to the chip set using a dedicated DTE or DCE cable.

Figure 58 is an example of a dedicated DCE port using a female DB-25 connector. The complement to this port is the DTE-only port using a male DB-25 connector, as shown in Figure 59.

If the port must accommodate both DTE and DCE modes, the mapping of the drivers and receivers to connector pins must change accordingly. For example, in Figure 58, driver 1 in the LTC1543 is connected to pin 3 and pin 16 of the DB-25 connector. In DTE mode, as shown in Figure 59, driver 1 is mapped to pins 2 and 14 of the DB-25 connector. A port that can be configured for either DTE or DCE operation is shown in Figure 60. This configuration requires separate cables for proper signal routing.

Cable-Selectable Multiprotocol Interface

The interface protocol may be selected by simply plugging the appropriate interface cable into the connector. A cable-selectable multiprotocol DTE/DCE interface is shown in Figure 61. The mode pins are routed to the connector and are left unconnected (1) or wired to ground (0) in the cable. The internal pull-up current sources ensure a binary 1 when a pin is left unconnected and also ensure that the LTC1543/LTC1544/LTC1344A enter the no-cable mode when the cable is removed. In the no-cable mode, the LTC1543/LTC1544 power supply current drops to less than 200μA and all of the LTC1543/LTC1544 driver outputs will be forced into the high impedance state.

Adding Optional Test Signal

In some cases, the optional test signals local loopback (LL), remote loopback (RL) and test mode (TM) are required but there are not enough drivers and receivers available in the LTC1543/LTC1544 to handle these extra signals. The solution is to combine the LTC1544 with the LTC1343. By using the LTC1343 to handle the clock and data signals, the chip set gains one extra single-ended driver/receiver pair. This configuration is shown in Figure 62.

Compliance Testing

A European standard EN 45001 test report is available for the LTC1543/LTC1544/LTC1344A chip set. The report provides documentation on the compliance of the chip set to Layer 1 of the NET1 and NET2 standard. A copy of this test report is available from LTC or from Detecon, Inc. at 1175 Old Highway 8, St. Paul, MN 55112.

Conclusion

In the world of network equipment, the product differentiation is mostly in the software and not in the serial interface. The LTC1543, LTC1544 and LTC1344A provide a simple yet comprehensive solution to standards compliance for multiple-protocol serial interface.
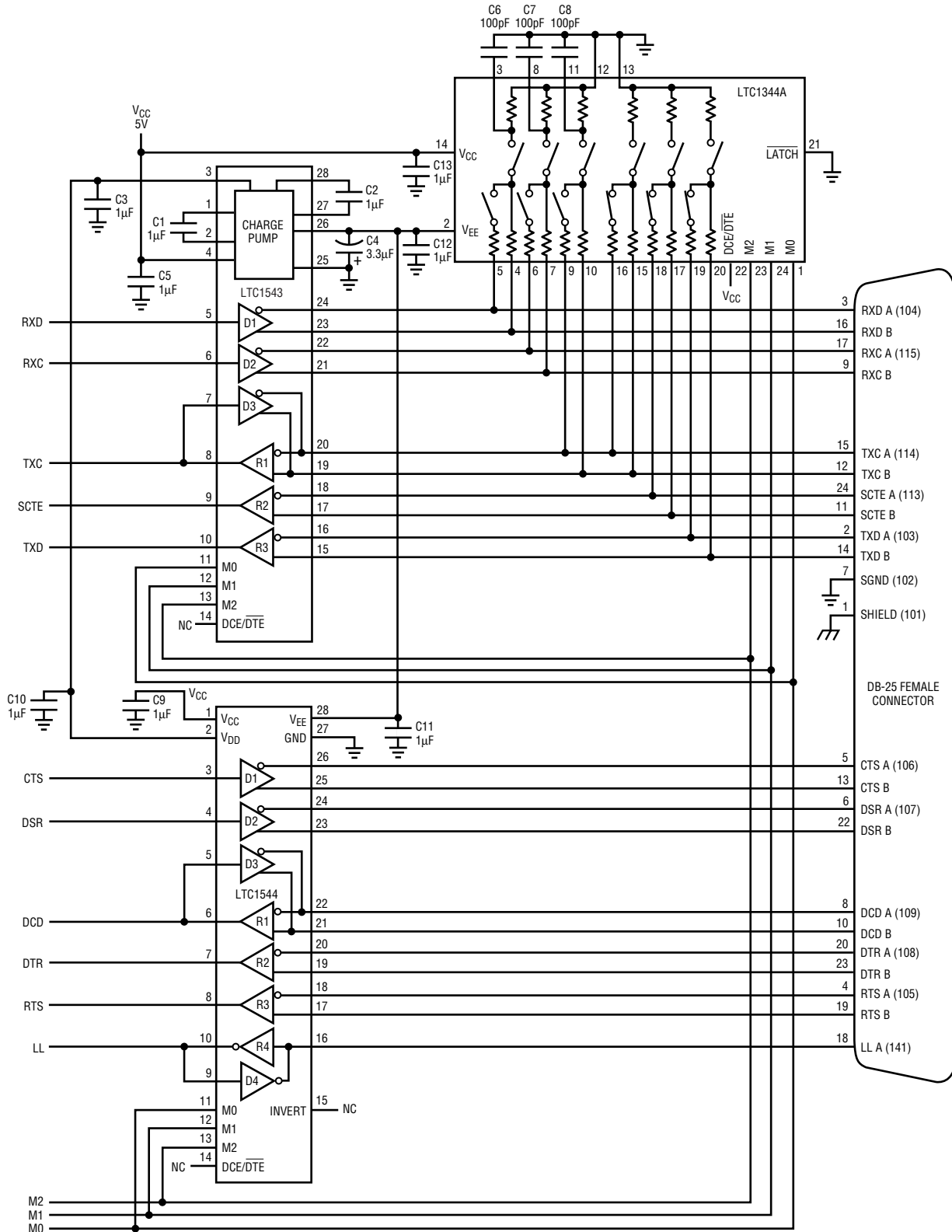
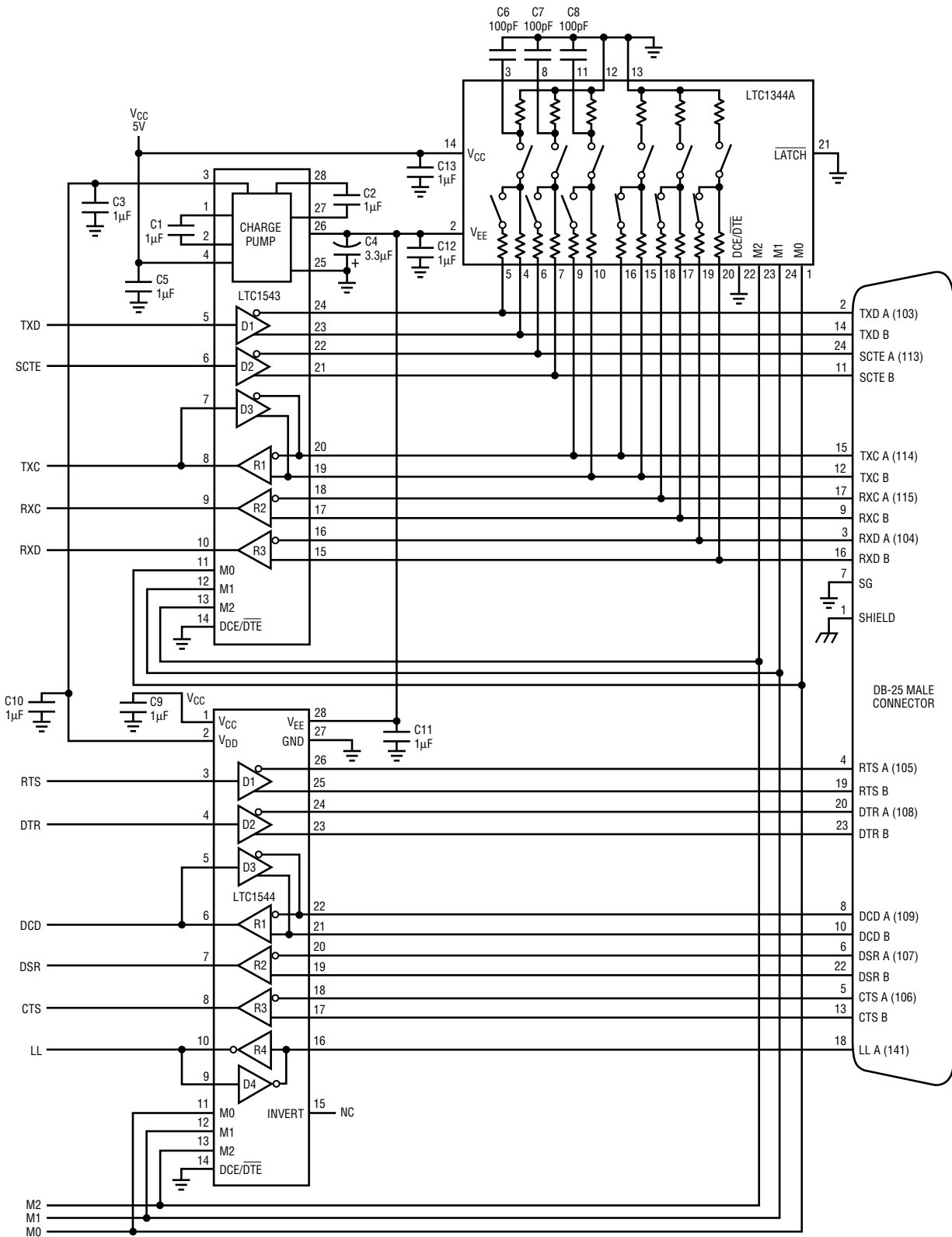**Figure 58. Controller-Selectable DCE Port with DB-25 Connector**

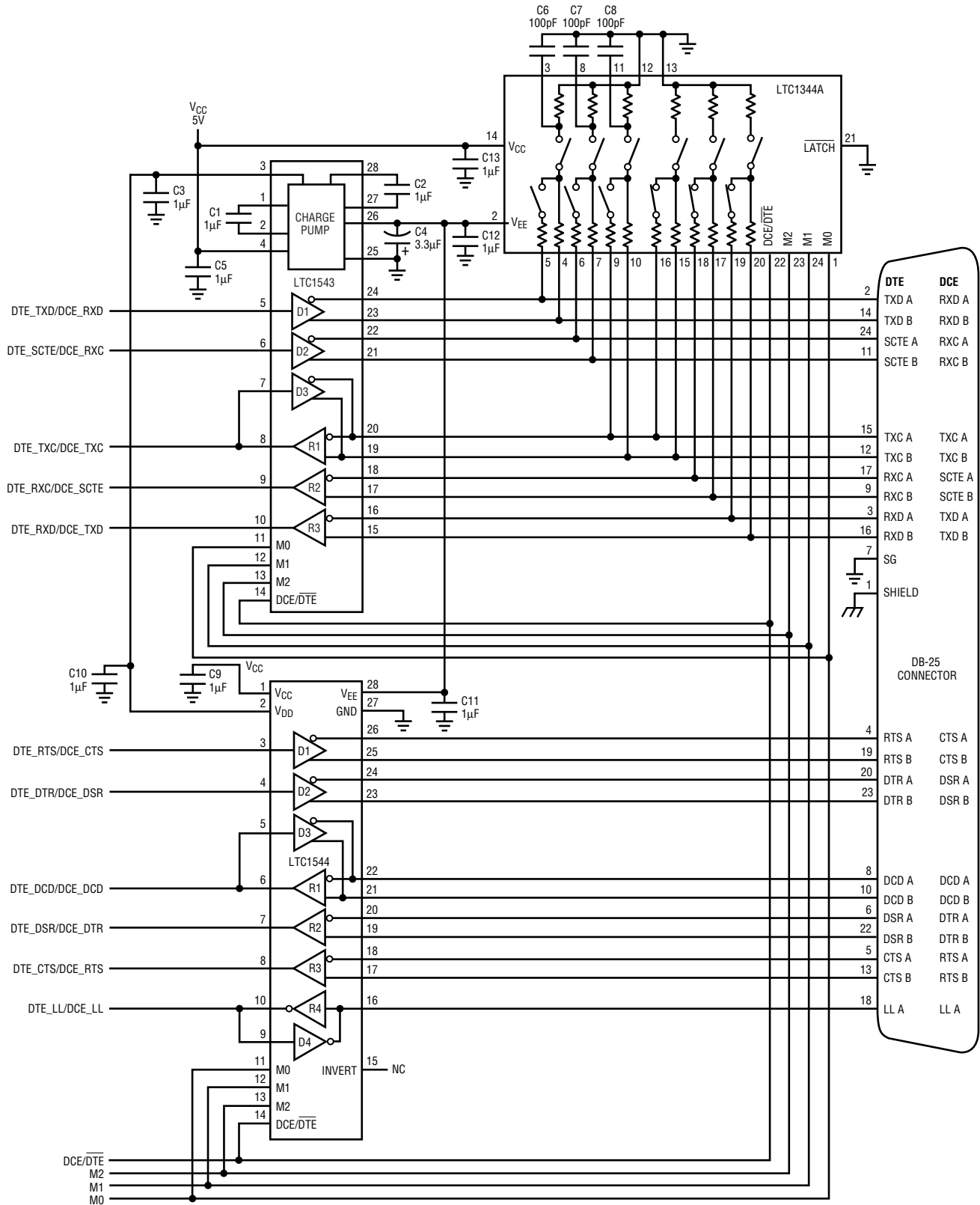**Figure 59. Controller-Selectable Multiprotocol DTE Port with DB-25 Connector**

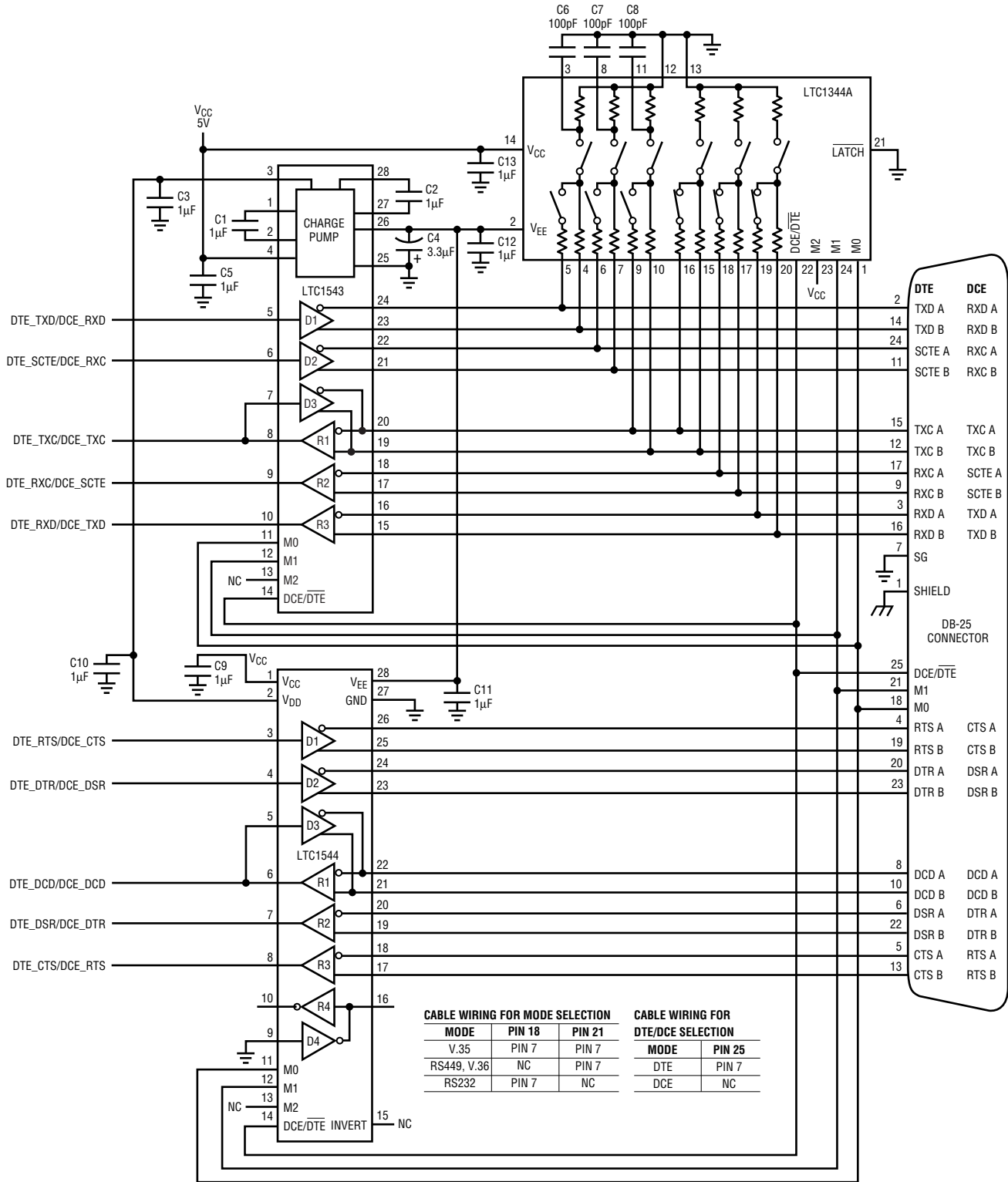**Figure 60. Controller-Selectable DTE/DCE Port with DB-25 Connector**

Figure 61. Cable-Selectable Multiprotocol DTE/DCE Port

CABLE WIRING FOR MODE SELECTION		
MODE	**PIN 18**	**PIN 21**
V.35	PIN 7	PIN 7
RS449, V.36	NC	PIN 7
RS232	PIN 7	NC

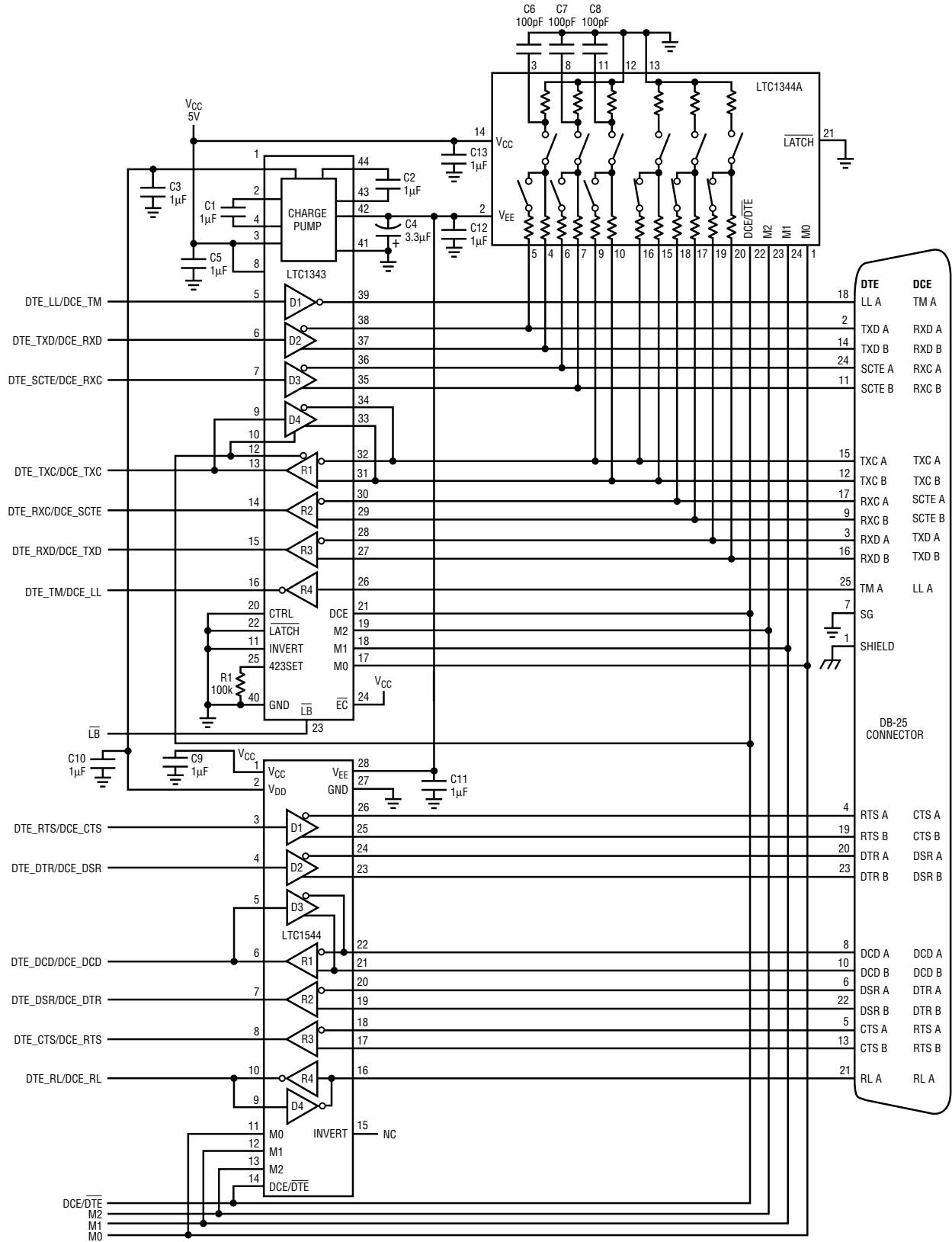| CABLE WIRING FOR DTE/DCE SELECTION	
MODE	**PIN 25**
DTE	PIN 7
DCE	NC

Figure 62. Controller-Selectable Multiprotocol DTE/DCE Port with RLL, LL, TM and DB-25 Connector

NET1 AND NET2 SERIAL INTERFACE CHIP SET SUPPORTS TEST MODE
by David Soo

Some serial networks use a test mode to exercise all of the circuits in the interface. The network is divided into local and remote data terminal equipment (DTE) and data-circuit-terminating equipment (DCE), as shown in Figure 63. Once the network is placed in a test mode, the local DTE will transmit on the driver circuits and expect to receive the same signals back from either a local or remote DCE. These tests are called local or remote loopback.

The LTC1543/LTC1544/LTC1344A chip set has taken the integrated approach to multiple protocol. By using this chip set, the Net1 and Net2 design work is done. The LTC1545 extends the family by offering test mode capability. By replacing the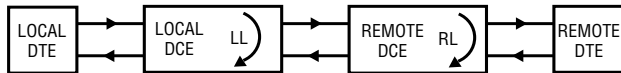 6-circuit LTC1544 with the 9-circuit LTC1545, the optional circuits TM (Test Mode), RL (Remote Loopback) and LL (Local Loopback) can now be implemented.

Figure 64 shows a typical application using the LTC1543, LTC1545 and LTC1344A. By just mapping the chip pins to the connector, the design of the interface port is complete. The chip set supports the V.28, V.35, V.36, RS449, EIA-530, EIA-530A or X.21 protocols in either DTE or DCE mode. Shown here is a DCE mode connection to a DB-25 connector. The mode-select pins, M0, M1 and M2, are used to select the interface protocol, as summarized in Table 5.

Table 5. Mode-Pin Functions

LTC1543/LTC1544 Mode Name	M2	M1	M0
Not Used	0	0	0
EIA-530A	0	0	1
EIA-530	0	1	0
X.21	0	1	1
V.35	1	0	0
RS449/V.36	1	0	1
RS232/V.28	1	1	0
No Cable	1	1	1

Figure 63. Serial Network

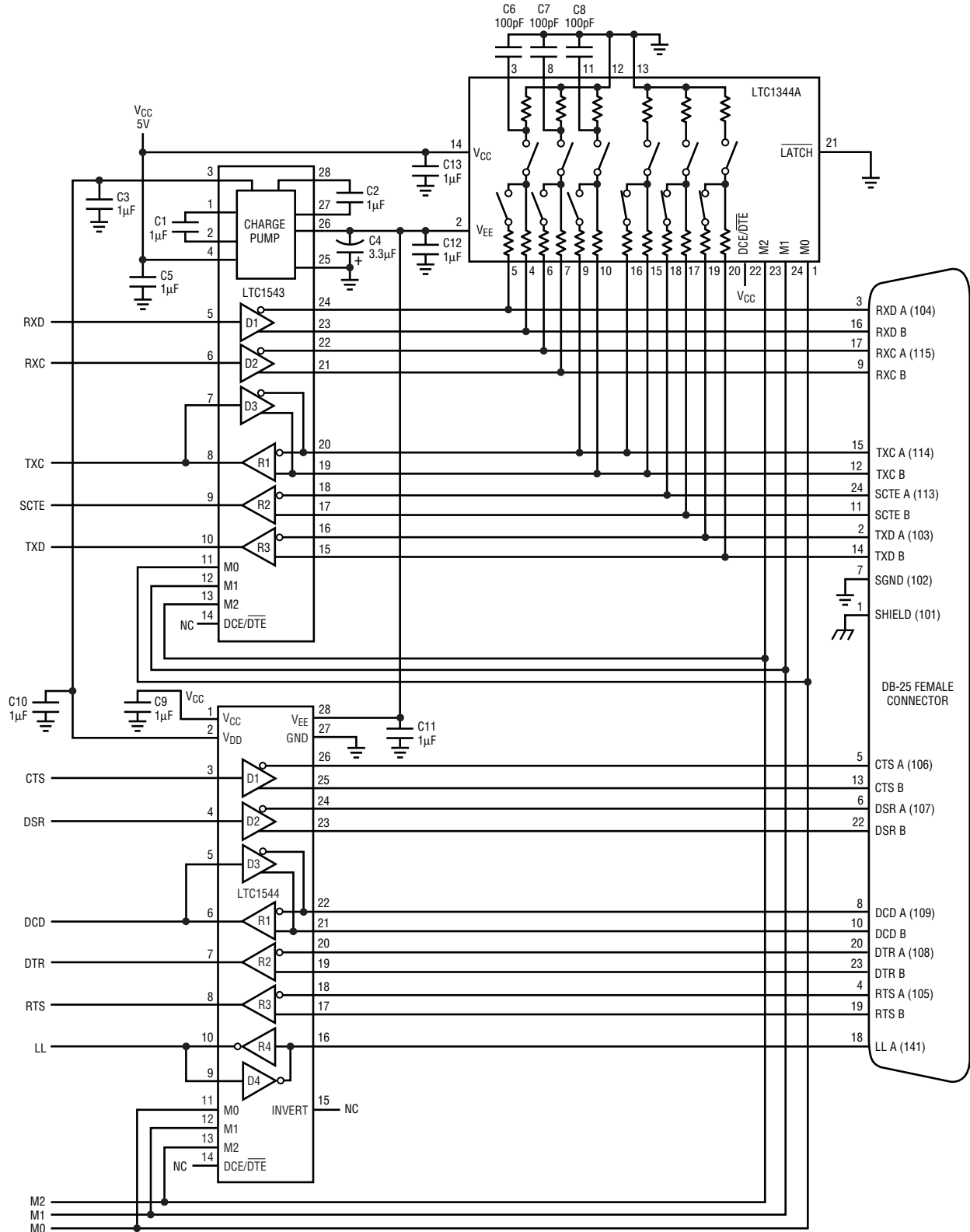**Figure 64. Typical Application: Controller-Selectable DCE Port with DB-25 Connector**

Operational Amplifiers/Video Amplifiers

LT1490/LT1491 OVER-THE-TOP DUAL AND QUAD MICROPOWER RAIL-TO-RAIL OP AMPS
by Jim Coelho-Sousae

Introduction

The LT1490 is Linear Technology's lowest power, lowest cost and smallest dual rail-to-rail input and output operational amplifier. The ability to operate with its inputs above V_{CC}, its high performance-to-price ratio and its availability in the MSOP package, sets the LT1490 apart from other amplifiers.

An Over-the-Top Application

The battery current monitor circuit shown in Figure 65 demonstrates the LT1491's ability to operate with its inputs above the positive supply rail. In this application, a conventional amplifier would be limited to a battery voltage between 5V and ground, but the LT1491 can handle battery voltages as high as 44V. The LT1491 can be shut down by removing V_{CC}. With V_{CC} removed the input leakage is less than 0.1nA. No damage to the LT1491 will result from inserting the 12V battery backward.

When the battery is charging, Amp B senses the voltage drop across RS. The output of Amp B causes QB to drain sufficient current through RB to balance the inputs of Amp B. Likewise, Amp A and QA form a closed loop when the battery is discharging. The current through QA or QB is proportional to the current in RS; this current flows into RG, which converts it back to a voltage. Amp D buffers and amplifies the voltage across RG. Amp C compares the output of Amp A and Amp B to determine the polarity of the current through RS. The scale factor for V_{OUT} with S1 open is 1V/A. With S1 closed the scale factor is 1V/100mA, and current as low as 5mA can be measured.
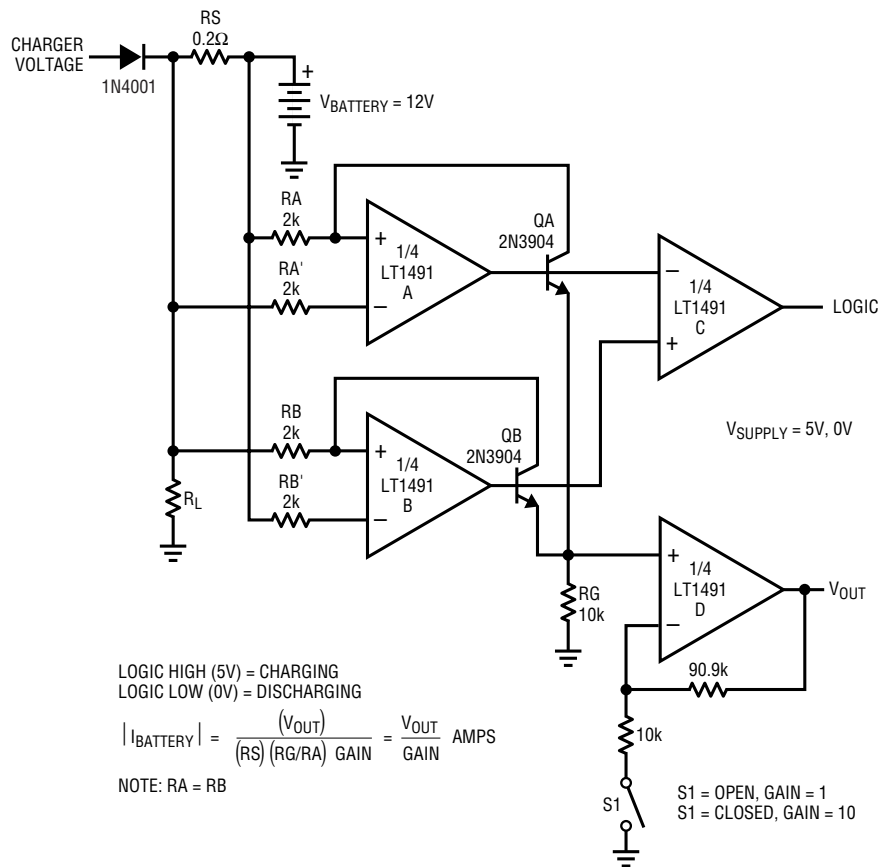

LOGIC HIGH (5V) = CHARGING
LOGIC LOW (0V) = DISCHARGING

$$\left| I_{BATTERY} \right| = \frac{(V_{OUT})}{(RS)\,(RG/RA)\,\text{GAIN}} = \frac{V_{OUT}}{\text{GAIN}} \ \text{AMPS}$$

NOTE: RA = RB

Figure 65. LT1491 Battery Current Monitor—an "Over-The-Top" Application

THE LT1210: A 1-AMPERE, 35MHz CURRENT FEEDBACK AMPLIFIER

by William Jett and Mitchell Lee

Introduction

The LT1210 current feedback amplifier extends Linear Technology's high speed driver solutions to the 1 ampere level. The device combines a 35MHz bandwidth with a guaranteed 1A output current, operation with ±5V to ±15V supplies and optional compensation for capacitive loads, making it well suited for driving low impedance loads. Short circuit protection and thermal shutdown ensure the device's ruggedness. A shutdown feature allows the device

to be switched into a high impedance, low current mode, reducing dissipation when the device is not in use. The LT1210 is available in the 7-pin TO-220 package, the 7-pin DD surface mount package and the 16-pin SO-16 surface mount package.

Twisted Pair Driver

Figure 66 shows a transformer-coupled application of the LT1210 driving a 100Ω twisted pair. This surge impedance is typical of PVC-insulated, 24 gauge, telephone-grade twisted pair wiring. The 1:3 transformer ratio allows just over 1W to reach the twisted pair at full output. Resistor R_T acts as a primary side back-termination. The
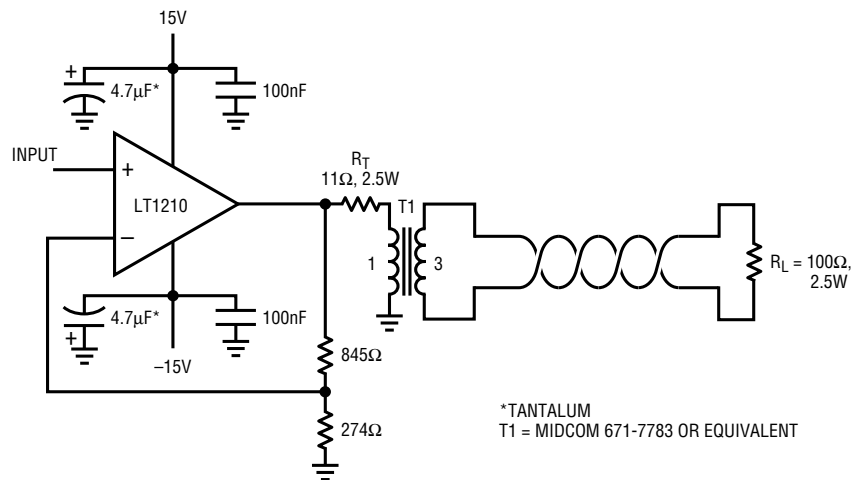

Figure 66. Twisted Pair Is Easily Driven for Applications Such as ADSL. Voltage Gain is About 12. 5V$_{P-P}$ Input Corresponds to Full Output
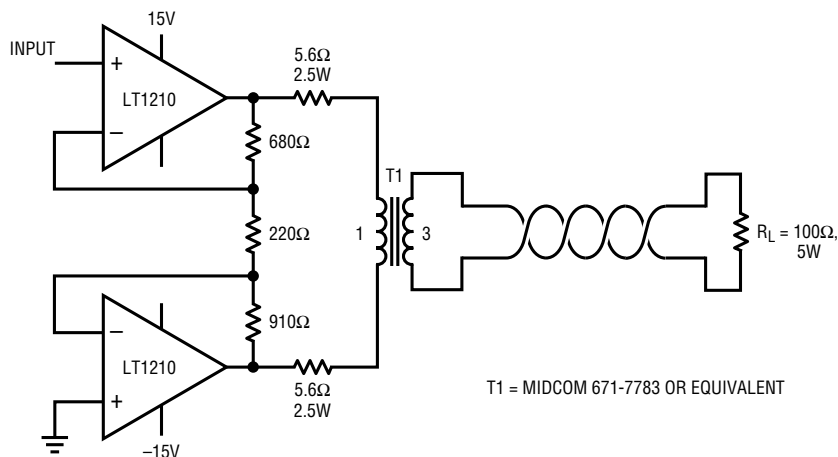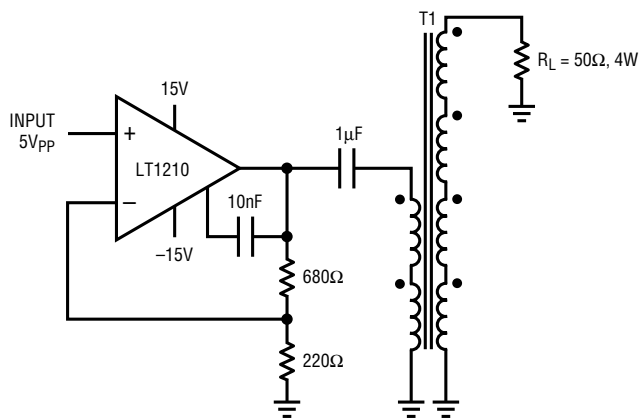

Figure 67. In a Bridge Configuration, the LT1210 Can Deliver Almost 5W to a Twisted Pair (and Another 5W to the Back Termination)

Figure 68. Matched to a 50Ω Load with a Balun-Mode Transformer, this Circuit Delivers a Measured 35.6dBm (almost 4W). Full-Power Band Limits are 15kHz to Slightly Over 10MHz
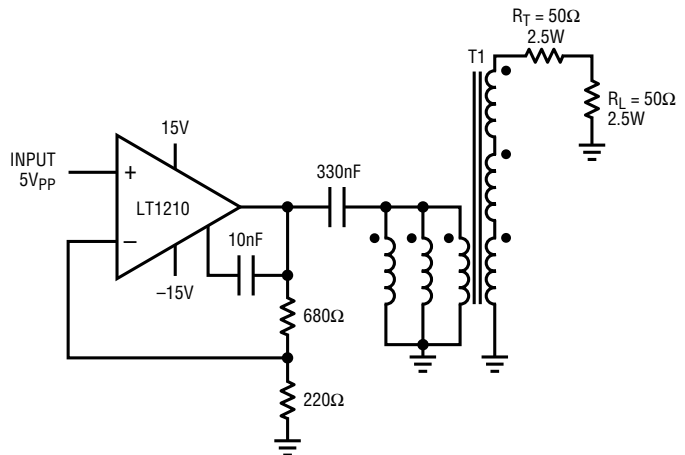
Figure 69. Wide Bandwidth can be Obtained with Even Higher Impedance Transformations. Here, a 1:3 Step-Up Matches 100Ω and Develops Nearly 4.5W. A Measured +33dBm Reaches the 50Ω Load. Full-Power Band Limits Are 80kHz to 18MHz

overall frequency response is flat to within 1dB from 500Hz to 2MHz. Distortion products at 1MHz are below –70dBc at a total output power of 560mW (load plus termination), rising to –56dBc at 2.25W.

On a ±15V supply, a maximum output power of 5W is available when a 10Ω load is presented to the LT1210. With the transformer shown in Figure 66, a total load impedance of approximately 22Ω limits the output to 2.25W. Bridging allows nearly maximum output power to be delivered into standard 1:3 data communications transformers. Figure 67 shows a bridged application with two LT1210s, delivering approximately 9W maximum into the load and termination.

At first glance the resistor values would suggest a gain imbalance between the inverting and noninverting sides of the bridge. On close inspection, however, it is apparent that both sides operate at a closed loop gain of 4 relative to the input signal. This ensures symmetric swing and maximum undistorted output.

Matching 50Ω Systems

Few practical systems exhibit a 10Ω impedance, so a matching transformer is necessary for applications driving other loads, such as 50Ω. Multifilar winding techniques exhibit the best high frequency characteristics.

Suitable off-the-shelf components are available, such as the Coiltronics Versa-Pac™ series. These are hexafilar wound and give power bandwidths in excess of 10MHz. One disadvantage is that using a limited number of 1:1 windings makes it impossible to exactly transform 50Ω to the optimum 10Ω load. Nevertheless, there are several useful connections.

In Figure 68 the windings are configured for a 2:4 step-up, reflecting 12.5Ω into the LT1210. The circuit exhibits 18dB gain and drives 50Ω to nearly +36dBm. The large-signal, low frequency response is limited by the magnetizing inductance of the transformer to about 15kHz. The high frequency response is limited to 10MHz by the stack of four secondary windings.

Reconfiguring the transformer windings allows double termination at full power (Figure 69). Here the transformer reflects 11.1Ω and the amplifier delivers over +33dBm to the load. Paralleled input windings limit the low frequency response to 80kHz, but fewer series secondary windings extend the high frequency corner to 18MHz.

The coupling capacitor shown in these examples is added to block current flow through the transformer primary, arising from amplifier offsets. The capacitor value is based on setting X_C equal to the reflected load impedance at the
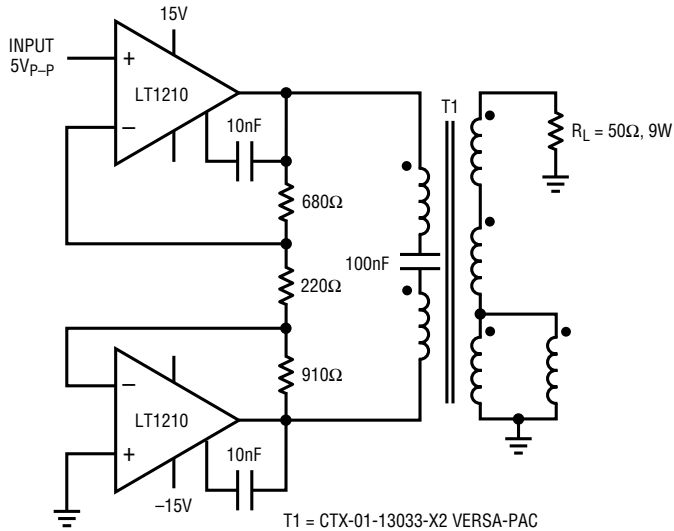
Figure 70. In this Bridge Amplifier, the LT1210 Delivers +39.5dBm (9W) to a 50Ω Load. Power Band Limits Range from 40kHz to 14.5MHz. The Sixth, Otherwise-Unused Winding is Connected in Parallel with One Secondary Winding to Avoid Parasitic Effects Arising from a Floating Winding.
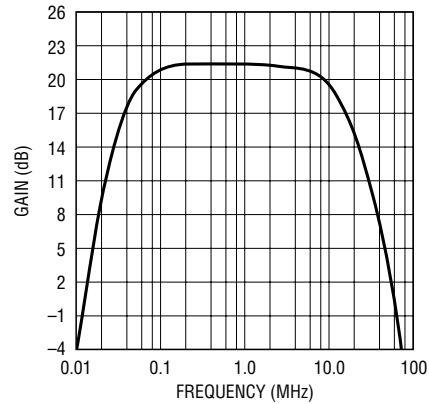

Figure 71. Frequency Response of Figure 70's Circuit

Another useful connection for the Versa-Pac transformer is shown in Figure 70. A 2:3 transformation presents 11.1Ω to each LT1210 in a bridge, delivering a whopping 9W into 50Ω. In this circuit the lower frequency cutoff was limited by the choice of coupling capacitor to approximately 40kHz (the transformer is capable of 15kHz). The frequency response is shown in Figure 71.

Conclusion

The LT1210 combines high output current with a high slew rate to form an effective solution for driving low impedance loads. Power levels of up to 5W can be supplied to a load at frequencies ranging from DC to beyond 10MHz.

frequency where X_L of the primary is also equal to the reflected load. This isolates the amplifier from a low impedance short at frequencies below transformer cutoff. In applications where a termination resistor is positioned between the LT1210 amplifier and the transformer, no coupling capacitor is necessary. Note that a low frequency signal, well below the transformer's cutoff frequency, could result in high dissipation in the termination resistor.

THE LT1207: AN ELEGANT DUAL 60MHZ, 250mA CURRENT FEEDBACK AMPLIFIER
by LTC Applications Staff

Introduction

The LT1207 is a dual version of Linear Technology's LT1206 current feedback amplifier. Each amplifier has 60MHz bandwidth, guaranteed 250mA output current, operates on ±5V to ±15V supply voltages and offers optional external compensation for driving capacitive loads. These features and capabilities combine to make it well suited for such difficult applications as driving cable loads, wide-bandwidth video and high speed digital communication.

LT1088 Differential Front End

Using thermal conversion, the LT1088 wideband RMS/DC converter is an effective solution for applications such as RMS voltmeters, wideband AGC, RF leveling loops and high frequency noise measurements. Its thermal conversion method achieves vastly wider bandwidth than any other approach. It can handle input signals that have a 300MHz bandwidth and a crest factor of at least 40:1. The thermal technique employed relies on first principles: a wave form's RMS value is defined as its heating value in a load. Another characteristic of the LT1088 is its low impedance inputs (50Ω and 250Ω), common to thermal converters. Though this low impedance represents a difficult load to most drive circuits, the LT1207 can handle it with ease.

Featuring high input impedance and overload protection, the differential input, wideband thermal RMS/DC converter in Figure 72 performs true RMS/DC conversion over a 0Hz to 10MHz bandwidth with less than 1% error, independent of input-signal wave shape. The circuit consists of a wideband input amplifier, RMS/DC converter and overload protection.[1] The LT1207 provides high input impedance, gain and output current capability necessary to drive the LT1088's input heater. The 5k/24pF network across the LT1207's 180Ω gain-set resistor is used to adjust a slight peaking characteristic at high frequencies, ensuring 1% flatness at 10MHz. The converter uses matched pairs of heaters and diodes and a control ampli-

fier. R1 produces heat when the LT1207 drives it differentially. This heat lowers D1's voltage. Differentially connected A3 responds by driving R2, heating D2 and closing the loop. A3's DC output directly relates to the input signal's RMS value, regardless of input frequency or wave shape. A4's gain trim compensates residual LT1088 mismatches. The RC network around A3 frequency compensates the loop, ensuring good settling time.

The LT1088 can suffer damage if the 250Ω input is driven beyond $9V_{RMS}$ at 100% duty cycle. An easy remedy to this possibility is to reduce the driver supply voltage. This, however, sacrifices crest factor. Instead, a means of overload protection is included. The LT1018 monitors D1's anode voltage. Should this voltage become abnormally low, A5's output goes low and pulls A6's input low. This causes A6's output to go high, shutting down the LT1207 and eliminating the overload condition. The RC network on A6's input delays the LT1207's reactivation. If the overload condition remains, shutdown is reinstated. This oscillatory action continues, protecting the LT1088 until the overload is corrected. The RMS/DC circuit's 1% error bandwidth and CMRR performance are shown in Figures 73 and 74, respectively.

CCD Clock Driver

Charge-coupled-devices (CCDs) are used in many imaging applications, such as surveillance, hand-held and desktop computer video cameras, and document scanners. Using a "bucket-brigade," CCDs require a precise multiphase clock signal to initiate the transfer of light-generated pixel charge from one charge reservoir to the next. Noise, ringing or overshoot on the clock signal must be avoided, since they introduce errors into the CCD output signal. These errors cause aberrations and perturbations in a displayed or printed image.

Two challenges surface in the effort to avoid these error sources when driving a CCD's input. First, CCDs have an input capacitance that varies over a range of 100pF to 2000pF and varies directly with the number of sensing elements (pixels). This presents a high capacitive load to the clock-drive circuitry. Second, CCDs typically require a clock signal whose magnitude is greater than the output capabilities of 5V interfaces and control circuitry. An
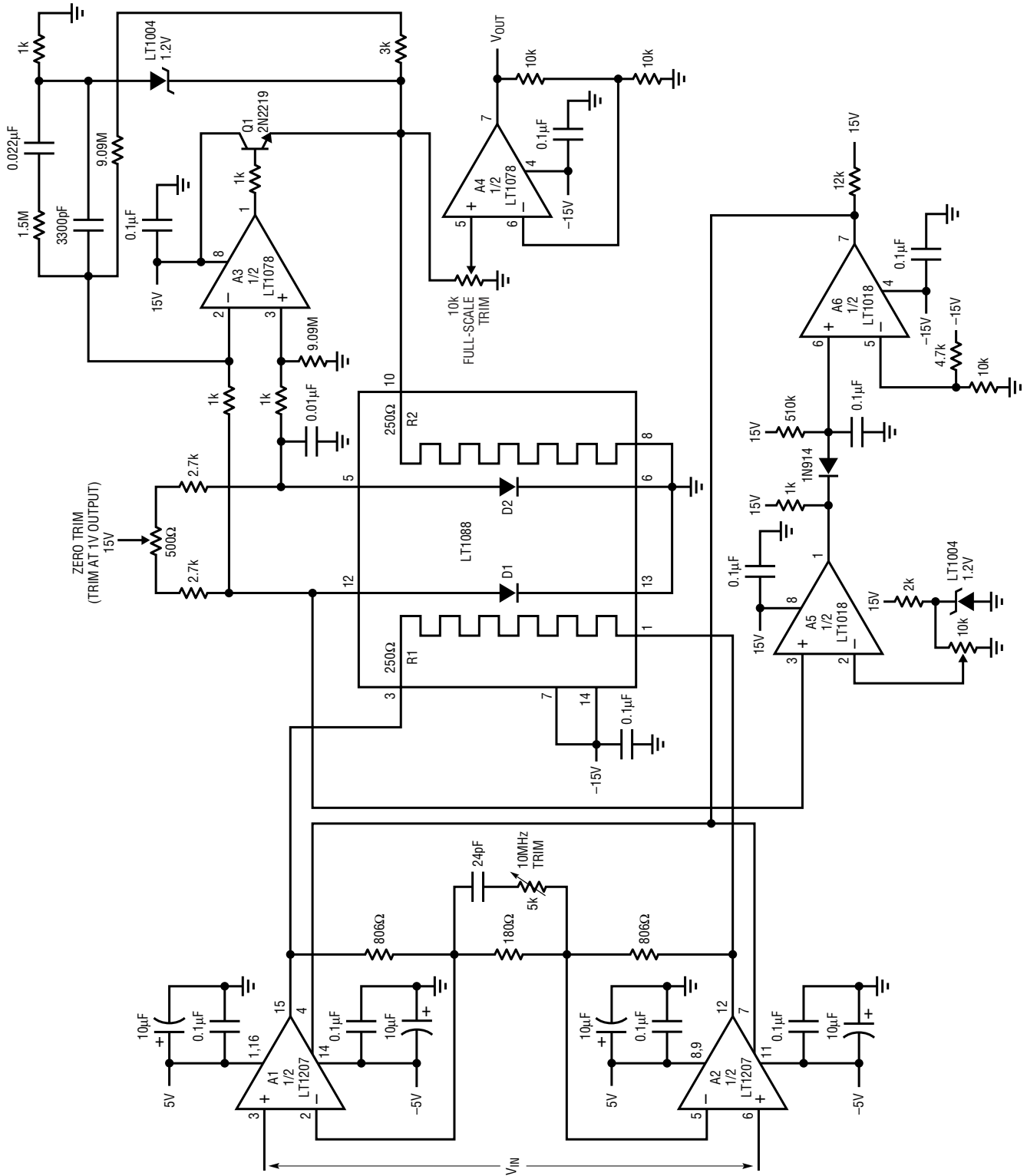
Figure 72. Differential Input 10MHz RMS/DC Converter has 1% Accuracy, High Input Impedance and Overload Protection.
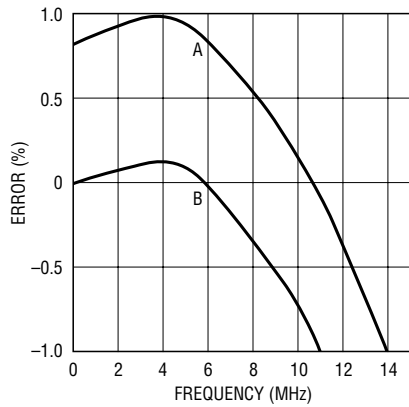
Figure 73. Error Plot for the Differential-Input RMS/DC Converter. Gain Boost at A2 Preserves 1% Accuracy but Causes Slight Peaking before Roll-Off. Boost Can be Set for Maximum Bandwidth (A) or Minimum Error (B)
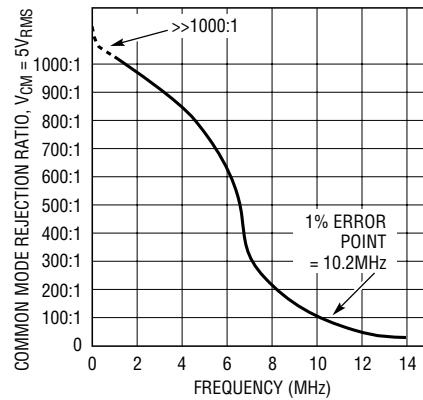

Figure 74. Common Mode Rejection Ratio vs Frequency for the Differential-Input RMS/DC Converter. Layout, Amplifier Bandwidth and AC Matching Characteristics Determine the Curve
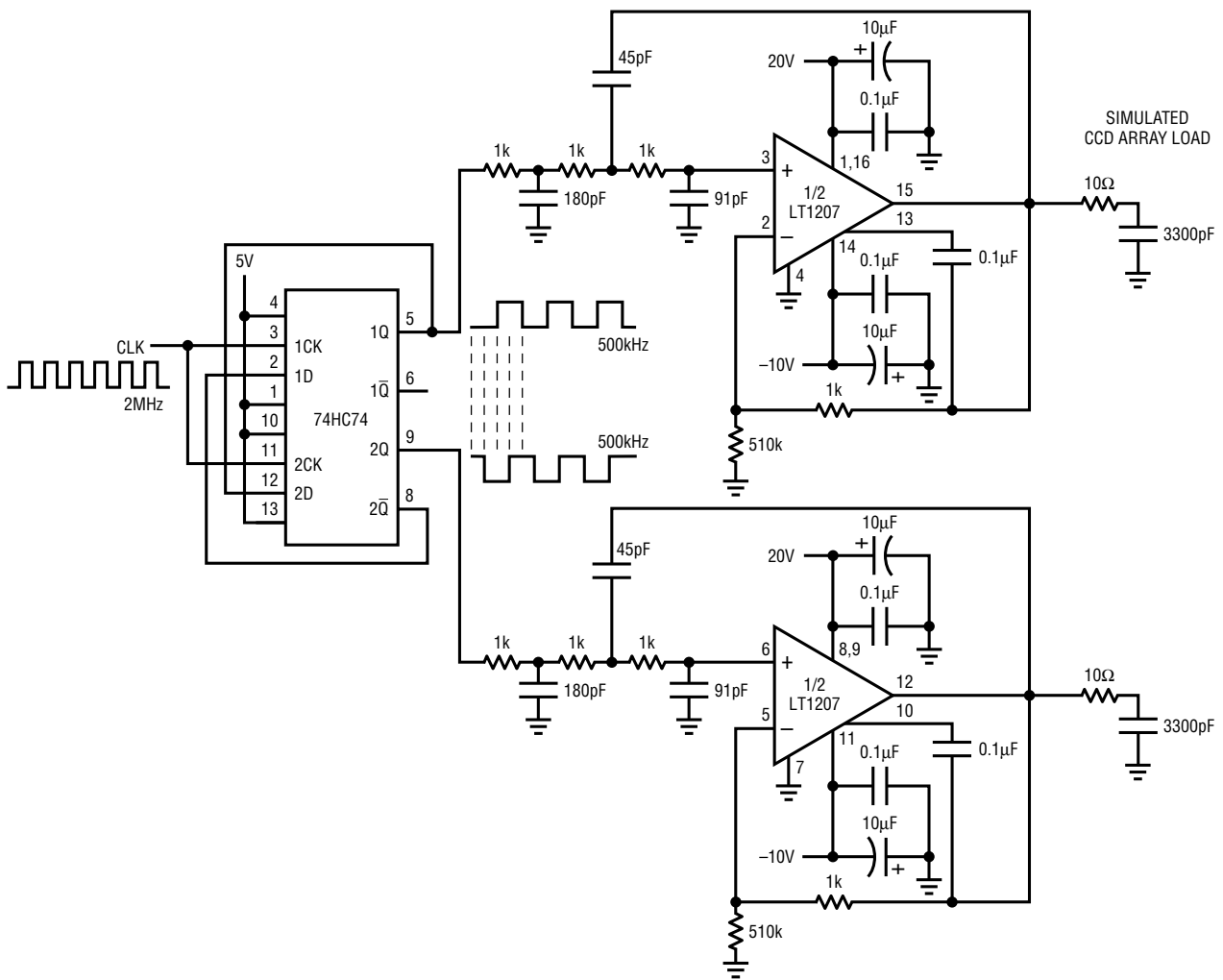

Figure 75. The LT1207 Easily Tames the High Capacitance Loads of CCD Clock Inputs without Ringing or Overshoot
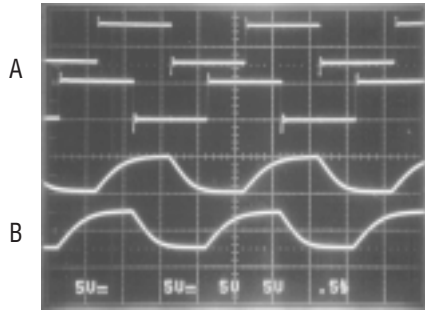
Figure 76a. Trace A is the Quadrature Drive Signals. Trace B. is the Voltage at the Input of the Simulated CCD of Figure 75, Driven by HC Logic
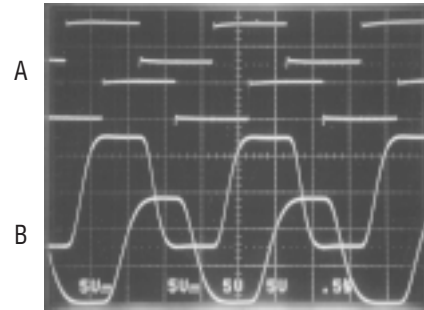

Figure 76b. Trace A is the Quadrature Signals. Trace B Shows the Voltage at the Input of the Simulated CCD of Figure 75, Driven by the LT1207

amplifying filter built around the LT1207 will meet both challenges.

Controlling clock signal rise and fall times is one way to avoid ringing or overshoot. This is done by conditioning the clock signal with a nonringing Gaussian filter. The circuit shown in Figure 75 uses the LT1207 to filter and amplify control circuitry clock output signals. To reduce ringing and overshoot, each amplifier is configured as a third-order Gaussian lowpass filter with a 1.6MHz cutoff frequency.

Figures 76a and 76b compare the response of a digital 5V clock-drive signal and the output of the LT1207, each driving a 3300pF load. The digital clock circuit has two major weaknesses that lead to jitter and image distortion. The CCD's output is changing during charge transfer, producing glitches that decay exponentially. Conversely, the LT1207 circuit's output has a flat top and controlled rise and fall. If an ADC is used to sample a CCD output, the conversion will be much more accurate when the LT1207 circuit is used to clock the pixel changes. With the LT1207's filter configuration, the output has a controlled rise and fall time of approximately 300ns. Ringing and overshoot are absent from the LT1207's output. Wide bandwidth, high output current capability and external compensation allow the LT1207 to easily drive the difficult load of a CCD's clock input.

1. Thanks to Jim Williams for this Circuit

MICROPOWER, DUAL AND QUAD JFET OP AMPS FEATURE C-LOAD CAPABILITY AND PICOAMPERE INPUT BIAS CURRENTS
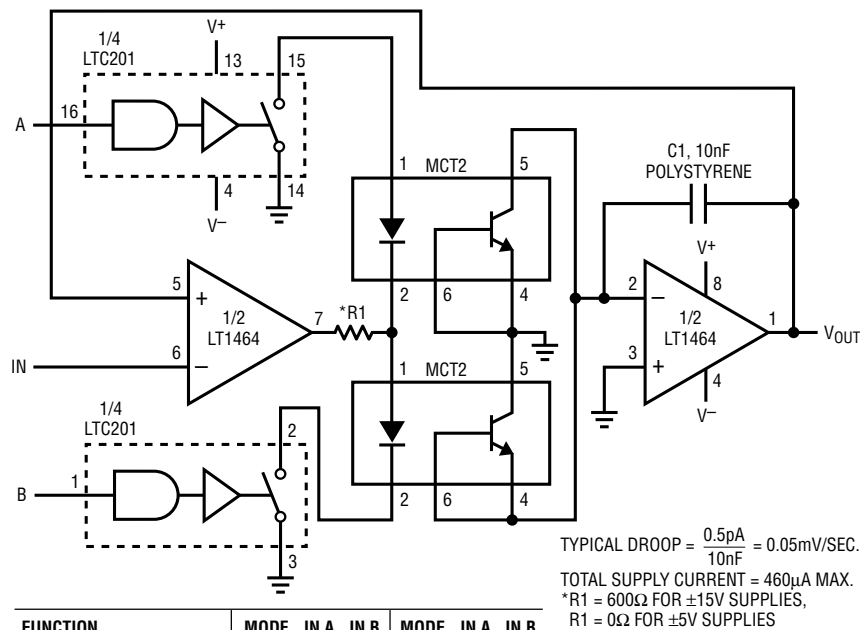*by Alexander Strong*

Introduction

The LT1462/LT1464 duals and the LT1463/LT1465 quads are the first micropower op amps (30µA typical, 40µA maximum per amp for the LT1462; 140µA typical, 200µA maximum per amp for the LT1464) to offer both pico ampere input bias currents (500fA typical) and unity-gain stability for capacitive loads up to 10nF. The outputs can swing a 10k load to within 1.5 volts of either supply. Just like op amps that require an order of magnitude more supply current, the LT1462/LT1463 and the LT1464/LT1465 have open loop gains of 600,000 and 1,000,000, respectively. These unique features, along with a 0.8mV offset, have not been incorporated into a single monolithic amplifier before.

Applications

Figure 77 is a track-and-hold circuit that uses a low cost optocoupler as a switch. Leakages for these parts are usually in the nano amp region with 1 to 5 volts across the output. Since there is less than 2mV across the junctions, less than 0.5pA leakage can be achieved for both opto-couplers. The input signal is buffered by one op amp while the other buffers the stored voltage; this results in a droop of 50µV/s with a 10nF cap.

Figure 78 is a logging photodiode sensor using two LT1462 duals or an LT1463 quad. The low input bias current of the LT1462/LT1463 makes it a natural for amplifying low level signals from high impedance trans-ducers. The 500fA of input bias current contributes only $0.4fA/\sqrt{Hz}$ of current noise. For example, a 1M input impedance converts the noise current to a noise voltage of only $0.4nV/\sqrt{Hz}$. Here, a photodiode converts light to a

$$\text{TYPICAL DROOP} = \frac{0.5pA}{10nF} = 0.05mV/SEC.$$

TOTAL SUPPLY CURRENT = 460µA MAX.
*R1 = 600Ω FOR ±15V SUPPLIES,
R1 = 0Ω FOR ±5V SUPPLIES

FUNCTION	MODE	IN A	IN B	MODE	IN A	IN B
TRACK AND HOLD	TRACK	0	0	HOLD	1	1
POSITIVE PEAK DETECTOR	RESET	0	0	STORE	0	1
NEGATIVE PEAK DETECTOR	RESET	0	0	STORE	1	0

LTC201 SWITCH IS OPEN FOR LOGIC "1"
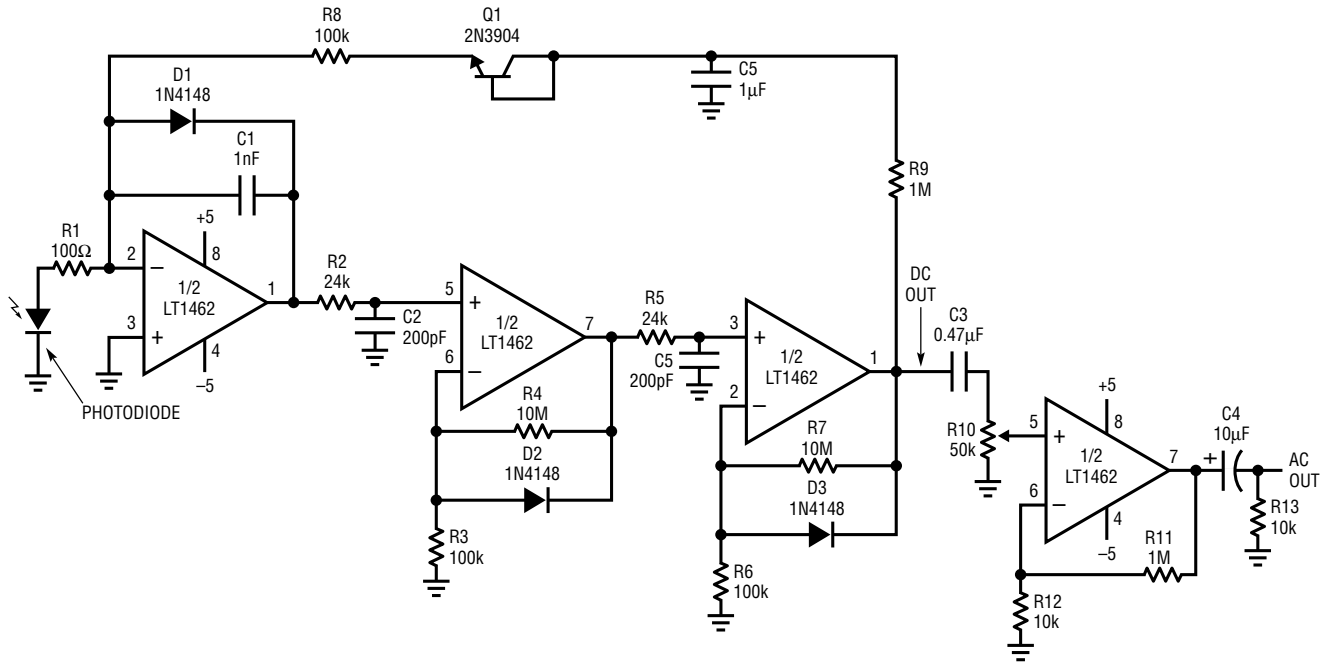
Figure 77. Low-Droop Track-and-Hold Circuit/Peak Detector

Figure 78. Logging Photodiode Amplifier

current, which is converted to a voltage by the first op amp. The first, second and third gain stages are logarithmic amplifiers that perform a logarithmic compression. A DC feedback path comprising R8, R9, C5 and Q1 is active only for no-light conditions, which are very rare, due to the picoampere sensitivity of the input. Q1 is off when light is present, isolating the photodiode from C5. When the feedback path is needed, a small filtered current through R8 keeps the output of the third op amp within an acceptable range. The third op amp's output voltage, which is proportional to the photodiode current, can serve as a logarithmic DC light meter. Figure 79 shows the relationship between DC output voltage and photodiode current. The AC component of the output of third op amp is compressed logarithmically and passed through capacitor C3 and pot R10 for amplitude control. The fourth op amp amplifies this AC signal which is generated across R13. The logarithmic compression of the AC photodiode current allows the user to examine the AC signals for a wide range of input currents.

Conclusion

The LT1462/LT1464 duals and the LT1463/LT1465 quads combine many advantages found in many different op amps, such as low power, (LT1464/LT1465 are 140µA, LT1462/LT1463 are 30µA typical per amplifier), wide input common mode range that includes the positive rail and pico ampere input bias currents. Not only is the output swing specified with 2k and 10k loads, gain is also specified for the same load conditions, which is unheard-
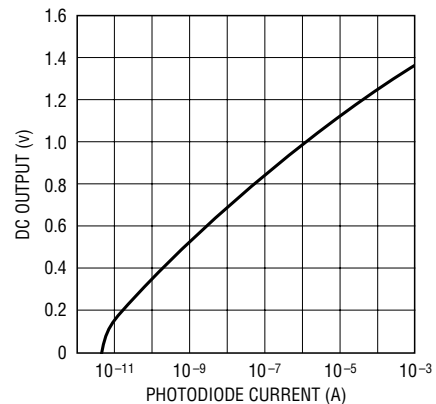

Figure 79. DC Output of Logging Photodiode Amplifier

of for micropower op amps. The 1MHz (LT1464/LT1465) or 250kHz (LT1462/LT1463) bandwidth self adjusts to maintain stability for capacitive loads up to 10nF. And don't forget the low 0.8mV offset voltage and DC gains of 1 million (LT1464/LT1465) or 600,000 (LT1462/LT1463) even with 10k loads.

THE LT1210: HIGH POWER OP AMP YIELDS HIGHER VOLTAGE AND CURRENT
by Dale Eagar

Introduction

The LT1210, a 1 amp current feedback operational amplifier, opens up new frontiers. With 30MHz bandwidth, operation on ±15V supplies, thermal shutdown and 1 amp of output current, this amplifier single-handedly tackles many tough applications. But can it handle output voltages higher than ±15V or currents greater than 1 ampere? This Design Idea features a collection of circuits that open the door to high voltage and high current for the LT1210.

Fast and Sassy—Telescoping Amplifiers

Need ±30V? Cascading LT1210's will get you there. This circuit (Figure 80) will provide the ±30V at ±1A and has 13MHz of full-power bandwidth (see Figure 81). How does it work? The first LT1210 drives the "ground" of the second LT1210 subcircuit, effectively raising and lowering

it while the second LT1210 further amplifies the input signal. This telescoping arrangement can be cascaded with additional stages to get more than ±30V. This amplifier is stable into capacitive loads, is short-circuit protected and thermally shuts down when overheated.

Extending Power Supply Voltages

Another method of getting high voltage from an amplifier is the extended-supply mode (see "Extending Op Amp Supplies to Get More Voltage"; *Linear Technology* Volume IV Number 2 (June 1994), pp. 20–22). This involves steering two external regulators with the power supply pins of an op amp to get a high voltage amplifier.

Figure 82 shows the LT1210 connected in the extended-supply mode. Placing an amplifier in the extended-supply mode requires changing the return of the compensation node from the power supply pins to system ground. R9 and C5 are selected for clean step response. The process of relocating the return of the compensation node slows the amplifier down to approximately 1MHz (see Figure 83).
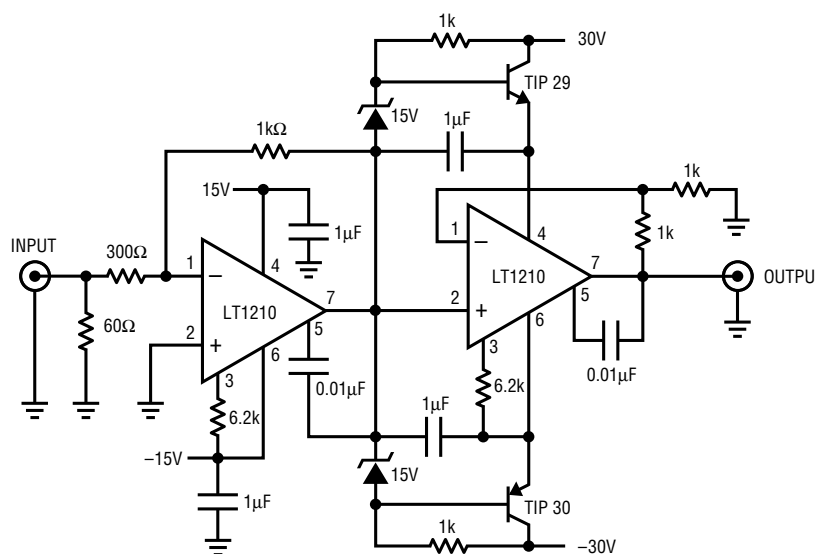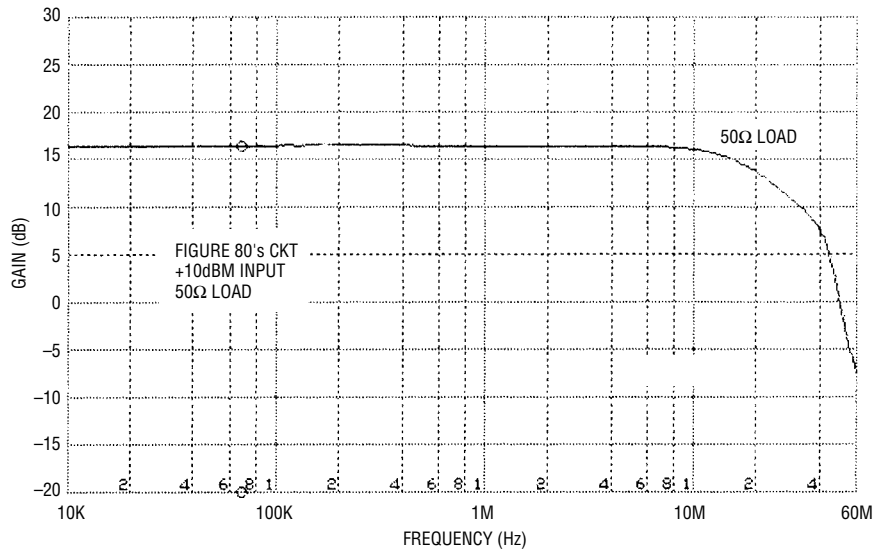

Figure 80. Telescoping Amplifiers

Figure 81. Gain vs Frequency Plot of Telescoping Amplifier

Figure 82's circuit will provide ±1A at ±100V, is stable into capacitive loads and is short-circuit protected. The two external MOSFETs need heat sinking.

Gateway to the Stars

The circuit of Figure 82 can be expanded to yield much higher voltages; the first and most obvious way is to use higher voltage MOSFETs. This causes two problems: first, high voltage P-channel MOSFETs are hard to get; second, and more importantly, at ±1A the power dissipated by the MOSFETs is too high for single packages. The solution is to build telescoping regulators, as shown in Figure 84. This circuit can provide ±1A of current at ±200V and has the additional power-dissipation ability of four MOSFETs.

Boosting Output Current

The current booster detailed in Figure 85 illustrates a technique for amplifying the output current capability of an op amp while maintaining speed. Among the many niceties of this topology is the fact that both Q1 and Q2 are normally off and thus consume no quiescent current. Once the load current reaches approximately 100mA, Q1 or Q2 turns on, providing additional drive to the output. This transition is seamless to the outside world and takes advantage of the full speed of Q1 and Q2. This circuit's small-signal bandwidth and full-power bandwidth are shown in Figure 86.

Boosting Both Current and Voltage

The current-boosted amplifier shown in Figure 85 can be used to replace the amplifiers in Figure 80, yielding ±10A at ±30V. Placing the boosted amplifier in the circuits shown in Figures 82 or 84 will yield peak powers into the kilowatts.

Thermal Management

When the LT1210 is used with external transistors to increase its output voltage and/or current range an
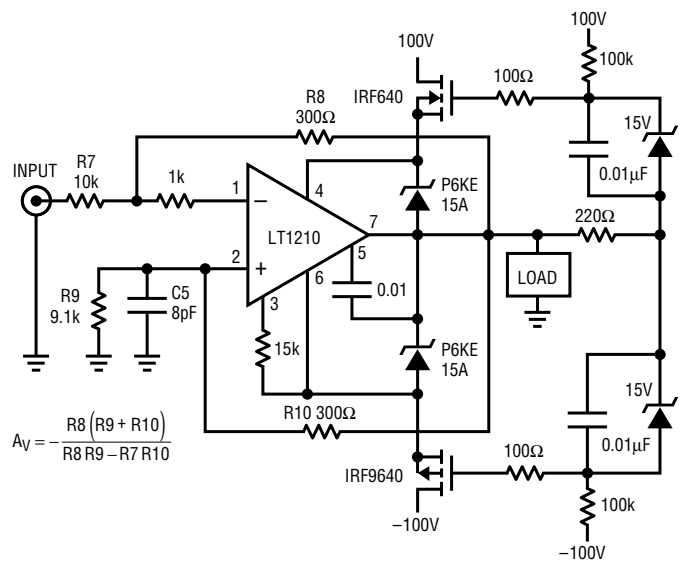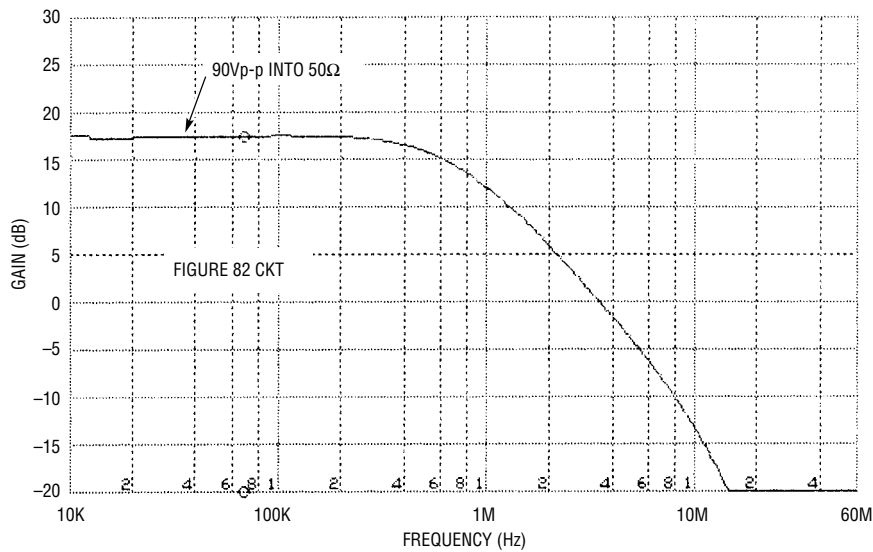

$$A_V = -\frac{R8\,(R9 + R10)}{R8\,R9 - R7\,R10}$$

Figure 82. ±100V, ±1A Power Driver

Figure 83. Gain vs Frequency Plot of Extended-Supply Amplifier
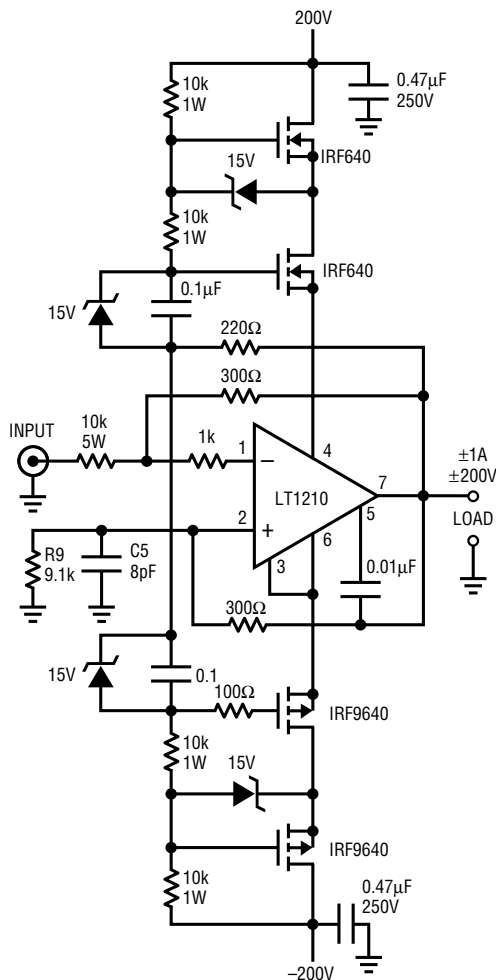
additional benefit can often be realized: system thermal shutdown. Careful analysis of the thermal design of the system can coordinate the overtemperature shutdown of the LT1210 with the junction temperatures of the external transistors. This essentially extends the umbrella of protection of the LT1210's thermal shutdown to cover the external transistors. The thermal shutdown of the LT1210 activates when the junction temperature reaches 150°C and has about 10°C hysteresis. The thermal resistance $R_{\theta JC}$ of the TO-220 package (LT1210CY) is 5°C/Watt).
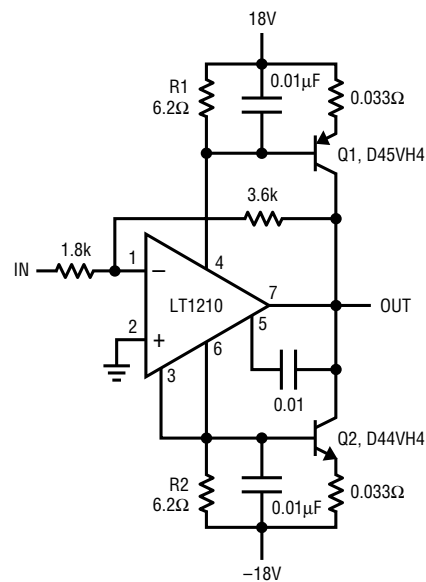

Figure 84. Cascode Power Amplifier

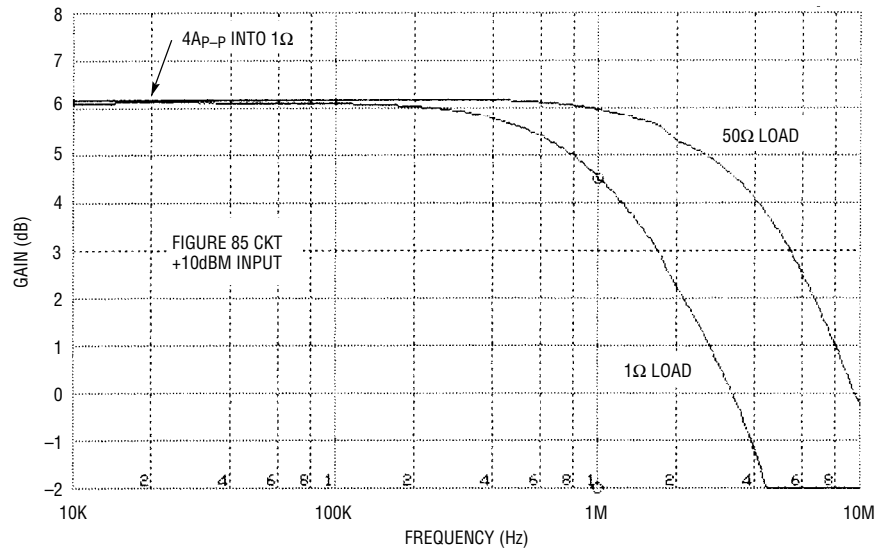Figure 85. ±10A/1MHz Current-Boosted Power Op Amp

Figure 86. Gain vs Frequency Response of Current-Boosted Amplifier

Summary

The LT1210 is a great part; its performance in terms of speed, output current and output voltage is unsurpassed. Its C-Load™ output drive and thermal shutdown allow it to take its place in the real world—no kid gloves are required here. If the generous output specification of the LT1210 isn't big enough for your needs, just add a couple of transistors to dissipate the additional power and you are on your way. Only the worldwide supply of transistors limits the amount of power you could command with one of these parts.

NEW RAIL-TO-RAIL AMPLIFIERS: PRECISION PERFORMANCE FROM MICROPOWER TO HIGH SPEED
by William Jett and Danh Tran

Introduction

Linear Technology's latest offerings expand the range of rail-to-rail amplifiers with precision specifications. Rail-to-rail amplifiers present an attractive solution for signal conditioning in many applications. For battery-powered or other low voltage circuitry, the entire supply voltage can be used by both input and output signals, maximizing the system's dynamic range. Circuits that require signal sensing near the positive supply are straightforward using a rail-to-rail amplifier.

Applications

The ability to accommodate any input or output signal that falls within the amplifier supply range makes these amplifiers very easy to use. The following applications demonstrate the versatility of the family of amplifiers.
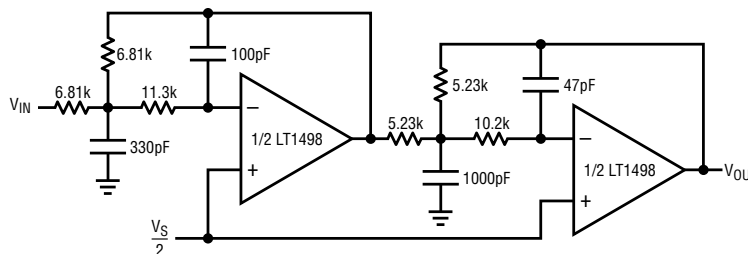

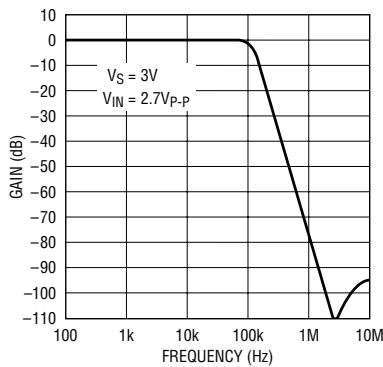Figure 87. 100kHz 4th Order Butterworth Filter

Application Note 87

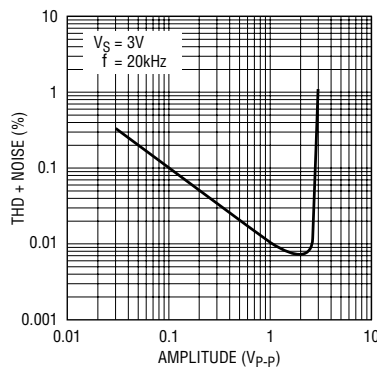**Figure 88. Filter Frequency Response**

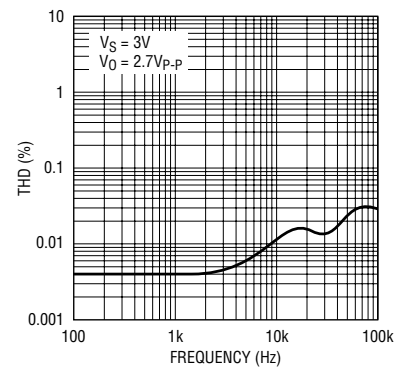**Figure 89. Filter Distortion vs Amplitude**

Figure 90. Filter Distortion vs Frequency

100kHz 4th Order Butterworth Filter for 3V Operation

The filter shown in Figure 87 uses the low voltage operation and wide bandwidth of the LT1498. Operating in the inverting mode for lowest distortion, the output swings rail-to-rail. The graphs in Figures 88–90 display the measured lowpass and distortion characteristics with a 3V power supply. As seen from the graphs, the distortion with a $2.7V_{P-P}$ output is under 0.03% for frequencies up to the cutoff frequency of 100kHz. The stop band attenuation of the filter is greater than 90dB at 10MHz.

Multiplexer

A buffered MUX with good offset characteristics can be constructed using the shutdown feature of the LT1218. In shutdown, the output of the LT1218 assumes a high impedance, so the outputs of two devices can be tied together (wired OR, as they say in the digital world). As shown in Figure 91, the shutdown pins of each LT1218 are driven by a 74HC04 buffer. The LT1218 is active with the shutdown pin high. The photo in Figure 92 shows the switching characteristics with a 1kHz sine wave applied to one input and the other input tied to ground. As shown, each amplifier is connected for unity gain, but either amplifier or both could be configured for gain.

Conclusion

The latest members of LTC's family of rail-to-rail amplifiers expand the versatility of rail-to-rail operation to micropower and high speed applications. The devices maintain

precision V_{OS} specifications over the entire rail-to-rail input range and have open loop gains of one million or more. These characteristics, combined with low voltage operation, makes for truly versatile amplifiers.
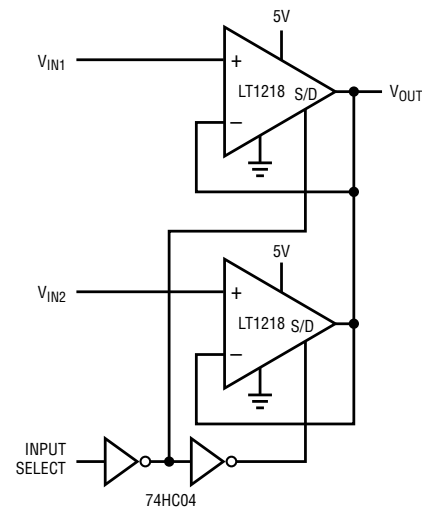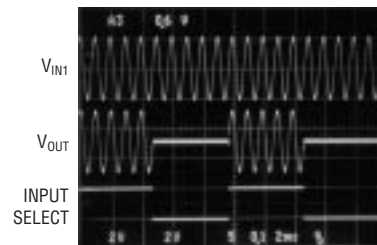

Figure 91. MUX Amplifier

Figure 92. MUX Amplifier Waveforms

LT1256 VOLTAGE-CONTROLLED AMPLITUDE LIMITER
by Frank Cox

Amplitude-limiting circuits are useful where a signal should not exceed a predetermined maximum amplitude, such as when feeding an A/D or a modulator. A clipper, which completely removes the signal above a certain level, is useful for many applications, but there are times when it is not desirable to lose information. For instance, when video signals have amplitude peaks that exceed the dynamic range of following processing stages, simply clipping the peaks at the maximum level will result in the loss of all detail in the areas where clipping takes place. Often these well illuminated areas are the primary subject of the scene. Because these peaks usually correspond to the highest level of luminosity, they are referred to as "highlights." One way to preserve some of the detail in the highlights is to automatically reduce the gain (compress) at high signal levels.

The circuit in Figure 93 is a voltage-controlled breakpoint amplifier that can be used for highlight compression. When the input signal reaches a predetermined level (the breakpoint), the amplifier gain is reduced. As both the breakpoint and the gain for signals greater than the breakpoint are voltage programmable, this circuit is useful for systems that adapt to changing signal levels. Adaptive highlight compression finds use in CCD video cameras,

which have a very large dynamic range. Although this circuit was developed for video signals, it can be used to adaptively compress any signal within the 40MHz bandwidth of the LT1256.

The LT1256 video fader is connected to mix proportional amounts of input signal and clipped signal to provide a voltage-controlled variable gain. The clipped signal is provided by a discrete circuit consisting of three transistors. Q1 acts as an emitter follower until the input voltage exceeds the voltage on the base of Q2 (the breakpoint voltage or V_{BP}). When the input voltage is greater than V_{BP}, Q1 is off and Q2 clamps the emitters of the two transistors to V_{BP} plus a V_{BE}. Q3, an NPN emitter follower,
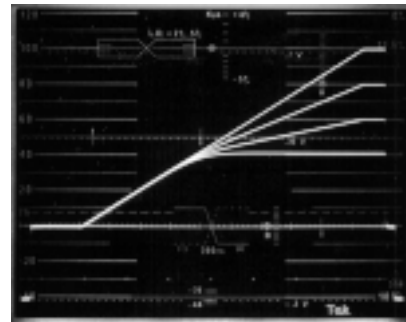

Figure 94. Multiple-Exposure Photograph of a Single Line of Monochrome Video, Showing Four Different Levels of Compression
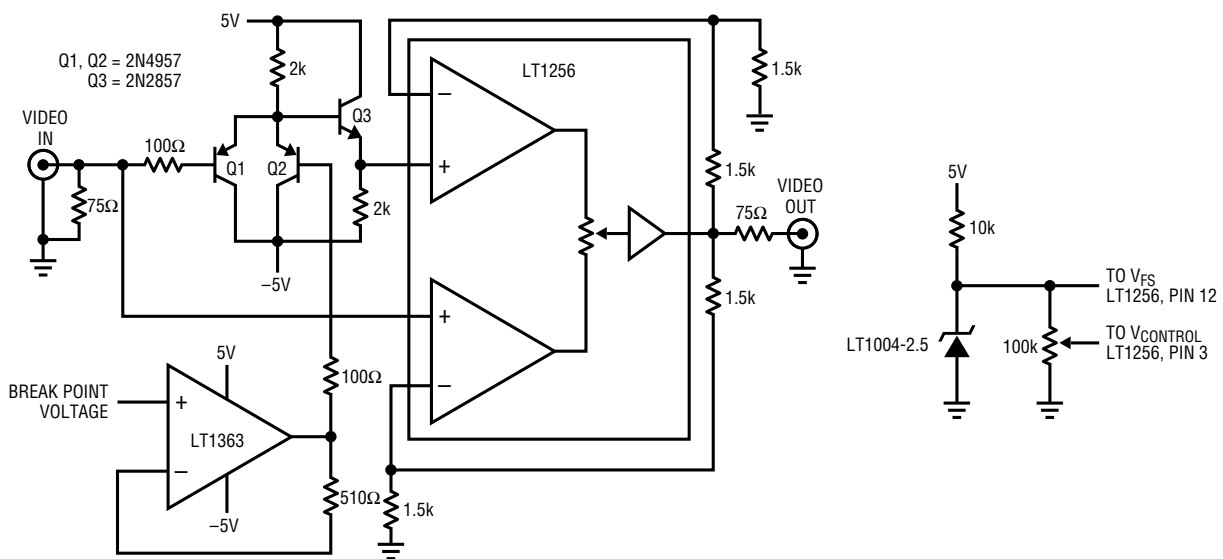

Figure 93. Voltage-Controlled Amplitude Limiter

buffers the output and drops the voltage a V_{BE} and thus the DC level of the input signal is preserved to the extent allowed by the V_{BE} matching and temperature tracking of the transistors used. The breakpoint voltage at the base of Q2 must remain constant when this transistor is turning on or the signal will be distorted. The LT1363 maintains a low output impedance well beyond video frequencies and makes an excellent buffer.

Figure 94 is a multiple-exposure photograph of a single line of monochrome video, showing four different levels of compression ranging from fully limited signal to unprocessed input signal. The breakpoint is set to 40% of the peak amplitude to clearly show the effect of the circuit; normally only the top 10% of video would be compressed.

THE LT1495/LT1496: 1.5μA RAIL-TO-RAIL OP AMPS
by William Jett

Introduction

Micropower rail-to-rail amplifiers present an attractive solution for battery-powered and other low voltage circuitry. Low current is always desirable in battery-powered applications, and a rail-to-rail amplifier allows the entire supply range to be used by both the inputs and the output, maximizing the system's dynamic range. Circuits that require signal sensing near either supply rail are easier to implement using rail-to-rail amplifiers. However, until now, no amplifier combined precision offset and drift specifications with a maximum quiescent current of 1.5μA.

Operating on a minuscule 1.5μA per amplifier, the LT1495 dual and LT1496 quad rail-to-rail amplifiers consume almost no power while delivering precision performance associated with much higher current amplifiers.

The LT1495/LT1496 feature "Over-The-Top" operation: the ability to operate normally with the inputs above the positive supply. The devices also feature reverse-battery protection.

Applications

The ability to accommodate any input or output signal that falls within the amplifier supply range makes the LT1495/LT1496 very easy to use. The following applications highlight signal processing at low currents.

Nanoampere Meter

A simple 0nA–200nA meter operating from two flashlight cells or one lithium battery is shown in Figure 95. The readout is taken from a 0μA–200μA, 500Ω analog meter; the LT1495 supplies a current gain of 1000 in this application. The op amp is configured as a floating I-to-I converter. It consumes only 3μA when not in use, so there is no need for an on/off switch. Resistors R1, R2 and R3 set the current gain. R3 provides a ±10% full-scale adjust for the meter movement. With a 3V supply, maximum current in the meter is limited by R2 + R3 to less than 300μA, protecting the movement. Diodes D1 and D2 and resistor R4 protect the inputs from faults up to 200V. Diode currents are below 1nA in normal operation, since the maximum voltage across the diodes is 375μV, the V_{OS} of the LT1495. C1 acts to stabilize the amplifier, compensating for capacitance between the inverting input and ground. The unused amplifier should be connected as shown for minimum supply current. Error terms from the amplifier (base currents, offset voltage) sum to less than 0.5% over the operating range, so the accuracy is limited by the analog meter movement.
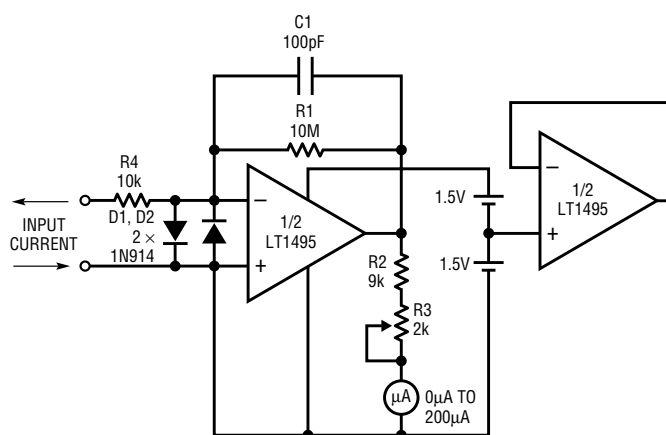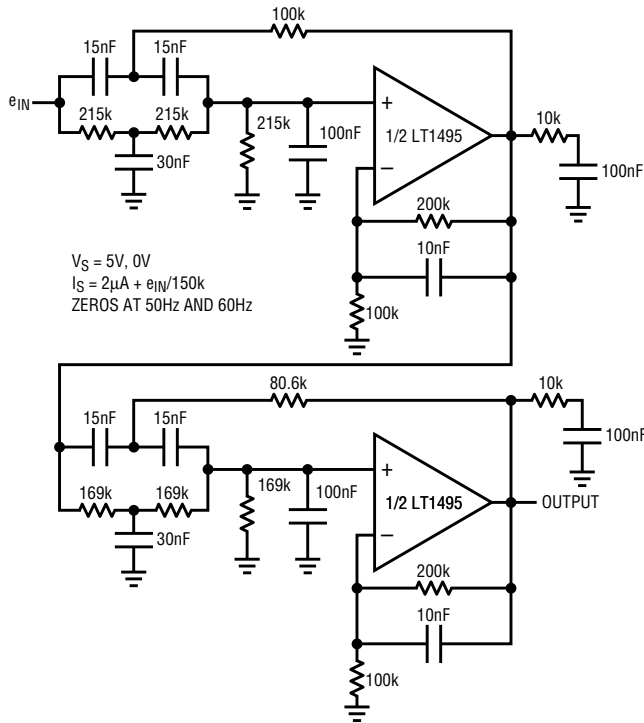

Figure 95. 0nA–200nA Current Meter

$V_S = 5V, 0V$
$I_S = 2\mu A + e_{IN}/150k$
ZEROS AT 50Hz AND 60Hz

Figure 96. 6th Order 10Hz Elliptic Lowpass Filter

6th Order, 10Hz Elliptic Lowpass Filter

Figure 96 shows a 6th order, 10Hz elliptic lowpass filter with zeros at 50Hz and 60Hz. Supply current is primarily determined by the DC load on the amplifiers and is approximately $2\mu A + V_O/150k$ ($9\mu A$ for $V_O = 1V$). The overall frequency response is shown in Figure 97. The notch depth of the zeros at 50Hz and 60Hz is nearly 60dB and the stopband attenuation is greater than 40dB out to
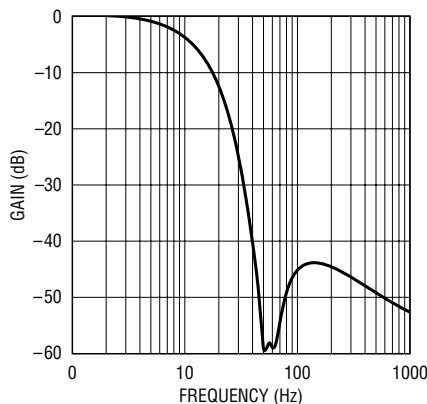
1kHz. As with all RC filters, the filter characteristics are determined by the absolute values of the resistors and capacitors, so resistors should have a 1% tolerance or better and capacitors a 5% tolerance or better.

Battery-Current Monitor with Over-the-Top Operation

The bidirectional current sensor shown in Figure 98 takes advantage of the extended common mode range of the LT1495 to sense currents into and out of a 12V battery while operating from a 5V supply. During the charge cycle, op amp A1 controls the current in Q1 so that the voltage drop across R_A is equal to $I_L \cdot R_{SENSE}$. This voltage is then amplified at the charge output by the ratio of R_A to R_B. During this cycle, amplifier A2 sees a negative offset, which keeps Q2 off and the discharge output low. During the discharge cycle, A2 and Q2 are active and operation is similar to that during the charge cycle.

Conclusion

The LT1495/LT1496 extends Linear Technology's range of rail-to-rail amplifier solutions to a truly micropower level. The combination of extremely low current and precision specifications provides designers with a versatile solution for battery-operated devices and other low power systems.
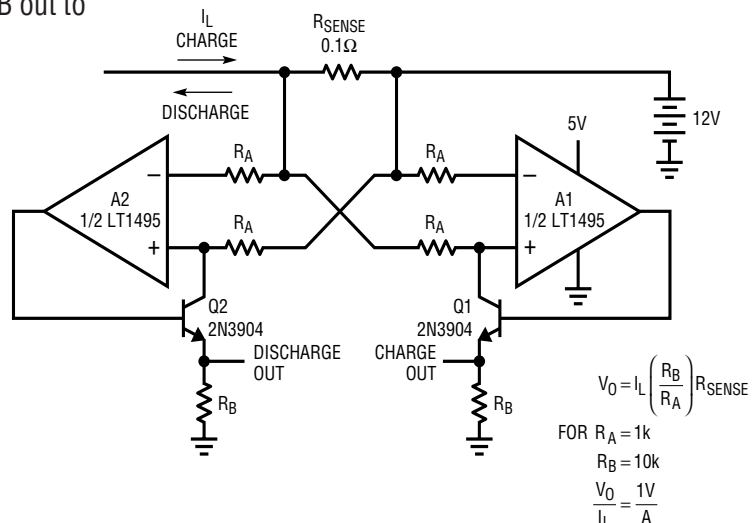

Figure 97. Frequency Response of Figure 96's 6th Order Elliptic Lowpass Filter

$$V_O = I_L \left(\frac{R_B}{R_A} \right) R_{SENSE}$$

FOR $R_A = 1k$
$R_B = 10k$
$\dfrac{V_O}{I_L} = \dfrac{1V}{A}$

Figure 98. Battery-Current Monitor

SEND CAMERA POWER AND VIDEO
ON THE SAME COAX CABLE
by Frank Cox

Because remotely located video surveillance cameras do not always have a ready source of power, it is convenient to run both the power and the video signal through a single coax cable. One way to do this is to use an inductor to present a high impedance to the video and a low impedance to the DC. The difficulty with this method is that the frequency spectrum of a monochrome video signal extends down to at least 30Hz. The composite color video spectrum goes even lower, with components at 15Hz. This implies a rather large inductor. For example, a 0.4H inductor has an impedance of only 75Ω at 30Hz, which is about the minimum necessary. Large inductors have a large series resistance that wastes power. More importantly, large inductors can have a significant amount of parasitic capacitance and stand a good chance of going into self resonance below the 4MHz video bandwidth and

thus corrupting the signal. The circuit shown in Figure 99 takes a different approach to the problem by using all active components.

The circuitry at the monitor end of the coax cable supplies all the power to the system. U1, an LT1206 current feedback amplifier, forms a gyrator or synthetic inductor. The gyrator isolates the low impedance power supply from the cable by maintaining a reasonably high impedance over the video bandwidth while, at the same time, contributing only 0.1Ω of series resistance. This op amp needs to have enough bandwidth for video and sufficient output drive to supply 120mA to the camera. The selected part has a guaranteed output current of 250mA and a 3dB bandwidth of 60MHz, making it a good fit. Because the video needs to be capacitively coupled, there is no need for split supplies; hence a single 24V supply is used. The 24V supply also gives some headroom for the voltage drop in long cable runs.
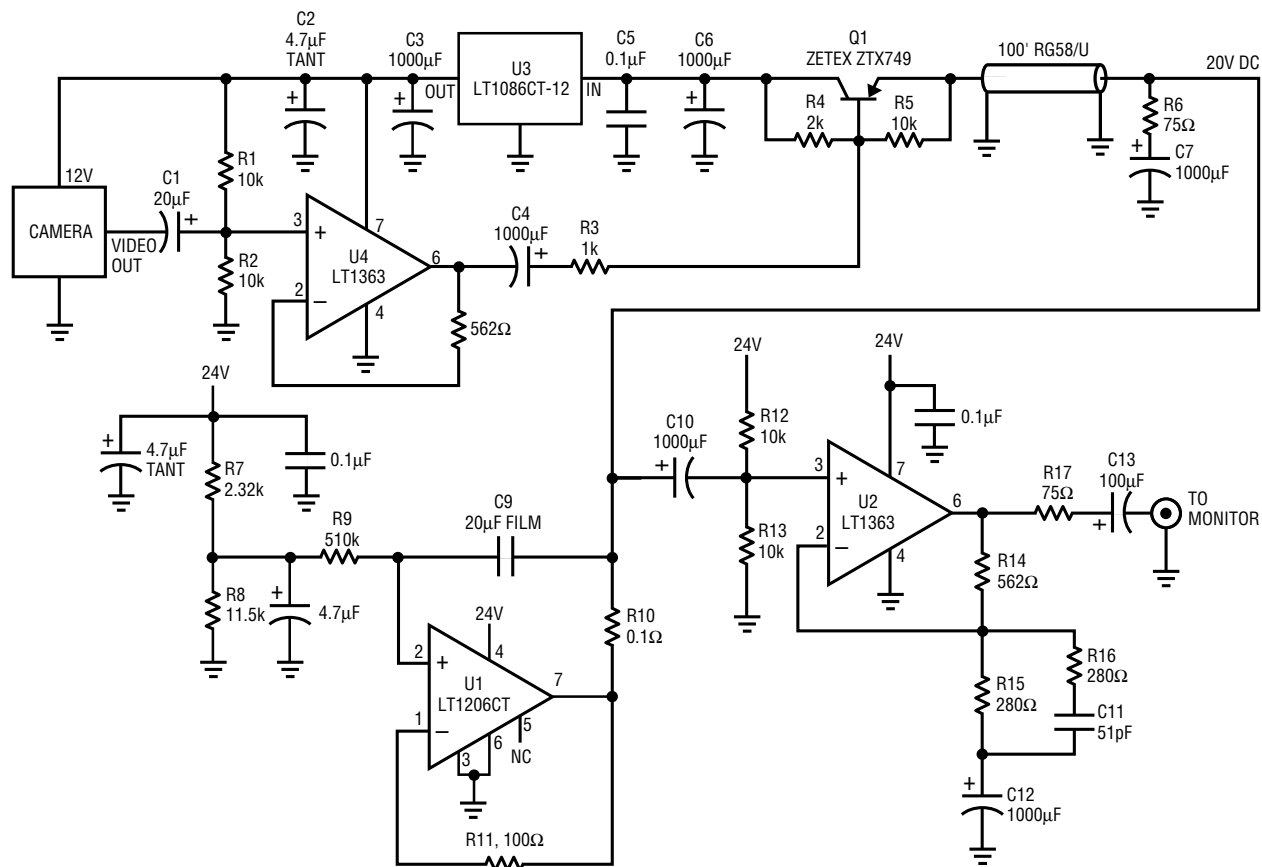

Figure 99. Circuit Transmits Video and 12V Power on the Same Coax Cable

The camera end has an LT1086 fixed 12V regulator (U3) to supply 12V to a black and white CCD video camera. U4, an LT1363 op amp, supplies the drive for Q1, a fast, high current transistor. Q1, in turn, modulates the video on the 20V DC. The collector of Q1 is the input to the 12V regulator. This point is AC ground because it is well bypassed as required by U3. U1 is set up to deliver 20V to the cable. Because the 12V regulator in the camera end needs 1.5V of dropout voltage, the balance of 6.5V can be dropped in the series resistance of the cable. The output of the LT1206 is set to 20V to give headroom between the supply and the video.

U2, another LT1363 video-speed op amp, receives video from the cable, supplies some frequency equalization and drives the cable to the monitor. Equalization is used to compensate for high frequency roll off in the camera cable. The components shown (R16, C11) gave acceptable monochrome video with 100 feet of RG58/U cable.

200μA, 1.2MHz RAIL-TO-RAIL OP AMPS HAVE OVER-THE-TOP INPUTS
by Raj Ramchandani

Introduction

The LT1638 is Linear Technology's latest general-purpose, low power, dual rail-to-rail operational amplifier; the LT1639 is a quad version. The circuit topology of the LT1638 is based on Linear Technology's popular LT1490/LT1491 op amps, with substantial improvements in speed. The LT1638 is five times faster than the LT1490.

Battery Current Monitor

The battery-current monitor shown in Figure 100 demonstrates the LT1639's ability to operate with its inputs above the positive rail. In this application, a conventional amplifier would be limited to a battery voltage between 5V and ground, but the LT1639 can handle battery voltages
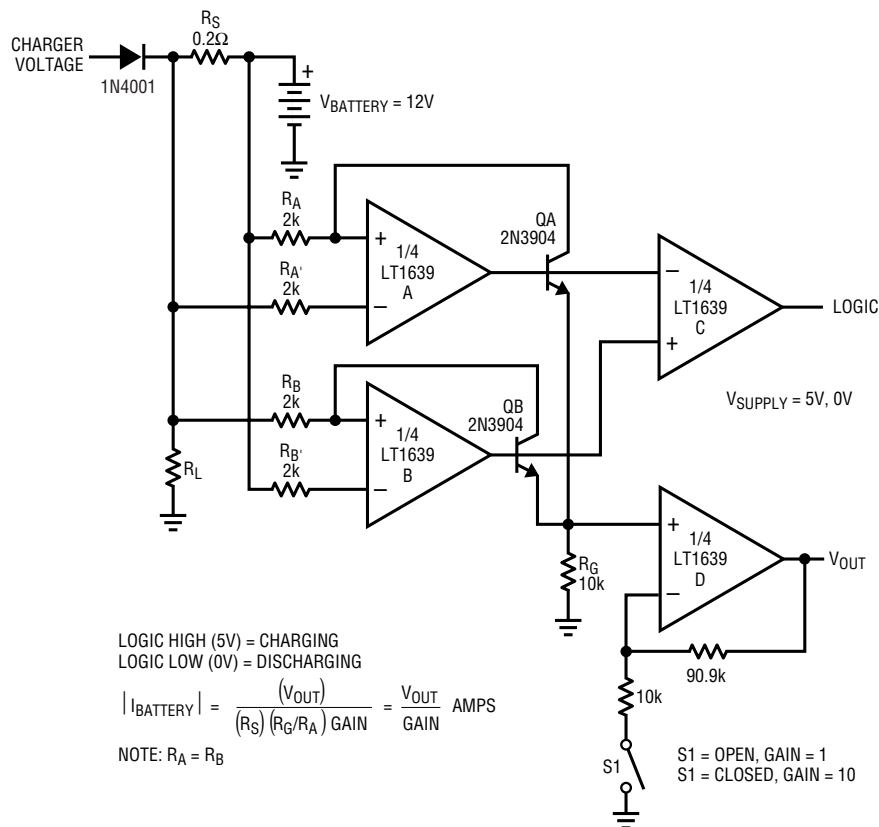

$$|I_{BATTERY}| = \frac{(V_{OUT})}{(R_S)(R_G/R_A) \, GAIN} = \frac{V_{OUT}}{GAIN} \, AMPS$$

LOGIC HIGH (5V) = CHARGING
LOGIC LOW (0V) = DISCHARGING

NOTE: $R_A = R_B$

S1 = OPEN, GAIN = 1
S1 = CLOSED, GAIN = 10

Figure 100. LT1639 Battery Current Monitor—an Over-The-Top Application

as high as 44V. The LT1639 can be shut down by removing V_{CC}. With V_{CC} removed, the input leakage is less then 0.1nA. No damage to the LT1639 will result from inserting the 12V battery backward.

When the battery is charging, amplifier B senses the voltage drop across R_S. The output of amplifier B causes Q_B to drain sufficient current through R_B to balance the inputs of amplifier B. Likewise, amplifier A and Q_A form a closed loop when the battery is discharging. The current

through Q_A or Q_B is proportional to the current in R_S. This current flows into R_G and is converted into a voltage. Amplifier D buffers and amplifies the voltage across R_G. Amplifier C compares the outputs of amplifier A and amplifier B to determine the polarity of current through R_S. The scale factor for V_{OUT} with S1 open is 1V/A. With S1 closed the scale factor is 1V/100mA and currents as low as 5mA can be measured.

LOW DISTORTION RAIL-TO-RAIL OP AMPS HAVE 0.003% THD WITH 100kHz SIGNAL
by Danh Tran

Introduction

The LT1630/LT1632 duals and LT1631/LT1633 quads are the newest members of Linear Technology's family of rail-to-rail op amps, which provide the best combination of AC performance and DC precision over the widest range of supply voltages. The LT1630/LT1631 deliver a 30MHz gain-bandwidth product, a 10V/µs slew rate and 6nV/√Hz input-voltage noise. Optimized for higher speed applications, the LT1632/LT1633 have a 45MHz gain-bandwidth product, a 45V/µs slew rate and 12nV/√Hz input voltage noise.

Applications

The ability to accommodate any input and output signals that fall within the device's supplies makes these amplifiers very easy to use. They exhibit a very good transient

response and can drive low impedance loads, which makes them suitable for high performance applications. The following applications demonstrate the versatility of these amplifiers.

400kHz 4th Order Butterworth Filter for 3V Operation

The circuit shown in Figure 101 makes use of the low voltage operation and the wide bandwidth of the LT1630 to create a 400kHz 4th order lowpass filter with a 3V supply. The amplifiers are configured in the inverting mode for the lowest distortion and the output can swing rail-to-rail for the maximum dynamic range. Figure 102 displays the frequency response of the filter. Stopband attenuation is greater than 85dB at 10MHz. With a 2.25V_{P-P}, 100kHz input signal, the filter has harmonic distortion products of less than –87dBc.
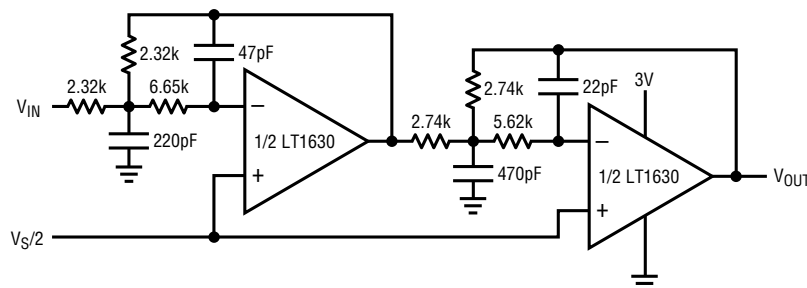

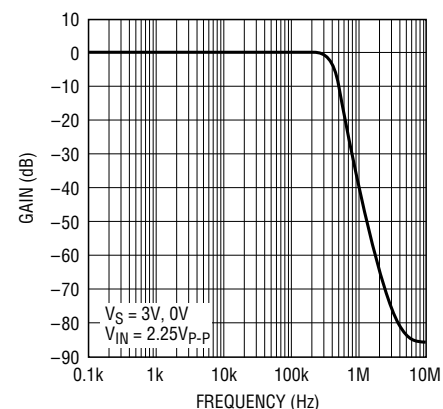**Figure 101. Single-Supply, 400kHz, 4th Order Butterworth Filter**

Figure 102. Frequency Response of Filter in Figure 101

40dB Gain, 550kHz Instrumentation Amplifier

An instrumentation amplifier with a rail-to-rail output swing, operating from a 3V supply, can be constructed with the LT1632, as shown in Figure 103. The amplifier has a nominal gain of 100, which can be adjusted with resistor R5. The DC output level is equal to the input voltage (V_{IN}) between the two inputs multiplied by the gain of 100.

Common mode range can be calculated by the equations shown with Figure 103. For example, the common mode range is from 0.15V to 2.65V if the output voltage is at one-half of the 3V supply. The common mode rejection is greater than 110dB at 100Hz when trimmed with resistor R1. Figure 103 shows the amplifier's cutoff frequency of 550kHz.
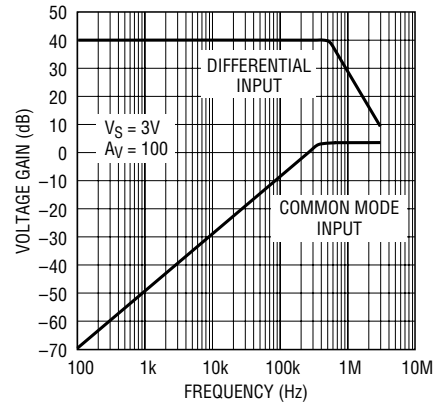

$$V_{CM_L} = \left[\left(\frac{V_{OUT(DC)}}{A_V}\right)\frac{R2}{R5} + 0.1V\right]\frac{1.0}{1.1}$$
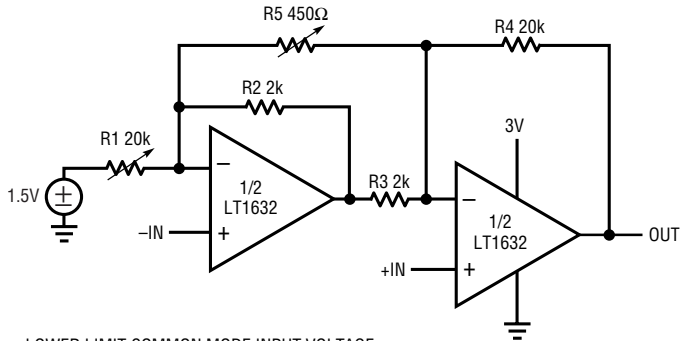
UPPER LIMIT COMMON MODE INPUT VOLTAGE

$$V_{CM_H} = \left[\left(\frac{V_{OUT(DC)}}{A_V}\right)\frac{R2}{R5} + 2.85V\right]\frac{1.0}{1.1}$$

$$A_V = \frac{R4}{R3}\left(1 + \frac{R2}{R1} + \frac{R3 + R2}{R5}\right) = 100$$

$$BW = 550kHz$$

$$V_{OUT(DC)} = (+IN - (-IN))_{DC} \times GAIN$$

Figure 103. Single-Supply Instrumentation Amplifier

Figure 104. Frequency Response of Figure 103's Instrumentation Amplifier

THE LT1167: PRECISION, LOW COST, LOW POWER INSTRUMENTATION AMPLIFIER REQUIRES A SINGLE GAIN-SET RESISTOR
by Alexander Strong

Introduction

The LT1167 is the next-generation instrumentation amplifier designed to replace the previous generation of monolithic instrumentation amps, as well as discrete, multiple op amp solutions. Instrumentation amplifiers differ from operational amplifiers in that they can amplify input signals that are not ground referenced. The output of an instrumentation amplifier is referenced to an external voltage that is independent of the input. Conversely, the output voltage of an op amp, due to the nature of its feedback, is referenced to the differential and common mode input voltage.

Applications

Single-Supply Pressure Monitor

The LT1167's low supply current, low supply voltage operation and low input bias current (350pA max) allow it to fit nicely into battery powered applications. Low overall power dissipation necessitates using higher impedance bridges. Figure 105 shows the LT1167 connected to a 3kΩ bridge's differential output. The picoampere input bias currents will still keep the error caused by offset current to a negligible level. The LT1112 level shifts the LT1167's reference pin and the ADC's analog ground pins above ground. This is necessary in single-supply applications because the output cannot swing to ground. The LT1167's and LT1112's combined power dissipation is still less than the bridge's. This circuit's total supply current is just 3mA.
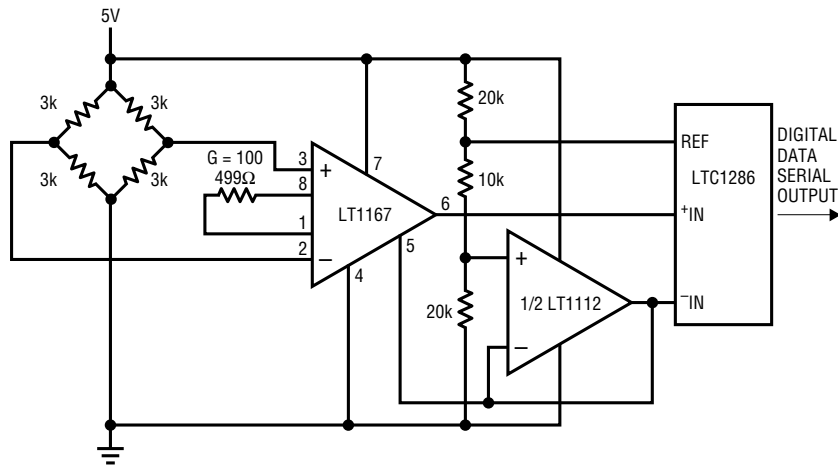
Figure 105. Single-Supply Pressure Monitor

ADC Signal Conditioning

The LT1167 is shown in Figure 106 changing a differential signal into a single-ended signal. The single-ended signal is then filtered with a passive 1st order RC lowpass filter and applied to the LTC1400 12-bit analog-to-digital converter (ADC). The LT1167's output stage can easily drive the ADC's small nominal input capacitance, preserving signal integrity. Figure 107 shows two FFTs of the amplifier/ADC's output. Figures 107a and 107b show the results of operating the LT1167 at unity gain and a gain of ten, respectively. This results in a typical SINAD of 70.6dB.
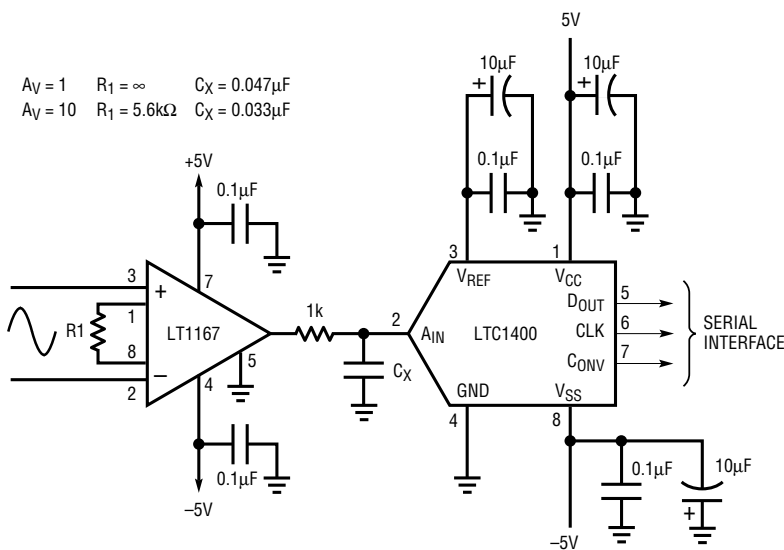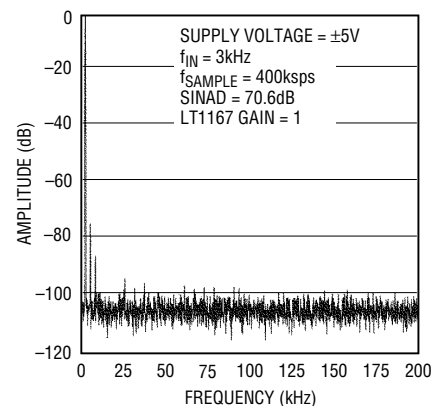

(A)

(B)

$A_V = 1$ $R_1 = \infty$ $C_X = 0.047\mu F$
$A_V = 10$ $R_1 = 5.6k\Omega$ $C_X = 0.033\mu F$
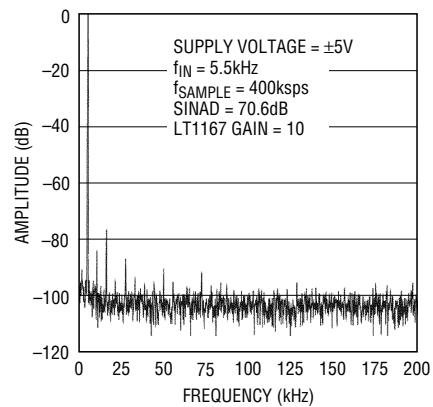
Figure 106. The LT1167 Converting Differential Signals to Single-Ended Signals; the LT1167 is Ideal for Driving the LTC1400

Figure 107. Operating at a Gain of One (A) or Ten (B), Figure 106's Circuit Achieves 12-Bit Operation with a SINAD of 70.6dB

Current Source

Figure 108 shows a simple, accurate, low power programmable current source. The differential voltage across pins 2 and 3 is mirrored across R_G. The voltage across R_G is amplified and applied across R1, defining the output current. The 50μA bias current flowing from pin 5 is buffered by the LT1464 JFET operational amplifier, which increases the resolution of the current source to 3pA.

Nerve-Impulse Amplifier

The LT1167's low current noise makes it ideal for ECG monitors that have MΩ source impedances. Demonstrating the LT1167's ability to amplify low level signals, the circuit in Figure 109 takes advantage of the amplifier's high gain and low noise operation. This circuit amplifies the low level nerve impulse signals received from a patient at pins 2 and 3 of the LT1167. R_G and the parallel combination of R3 and R4 set a gain of ten. The potential on LT1112's pin 1 creates a ground for the common mode signal. The LT1167's high CMRR of 110db ensures that the desired differential signal is amplified and unwanted common mode signals are attenuated. Since the DC portion of the signal is not important, R6 and C2 make up a 0.3Hz highpass filter. The AC signal at LT1112's pin 5 is amplified by a gain of 101 set by R7/R8 + 1. The parallel combination of C3 and R7 forms a lowpass filter that decreases this gain at frequencies above 1kHz.
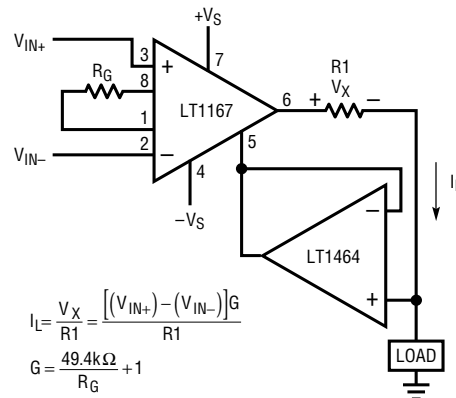

$$I_L = \frac{V_X}{R1} = \frac{[(V_{IN+}) - (V_{IN-})]G}{R1}$$

$$G = \frac{49.4k\Omega}{R_G} + 1$$

Figure 108. Precision Current Source

The ability to operate at ±3V on 0.9mA of supply current makes the LT1167 ideal for battery-powered applications. Total supply current for this application is 1.7mA. Proper safeguards, such as isolation, must be added to this circuit to protect the patient from possible harm.

Conclusion

The LT1167 instrumentation amplifier delivers the best precision, lowest noise, highest fault tolerance, plus the ease of use provided by single-resistor gain setting. The LT1167 is offered in 8-pin PDIP and SO packages. The SO uses significantly less board space than discrete designs.
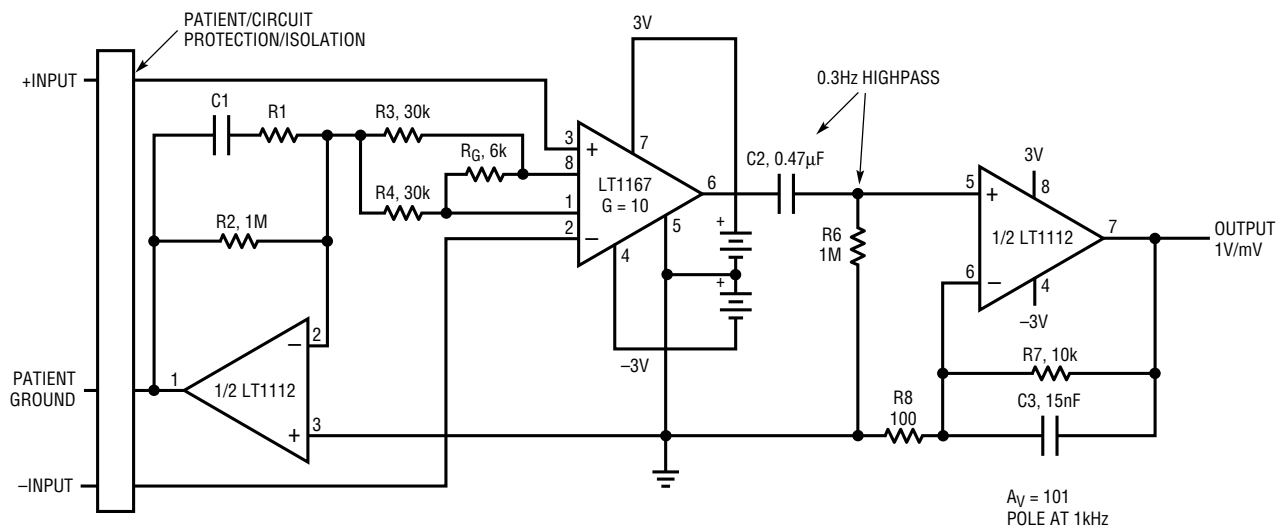

Figure 109. Medical ECG Monitor

LEVEL SHIFT ALLOWS CFA VIDEO AMPLIFIER TO SWING TO GROUND ON A SINGLE SUPPLY
by Frank Cox

A current feedback (CFA) video amplifier can be made to run off a single supply and still amplify ground-referenced video with the addition of a simple and inexpensive level shifter. The circuit in Figure 110 is an amplifier and cable driver for a current output video DAC. The video can be composite or component but it must have sync. The single positive supply is 12V but could be as low as 6V for the LT1227.

The output of the LT1227 CFA used here can swing to within 2.5V of the negative supply with a 150Ω load over the commercial temperature range of 0°C to 70°C. Five diodes in the feedback loop are used, in conjunction with C5, to level shift the output to ground. The video from the output of the LT1227 charges C5 and the voltage across it allows the output to swing to ground or even slightly negative. However, the level of this negative swing will depend on the video signal and so will be unpredictable. When the scene is black, there must be sync on the video for C5 to remain charged. A zero-level component video signal with no sync will not work with this circuit. The CFA output will try to go to zero, or as low as it can, and the

diodes will turn off. The load will be disconnected from the CFA output and connected through the feedback resistor to the network of R6 and R7. This causes about 150mVDC to appear at the output, instead of the 0V that should be there.

The ground-referenced video signal at the input needs to be level shifted into the input common mode range of the LT1227 (3V above negative supply). R4 and R5 shift the input signal to 3V. In the process, the input video is attenuated by a factor of 2.5. For correct gain, no offset and with a zero source impedance, R4 would be 1.5k. To compensate for the presence of R3, R4 is made 1.5k minus R3, or 1.46k. The trade off is a gain error of about 1.5%. If R4 is left 1.5k, the gain is correct, but there is an offset error of 75mV. R6, R7 and R8 set the gain and the output offset of the amplifier. A noninverting gain of five is taken to compensate for the attenuation in the input level shifter and the cable termination.

The voltage offset on the output of this circuit is a rather sensitive function of the value of the input resistors. For instance, an error of 1% in the value of R6 will cause an offset of 30mV (1% of 3V) on the output. This is in addition to the offset error introduced by the op amp. Precision resistor networks are available (BI Technologies,
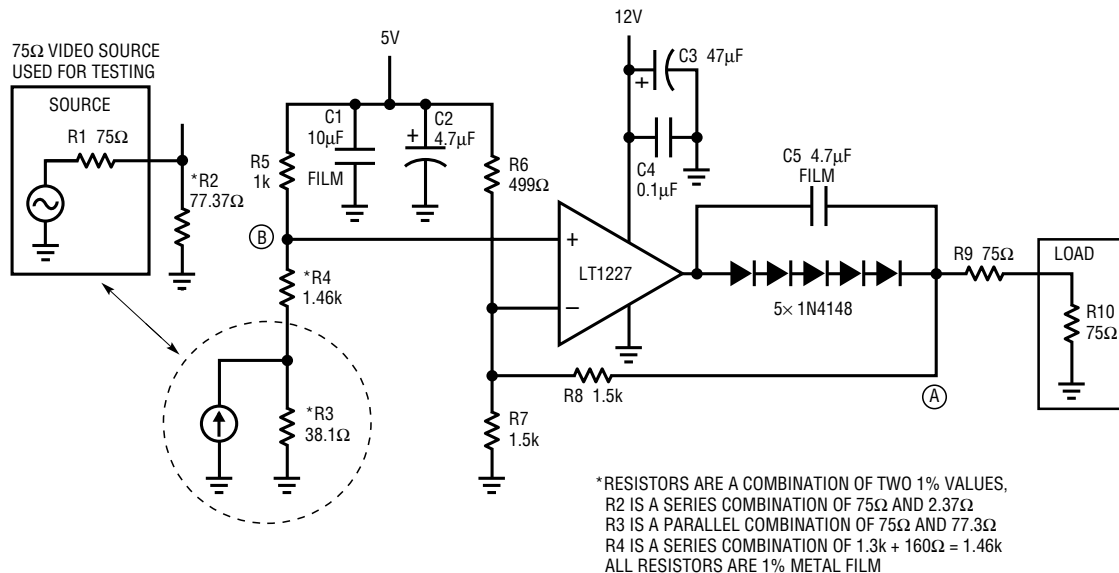

*RESISTORS ARE A COMBINATION OF TWO 1% VALUES,
R2 IS A SERIES COMBINATION OF 75Ω AND 2.37Ω
R3 IS A PARALLEL COMBINATION OF 75Ω AND 77.3Ω
R4 IS A SERIES COMBINATION OF 1.3k + 160Ω = 1.46k
ALL RESISTORS ARE 1% METAL FILM

Figure 110. Amplifier and Cable Driver for Current-Output Video DAC

714-447-2345) with matching specifications of 0.1% or better. These could be used for the level shifting resistors, although this would make adjustments like the one made to R4 difficult.

Fortunately, there is always synchronization information associated with video. A simple circuit can be used to DC restore voltage offsets produced by resistor mismatch, op amp offset or DC errors in the input video. Figure 111 shows the additional circuitry needed to perform this

function. The LTC201A analog switch and C1 store the offset error during blanking. The clamp pulse should be 3μs or wider and should occur during blanking. It can conveniently be made by delaying the sync pulse with one shots. If the sync tip is clamped, the clamp pulse must start after and end before the sync pulse or offset errors will be introduced. The integrator made with the LT1632 adjusts the voltage at point B (see Figure 110) to correct the offset.
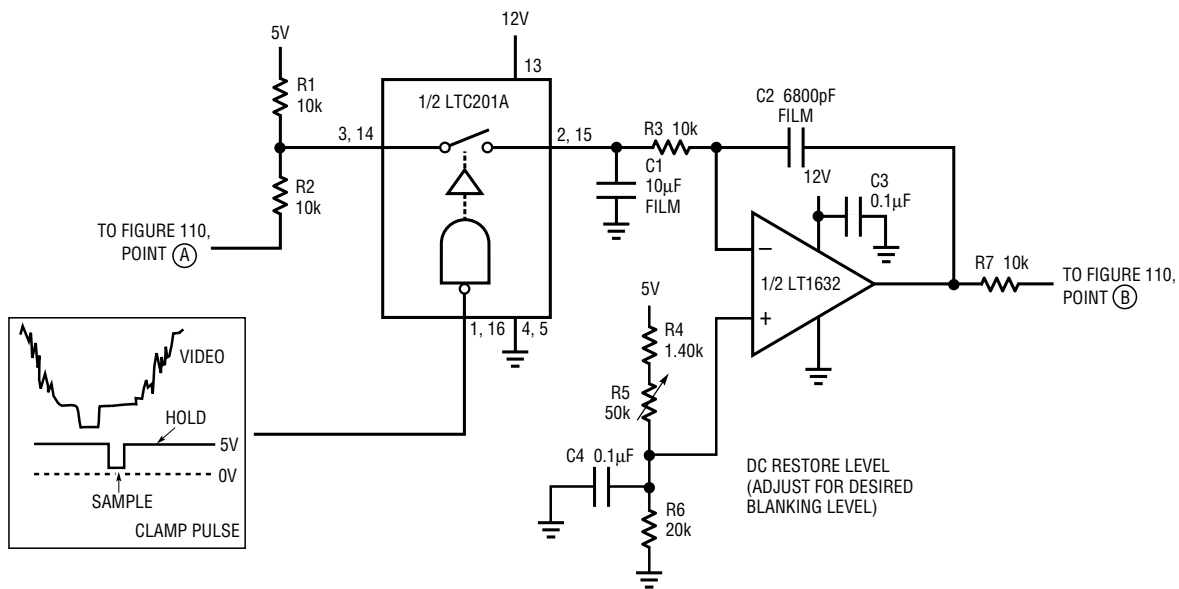
Figure 111. DC Restore Subcircuit

LT1468: AN OPERATIONAL AMPLIFIER FOR FAST, 16-BIT SYSTEMS
by George Feliz

Introduction

The LT1468 is a single operational amplifier that has been optimized for accuracy and speed in 16-bit systems. Operating from ±15V supplies, the LT1468 in a gain of –1 configuration will settle in 900ns to 150μV for a 10V step. The LT1468 also features the excellent DC specifications required for 16-bit designs. Input offset voltage is 75μV max, input bias current is 10nA maximum for the inverting input and 40nA maximum for the noninverting input and DC gain is 1V/μV minimum.

16-Bit DAC Current-to-Voltage Converter with 1.7μs Settling Time

The key AC specification of the circuit of Figure 112 is settling time as it limits the DAC update rate. The settling time measurement is an exceptionally difficult problem that has been ably addressed by Jim Williams, in Linear Technology Application Note 74. Minimizing settling time is limited by the need to null the DAC output capacitance, which varies from 70pF to 115pF, depending on code. This capacitance at the amplifier input combines with the feedback resistor to form a zero in the closed-loop frequency response in the vicinity of 200kHz–400kHz. Without a feedback capacitor, the circuit will oscillate. The choice of 20pF stabilizes the circuit by adding a pole at
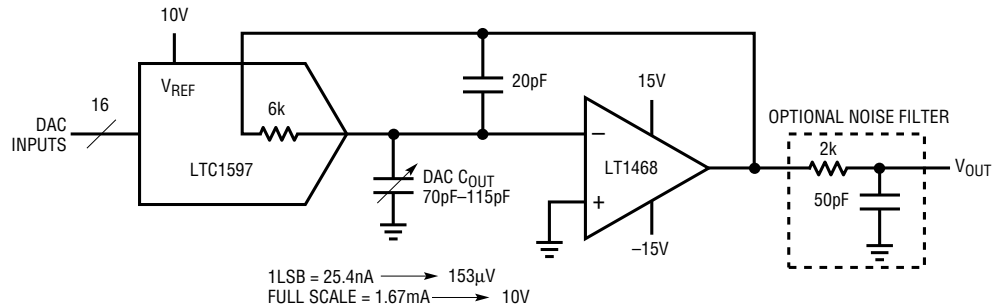
Figure 112. 16-Bit DAC I/V Converter with 1.7μs Settling Time

1.3MHz to limit the frequency peaking and is chosen to optimize settling time. The settling time to 16-bit accuracy is theoretically bounded by 11.1 time constants set by the 6kΩ and 20pF. Figure 112's circuit settles in 1.7μs to 150μV for a 10V step. This compares favorably with the 1.33μs theoretical limit and is the best result obtainable with a wide variety of LTC and competitive amplifiers. This excellent settling requires the amplifier to be free of thermal tails in its settling behavior.

The LTC1597 current output DAC is specified with a 10V reference input. The LSB is 25.4nA, which becomes 153μV after conversion by the LT1468, and the full-scale output is 1.67mA, which corresponds to 10V at the amplifier output. The zero-scale offset contribution of the LT1468 is the input offset voltage and the inverting input current flowing through the 6k feedback resistor. This worst-case total of 135μV is less than one LSB. At full-scale there is an insignificant additional 10μV of error due to the 1V/μV minimum gain of the amplifier. The low input offset of the amplifier ensures negligible degradation of the DAC's outstanding linearity specifications.

With its low 5nV/√Hz input voltage noise and 0.6pA/√Hz input current noise, the LT1468 contributes only an additional 23% to the DAC output noise voltage. As with any precision application, and particularly with wide bandwidth amplifiers, the noise bandwidth should be minimized with an external filter to maximize resolution.

ADC Buffer

The important amplifier specifications for an analog-to-digital converter buffer application (Figure 113) are low noise and low distortion. The LTC1604 16-bit ADC signal-to-noise ratio (SNR) of 90dB implies 56μV$_{RMS}$ noise at the input. The noise for the amplifier, 100Ω/3000pF filter and a high value 10kΩ source is 15μV$_{RMS}$, which degrades the SNR by only 0.3dB. The LTC1604 total harmonic distortion (THD) is a low −94dB at 100kHz. The buffer/filter combination alone has 2nd and 3rd harmonic distortion better than −100dB for a 5V$_{P-P}$, 100kHz input, so it does not degrade the AC performance of the ADC.

The buffer also drives the ADC from a low source impedance. Without a buffer, the LTC1604 acquisition time increases with increasing source resistance above 1k and therefore the maximum sampling rate must be reduced. With the low noise, low distortion LT1468 buffer, the ADC can be driven at maximum speed from higher source resistances without sacrificing AC performance.

The DC requirements for the ADC buffer are relatively modest. The input offset voltage, CMRR (96dB minimum) and noninverting input bias current through the source resistance, R$_S$, affect the DC accuracy, but these errors are an insignificant fraction of the ADC offset and full-scale errors.
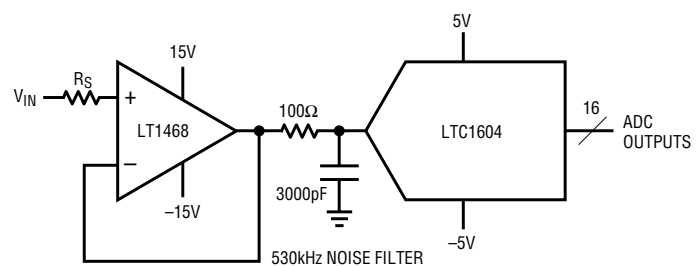

Figure 113. ADC Buffer

Telecommunications Circuits

HOW TO RING A PHONE WITH A QUAD OP AMP
by Dale Eagar

Requirements

When your telephone rings, exactly what is the phone company doing? This question comes up frequently, as it seems everyone is becoming a telephone company. Deregulation opens many new opportunities, but if you want to be the phone company you must ring bells. The voltage requirement for ringing a telephone bell is a $87V_{RMS}$ 20Hz sine wave superimposed on –48VDC.

An Open-Architecture Ring-Tone Generator

What the module makers offer is a solution to a problem that, by its nature, calls for unusual design techniques. What we offer here is a design that you can own, tailor to your specific needs, lay out on your circuit board and put on your bill of materials. Finally, you will be in control of the black magic (and high voltages) of ring-tone generation.

Not Your Standard Bench Supply

Ring-tone generation requires two high voltages, 60VDC and –180VDC. Figure 114 details the switching power supply that delivers the volts needed to run the ring-tone circuit. This switcher can be powered from any voltage from 5V to 30V, and is shut down when not in use, conserving power. The transformer and optocoupling yield a fully floating output. Faraday shields in the transformer eliminate most switcher noise, preventing mystery system noise problems later. Table 6 is the build diagram of the transformer used in the switching power supply.

Quad Op Amp Rings Phones

When a phone rings, it rings with a cadence, a sequence of rings and pauses. The standard cadence is one second ringing followed by two seconds of silence. We use the first 1/4 of the LT1491 as a cadence oscillator (developed in Figures 115 and 116) whose output is at V_{CC} for one second and then at V_{EE} for two seconds (see Figure 120).

Figure 114. The Switching Power Supply
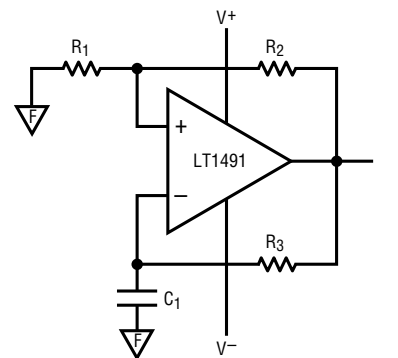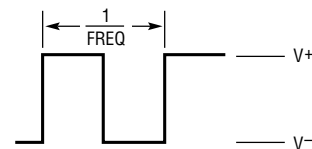
$$R_1 = \frac{2}{3} R_2$$

$$FREQ = \frac{1}{R_3 C_1}$$

DUTY FACTOR = 50%

Figure 115. Op Amp Intentionally Oscillates

FREQ = $\frac{1}{3}$ Hz

DUTY FACTOR = 33.3%

OUTPUT STARTS HIGH ON POWERUP.

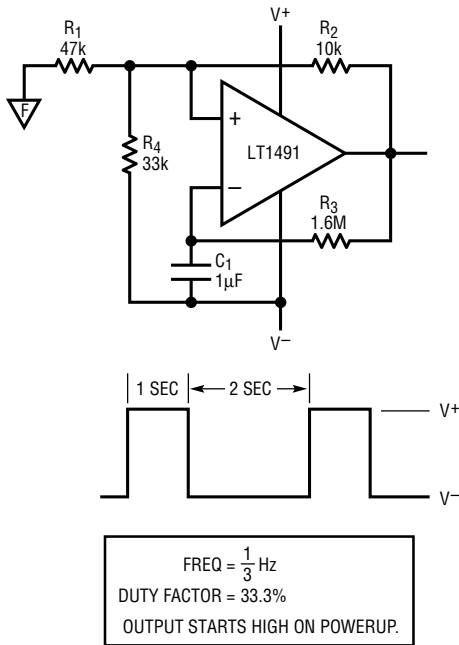**Figure 116. Duty Factor is Skewed**

DUTY FACTOR = 50%

Figure 117. Gated 20Hz Oscillator

This sequence repeats every three seconds, producing the all-too-familiar pattern.

The actual ringing of the bell is performed by a 20Hz AC sine wave signal at a level of 87V$_{RMS}$, superimposed on –48VDC. The 20Hz signal is implemented with the second amplifier in the LT1491 (Figure 117) which acts as a gated 20Hz oscillator. Connecting the circuit shown in Figure 116 to the circuit shown in Figure 117 and adding three resistors yields the sequencer as shown in Figure 118. The waveform, labled "Square Out," is the fourth trace in Figure 120. This waveform is the output of Figure 121.

Square Wave Plus Filter Equals Sine Wave

Thevenin will tell you that the output impedance of the sequencer shown in Figure 118 is 120kΩ. This impedance can be recycled and used as the input resistance of the filter that follows. The filter detailed in Figure 119 uses the Thevenin resistor on its input, yielding a slick, compact design while distorting the nice waveform on the node labeled "square out" to a half sine wave, half square wave.

Appending the filter to the waveform sequencer creates the waveform engine detailed in Figure 119. The output of this waveform engine is shown in the bottom trace in
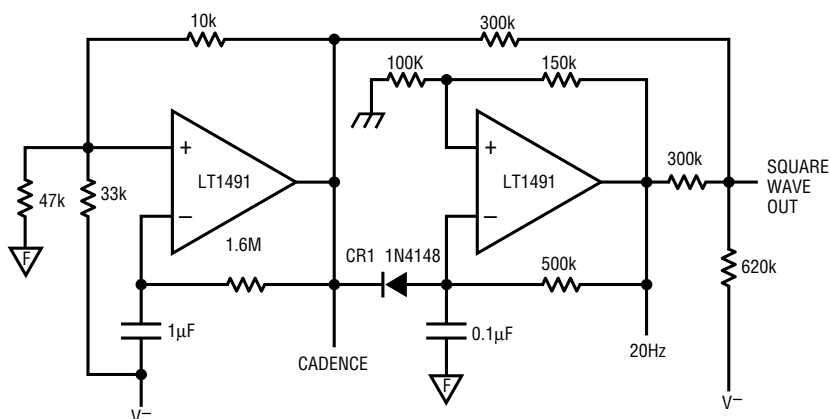

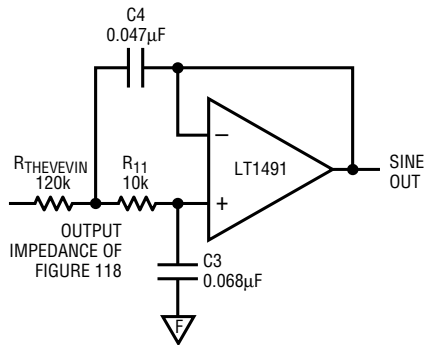**Figure 118. Sequencer: Cadenced 20Hz Oscillator**

Figure 119. Filter to Remove the Sharp Edges

Figure 120. This waveform engine is shown in block form in Figure 122.

Mapping Out the Ring-Tone Generator in Block Form

We now build a system-level block diagram of our ring tone generator. We start with the waveform engine of Figure 122, add a couple of 15V regulators and a DC offset (47k resistor), then apply some voltage gain with a high voltage amplifier to ring the bell. This hypothetical system-level block diagram is detailed in Figure 123. Figure 124 shows the output waveform of the ring tone generator; the sequenced ringing starts when the high voltage supply (Figure 114) is turned on, and continues as long as the power supply is enabled.
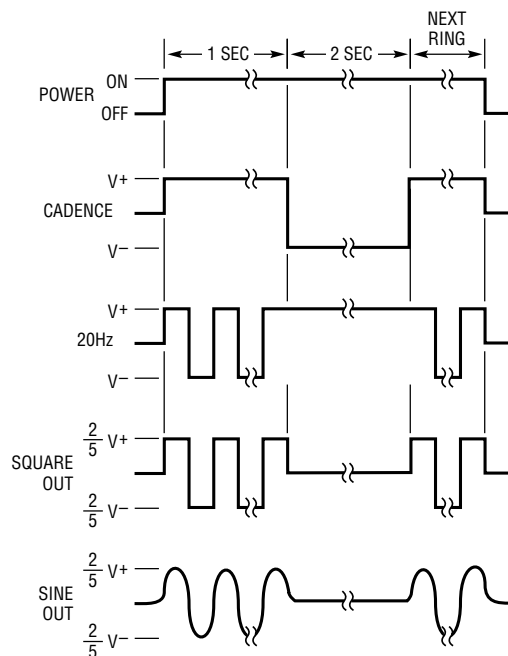
Figure 120. Timing of Waveform Engine

Table 6. Ring-Tone High Voltage Transformer Build Diagram

	Materials
2	EFD 20–15–3F8 Cores
1	EFD 20–15–8P Bobbin
2	EFD 20– Clip
2	0.007" Nomex Tape for Gap
Winding 1	Start Pin 1 200T #34
	Term Pin 8
	1 Wrap 0.002" Mylar Tape
Winding 2	Start Pin 2 70T #34
	Term Pin 7
	1 Wrap 0.002" Mylar Tape
Shields	Connect Pin 3 1T Foil Tape Faraday Shield
	1 Wrap 0.002" Mylar Tape
	Connect Pin 6 1T Foil Tape Faraday Shield
	1 Wrap 0.002" Mylar Tape
Winding 3	Start Pin 4 20T #26
	Term Pin 5
	Finish with Mylar Tape

What's Wrong with This Picture (Figure 123)

Careful scrutiny of Figure 123 reveals an inconsistency: even though the three fourths of the LT1491 in the waveform engine block are powered by ±15V, the final amplifier is shown as powered from 60V and –180V; this poses two problems: first the LT1491 is a quad op amp and all four sections have to share the same supply pins, and second, the LT1491 will not meet specification when powered from 60V and –180V. This is because 240V is greater than the **absolute maximum rating** of 44V (V+ to V-). Linear Technology products are noted for their robustness and conservative "specmanship," but this is going too far. It is time to apply some tricks of the trade.
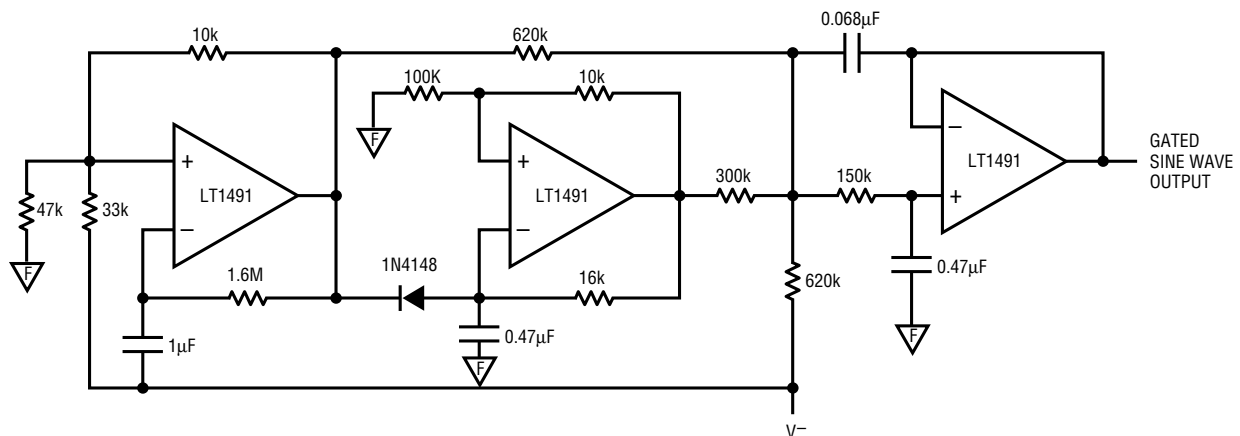
Figure 121. Waveform synthesizer

Building High Voltage Amplifiers

Setting aside the waveform engine for a moment, we will develop a high voltage amplifier. We start with the ±15V regulators shown in Figure 123; these are not your run-of-the-mill regulators, these are high differential voltage regulators, constructed as shown in Figure 125. Using these regulators and the final section of the LT1491 quad op amp, we can build a high voltage amplifier. We will use the ±15V regulators as the "output transistors" of our

amplifier, because they can both take the voltage and dissipate the power required to provide the ring voltage and current. By connecting the op amp to the regulators, one gets a free cascode high voltage amplifier. This is because the supply current for the op amp is also the regulator current. The trouble one encounters when so doing is that the input common mode range of the op amp is not wide enough to accommodate the full output voltage range of the composite amplifier. This would not be a problem if the amplifier were used as a unity-gain noninverting amplifier, but in this system we need gain to get from our $12V_{P-P}$ to $87V_{RMS}$.
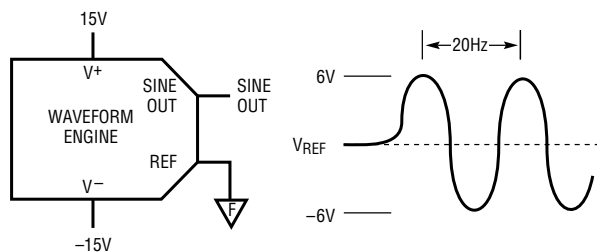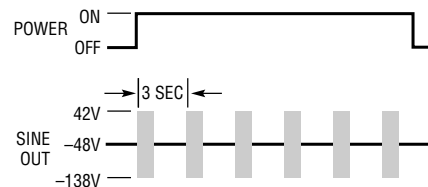

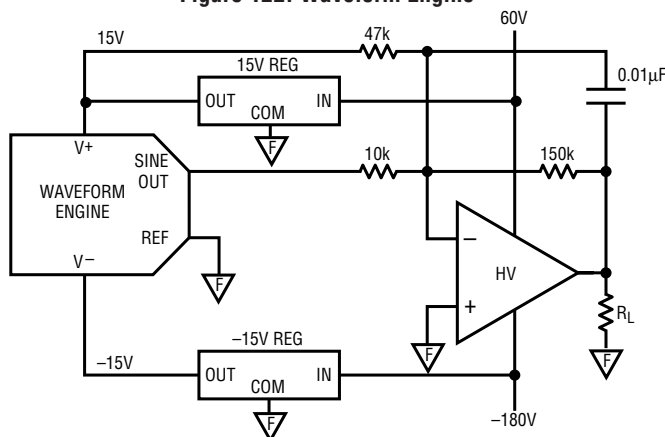**Figure 122. Waveform Engine**

Figure 124. System Output

Figure 123. High Voltage Amplifier
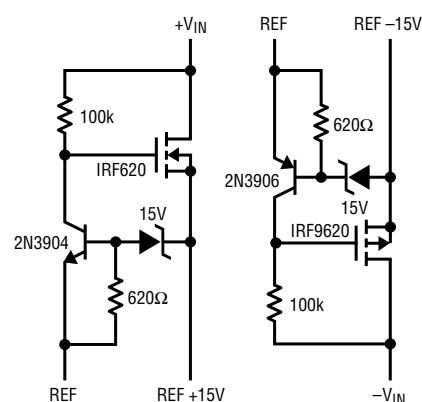
Figure 125. High Differential Voltage Regulators
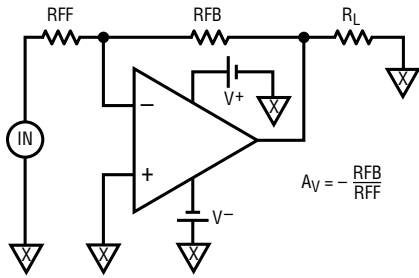
Figure 126. Standard Op Amp Form

$$A_V = -\frac{RFB}{RFF}$$
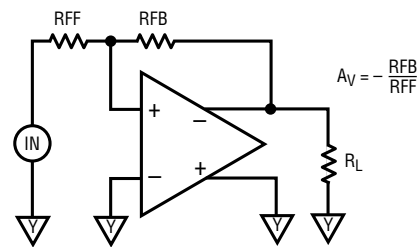

Figure 128. Trade Inputs and Outputs

$$A_V = -\frac{RFB}{RFF}$$
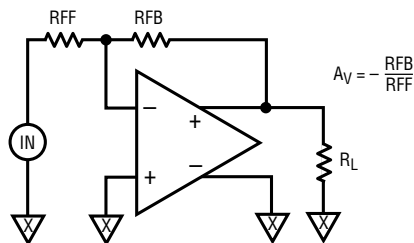
Figure 127. Hide the Batteries Inside the Op Amp

$$A_V = -\frac{RFB}{RFF}$$
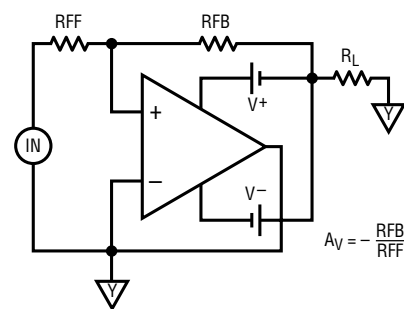
Figure 129. Pull the Batteries Back out of the Amplifier

$$A_V = -\frac{RFB}{RFF}$$

Moving the amplifier's output transistor function out of the op amp and into the ±15V regulators moves the effective amplifier output from the op amp output to the center of the two supplies sourcing the ±15V regulators. This is a transformative step in the evolution of amplifiers from low voltage op amps to high voltage, extended supply amplifiers.

Inverting Op Amp Circuit Gets Morphed

Let's focus on this transformative step as it relates to the simple inverting amplifier shown in Figure 126.* Were we to look at the amplifier in Figure 126 in some strange

Darwinistic mood, we might see that the power supplies (batteries) are in fact an integral part of our amplifier. Such an observation would lead us to redraw the circuit to look like Figure 127 where the center of the two batteries are brought out of the amplifier as the negative terminal of the output.

Once that is done, one is free to swap the polarities of the inputs and outputs, yielding the circuit shown in Figure 128. Finally we pull the two batteries back out of the amplifier to get our morphed inverting amplifier (Figure 129). Isn't assisting evolution fun?[†]
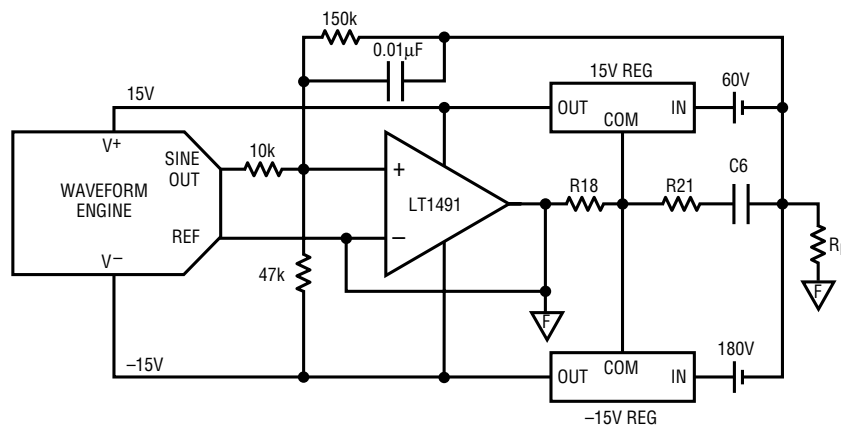

Figure 130. Post-Evolution Block Diagram

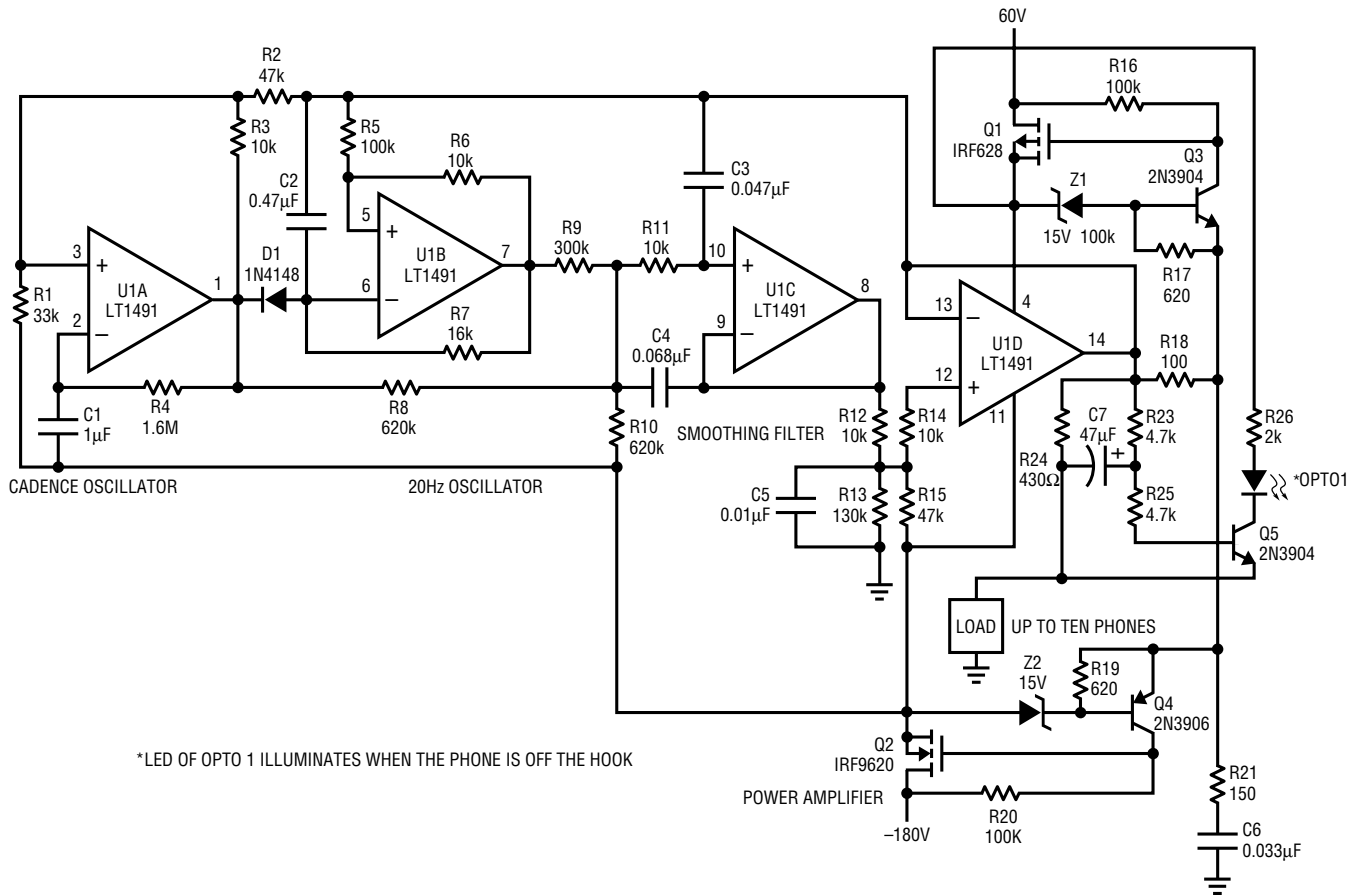**Figure 131. Ring-Tone Generator**

*LED OF OPTO 1 ILLUMINATES WHEN THE PHONE IS OFF THE HOOK

Applying the evolutionary forces just described to the block diagram in Figure 123, we get the block diagram in Figure 130. Actually Figure 130 contains three strangers, R18, R21 and C6, parts not predicted by our evolutionary path (unless R18 = 0Ω and R21 is open) These parts are needed because, in our metamorphosis going from Figure 127 to Figure 128, the amplifier's internal compensation node was moved from ground to the amplifier's output. These parts correct the compensation for the new configuration.

Ring-Trip Sense

Now that we can ring the telephone, we must sense when the phone is picked up. This is done by sensing the DC current flowing to the phone while it is ringing, using the ring-trip sense circuit comprising R23–R26, C7, Q5 and Opto1 of Figure 131, the complete ring-tone generator. This circuit will ring more than ten phones at once, and is

protected on its output from shorts to ground or to either the +60V or the –180V supply.

Conclusion

Here is a ring tone generator you can own, a robust circuit that is stable into any load. If your system design requires a circuit with different specifications, you can easily tailor this circuit to meet your needs. Don't hesitate to call us if we can help you with your design.

Editor's Notes:

* The grounds X and Y, shown in Figures 126–129, are for illustrating the effects of "evolution." Ground X may be regarded as "arbitrary exemplary ground," and ground Y as "postmetamorphic exemplary ground." Ground X and ground Y are not the same.

† Evolutionary theory invloves pure, random chance. What you have done here requires purposeful thought and design.

A LOW DISTORTION, LOW POWER, SINGLE-PAIR HDSL DRIVER USING THE LT1497

by George Feliz and Adolfo Garcia

Introduction

High speed digital subscriber line (HDSL) interfaces support full-duplex data rates up to 1.544Mbps over 12,000 feet using two standard 135Ω twisted-pair telephone wires. The high data rate is achieved with a combination of encoding 2 bits per symbol using two-binary, one-quaternary (2B1Q) modulation, and sophisticated digital signal processing to extract the received signal. This performance is possible only with low distortion line drivers and receivers. In addition, the power dissipation of the transceiver circuitry is critical because it may be loop-powered from the central office over the twisted pair. Lower power dissipation also increases the number of transceivers that can placed in a single, non-forced–air enclosure. Single-pair HDSL requires the same performance as two-pair HDSL over a single twisted pair and operates at twice the fundamental 2B1Q symbol rate. In HDSL systems that use 2B1Q line coding, the signal passband necessary to carry a data rate of 1.544Mbps is 392kHz. This signal rate will be used to quantify the performance of the LT1497 in this article.

Low Distortion Line Driver

The circuit of Figure 132 transmits signals over a 135Ω twisted pair through a 1:1 transformer. The LT1497 dual 125mA, 50MHz current feedback amplifier was chosen for its ability to cleanly drive heavy loads, while consuming a modest 7mA maximum supply current per amplifier in a thermally enhanced SO-8 package. The driver amplifiers are configured in gains of two (A1) and minus one (A2) to compensate for the attenuation inherent in the back-termination of the line and to provide differential drive to the transformer. The transmit power requirement for HDSL is 13.5dBm (22.4mW) into 135Ω, corresponding to a 1.74V_{RMS} signal. Since 2B1Q modulation is a 4-level pulse amplitude modulated signal, the crest factor (peak to RMS) of this signal is 1.61. Thus, a 13.5dBm, 2B1Q modulated signal yields 5.6V_{P-P} across the 135Ω load. The corresponding output signal current is ±20.7mA peak. This modest drive level increases for varying line conditions and is tested with a standardized collection of test loops that can have line impedances as low as 25Ω. The LT1497's high output current and voltage swing drive the 135Ω line at the required distortion level of –72dBc. For a data rate of 1.544Mbps and 2-bit-per-symbol encoding, the fundamental frequency of operation is 392kHz.
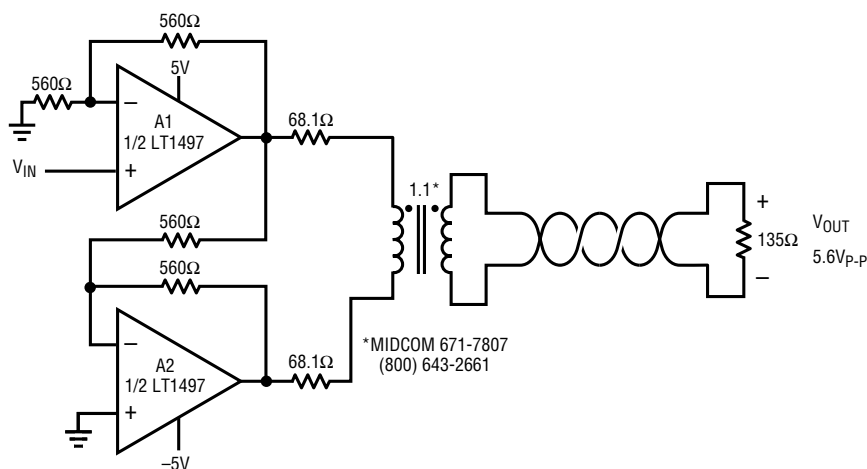

Figure 132. LT1497 HDSL Driver

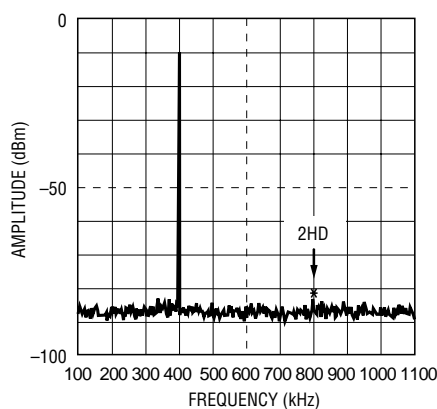**Figure 133. Harmonic Distortion of Figure 132's Circuit with a 400kHz Sine Wave and an Output Level of 5.6V_P-P into 135Ω**

Figure 134. 2-Tone Intermodulation for Figure 132's Circuit

The LT1497 provides such low distortion because it operates at only a fraction of its output current capability and is well within its voltage swing limitations. There are other LTC amplifiers that can achieve this performance, but at the expense of higher power dissipation or a larger package.

Performance

The circuit of Figure 132 was evaluated for harmonic distortion with a 400kHz sine wave and an output level of 5.6V_P-P into 135Ω. Figure 133 shows that the second harmonic is –72.3dB relative to the fundamental for the 135Ω load. Third harmonic distortion is not critical, because received signals are heavily filtered before being digitized by an A/D converter. Performance with a 50Ω load (to simulate more challenging test loops) is slightly better at –75dB. The output signal was attenuated to obtain maximum sensitivity of the HP4195A network analyzer used for the measurements.
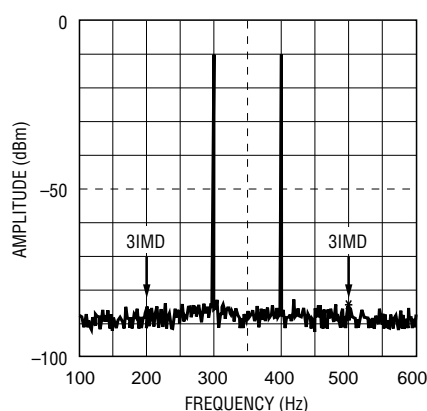
With multicarrier applications such as discrete multitone modulation (DMT) becoming as prevalent as single-carrier applications, another important measure of amplifier dynamic performance is 2-tone intermodulation. This evaluation is a valuable tool to gain insight to amplifier linearity when processing more than one tone at a time.

For this test, two sine waves at 300kHz and 400kHz were used with levels set to obtain 5.6V_P-P across the 135Ω load. Figure 134 shows that the third-order intermodulation products are well below –72dB. With a 50Ω load, performance is within 1dB–2dB of that with the 135Ω load.

Conclusion

The circuit presented provides outstanding distortion performance in an SO-8 package with remarkably low power dissipation. It is ideally suited for single pair digital subscriber line applications, especially for remote terminals.

Comparators

ULTRALOW POWER COMPARATORS INCLUDE REFERENCE
by James Herr

The LTC1440–LTC1445 family features 1μA comparators with adjustable hysteresis and TTL/CMOS outputs that sink and source current and a 1μA reference that can drive a bypass capacitor of up to 0.01μF without oscillation. The parts operate from a 2V to 11V single supply or a ±1V to ±5V dual supply.

Undervoltage/Overvoltage Detector

The LTC1442 can be easily configured as a window detector, as shown in Figure 135. R1, R2 and R3 form a resistive divider from V_{CC} so that comparator A goes low when V_{CC} drops below 4.5V, and comparator B goes low when V_{CC} rises above 5.5V. A 10mV hysteresis band is set by R4 and R5 to prevent oscillations near the trip points.
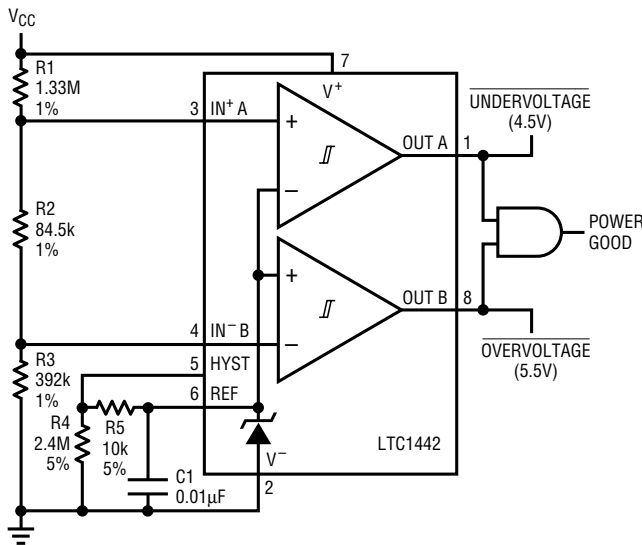
Figure 135. Window Detector

Single-Cell Lithium-Ion Battery Supply

Figure 136 shows a single cell lithium-ion battery to 5V supply with the low-battery warning, low-battery shutdown and reset functions provided by the LTC1444. The LT1300 micropower step-up DC/DC converter boosts the battery voltage to 5V using L1 and D1. Capacitors C2 and C3 provide input and output filtering.

The voltage-monitoring circuitry takes advantage of the LTC1444's open-drain outputs and low supply voltage

operation. Comparators A and B, along with R1, R2 and R3, monitor the battery voltage. When the battery voltage drops below 2.65V comparator A's output pulls low to generate a nonmaskable interrupt to the microprocessor to warn of a low-battery condition. To protect the battery from over discharge, the output of comparator B is pulled high by R7 when the battery voltage falls below 2.45V. P-channel MOSFET Q1 and the LT1300 are turned off, dropping the quiescent current to 20μA. Q1 is needed to prevent the load circuitry from discharging the battery through L1 and D1.

Comparators C and D provide the reset input to the microprocessor. As soon as the boost converter output rises above the 4.65V threshold set by R8 and R9, comparator C turns off and R10 starts to charge C4. After 200ms, comparator D turns off and the Reset pin is pulled high by R12.

Conclusion

With their built-in references, low supply current requirements and variety of configurations, Linear Technology's LTC1440–45 family of micropower comparators is ideal for system monitoring in battery-powered devices such as PDAs, laptop and palmtop computers and hand-held instruments.
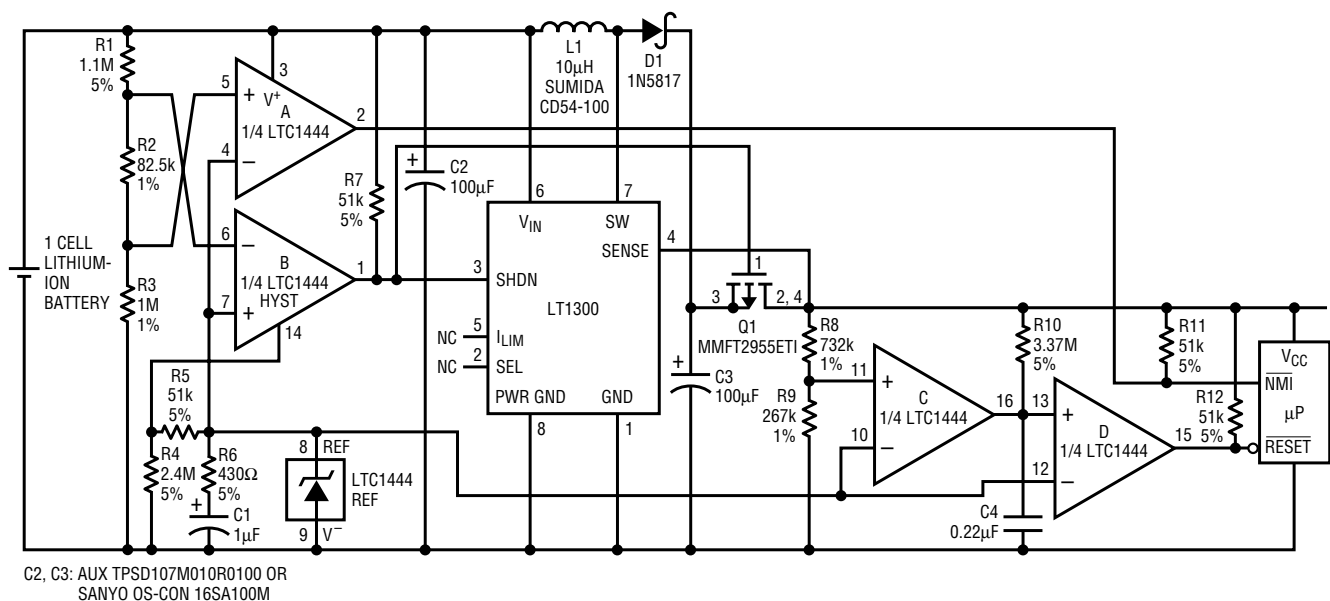

C2, C3: AUX TPSD107M010R0100 OR
SANYO OS-CON 16SA100M

Figure 136. Single-Cell to 5V Supply

A 4.5ns, 4mA, SINGLE-SUPPLY, DUAL COMPARATOR OPTIMIZED FOR 3V/5V OPERATION
by Joseph G. Petrofsky

Introduction

The LT1720 is an UltraFast™ (4.5ns), low power (4mA/ comparator), single-supply, dual comparator designed to operate on a single 3V or 5V supply. These comparators feature internal hysteresis, making them easy to use, even with slowly moving input signals. The LT1720 is fabricated in Linear Technology's 6GHz complementary bipolar process, resulting in unprecedented speed for its low power consumption.

Applications

Crystal Oscillators

Figure 137 shows a simple crystal oscillator using one half of an LT1720. The 2k–620Ω resistor pair set a bias point at the comparator's noninverting input. The 2k–1.8k–0.1μF path sets the inverting input node at an appropriate DC average level based on the output. The crystal's path provides resonant positive feedback and stable oscillation occurs. Although the LT1720 will give the correct logic output when one input is outside the common mode range, additional delays may occur when it is so operated, opening the possibility of spurious operating modes. Therefore, the DC bias voltages at the inputs are set near the center of the LT1720's common mode range and the 220Ω resistor attenuates the feedback to the noninverting input. The circuit will operate with any AT-cut crystal from 1MHz to 10MHz over a 2.7V to 6V supply range.

The output duty cycle for the circuit of Figure 137 is roughly 50% but it is affected by resistor tolerances and, to a lesser extent, by comparator offsets and timings.

Timing Skews

For a number of reasons, the LT1720 is an excellent choice for applications requiring differential timing skew. The two comparators in a single package are inherently well matched, with just 300ps Δt_{PD} typical. Monolithic construction keeps the delays well matched vs supply voltage
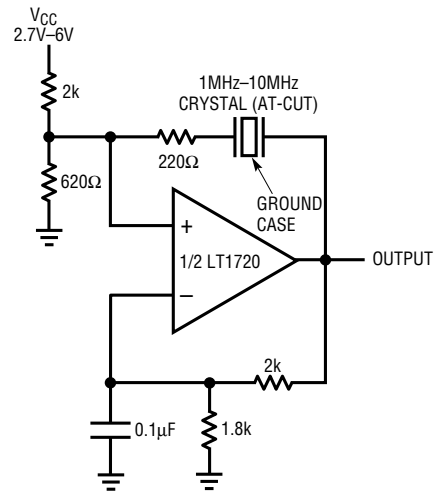

Figure 137. Simple 1MHz to 10MHz Crystal Oscillator

and temperature. Crosstalk between the comparators, usually a disadvantage in monolithic duals, has minimal effect on the LT1720 timing due to the internal hysteresis.

The circuits of Figure 138 show basic building blocks for differential timing skews. The 2.5k resistance interacts with the 2pF typical input capacitance to create at least ±4ns delay, controlled by the potentiometer setting. A differential and a single-ended version are shown. In the differential configuration, the output edges can be smoothly scrolled through Δt = 0 with negligible interaction.

Fast Waveform Sampler

Figure 139 uses a diode-bridge-type switch for clean, fast waveform sampling. The diode bridge, because of its inherent symmetry, provides lower AC errors than other semiconductor-based switching technologies. This circuit features 20dB of gain, 10MHz full power bandwidth and 100μV/°C baseline uncertainty. Switching delay is less than 15ns and the minimum sampling window width for full power response is 30ns.

The input waveform is presented to the diode bridge switch, the output of which feeds the LT1227 wideband amplifier. The LT1720 comparators, triggered by the sample command, generate phase-opposed outputs. These sig-
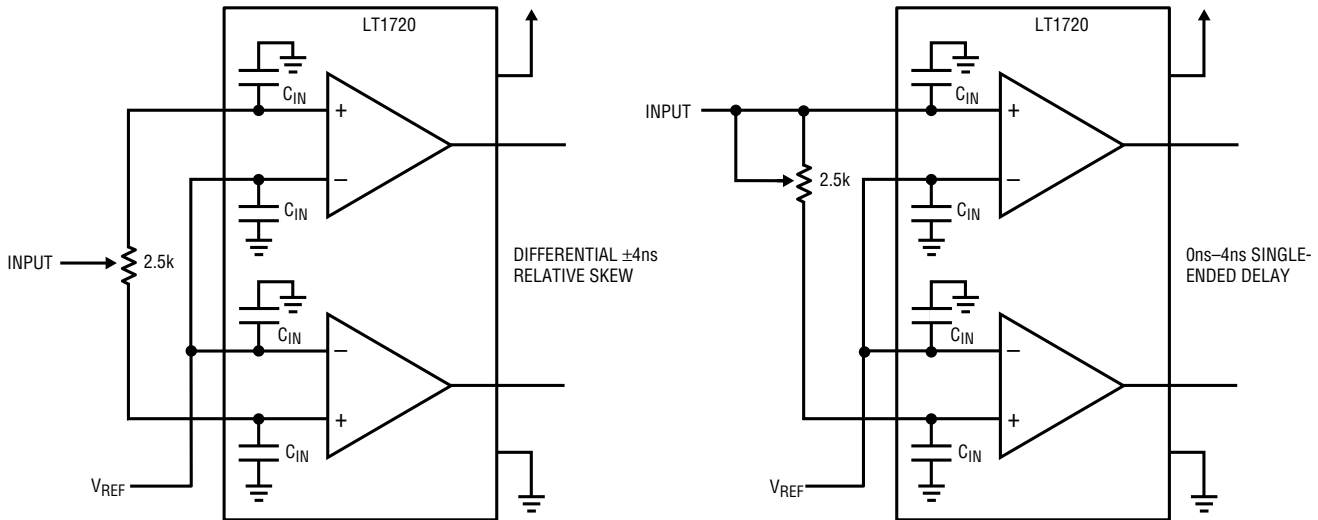
Figure 138. Timing-Skew Generation is Easy with the LT1720

nals are level shifted by the transistors, providing complementary bipolar drive to switch the bridge. A skew compensation trim ensures bridge-drive signal simultaneity within 1ns. The AC balance corrects for parasitic capacitive bridge imbalances. A DC balance adjustment trims bridge offset.

The trim sequence involves grounding the input via 50Ω and applying a 100kHz sample command. The DC balance is adjusted for minimal bridge ON vs OFF variation at the output. The skew compensation and AC balance adjustments are then optimized for minimum AC disturbance in the output. Finally, unground the input and the circuit is ready for use.

Coincidence Detector

High speed comparators are especially suited for interfacing pulse-output transducers, such as particle detectors, to logic circuitry. The matched delays of a monolithic dual are well suited for those cases where the coincidence of two pulses needs to be detected. The circuit of Figure 140 is a coincidence detector that uses an LT1720 and discrete components as a fast AND gate.

The reference level is set to 1V, an arbitrary threshold. Only when both input signals exceed this will a coincidence be detected. The Schottky diodes from the comparator outputs to the base of the MRF-501 form the AND gate, while

the other two Schottkys provide for fast turn-off. A logic AND gate could instead be used, but would add considerably more delay than the 300psec contributed by this discrete stage.

This circuit can detect coincident pulses as narrow as 2.5ns. For narrower pulses, the output will degrade gracefully, responding, but with narrow pulses that don't rise all the way to high before starting to fall. The decision delay is 4.5ns with input signals 50mV or more above the reference level. This circuit creates a TTL compatible output but it can typically drive CMOS as well.

Pulse Stretcher

For detecting short pulses from a single sensor, a pulse stretcher is often required. The circuit of Figure 141 acts as a one-shot, stretching the width of an incoming pulse to a consistent 100ns. Unlike a logic one-shot, this LT1720-based circuit requires only 100pV-s of stimulus to trigger.

The circuit works as follows: Comparator C1 functions as a threshold detector, whereas comparator C2 is configured as a one-shot. The first comparator is prebiased with a threshold of 8mV to overcome comparator and system offsets and establish a low output in the absence of an input signal. An input pulse sends the output of C1 high, which in turn latches C2's output high. The output of C2 is fed back to the input of the first comparator, causing
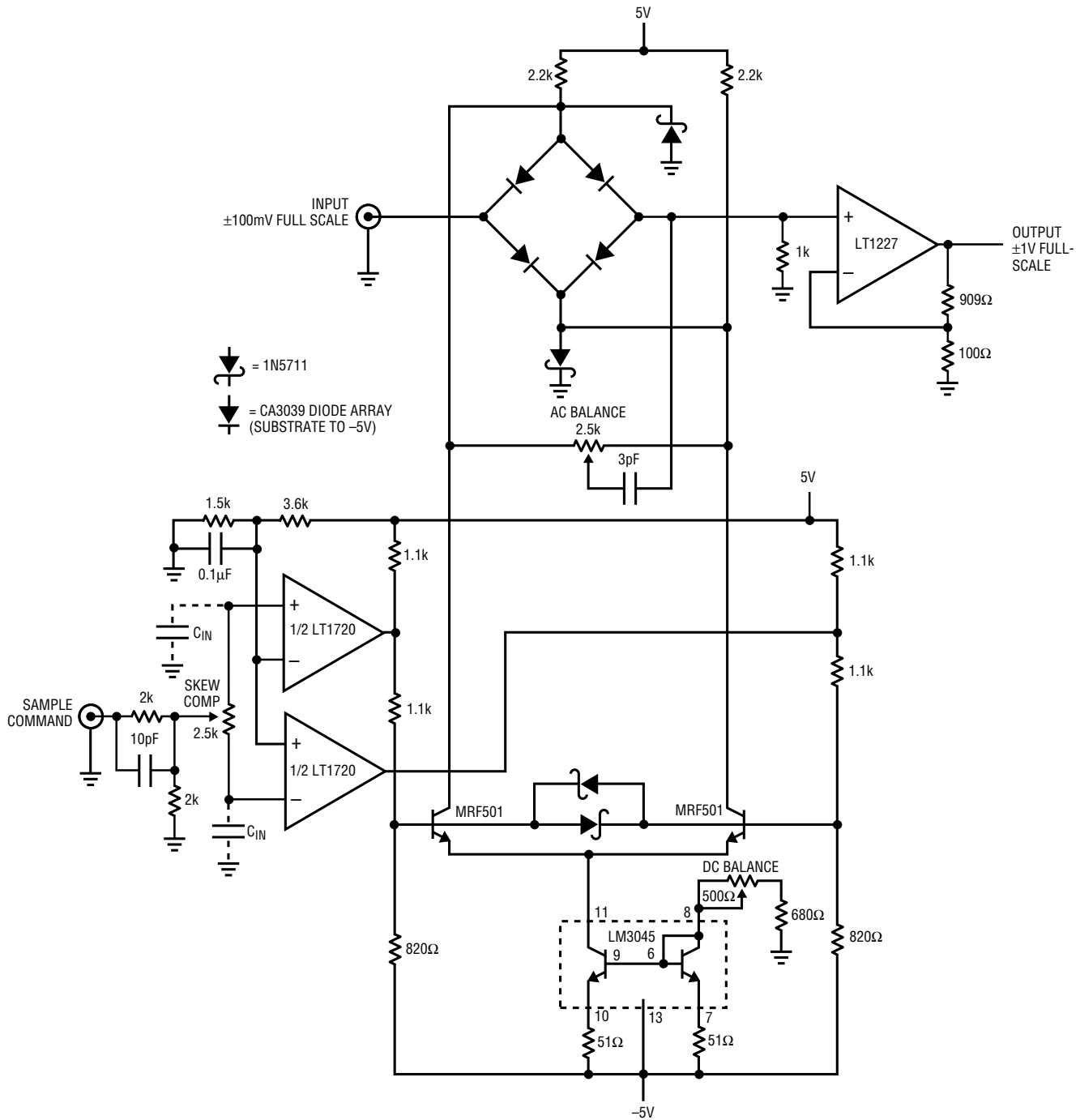
Figure 139. Fast Waveform Sampler Using the LT1720 for Timing-Skew Compensation

regeneration and latching both outputs high. Timing capacitor C now begins charging through R and, at the end of 100ns, C2 resets low. The output of C1 also goes low,

latching both outputs low. A new pulse at the input of C1 can now restart the process. Timing capacitor C can be increased without limit for longer output pulses.

This circuit has an ultimate sensitivity of better than 14mV with 5ns–10ns input pulses. It can even detect an avalanche generated test pulse of just 1ns duration with sensitivity better than 100mV.[1] It can detect short events better than the coincidence detector above because the one-shot is configured to catch just 100mV of upward movement from C1's V_{OL}, whereas the coincidence detector's 2.5ns specification is based on a full, legitimate logic high.

Conclusion

The new LT1720 dual 4.5ns single-supply comparators feature high speeds and low power consumption. They are versatile and easy-to-use building blocks for a wide variety of system design challenges.

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1 See Linear Technology Application Note 47, Appendix B. This circuit can detect the output of the pulse generator described after 40dB of attenuation.
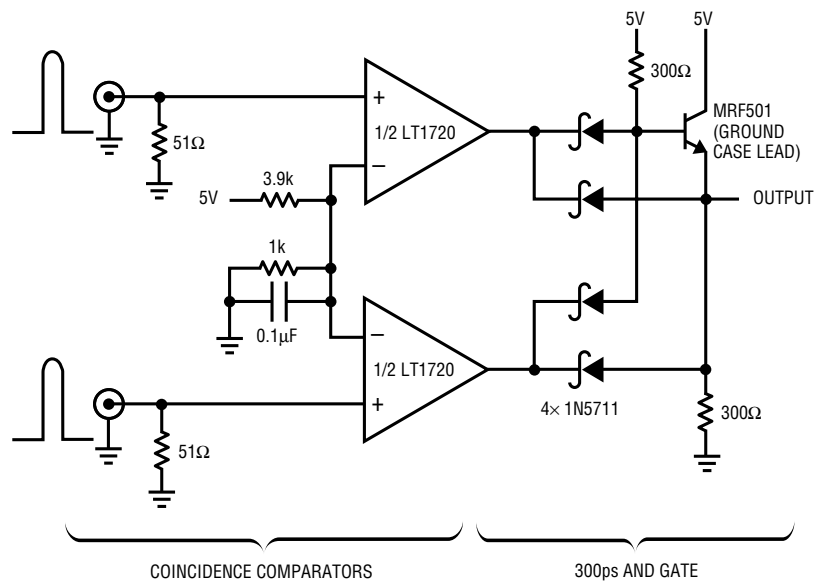
Figure 140. A 2.5ns Coincidence Detector
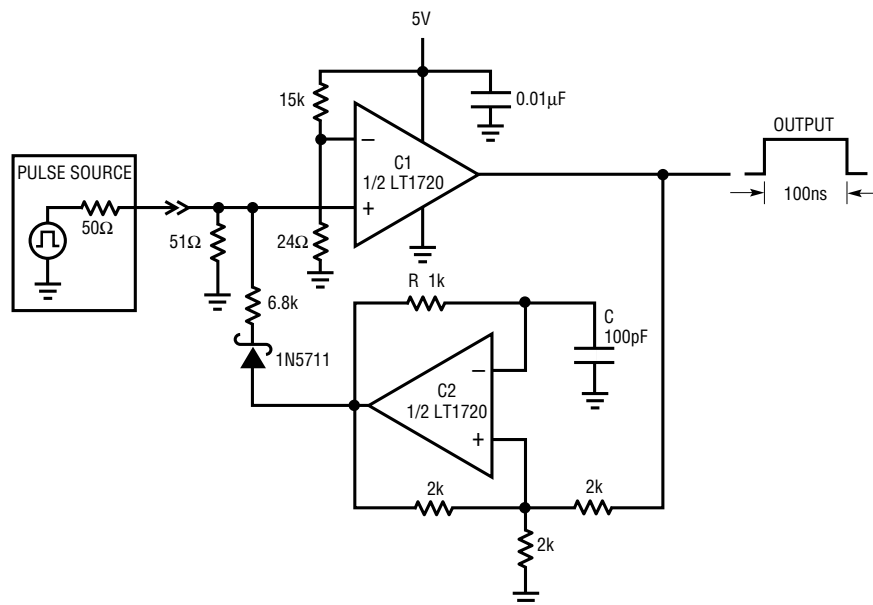
Figure 141. A 1ns Pulse Stretcher

Instrumentation Circuits

LTC1441-BASED MICROPOWER
VOLTAGE-TO-FREQUENCY CONVERTER
by Jim Williams

Figure 142 is a voltage-to-frequency converter. A 0V–5V input produces a 0Hz–10kHz output, with a linearity of 0.02%. Gain drift is 60ppm/°C. Maximum current consumption is only 26μA, 100 times lower than currently available units.

To understand the circuit's operation, assume that C1's negative input is slightly below its positive input (C2's output is low). The input voltage causes a positive-going ramp at C1's input (trace A, Figure 143). C1's output is high, allowing current flow from Q1's emitter, through C1's output stage to the 100pF capacitor. The 2.2μF capacitor provides high frequency bypass, maintaining low impedance at Q1's emitter. Diode connected Q6 pro-

A = 50mV/DIV
B = 5V/DIV
C = 5V/DIV
D = 1mA/DIV
E = 5V/DIV

HORIZ = 20μs/DIV

Figure 143. Waveforms for the Micropower V/F Converter: Charge-Based Feedback Provides Precision Operation with Extremely Low Power Consumption.

vides a path to ground. The voltage to which the 100pF unit charges is a function of Q1's emitter potential and Q6's drop. C1's CMOS output, purely ohmic, contributes no voltage error. When the ramp at C1's negative input goes high enough, C1's output goes low (trace B) and the inverter switches high (trace C). This action pulls current from C1's negative input capacitor via the Q5 route (trace D). This current removal resets C1's negative input ramp
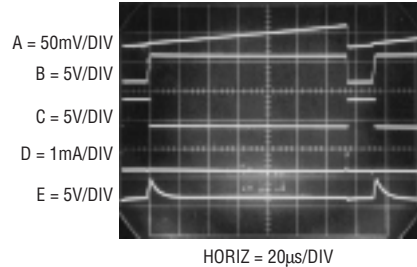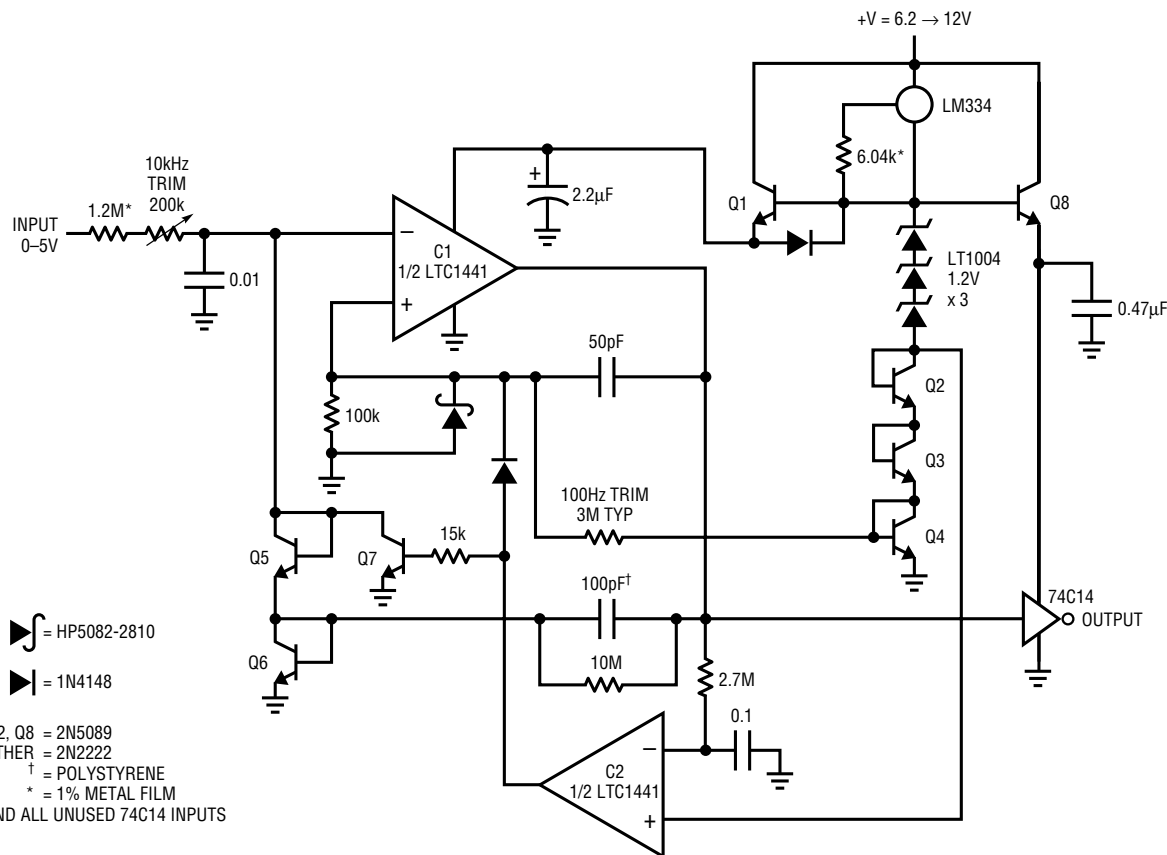

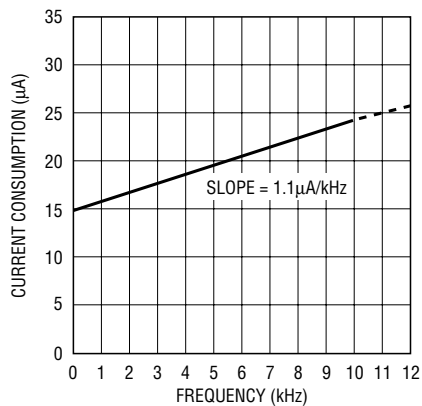**Figure 142. 0.02% V/F Converter Requires only 26μA Supply Current**

Figure 144. Current Consumption vs Frequency for the V/F Converter: Charge/Discharge Cycles Account for 1.1µA/kHz Current Drain Increase

to a potential slightly below ground. The 50pF capacitor furnishes AC positive feedback (C1's positive input is trace E) ensuring that C1's output remains negative long enough for a complete discharge of the 100pF capacitor. The Schottky diode prevents C1's input from being driven outside its negative common mode limit. When the 50pF unit's feedback decays, C1 again switches high and the entire cycle repeats. The oscillation frequency depends directly on the input-voltage-derived current.

Q1's emitter voltage must be carefully controlled to get low drift. Q3 and Q4 temperature compensate Q5 and Q6 while Q2 compensates Q1's V_{BE}. The three LT1004s are the actual voltage reference and the LM334 current source provides 12µA bias to the stack. The current drive provides excellent supply immunity (better than 40ppm/V) and also aids circuit temperature coefficient. It does this by using the LM334's 0.3%/°C tempco to slightly temperature

modulate the voltage drop in the Q2–Q4 trio. This correction's sign and magnitude directly oppose the –120ppm/°C 100pF polystyrene capacitor's drift, aiding overall circuit stability. Q8's isolated drive to the CMOS inverter prevents output loading from influencing Q1's operating point. This makes circuit accuracy independent of loading.

The Q1 emitter-follower delivers charge to the 100pF capacitor efficiently. Both base and collector current end up in the capacitor. The 100pF capacitor, as small as accuracy permits, draws only small transient currents during its charge and discharge cycles. The 50pF–100k positive feedback combination draws insignificantly small switching currents. Figure 144, a plot of supply current versus operating frequency, reflects the low power design. At zero frequency, comparator quiescent current and the 12µA reference stack bias account for all current drain. There are no other paths for loss. As frequency scales up, the 100pF capacitor's charge-discharge cycle introduces the 1.1µA/kHz increase shown. A smaller value capacitor would cut power, but effects of stray capacitance and charge imbalance would introduce accuracy errors.

Circuit start-up or overdrive can cause the circuit's AC-coupled feedback to latch. If this occurs, C1's output goes low; C2, detecting this via the 2.7M–0.1µF lag, goes high. This lifts C1's positive input and grounds the negative input with Q7, initiating normal circuit action.

To calibrate this circuit, apply 50mV and select the indicated resistor at C1's positive input for a 100Hz output. Complete the calibration by applying 5V and trimming the input potentiometer for a 10kHz output.

BRIDGE MEASURES SMALL CAPACITANCE IN PRESENCE OF LARGE STRAYS
by Jeff Witt

Capacitance sensors measure a wide variety of physical quantities, such as position, acceleration, pressure and fluid level. The capacitance changes are often much smaller than stray capacitances, especially if the sensor is remotely placed. I needed to make measurements with a 50pF cryogenic fluid level detector, with only 2pF full-scale change, hooked to several hundred pF of varying cable

capacitance. This required a circuit with high stability, sensitivity and noise rejection, but one insensitive to stray capacitance caused by cables and shielding. I also wanted battery operation and analog output for easy interfacing to other instruments. Two traditional circuit types have drawbacks: integrators are sensitive to noise at the comparator and voltage-to-frequency converters typically measure stray as well as sensor capacitance. The capacitance bridge presented here measures small transducer capacitance changes, yet rejects noise and cable capacitance.

The bridge, shown in Figure 145, is designed around the LTC1043 switched-capacitor building block. The circuit compares a capacitor, C_X, of unknown value, with a reference capacitor, C_{REF}. The LTC1043, programmed with C1 to switch at 500Hz, applies a square wave of amplitude V_{REF} to node A, and a square wave of amplitude V_{OUT} and opposite phase to node B. When the bridge is balanced, the AC voltage at node C is zero, and

$$V_{OUT} = V_{REF} \frac{C_X}{C_{REF}}$$

Balance is achieved by integrating the current from node C using an op amp (LT1413) and a third switch on the LTC1043 for synchronous detection. With $C_{REF} = 500pF$ and $V_{REF} = 2.5V$, this circuit has a gain of 5mV/pF, and when measured with a DMM achieves a resolution of 10fF for a dynamic range of 100dB. It also rejects stray capacitance (shown as ghosts in Figure 145) by 100dB. If this rejection is not important, the switching frequency f can be increased to extend the circuit's bandwidth, which is

$$BW = f \frac{C_{REF}}{C_{OUT}}$$

C_{OUT} should be larger than C_{REF}.

The circuit operates from a single 5V supply and consumes 800µA. If the capacitances at nodes A and C are kept below 500pF, the LT1078 micropower dual op amp may be used in place of the LT1413, reducing supply current to just 160µA.

If the relative capacitance change is small, the circuit can be modified for higher resolution, as shown in Figure 146. A JFET input op amp (LT1462) amplifies the signal before demodulation for good noise performance, and the output of the integrator is attenuated by R1 and R2 to increase the sensitivity of the circuit. If $\Delta C_X \ll C_X$, and $C_{REF} \approx C_X$, then

$$V_{OUT} - V_{REF} \approx V_{REF} \frac{\Delta C_X (R1 + R2)}{C_{REF} R2}$$

With $C_{REF} = 50pF$, the circuit has a gain of 5V/pF and can resolve 2fF. Supply current is 1mA. The synchronous detection makes this circuit insensitive to external noise sources and in this respect shielding is not terribly important. However, to achieve high resolution and stability, care should be taken to shield the capacitors being measured. I used this circuit for the fluid level detector mentioned above, putting a small trim cap in parallel with C_{REF} to adjust offset and trimming R2 for proper gain.
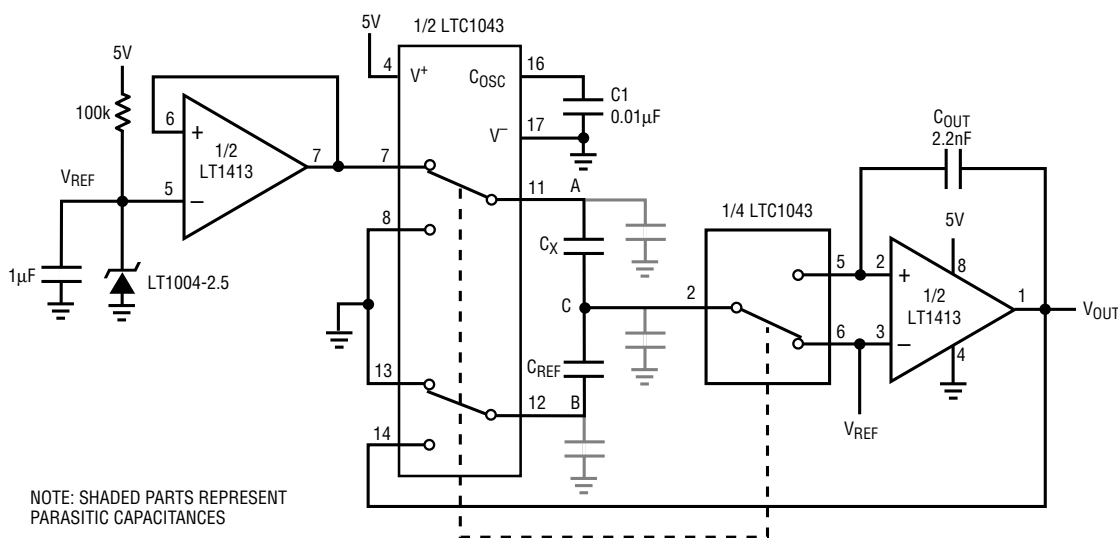

NOTE: SHADED PARTS REPRESENT PARASITIC CAPACITANCES

Figure 145. A Simple, High Performance Capacitance Bridge

Bridge circuits are particularly suitable for differential measurements. When C_X and C_{REF} are replaced with two sensing capacitors, these circuits measure differential capacitance changes, but reject common mode changes.

CMRR for the circuit in Figure 146 exceeds 70dB. In this case, however, the output is linear only for small relative capacitance changes.
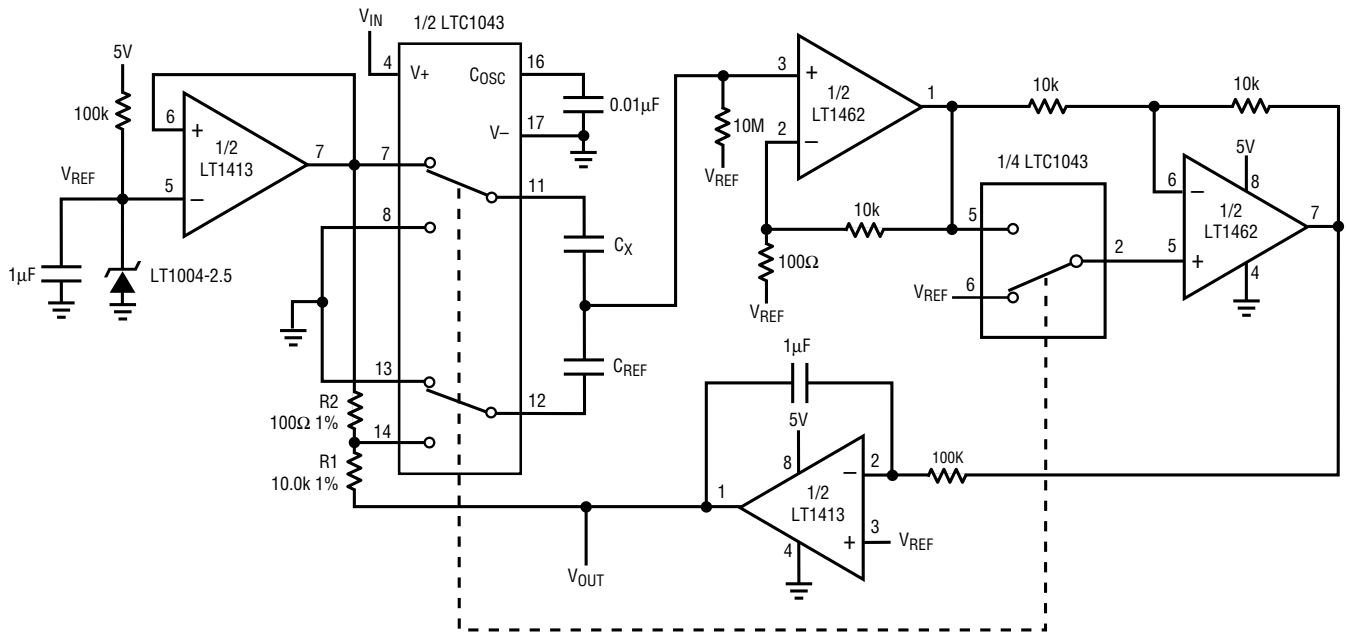

Figure 146. A Bridge with Increased Sensitivity and Noise Performance

WATER TANK PRESSURE SENSING, A FLUID SOLUTION
by Richard Markell

Introduction

Liquid sensors require a media compatible, solid state pressure sensor. The pressure range of the sensor is dependent on the height of the column or tank of fluid that must be sensed. This article describes the use of the E G & G IC Sensors Model 90 stainless steel diaphragm, 0 to 15psig sensor used to sense water height in a tank or column.

Because large chemical or water tanks are typically located outside in "tank farms," it is insufficient to provide only an analog interface to a digitization system for level sensing.

This is because the very long wires required to interconnect the system cause IR drops, noise and other corruption of the analog signal. The solution to this problem is to implement a system that converts the analog to digital signals at the sensor. In this application, we implement a "liquid height to frequency converter."

Circuit Description

Figure 147 shows the analog front-end of the system, which includes the LT1121 linear regulator for powering the system. The LT1121 is a micropower, low dropout linear regulator with shutdown. For micropower applications of this or other circuits, the ability to shut down the entire system via a single power supply pin allows the system to operate only when taking data (perhaps every hour), conserving power and improving battery life.
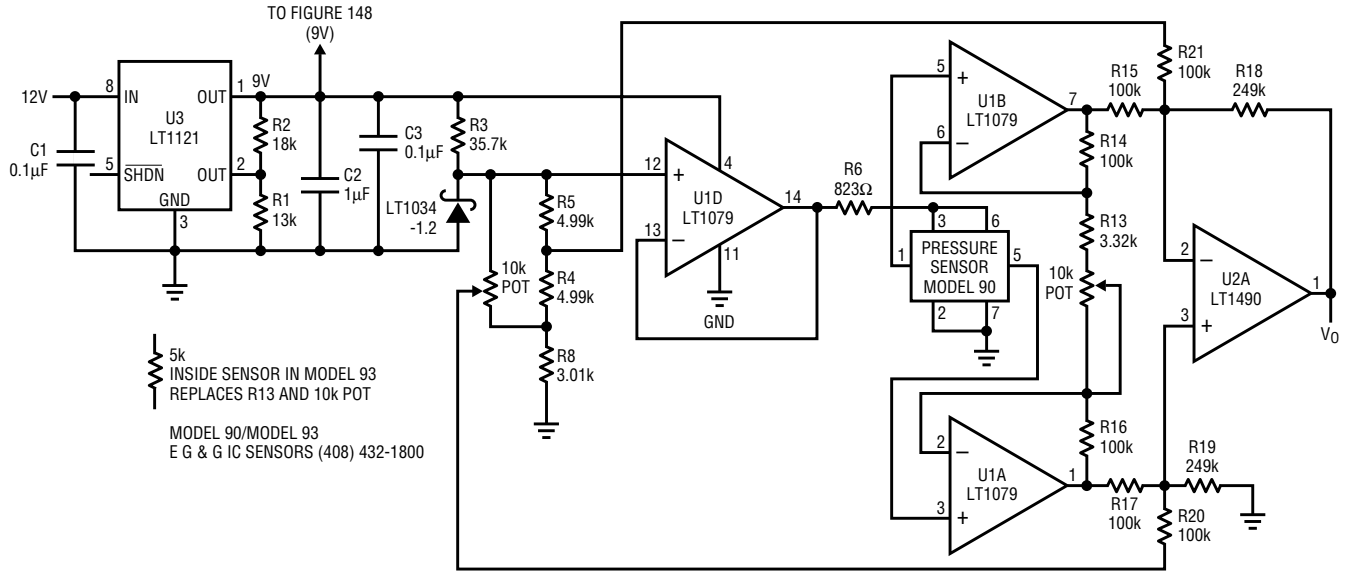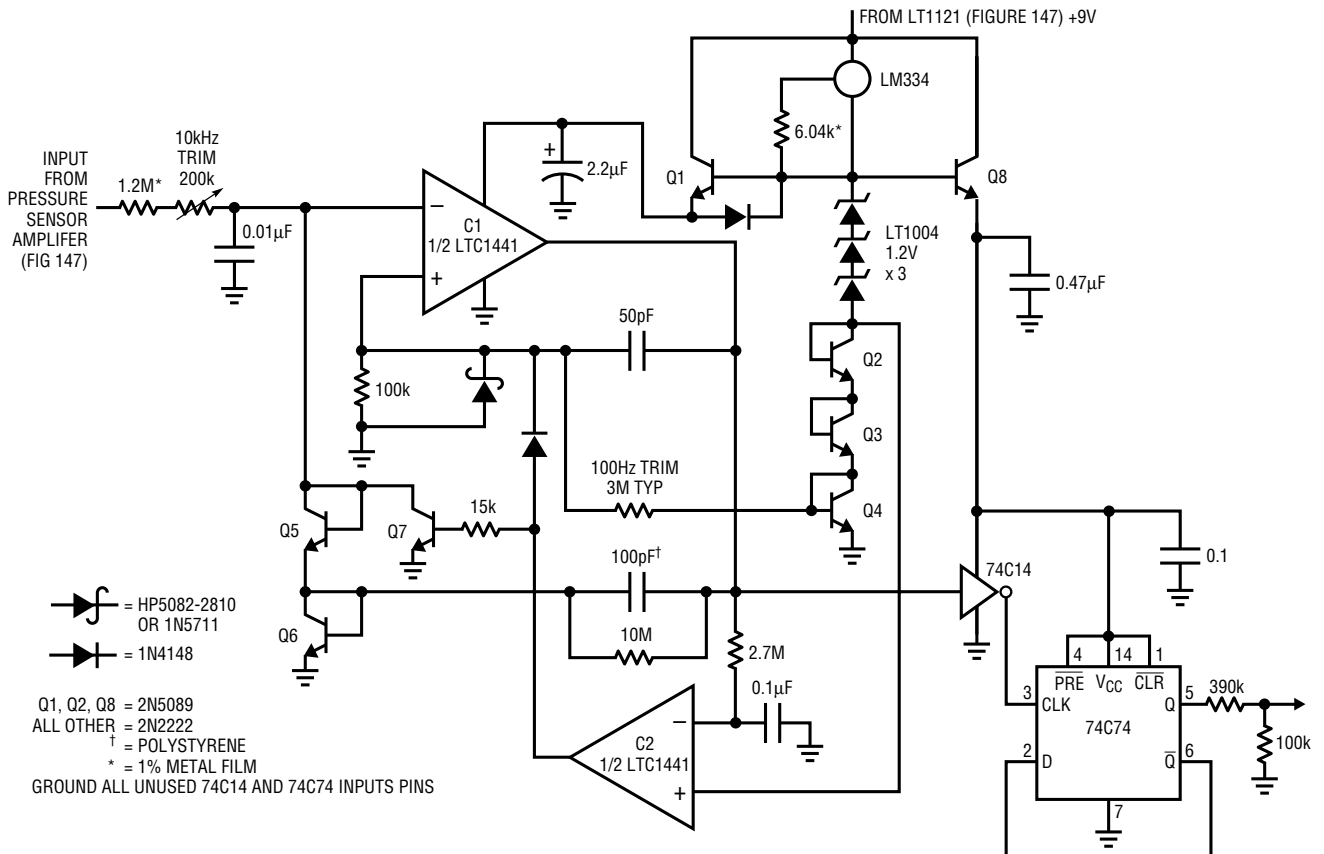
Figure 147. Pressure-Sensor Amplifier

Figure 148. This 0.02% V/F Converter Requires only 26µA Supply Current
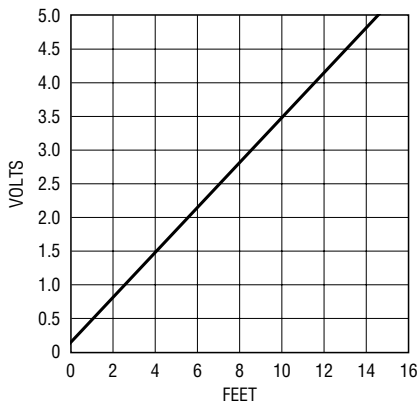
Figure 149. Output Voltage vs Column Height

In Figure 147, U3, the LT1121, converts 12V to 9V to power the system. The 12V may be obtained from a wall cube or batteries.

The LT1034, a 1.2V reference, is used with U1D, 1/4 of an LT1079 quad low power op amp, to provide a 1.5mA current source to the pressure sensor. The reference voltage is also divided down by R5, R8, R4 and the 10k potentiometer and used to offset the output amplifier, U2A, so that the signals are not too close to the supply rails.

Op amps U1A and U1B (each 1/4 of an LT1079) amplify the bridge pressure sensor's output and provide a differential signal to U2A (an LT1490). Note that U2A must be a rail-to-rail op amp. The system's analog output is taken from U2A's output.

Figure 149 plots the output voltage for the sensor system's analog front end versus the height of the water column that impinges on the pressure transducer. Note that the pressure change is independent of diameter of the water column, so that a tank of liquid would produce the same resulting output voltage. Figure 150 is a photograph of our test setup.

The remainder of the circuitry, shown in Figure 148, allows transmission of analog data over long distances. The circuit was designed by Jim Williams. The circuit takes a DC input from 0V to 5V and converts it to a frequency. For the pressure circuit in Figure 147, this translates to approximately 0Hz to 5kHz.

Figure 150. Test Setup for Water-Column Sensor

The voltage-to-frequency converter shown in Figure 148 has very low power consumption (26μA), 0.02% linearity, 60ppm/°C drift and 40ppm/V power supply rejection.

In operation, C1 switches a charge pump, comprising Q5, Q6 and the 100pF capacitor, to maintain its negative input at 0V. The LT1004s and associated components form a temperature-compensated reference for the charge pump.
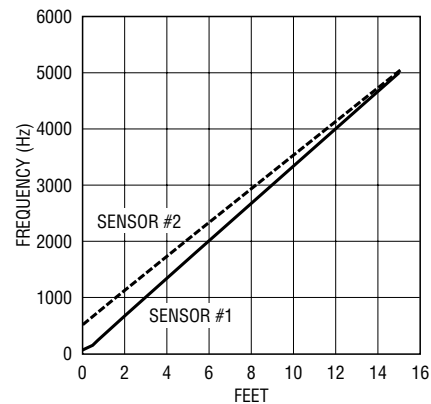

Figure 151. Output Frequency vs Column Height for Two Model 90 Sensors

The 100pF capacitor charges to a fixed voltage; hence, the repetition rate is the circuit's only degree of freedom to maintain feedback. Comparator C1 pumps uniform packets of charge to its negative input at a repetition rate precisely proportional to the input-voltage-derived current. This action ensures that circuit output frequency is determined strictly and solely by the input voltage.

Figure 151 shows the output frequency versus column height for two different Model 90 transducers. Note the straight lines, which are representative of excellent linearity.

Conclusion

A cost effective system is shown here consisting of a fluid pressure sensor, IC Sensors Model 90. This sensor's output is fed to signal processing electronics that convert the low level DC output of the bridge-based pressure sensor to a frequency in the audio range depending on the height of the fluid column impinging on the pressure transducer.

0.05μV/˚C CHOPPED AMPLIFIER REQUIRES ONLY 5μA SUPPLY CURRENT
by Jim Williams

Figure 152 shows a chopped amplifier that requires only 5.5μA supply current. Offset Voltage is 5μV, with 0.05μV/˚C drift. A gain exceeding 10^8 affords high accuracy, even at large closed-loop gains.

The micropower comparators (C1A and C1B) form a biphase 5Hz clock. The clock drives the input-related switches, causing an amplitude-modulated version of the DC input to appear at A1A's input. AC-coupled A1A takes

a gain of 1000, presenting its output to a switched demodulator similar to the aforementioned modulator.

The demodulator output, a reconstructed, DC-amplified version of the circuit's input, is fed to A1B, a DC gain stage. A1B's output is fed back, via gain setting resistors, to the input modulator, closing a feedback loop around the entire amplifier. The configuration's DC gain is set by the feedback resistor's ratio, in this case 1000.

The circuit's internal AC coupling prevents A1's DC characteristics from influencing overall DC performance, accounting for the extremely low offset uncertainty noted.
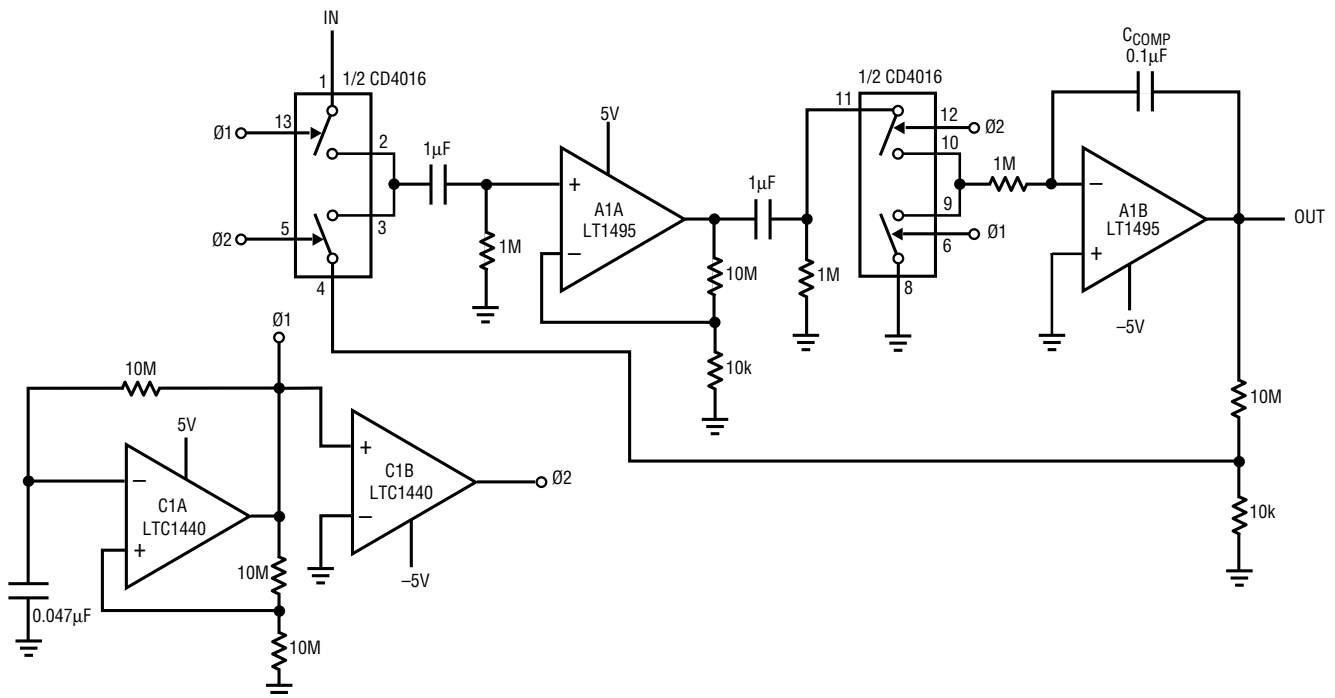

Figure 152. 0.05μV/˚C Chopped Amplifier Requires only 5μA Supply Current

The high open-loop gain permits 10ppm gain accuracy at a closed-loop gain of 1000.

The desired micropower operation and A1's bandwidth dictate the 5Hz clock rate. As such, the resultant overall bandwidth is *low*. Full-power bandwidth is 0.05Hz with a slew rate of about 1V/s. Clock-related noise, about 5µV, can be reduced by increasing C_{COMP}, with commensurate bandwidth reduction.

4.5ns DUAL-COMPARATOR-BASED CRYSTAL OSCILLATOR HAS 50% DUTY CYCLE AND COMPLEMENTARY OUTPUTS
by Joseph Petrofsky and Jim Williams

Figure 153's circuit uses the LT1720 dual comparator in a 50% duty cycle crystal oscillator. Output frequencies of up to 10MHz are practical.

The circuit of Figure 153 creates a pair of complementary outputs with a forced 50% duty cycle. Crystals are narrow-band elements, so the feedback to the noninverting input is a filtered analog version of the square wave output. Changing the noninverting reference level can therefore vary the duty cycle. C1 operates as in the previous example, where the 2k–600Ω resistor pair sets a bias point at the comparator's noninverting input. The 2k–1.8k–0.1µF path sets the inverting input at the node at an appropriate DC-average level based on the output. The

Figure 154. Output Skew Varies Only 800ps Over a 2.7V–6V Supply Excursion

crystal's path provides resonant positive feedback, and stable oscillation occurs. The DC bias voltages at the inputs are set near the center of the LT1720's common mode range and the 220Ω resistor attenuates the feedback to the noninverting input. C2 creates a complementary output by comparing the same two nodes with the opposite input polarity. A1 compares band-limited versions of the outputs and biases C1's negative input. C1's only degree of freedom to respond is variation of pulse width; hence, the outputs are forced to 50% duty cycle. The circuit operates from 2.7V to 6V and the skew between the edges of the of the two outputs is as shown in Figure 154. There is a slight duty-cycle dependence on comparator loading, so equal capacitive and resistive loading should be used in critical applications. This circuit works well because of the two matched delays and rail-to-rail–style outputs of the LT1720

Figure 153. Crystal Oscillator has Complementary Outputs and 50% Duty Cycle. A1's Feedback Maintains Output Duty Cycle Despite Supply Variations

LTC1531 ISOLATED COMPARATOR
by Wayne Shumaker

Introduction

The LTC1531 is an isolated, self-powered comparator that receives power and communicates through internal isolation capacitors. The internal isolation capacitors provide $3000V_{RMS}$ of isolation between the comparator and its output. This allows the part to be used in applications that require high voltage isolated sensing without the need to provide an isolated power source. The isolated side provides a 2.5V pulsed reference output that can deliver 5mA

for 100μs using the power stored on the isolated external capacitor. A 4-input, dual-differential comparator samples at the end of the reference pulse and transmits the result back to the nonisolated side. The nonisolated, powered side latches the result of the comparator and provides a zero-cross comparator output for triggering a triac.

Applications

The LTC1531 can be used to isolate sensors such as in the isolated thermistor temperature controller in Figure 155. In this circuit, a comparison is made between the voltages across a thermistor and a resistor that is driven by the 2.5V
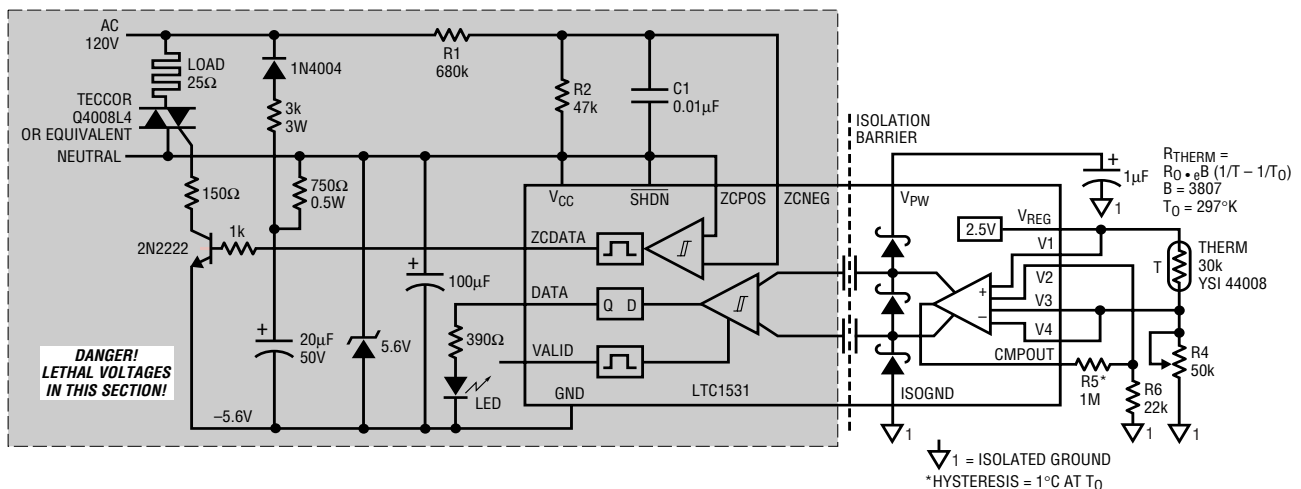
Figure 155. Isolated Thermistor Temperature Controller
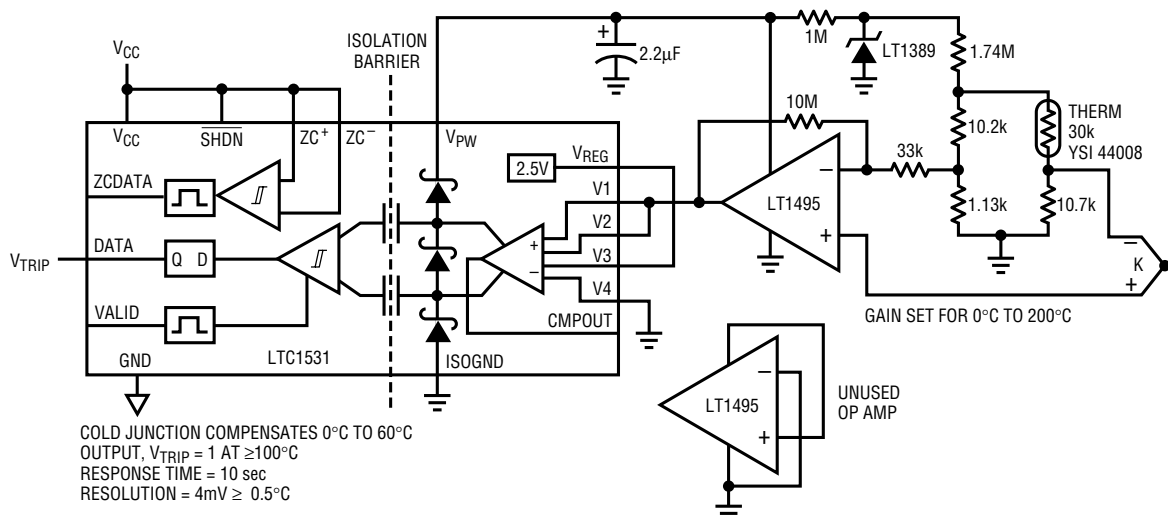
Figure 156. Overtemperature Detect

V_{REG} output. As the thermistor resistance rises with temperature, the voltage across the thermistor increases. When it exceeds the voltage across R4, the comparator output becomes zero and the triac control to the heater is turned off. Hysteresis can be added in the temperature control by using CMPOUT and R5. A 10° phase-shifted AC line signal is supplied through R1, R2 and C1 to the zero-cross comparator for firing the triac.

In the overtemperature detect application in Figure 156, an isolated thermocouple is cold junction compensated with the micropower LT1389 reference and the Yellow Springs thermistor. The micropower LT1495 op amp provides gain to give an overall 0°C–200°C temperature range, adjustable by changing the 10M feedback resistor. The isolated comparator is connected to compare at 1.25V or the center of the temperature range. In this case, V_{TRIP} goes high when the temperature exceeds 100°C.

The LTC1531 can use the high impedance nature of CMPOUT as a duty-cycle modulator, as in the isolated voltage sense application in Figure 157. The duty-cycle output of the comparator is smoothed with the LT1490 rail-to-rail op amp to reproduce the voltage at V_{IN}. The output time constant, $R2 \bullet C2$, should approximately equal the input time constant, $35 \bullet R1 \bullet C1$. The factor of 35 results from CMPOUT being on for only 100μs at an average sample rate of 300Hz.

Conclusion

The LTC1531 is a versatile part for sensing signals that require large isolation voltages. The ability of the LTC1531 to supply power through the isolation barrier simplifies applications; it can be combined with other micropower circuits in a variety of isolated signal conditioning and sensing applications.
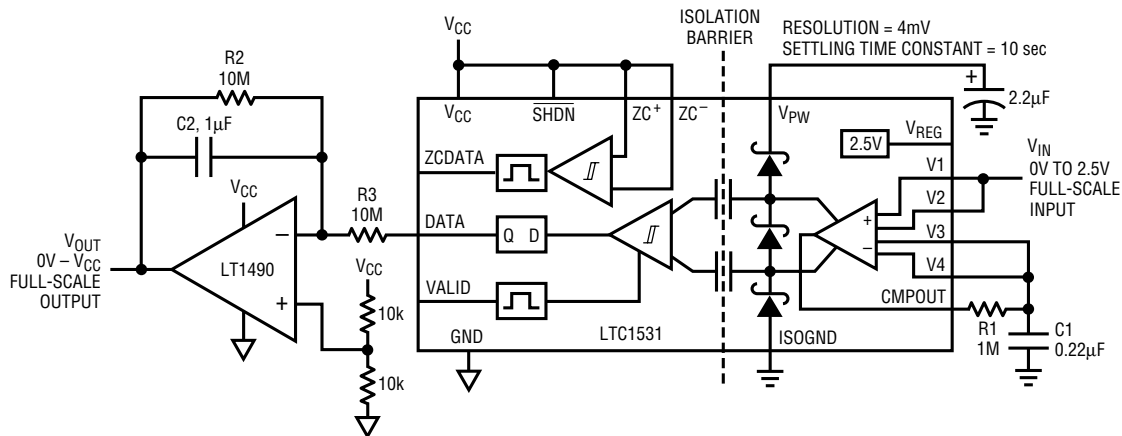

Figure 157. Isolated Voltage Detect

Filters

THE LTC1560-1: A 1MHz/500kHz CONTINUOUS-TIME, LOW NOISE, ELLIPTIC LOWPASS FILTER
by Nello Sevastopoulos

Introduction

The LTC1560-1 is a high frequency, continuous-time, low noise filter in an SO-8 package. It is a single-ended input, single-ended output, 5th order elliptic lowpass filter with a pin-selectable cutoff frequency (f_C) of 1MHz or 500kHz.

The LTC1560-1 delivers accurate fixed cutoff frequencies of 500kHz and 1MHz without the need for internal or external clocks.

Applications and Experimental Results

The LTC1560-1 can be used as part of a more complete frequency-shaping system. Two representative examples follow.

Highpass-Lowpass Filter

As a typical application in communication systems, where there is a need to reject DC and some low frequency signals, a 2nd order RC highpass network can be inserted in front of the LTC1560-1 to obtain a highpass-lowpass response. Figures 158 and 159 depict the network and its measured frequency response, respectively. Notice that the second resistor in the highpass filter is the input resistance of the LTC1560-1, which is about 8.1k.

Delay-Equalized Elliptic Filter

Although elliptic filters offer high Q and a sharp transition band, they lack a constant group delay in the passband, which implies more ringing in the time-domain step response. In order to minimize the delay ripple in the passband of the LTC1560-1, an allpass filter (delay equalizer) is cascaded with the LTC1560-1, as shown in Figure 160. Figures 161 and 162 illustrate the eye diagrams before and after the equalization, respectively.

An eye diagram is a qualitative representation of the time-domain response of a digital communication system. It shows how susceptible the system is to *intersymbol interference* (ISI). *Intersymbol interference* is caused by erroneous decisions in the receiver due to pulse overlapping and decaying oscillations of a previous symbol. A pseudorandom 2-level sequence has been used as the input of the LTC1560-1 to generate these eye diagrams. The larger eye opening in Figure 162 is an indication of the equalization effect that leads to reduced ISI. Note that in Figure 160, the equalizer section has a gain of 2 for driving and back-terminating 50Ω cable and load. For a simple unterminated gain-of-1 equalizer, the 40.2k resistor changes to 20k and the 49.9Ω resistor is removed from the circuit. The 22pF capacitors are 1% or 2% dipped silver mica or COG ceramic.
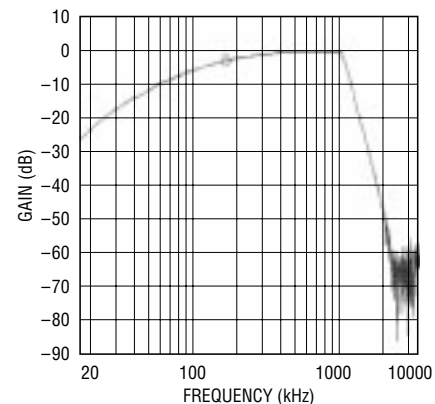

Figure 158. A Highpass-Lowpass Filter

Figure 159. Measured Frequency Response of Figure 158's Circuit

Conclusion

The LTC1560-1 is a 5th order elliptic lowpass filter that features a 10-bit gain linearity at signal ranges up to 1MHz. Being small and user friendly, the LTC1560-1 is suitable for any compact design. It is a monolithic replacement for larger, more expensive and less accurate solutions in communications, data acquisitions, medical instrumentation and other applications.
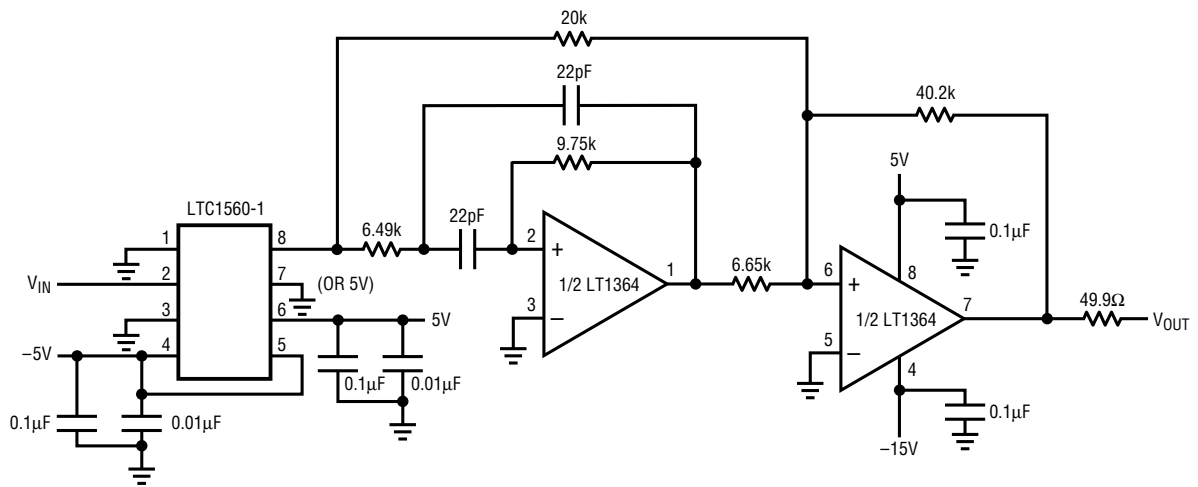

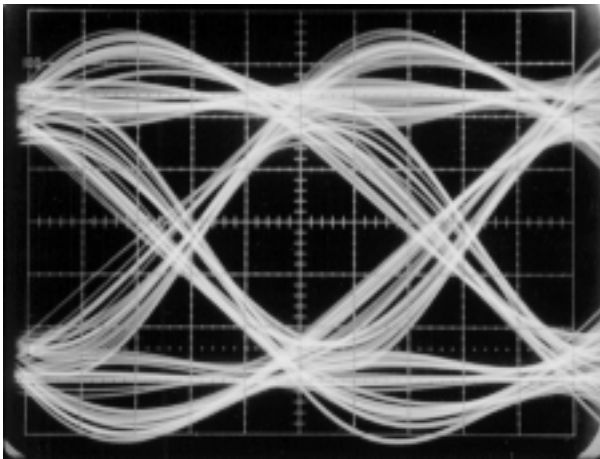**Figure 160. Augmenting the LTC1560-1 for Improved Delay Flatness**

Figure 161. 2-level Eye Diagram of the LTC1560-1 Before Equalization
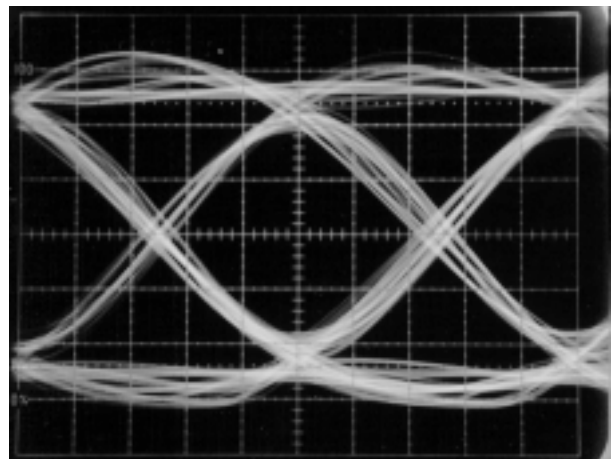
Figure 162. 2-level Eye Diagram of the Equalized Filter

THE LTC1067 AND LTC1067-50: UNIVERSAL 4TH ORDER LOW NOISE, RAIL-TO-RAIL SWITCHED CAPACITOR FILTERS
by Doug La Porte

LTC1067 and LTC1067-50 Overview

The LTC1067 and the LTC1067-50 are universal, 4th order switched capacitor filters with rail-to-rail operation. Each part contains two identical, high accuracy, very wide dynamic-range 2nd order filter building blocks. Each building block, together with three to five resistors, provides 2nd order filter transfer functions, including lowpass, bandpass, highpass, notch and allpass. These parts can be used to easily design 4th order or dual 2nd order filters.

Linear Technology's FilterCAD™ for Windows® filter design software fully supports designs with these parts.

The center frequency of each 2nd order section is tuned by an external clock. The LTC1067 has a 100:1 clock-to-center frequency ratio. The LTC1067-50's clock-to-center frequency ratio is 50:1.

Some LTC1067 and LTC1067-50 Applications

High Dynamic-Range Butterworth Lowpass Filter with Built-In Track-and-Hold Challenges Discrete Designs

Figure 163 shows an LTC1067 configured as a 5kHz Butterworth lowpass filter. This circuit runs on a 3.3V power supply and uses an external logic gate to stop the clock for track-and-hold operation. The transfer function for this circuit, shown in Figure 164, is the classical Butterworth response. This circuit can be used with either the LTC1067 or the LTC1067-50. The broad-band noise for the LTC1067 circuit is $45\mu V_{RMS}$ and the DC offset is typically less than 10mV. For the LTC1067-50, the broad-band noise is $55\mu V_{RMS}$ and the DC offset is typically less than 15mV.

This circuit has tremendous dynamic range, even on low supply voltages. Figure 165 shows a plot of the LTC1067's signal-to-noise plus total harmonic distortion (SINAD) vs input signal level for a 1kHz input at three different power supply voltages. SINAD is limited for small signals by the noise floor of the LTC1067, for medium signals by the part's linearity and for large signals by the output signal swing. The part's low noise input stage and excellent linearity allow the SINAD to exceed 80dB for signals as small as $700mV_{P-P}$, while the rail-to-rail output stage maintains this level for input signals approaching the

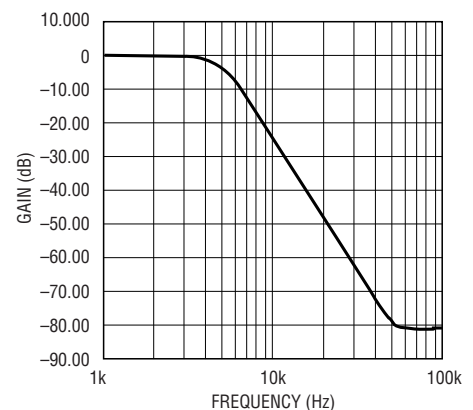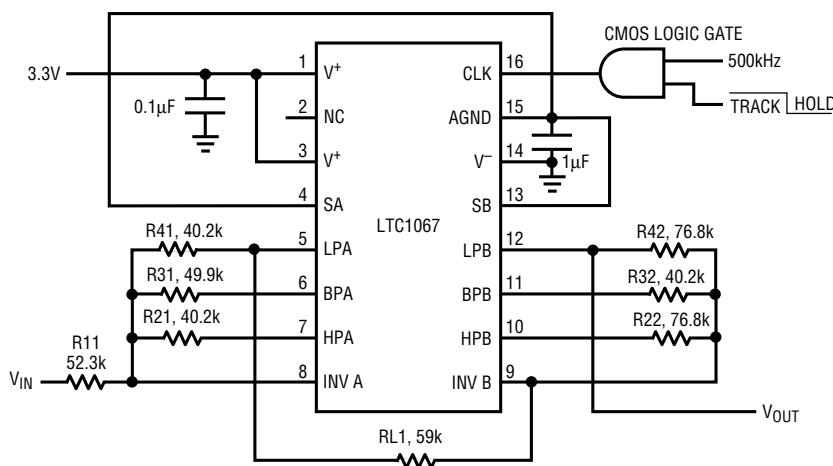**Figure 163. High Dynamic-Range Butterworth LPF with Track-and-Hold Control**

Figure 164. Transfer Function of the LTC1067 5kHz Butterworth LPF

Figure 165. Dynamic Range of LTC1067 Butterworth LPF
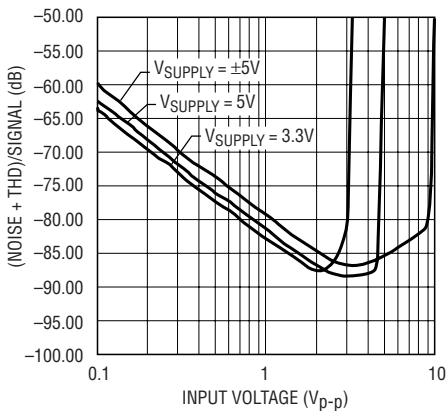

Figure 166. Dynamic Range of LTC1067-50 Butterworth LPF

supply rails. Previous parts could not attain this high dynamic range due to higher input noise levels, poor linearity and limited output-stage signal swing. The low noise and rail-to-rail output swing are especially crucial on the lower 3.3V power supply, where every bit of detectable signal range is precious. Figure 166 shows the same plot for the LTC1067-50 circuit. The dynamic range is not quite equal to that of the LTC1067, but is still very good. Recall that, for the same clock frequency, the LTC1067-50 based filter has double the bandwidth and half the supply current of the LTC1067.

The LTC1067 and LTC1067-50 also perform a track-and-hold function. Stopping the clock holds the output of the filter at its last value. The LTC1067 is the best performing part in this area. The LTC1067's hold step is less than

$-100\mu V$ and the droop rate is less than $-50\mu V/ms$ over the full temperature range. These numbers compare very favorably with dedicated track-and-hold amplifiers. When the clock is restarted, the filter resumes normal operation within ten clock cycles and the output will then correctly reflect the input as soon as the filter's mathematical response allows.

Elliptic Lowpass Filter

The LTC1067 family is capable of much more challenging filters. Figure 167 shows the schematic for a 25kHz elliptic lowpass filter using the LT1067-50 operating on a 5V supply. Maximum attenuation one octave from the −3dB corner is the design goal for this filter. Figure 168 shows the frequency response of the filter with the −3dB cutoff at
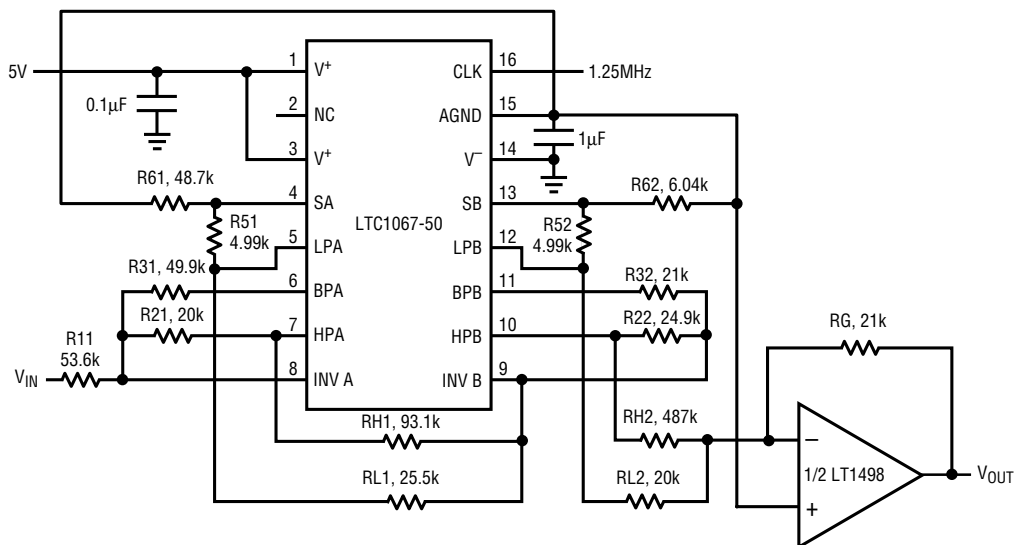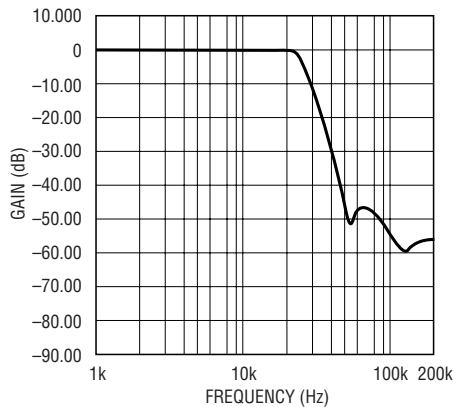

Figure 167. 25kHz Elliptic Lowpass Filter

Figure 168. Transfer Function of LTC1067-50 25kHz LPF

Figure 169. Low Noise, Low Voltage Narrow BPF

25kHz and –48dB of attenuation at 50kHz. The broad-band noise of the filter is 85μV_{RMS} and the DC offset is less than 15mV typically.

Although Figure 167 shows the filter powered by a single 5V supply, 3.3V or ±5V supply operation is also supported. The maximum cutoff frequency is 15kHz for the 3.3V supply and 35kHz for the ±5V supply. The same design and schematic used with an LTC1067 will achieve a somewhat lower noise, lower DC-offset filter. With the LTC1067, the broad-band noise is 70μV_{RMS} and the DC offset is typically less than 10mV. The maximum operating frequencies for the LTC1067 are one half of those for the LTC1067-50.

Narrow-Band Bandpass Filter Design Extracts Small Signals Buried in Noise

Narrow-band bandpass filters are difficult to design but are easily achievable with these parts. Most applications for these filters involve extracting a low level signal from a noisy environment. The noise may be the standard broad-band, Gaussian-type noise or it may consist of multiple interfering signals. For example, the signal may be a low level tone or a narrow-bandwidth modulated signal, in a voice-band system. The presence of the tone must be detected even while the large voice signals are present. A narrow-band bandpass filter will allow the tone to be separated and detected even in this hostile environment. Numerous systems also require a narrow bandpass filter to be swept across a band looking for the tones. Switched capacitor filters allow the filter to be swept by simply changing the clock frequency.
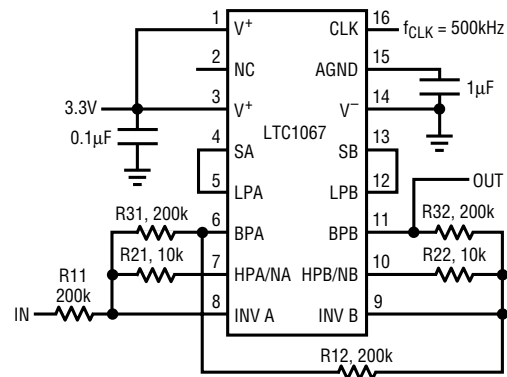
To achieve success in designing narrow-band bandpass filters, you must start with precision components. In an LC or RC design, you would have to start with 0.1% resistors, 1% inductors and 1% capacitors to have any hope of finishing with a successful, repeatable design in production. A competing solution, a digital filter implementation, also requires precision components. The full input signal (signal, noise and out-of-band interference) must be correctly digitized and then processed with a DSP device to finally determine the tone's presence. If an out-of-band interfering signal is 20dB greater than the desired tone, the ADC must have an extra 20dB of dynamic range above the signal's requirement. To pull a small-signal tone from a large signal interferer, you may need a 16-bit ADC to digitize the signal just to get 12-bit resolution of the tone after processing. The added cost, power, board space and development time make this approach unattractive.
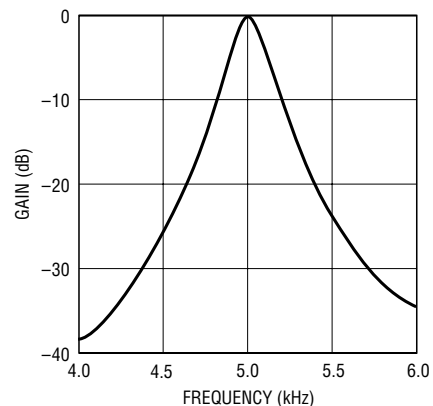

Figure 170. Frequency Response of Narrow BPF

A precision switched capacitor filter provides a simple, small, low power, repeatable, inexpensive solution. The older MF-10-type parts do not have the necessary f_O accuracy to achieve a reliable, repeatable design. Figure 169 shows the schematic of a narrow-band bandpass filter centered at 5kHz. The design uses two identical cascaded sections, each with a Q of 20. Multiply the individual Q of each section by 1.554 to calculate the total Q of a filter with two identical f_O, identical Q sections. This filter has a total Q of 31. For tunable filter applications, simply lowering the clock frequency lowers the center frequency of the filter. Figure 170 shows the frequency response of this filter. The broad-band noise of this filter is only 90μV_{RMS}. Highly selective bandpass filters are possible due to the LTC1067's excellent f_O accuracy.

Higher Q, narrower bandwidth filters are achievable with 0.1% resistors or matched resistor networks. An LTC1067 mask-programmed part is ideal for these ultranarrow filters. The well matched, on-chip resistors, coupled with specified test conditions, yield a fully functioning filter module, in an SO-8 package, without any of the hassles or cost of procuring precision resistors or resistor networks.
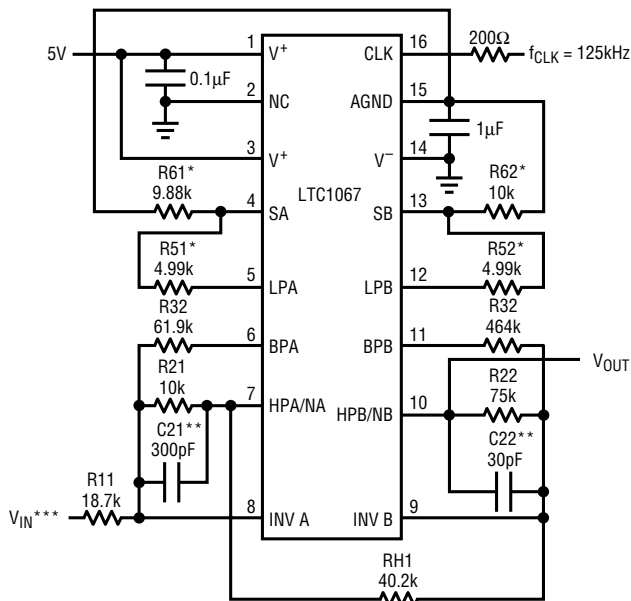
Narrow-Band Notch Filter Design Reaches 80dB Notch Depth

Narrow-band notch filters are especially challenging designs. The requirement for most notch filters is to remove a particular tone and not affect any of the remaining signal bandwidth. This requires an infinitesimally narrow filter that can only be approximated by a reasonably narrow bandwidth. These types of filters, like the narrow-band bandpass discussed above, require precision f_O accuracy. Figure 171 shows the schematic of this type of filter. This filter is a 1.02kHz notch filter that is often used in telecommunication test systems.

One of the challenges of designing a switched capacitor notch filter involves the broad-band nature of a notch filter. The broad-band noise can be aliased down into the band of interest. Optimal high performance notch filters should employ some form of noise-band limiting. To accomplish the noise-band limiting, the design in Figure 171 places capacitors in parallel with the R2 resistors of each 2nd order section. This forms a pole, set at $f_P = 1/(2 \bullet \pi \bullet R2 \bullet C2)$, that will limit the bandwidth. This pole frequency must be low enough to have a band-limiting effect but must not be so low as to affect the notch filter's response. The pole should be greater than thirty times the notch frequency and less than seventy-five times the notch frequency for the best results. Figure 172 shows the frequency response of the filter. Note that the notch depth is greater than –80dB. Without the use of the C21 and C22, the notch depth is only about –35dB.
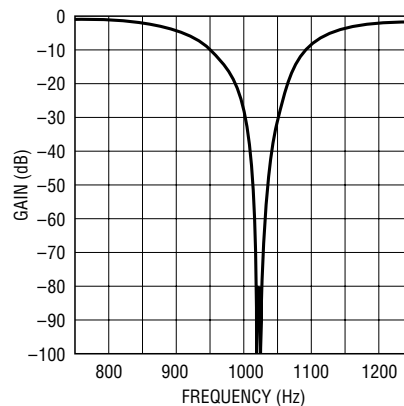

* R51, R61, R52, R62 ARE 0.1% TOLERANCE RESISTORS
** C21 AND C22 IMPROVE THE NOTCH DEPTH WHERE
$(30)(f_{NOTCH}) < \dfrac{1}{2\pi(R2X)(C2X)} < (75)(f_{NOTCH})$ WITHOUT
C21 AND C22 THE NOTCH DEPTH IS LIMITED TO –35dB
*** $V_{IN} \leq 1.25V_{P-P}$

Figure 171. Narrow-Band Notch Filter

Figure 172. Measured Frequency Response of Figure 171's Narrow-Band Notch Filter

UNIVERSAL CONTINUOUS-TIME FILTER CHALLENGES DISCRETE DESIGNS
by Max Hauser

The LTC1562 is the first in a new family of tunable, DC-accurate, continuous-time filter products featuring very low noise and distortion. It contains four independent 2nd order, 3-terminal filter blocks that are resistor program-mable for lowpass or bandpass functions up to 150kHz, and has a complete PC board footprint smaller than a dime. Moreover, the part can deliver arbitrary continuous-time pole-zero responses, including highpass, notch and elliptic, if one or more programming resistors are replaced with capacitors. The center frequency (f_0) of the LTC1562 is internally trimmed, with an absolute accuracy of 0.5%, and can be adjusted independently in each 2nd order section from 10kHz to 150kHz by an external resistor. Other features include:

❏ Rail-to-rail inputs and outputs
❏ Wideband signal-to-noise ratio (SNR) of 103dB
❏ Total harmonic distortion (THD) of –96dB at 20kHz, –80dB at 100kHz
❏ Built-in multiple-input summing and gain features; capable of 118dB dynamic range
❏ Single- or dual-supply operation, 4.75V to 10.5V total
❏ "Zero-power" shutdown mode under logic control
❏ No clocks, PLLs, DSP or tuning cycles required

The LTC1562 provides eight poles of programmable con-tinuous-time filtering in a total surface mount board area (including the programming resistors) of 0.24 square inches ($155\,mm^2$)—smaller than a U.S. 10-cent coin. This filter can also replace op amp–R-C active filter circuits and LC filters in applications requiring compactness, flexibil-ity, high dynamic range or fewer precision components.

Each of the four 3-terminal Operational Filter™ building blocks in an LTC1562 has a virtual ground input, INV, and two outputs, V1 and V2. These are described in detail in the LTC1562 data sheet.

Dual 4th Order 100kHz Butterworth Lowpass Filter

The practical circuit in Figure 173 is a dual lowpass filter with a Butterworth (maximally-flat-passband) frequency response. Each half gives a DC-accurate, unity-passband-gain lowpass response with rail-to-rail input and output. With a 10V total power supply, the measured output noise for one filter is $36\mu V_{RMS}$ in a 200kHz bandwidth, and the large-signal output SNR is 100dB. Measured THD at $1V_{RMS}$ input is –83.5dB at 50kHz and –80dB at 100kHz. Figure 174 shows the frequency response of one filter.

8th Order 30kHz Chebyshev Highpass Filter

Figure 175 shows a straightforward use of the highpass configuration. Each of the four cascaded 2nd order sections has an external capacitor in the input path. The resistors in Figure 175 set the f_0 and Q values of the four sections to realize a Chebyshev (equiripple-passband) response with 0.05dB ripple and a 30kHz highpass corner. Figure 176 shows the frequency response. Total output noise for this circuit is $40\mu V_{RMS}$.

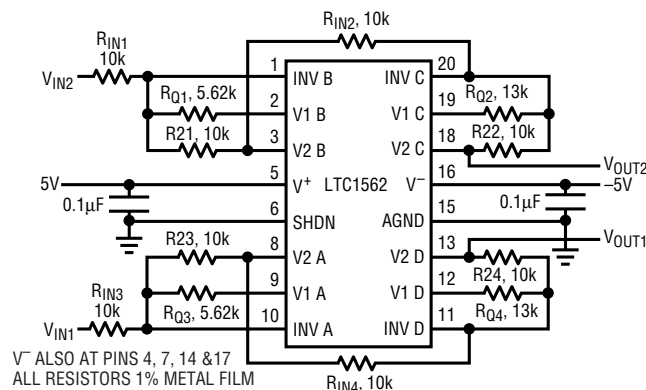**Figure 173. Dual, Matched 4th Order 100kHz Butterworth Lowpass Filter**

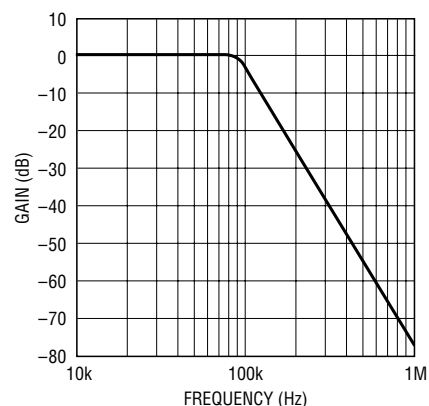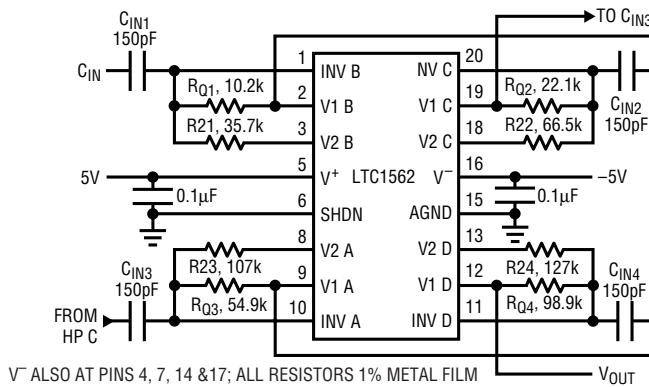**Figure 174. Frequency Response of Figure 173's Circuit**

Figure 175. 8th Order Chebyshev Highpass Filter with 0.05dB Ripple (f$_{CUTOFF}$ = 30kHz)

50kHz, 100dB Elliptic Lowpass Filter

Figure 177 illustrates how sharp-cutoff filtering can exploit the Operational Filter capabilities of the LTC1562. In this design, external capacitors are added and the virtual-ground inputs of the LTC1562 sum parallel paths to obtain three notches in the stopband of a lowpass filter, as plotted in Figure 178. This response falls 100dB in a little more than one octave; the total output noise is 60μV$_{RMS}$ with the rail-to-rail output for a peak SNR of 95dB from ±5V supplies.

Quadruple 3rd Order 100kHz Butterworth Lowpass Filter

Another example of the flexibility of the virtual-ground inputs is the ability to add an extra, independent real pole with an R-C-R "T" network. In Figure 179, a 10k input resistor has been split into two parts and the parallel combination of the two forms a 100kHz real pole with the 680pF external capacitor. Four such 3rd order Butterworth

Figure 177. 50kHz Elliptic Lowpass Filter with 100dB Stopband Rejection

lowpass filters can be built from one LTC1562. The same technique can add additional real poles to other filter configurations as well, for example, augmenting Figure 173's circuit to obtain a dual 5th order filter from a single LTC1562.

Conclusion

The LTC1562 is the first truly compact universal active filter, yet it offers instrumentation-grade performance rivaling much larger discrete-component designs. It serves applications in the 10kHz–150kHz range with an SNR as high as 100dB or more (16+ equivalent bits). The LTC1562 is ideal for modems and other communications systems and for DSP antialiasing or reconstruction filtering.
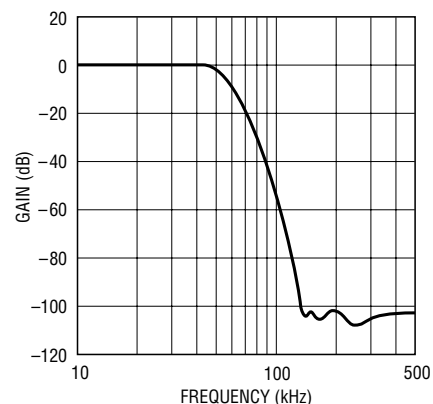

Figure 176. Frequency Response of Figure 175's Circuit

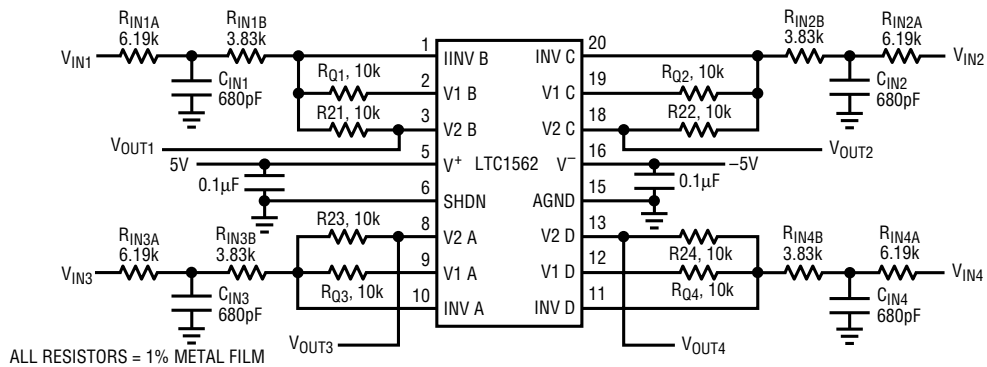**Figure 178. Frequency Response of Figure 177's Circuit.**

Figure 179. Quad 3-Pole 100kHz Butterworth Lowpass Filter

HIGH CLOCK-TO-CENTER FREQUENCY RATIO LTC1068-200 EXTENDS CAPABILITIES OF SWITCHED CAPACITOR HIGHPASS FILTER
by Frank Cox

The circuit in Figure 180 is a 1kHz 8th order Butterworth highpass filter built with the LTC1068-200, a switched capacitor filter (SCF) building block. In the past, commercially available switched capacitor filters have had limited use as highpass filters because of their sampled-data nature. Sampled-data systems generate spurious frequencies when the sampling clock of the filter and the input signal mix. These spurious frequencies can include

sums and differences of the clock and the input, in addition to sums and differences of their harmonics. The input of the filter must be band limited to remove frequencies that will mix with the clock and end up in the passband of the filter. Unfortunately, the passband of a highpass filter extends upward in frequency by its very nature. If you have to band limit the input signal too much you will also limit the passband of the filter, and hence its usefulness.

What makes this filter different is the 200:1 clock-to-center frequency ratio (CCFR) and the internal sampling scheme of the LTC1068-200. Figure 181a shows the amplitude response of the filter plotted against frequency from
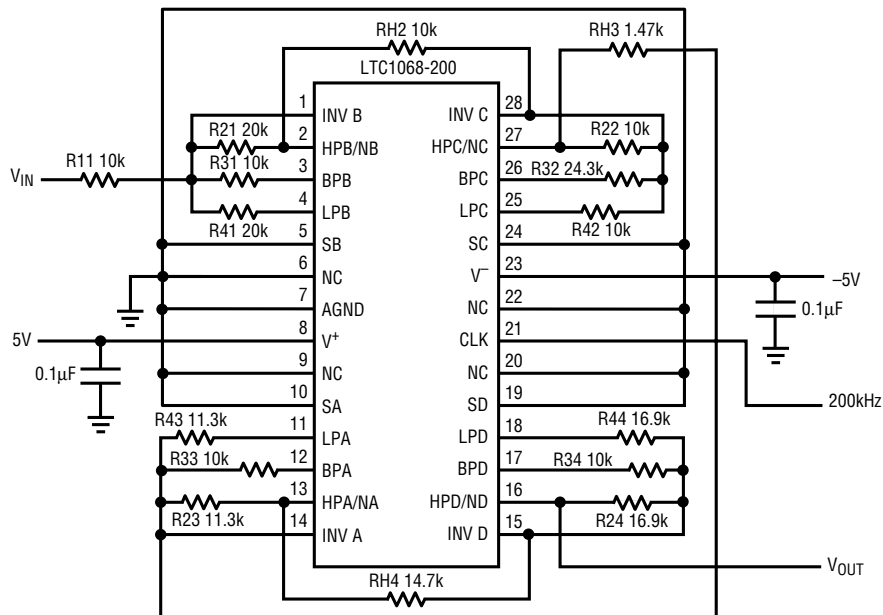

Figure 180. LTC1068-200 1kHz 8th Order Butterworth Highpass Filter

100Hz to 10kHz. For comparison, Figure 181b shows the same filter built with an LTC1068-25. This is a 25:1 CCFR part. The 200:1 CCFR filter delivers almost 30dB more ultimate attenuation in the stopband. A standard amplitude vs frequency plot of a highpass filter can be misleading because it masks some of the aforementioned spurious signals introduced into the passband. Figure 182a is a spectrum plot of the 200:1 filter with a single 10kHz tone on the input. This plot shows that the spurious free dynamic range (SFDR) of the LTC1068 highpass filter is in excess of 70dB. In fact, the filter has a 70dB SFDR for all input signals up to 100kHz. In a 200kHz sampled-data system, you would normally need to band limit the input below 100kHz, the Nyquist frequency. Because the LTC1068 uses double sampling techniques, its useful input frequency range extends to the Nyquist frequency

and even above, albeit with some care. Figure 182b shows the LTC1068-200 highpass filter with an input frequency of 150kHz. There is a spurious signal at 50kHz, but even though there is no input filtering, the SFDR is still 60dB. For input signals from 100kHz to 150kHz, the filter demonstrates an SFDR of at least 60dB. The SFDR plot of the same filter built with the LTC1068-25 is shown in Figure 183. Note that the lower CCFR (25:1) part still manages a respectable 55dB SFDR with a 10kHz input. The LTC1068-25 is used primarily for band-limited applications, such as lowpass and bandpass filters.

Note:

The filters for this article were designed using Linear Technology's Filter-CAD™ (version 2.0) for Windows®. This program made the design and optimization of these filters fast and easy.
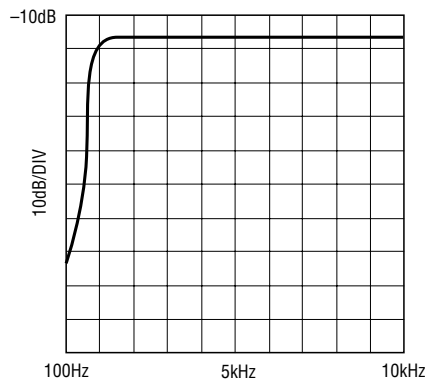

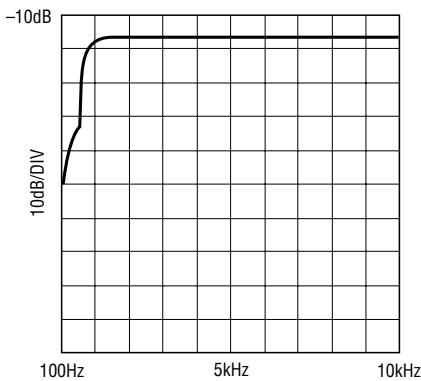**Figure 181a. Amplitude vs Frequency Response of Figure 180's Circuit**

Figure 181b. Amplitude vs Frequency Response of Comparable Filter Using the LTC1068-25
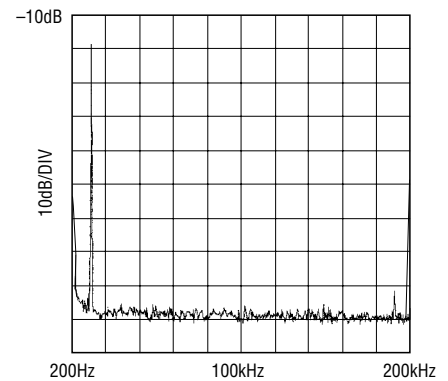

Figure 182a. Spectrum Plot of Figure 180's Circuit with a Single 10kHz Input
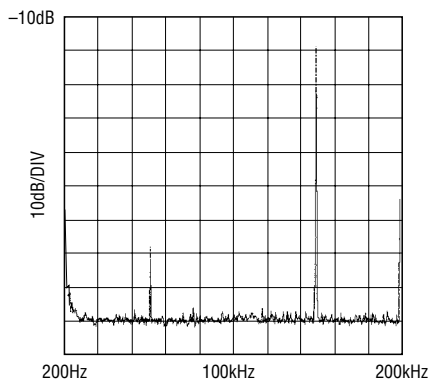

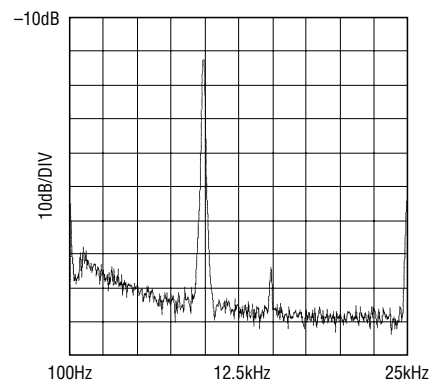**Figure 182b. Spectrum Plot of Figure 180's Circuit with a Single 150kHz Input**

Figure 183. Spectrum Plot of a Comparable Filter Using the LTC1068-25 with a Single 10kHz Input Shows a Respectable 55dB SFDR.

CLOCK-TUNABLE, HIGH ACCURACY, QUAD 2ND ORDER, ANALOG FILTER BUILDING BLOCKS

by Philip Karantzalis

Introduction

The LTC1068 product family consists of four monolithic, clock-tunable filter building blocks. Each product contains four matched, low noise, high accuracy 2nd order switched capacitor filter sections. An external clock tunes the center frequency of each 2nd order filter section. The LTC1068 products differ only in their clock-to-center frequency ratio. The clock-to-center frequency ratio is set to 200:1 (LTC1068-200), 100:1 (LTC1068), 50:1 (LTC1068-50) or 25:1 (LTC1068-25). External resistors can modify the clock-to-center frequency ratio. Designing filters with an LTC1068 product is fully supported by the FilterCAD 2.0 design software for Windows. The internal sampling rate of all the LTC1068 devices is twice the clock frequency. This allows the frequency of input signals to approach twice the clock frequency before aliasing occurs. Maximum clock frequency for LTC1068-200, LTC1068 and LTC1068-25 is 6MHz with ±5V supplies; that for the LTC1068-50 is 2MHz with a single 5V supply. For low power filter applications, the LTC1068-50 power supply current is 4.5mA with a single 5V supply and 2.5mA with a single 3V supply. The LTC1068 products are available in a 28-pin SSOP surface mount package. The LTC1068 (the 100:1 part) is also available in a 24-pin DIP package.

LTC1068-200 Ultralow Frequency Linear-Phase Lowpass Filter

Figure 184 shows an LTC1068-200 linear-phase 1Hz lowpass filter schematic and Figure 185 shows its gain and group delay responses. The clock frequency of this filter is 400 times the –3dB frequency (f_{-3dB} or f_{CUTOFF}). The large clock-to-f_{CUTOFF} frequency ratio of this filter is useful in ultralow frequency filter applications when minimizing aliasing errors could be an important consideration. For example, the 1Hz lowpass filter shown in Figure 184 requires a 400Hz clock frequency. For this filter, the input frequencies that can generate aliasing errors are in a band from 795Hz to 805Hz ($2 \cdot f_{CLK} \pm 5 \cdot f_{-3dB}$). For most very low frequency signal-processing applications, the signal spectrum is less than 100Hz. Therefore, Figure 184's filter will process very low frequency signals without significant aliasing errors, since its clock frequency is 400Hz and the aliasing inputs are in a small band around 800Hz.
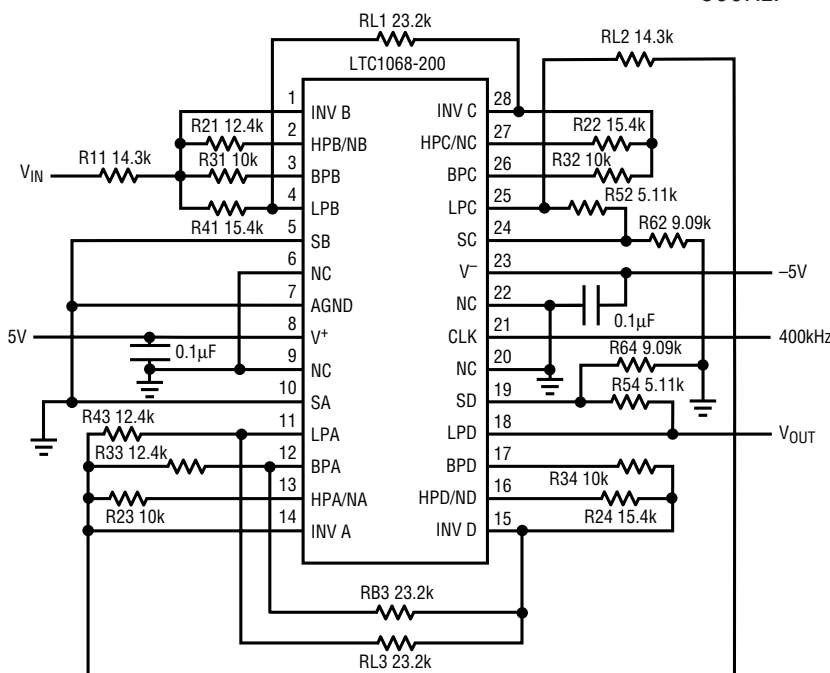

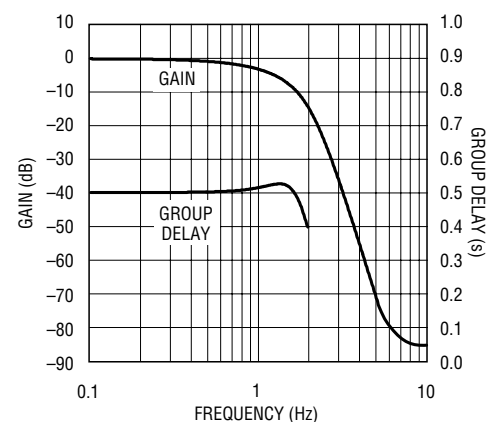**Figure 184. Linear-Phase Lowpass Filter: f_{-3dB} = 1Hz = f_{CLK}/400**

Figure 185. Gain and Group Delay Response of Figure 184's Circuit.

LTC1068-50 Single 3.3V Low Power Linear-Phase Lowpass Filter

Figure 186 is a schematic of an LTC1068-50-based, single 3.3V, low power, lowpass filter with linear phase. The clock-to-f_{CUTOFF} ratio is 50 to 1 (f_{CUTOFF} is the –3dB frequency). Figure 187 shows the gain and group delay response. The flat group delay response in the filter's passband implies a linear phase. A linear-phase filter has a transient response with very small overshoot that settles very rapidly. A linear-phase lowpass filter is useful for processing communication signals with minimum intersymbol interference in digital communications transmitters or receivers. The maximum clock frequency for this filter is 1MHz with a single 3.3V supply and 2MHz with a single 5V supply. Typical power supply current is 3mA with a single 3.3V supply and 4.5mA with a single 5V supply.
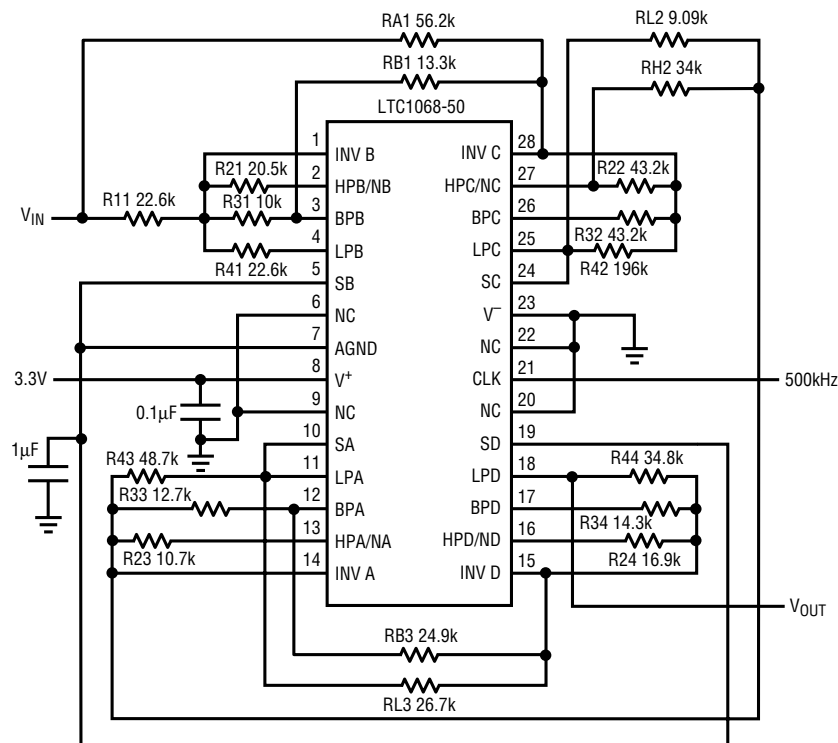
LTC1068-25 Selective Bandpass Filter is Clock Tunable to 80kHz

Figure 188 shows a 70kHz bandpass filter based on the LTC1068-25 operating with dual 5V power supplies. The clock-to-center frequency ratio is 25 to 1. Figure 189 shows the gain response of Figure 188's bandpass filter. The passband of this filter extends from $0.95 \cdot f_{CENTER}$ to $1.05 \cdot f_{CENTER}$. The stopband attenuation is greater than 40dB at $0.8 \cdot f_{CENTER}$ and $1.15 \cdot f_{CENTER}$. The center frequency can be clock tuned to 80kHz with dual 5V supplies and to 40kHz with a single 5V supply. With FilterCAD, the LTC1068-25 can be used to realize bandpass filters less selective than that shown in Figure 188, which can be clock tuned up to 160kHz with dual 5V supplies.
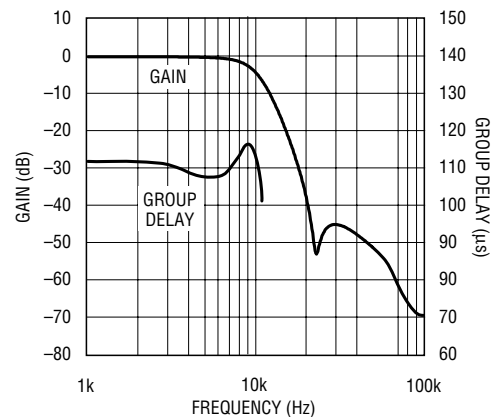

Figure 186. Low Power, Single 3.3V Supply, 10kHz, 8th Order, Linear-Phase Lowpass Filter

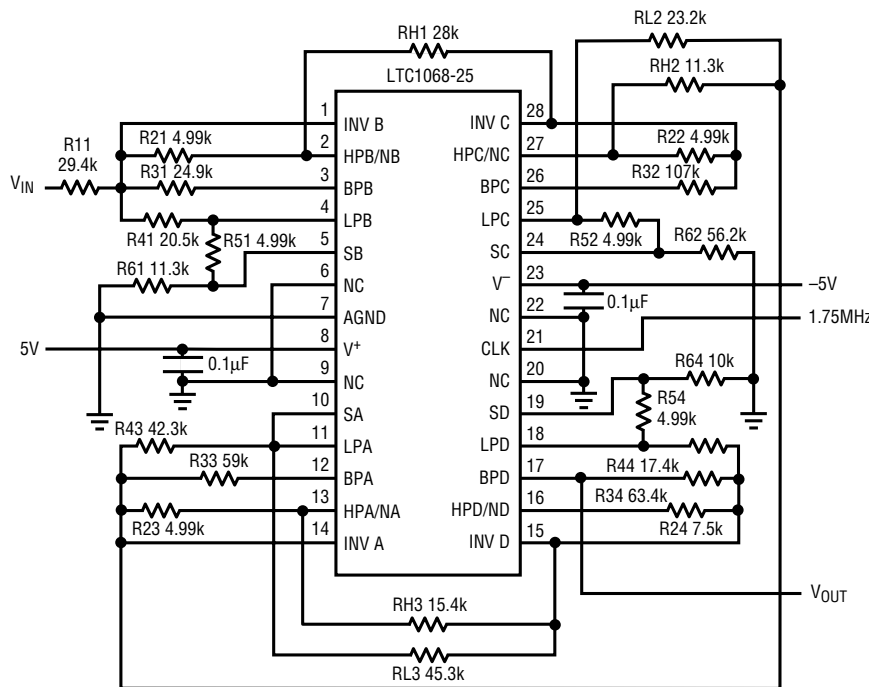**Figure 187. Gain and Group Delay Response of Figure 186's Filter**

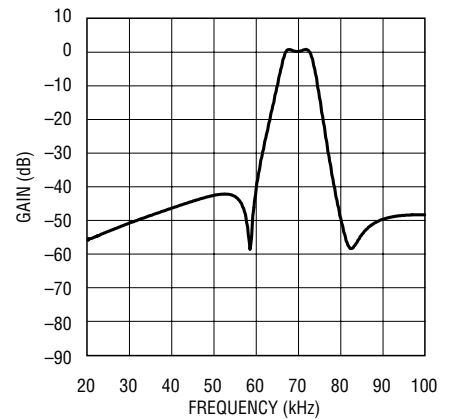Figure 188. 70kHz, 8th order, Bandpass Filter

Figure 189. Gain Response of Figure 188's Filter

LTC1068 Square-Wave-to-Quadrature Oscillator Filter

Figure 190 shows the schematic of a LTC1068 based filter that is specifically designed to produce a low harmonic distortion sine and cosine oscillator from a CMOS-level square wave input. The reference sine wave output of Figure 190's circuit is on pin 15 (BPD on the 24-pin LTC1068 package) and the cosine output is on pin 16 (LPD on the 24-pin LTC1068 package). The output frequency of this quadrature oscillator is the filter's clock frequency divided by 128. The output of a CMOS CD4520 divide-by-128 counter is coupled with a 0.47µF capacitor to the input to the LTC1068 filter operating with dual 5V power supplies. The filter's clock frequency is the input to the CD4520 counter. The LTC1068 filter is designed to pass the fundamental frequency component of a square wave and attenuate any harmonic components higher than the fundamental. An ideal square wave (50% duty cycle) will have only odd harmonics (3rd, 5th, 7th and so on), whereas a typical practical square wave has a duty cycle less or more than 50% and will also have even harmonics (2nd, 4th, 6th and so on). The filter of Figure 190 has a stopband notch at the 2nd and 3rd harmonics for a square wave input with a frequency equal to the filter's clock frequency divided by 128. The filter's sine wave output (pin 15) is 1V_{RMS} for a ±2.5V square wave input and has less than 0.025% THD (total harmonic distortion) for input frequencies up to 16kHz and less than 0.1% THD for frequencies up to 20kHz. The cosine output (on pin 16, referenced to pin 15's sine wave output) is 1.25V_{RMS} for a ±2.5V square wave input and has less than 0.07% THD for frequencies up to 20kHz.

The 20kHz frequency limit is due to the CD4520; with a 74HC type divide-by-128 counter, sine and cosine waves up to 40kHz can be generated with the LTC1068-based filter of Figure 190.
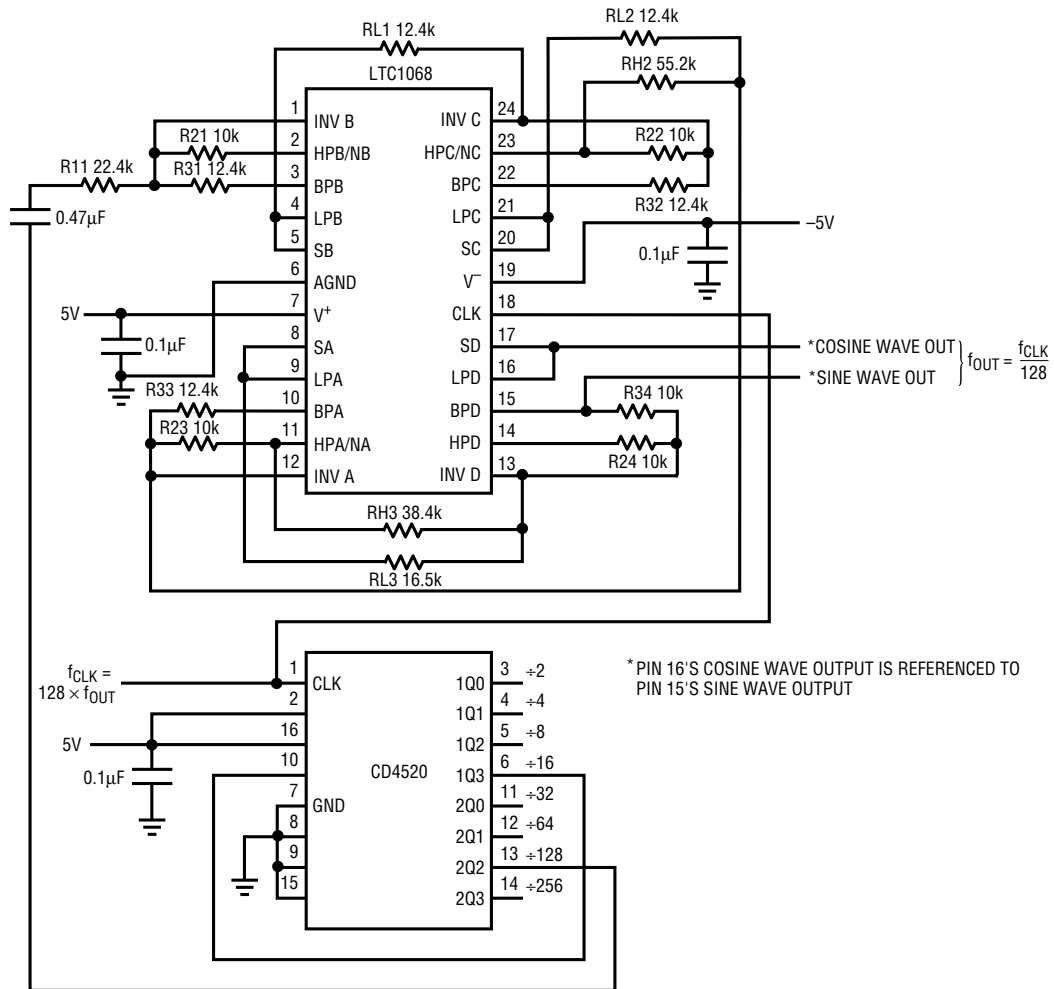
Figure 190. Square-Wave-to-Quadrature Oscillator Converter

Miscelleaneous

BIASED DETECTOR YIELDS HIGH SENSITIVITY WITH ULTRALOW POWER CONSUMPTION
by Mitchell Lee

RF ID tags, circuits that detect a "wake-up" call and return a burst of data, must operate on very low quiescent current for weeks or months, yet have enough battery power in reserve to answer an incoming call. For smallest size, most operate in the ultrahigh frequency range, where the design of a micropower receiver circuit is problematic. Familiar techniques, such as direct conversion, super regeneration or superheterodyne, consume far too much supply current for long battery life. A better method involves a technique borrowed from simple field-strength meters: a tuned circuit and a diode detector.

Figure 191 shows the complete circuit, which was tested at 470MHz. It contains a couple of improvements over the standard L/C-with-whip field-strength meter. Tuned circuits aren't easily constructed or controlled at UHF, so a transmission line is used to match the detector diode (1N5711) to a 6" whip antenna. The 0.22-wavelength section presents an efficient, low impedance match to the base of the quarter-wave whip, but transforms the received energy to a relatively high voltage at the diode for good sensitivity.

Biasing the detector diode improves the sensitivity by an additional 10dB. The forward threshold is reduced to essentially zero, so a very small voltage can generate a meaningful output change. The detector diode's bias point is monitored by an LTC1440 ultralow power comparator, and by a second diode, which serves as a reference.

When a signal at the resonant frequency of the antenna is received, Schottky diode D1 rectifies the incoming carrier and creates a negative-going DC bias shift at the noninverting input of the comparator. Note that the bias shift is sensed at the base of the antenna where the impedance is low, rather than at the Schottky where the impedance is high. This introduces less disturbance into the tuned antenna and transmission-line system. The falling edge of the comparator triggers a one-shot, which temporarily enables answer-back and other pulsed functions.

Total current consumption is approximately 5μA. Monolithic one-shots draw significant load current, but the venerable '4047 is about the best in this respect. Alternatively, a discrete one-shot constructed from a quad NAND gate draws negligible power.

Sensitivity is excellent. The finished circuit can detect 200mW radiated from a reference dipole at 100'. Range, of course, depends on operating frequency, antenna orientation and surrounding obstacles; in the clear, a more reasonable distance, such as 10', can be covered at 470MHz with only a few milliwatts.

All selectivity is provided by the antenna itself. Add a quarter-wave stub (shorted with a capacitor) to the base of the antenna for better selectivity and improved rejection of low frequency signals.
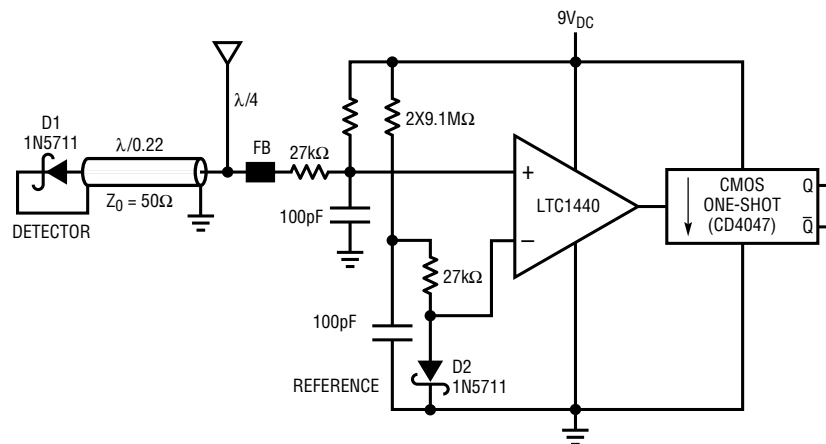

Figure 191. Micropower Field Detector for Use at 470MHz

ZERO-BIAS DETECTOR YIELDS HIGH SENSITIVITY WITH NANOPOWER CONSUMPTION
by Mitchell Lee

RF ID tags, circuits that detect a "wake-up" call and return a burst of data, must operate on very low quiescent current for months or years, yet have enough battery power in reserve to answer an incoming call. For smallest size, most operate in the ultrahigh frequency range, where the design of a micropower receiver circuit is problematic. Familiar techniques, such as direct conversion, super regeneration or superhetrodyne, consume far too much supply current for long battery life. A better method involves a technique borrowed from simple field-strength meters: a tuned circuit and a diode detector.

Figure 192 shows the complete circuit, which was tested for proof-of-concept at 445MHz. This circuit contains a couple of improvements over the standard L/C-with-whip field-strength meter. Tuned circuits aren't easily constructed or controlled at UHF, so a transmission line is used to match the detector diode (1N5712) to a quarter-wave whip antenna. The 0.23λ transmission-line section transforms the 1pF (350Ω) diode junction capacitance to a virtual short at the base of the antenna. At the same time, it converts the received antenna current to a voltage loop at the diode, giving excellent sensitivity.

Biasing the detector diode can improve sensitivity,[1] but only when the diode is loaded by an external DC resistance. Careful curve-tracer examination of the 1N5712 at the origin reveals that it follows the ideal diode equation, with scales of millivolts and nanoamperes. To use a zero-bias diode at the origin, the external comparator circuitry must not load the rectified output.

The LTC1540 nanopower comparator and reference is a good choice for this application because it not only presents no load to the diode, but also draws only 300nA from the battery. This represents a 10-times improvement in battery life over biased detector schemes.[2] The input is CMOS, and input bias current consists of leakage in a small ESD-protection cell connected between the input and ground. The input leakage measures in the picoampere range, whereas the 1N5712 leaks hundreds of picoamperes. Any rectified output from the diode is loaded by the diode itself, not by the LTC1540, and the sensitivity can match that of a loaded, biased detector.

The rectified output is monitored by the LTC1540 comparator. The LTC1540's internal reference is used to set up a threshold of about 18mV at the inverting input. A rising edge at the comparator output triggers a one-shot, which temporarily enables answer-back and any other pulsed functions.

Total supply current is 400nA, consuming just 7mAH battery life over a period of five years. Monolithic one-shots draw significant load current, but the '4047 is about the best in this respect. A one-shot constructed from discrete NAND gates draws negligible power.
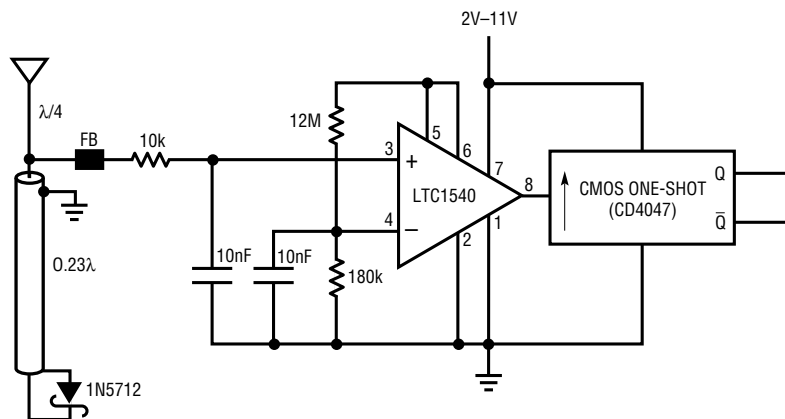

Figure 192. Nanopower Field Detector

Sensitivity is excellent, and the circuit can detect about 200mW from a reference dipole at 100 feet. Range, of course, depends on operating frequency, antenna orientation and surrounding obstacles. Sensitivity is independent of supply voltage; this receiver will work just as well with a 9V battery as with a single lithium cell.

The length of the transmission line does not scale with frequency. Owing to a decrease in diode reactance, the electrical length will shorten as frequency increases. Adjust the line length for minimum feed-point impedance at the operating frequency. If an impedance analyzer is used to measure the line, a 1pF capacitor can be substituted for the diode to avoid large signal effects in the diode itself. Consult the manufacturer's data sheet for accurate characterization of diode impedance at the frequency of interest.

Notes:

1. Eccles, W.H. Wireless Telegraphy and Telephony, Second Edition. Ben Brothers Limited, London, 1918, page 272.

2. Lee, Mitchell. "Biased Detector Yields High Sensitivity with Ultralow Power Consumption." Page 110 of this application note.

TRANSPARENT CLASS-D AMPLIFIERS FEATURING THE LT1336
by Dale Eagar

Introduction

Efficiency in the field of power conversion is like transparency in the field of light transmission. It is no wonder, then, that Class-D amplifiers are often called transparent, since they have no significant power losses. In contrast to class-D amplifiers' nearly lossless switching, class-A through class-C amplifiers are throttling devices that waste significant energy. Amplifiers of the "lower classes" (A–C) are modeled as rheostats (variable resistors), whereas class-D amplifiers are modeled as variacs (variable transformers). The ideal resistor dissipates power, whereas the ideal transformer does not. Like transformers (variacs), many class-D amplifiers can transfer energy in both directions—input to output and output to input.

Class-D amplifiers also have a way of ignoring reactive loads that can be uncanny. A class-D amplifier operating with an AC output will draw very little additional input power when a sizable capacitive or inductive load is placed at its output. This is because the reactive load has AC voltage across it and AC current flowing through it, but the phase angle of the voltage and current is such that no real power is dissipated. The class-D amplifier ends up shuttling power back and forth between its input and its output, doing both with minimal loss. An ideal class-D amplifier can be thought of as having no place to dissipate power, since all of its components are lossless; that is, it contains no resistors.

The Electric Heater—a Simple Class-D Amplifier

Class-D amplifiers can be simple or complex, depending on what is required by the application. A simple class-D amplifier is the thermostatic switch in an electric heater. The thermostat controls the heater by turning it on or off. The switch is essentially lossless, dissipating practically no power. This class-D amplifier is remarkably efficient, since even the energy lost in the switch, power cord and house wiring contributes to the desired result. The duty factor, and hence the average amount of power delivered to the heater, can assume an infinite number of values. This is true even though a constant amount of heat is delivered when the heater is on.

Quadrants of Energy Transfer

Class-D amplifiers have a property that requires new terminology, a property that generally isn't considered in lower-class amplifiers. This property, quadrants of energy transfer, describes the output characteristics of the class-D amplifier. The output characteristics are plotted on a imaginary X-Y plot (I've yet to see someone actually do one on paper), one axis representing output voltage and the other axis representing output current, with the intersection of the axes representing zero volts and zero amps. A simple switcher that can only provide a positive output current into a positive output voltage can be described as a 1-quadrant device. This 1-quadrant device could be a computer power supply, a battery charger or any supply that delivers a positive voltage into a device that can only consume power.

The 2-quadrant converter can be one of two different things: 1) A positive output voltage that can both source and sink current, or 2) A positive current that can comply both positive and negative output voltage. Finally, the 4-quadrant converter can both source and sink current into both positive and negitive output voltages.

1-Quadrant Class-D Converter

To illustrate the 1-quadrant class-D amplifier, we will focus on the boost mode converter detailed in Figure 193 This circuit removes power from the source (12V automotive battery) and delivers it to the load (some as-yet-unknown 55V device) This circuit is classified as "1 quadrant" because it can only regulate output voltage in one polarity (positive) and it can output current in only one polarity (positive).

Introducing the LT1336 Half-bridge Driver

Taking a side step from our main discussion, we will introduce a component, the half-bridge power amplifier. Figure 194 details the LT1336 driving power MOSFETs and shows the symbolic representation of this subcircuit that will appear in subsequent figures. Table 1 shows the logical states of this half-bridge power driver.

4-Quadrant Class-D Amplifier

Class-D amplifiers are commonly used in subwoofer drivers. This is because subwoofers require a great deal of power. A class AB amplifier driving a subwoofer will put about half of its input power into its heat sink. Driving the same subwoofer at the same volume with the same music, a class-D amplifier will put about five percent of its input
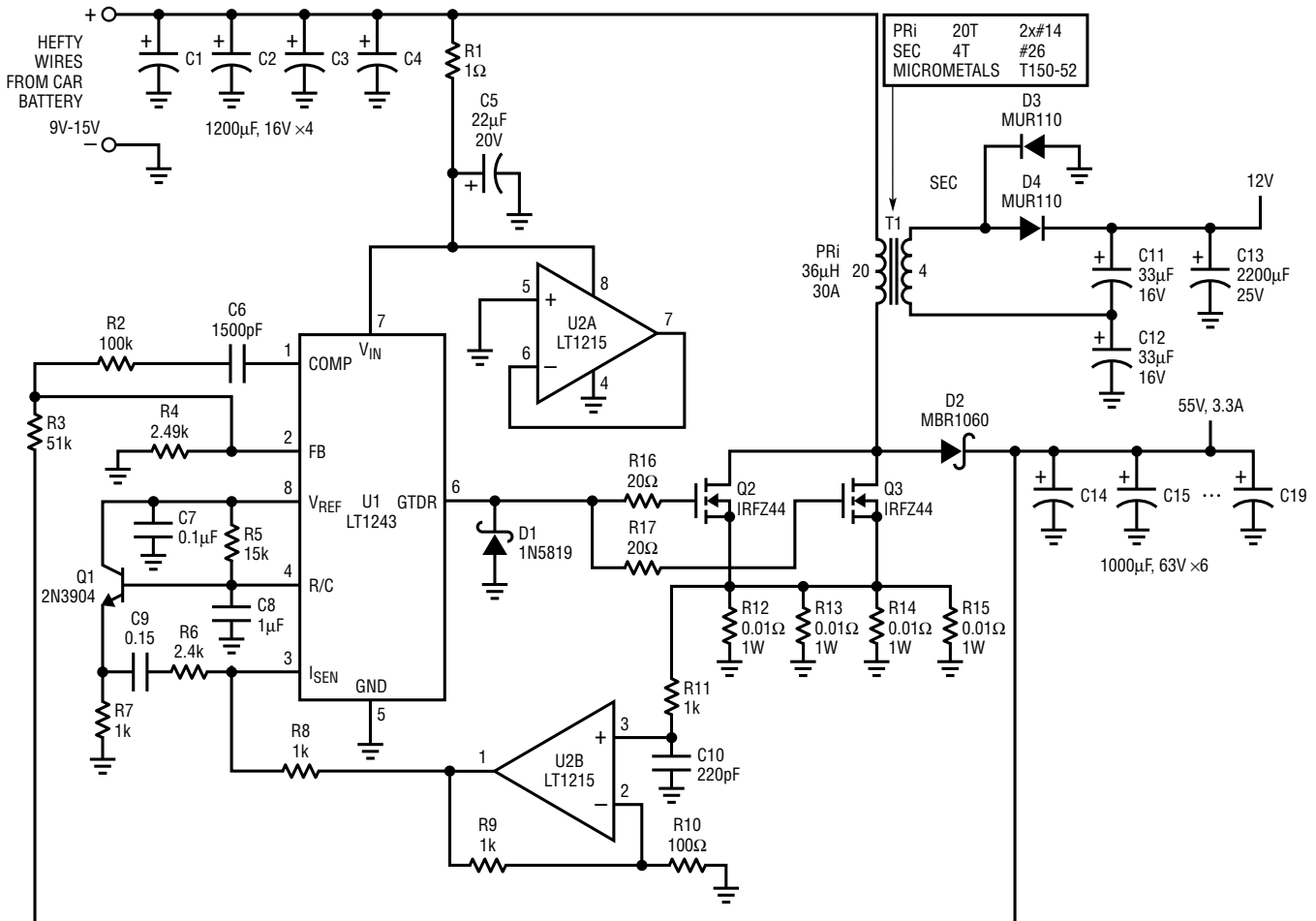
Figure 193. 200W, 12V to 55V Front End for Automotive Applications

power into the heat sink. The difference is ten to one on the heatsink size and two to one on the input power supply. Figure 195 is the 200W class-D subwoofer driver. This circuit uses the 200W front end developed in Figure 193 as its power source. The circuit in Figure 195 performs as follows: U1a, R1–R4 and C7 implement a 75kHz pseudosawtooth oscillator. U1d is the input amplifier/filter, with a gain of 6.1 and 200Hz Butterworth lowpass response. U1b and U1c are comparators that compare the sawtooth and the amplified/filtered input signal to form two complimentary, pulse-width modulated square waves. X1 and X2 are two half-bridge power drivers and M1 is the subwoofer driver.

One of the properties of Class-D, 4-quadrant amplification is the ability to transfer power both to and from the load. In our subwoofer driver, this happens when the driver reaches the end of any given excursion and the combination of the driver spring and the acoustic spring drive the cone back to center. During this time, energy is transferred from the driver back to the input of the class-D amplifier stage. In the case shown in Figure 195, the

Table 7. Half-Bridge Power Driver Truth Table

In Top	In Bottom	Output
L	L	Floating
L	H	Ground
H	L	55V
H	H	Floating

energy ends up on the 55V bus, where the bus voltage climbs during these periods of "negative energy delivered to the load." Fortunately, C14–C19 of Figure 193 can store this energy; otherwise the 55V bus would subject to excessive voltage until someplace was found for the energy to go.

Class-D for Motor Drives

Substituting a motor and an inductor for the subwoofer in Figure 195 and simplifying the control, we arrive at the circuit shown in Figure 196. Connecting this circuit to the front end shown in Figure 193 and then getting the motor up to speed is no problem, but when one wants to slow the
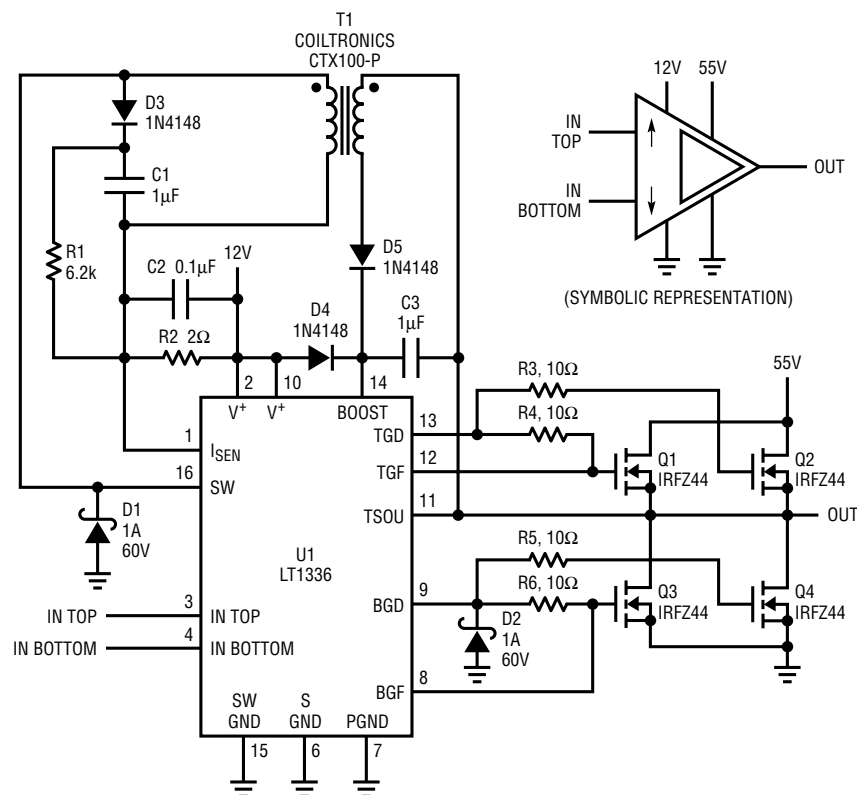
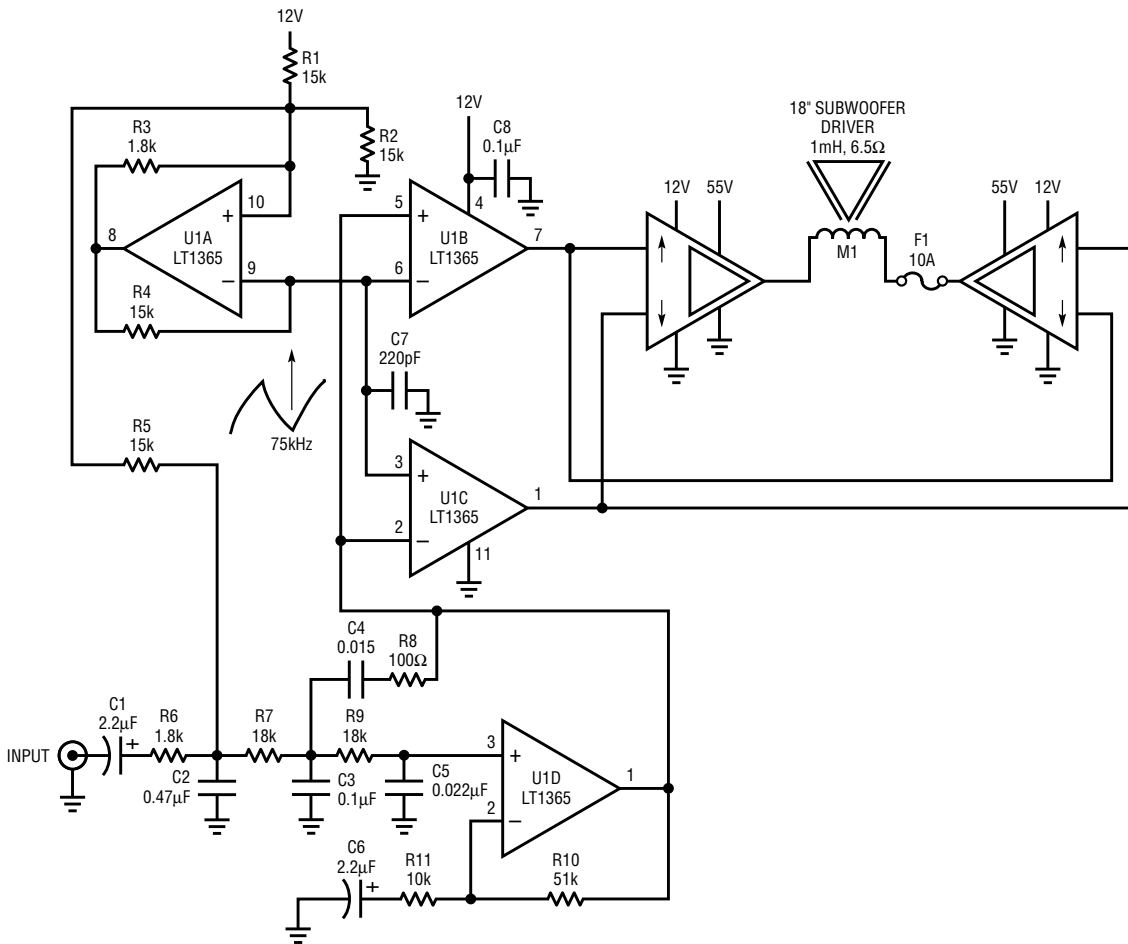**Figure 194. Half-Bridge Driver Subcircuit and Symbolic Representation**
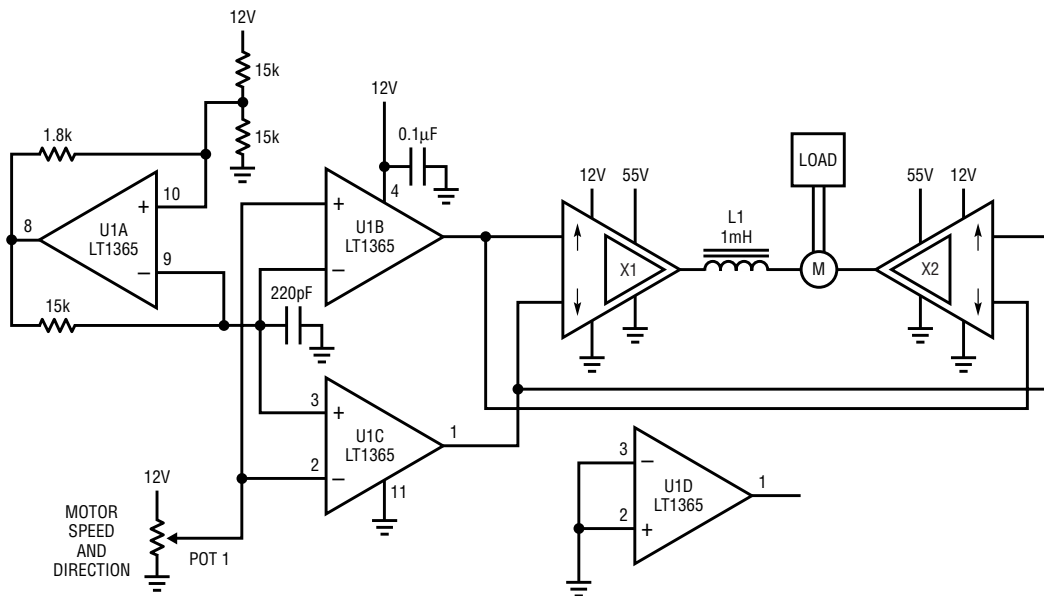
Figure 195. 200W-Powered Subwoofer

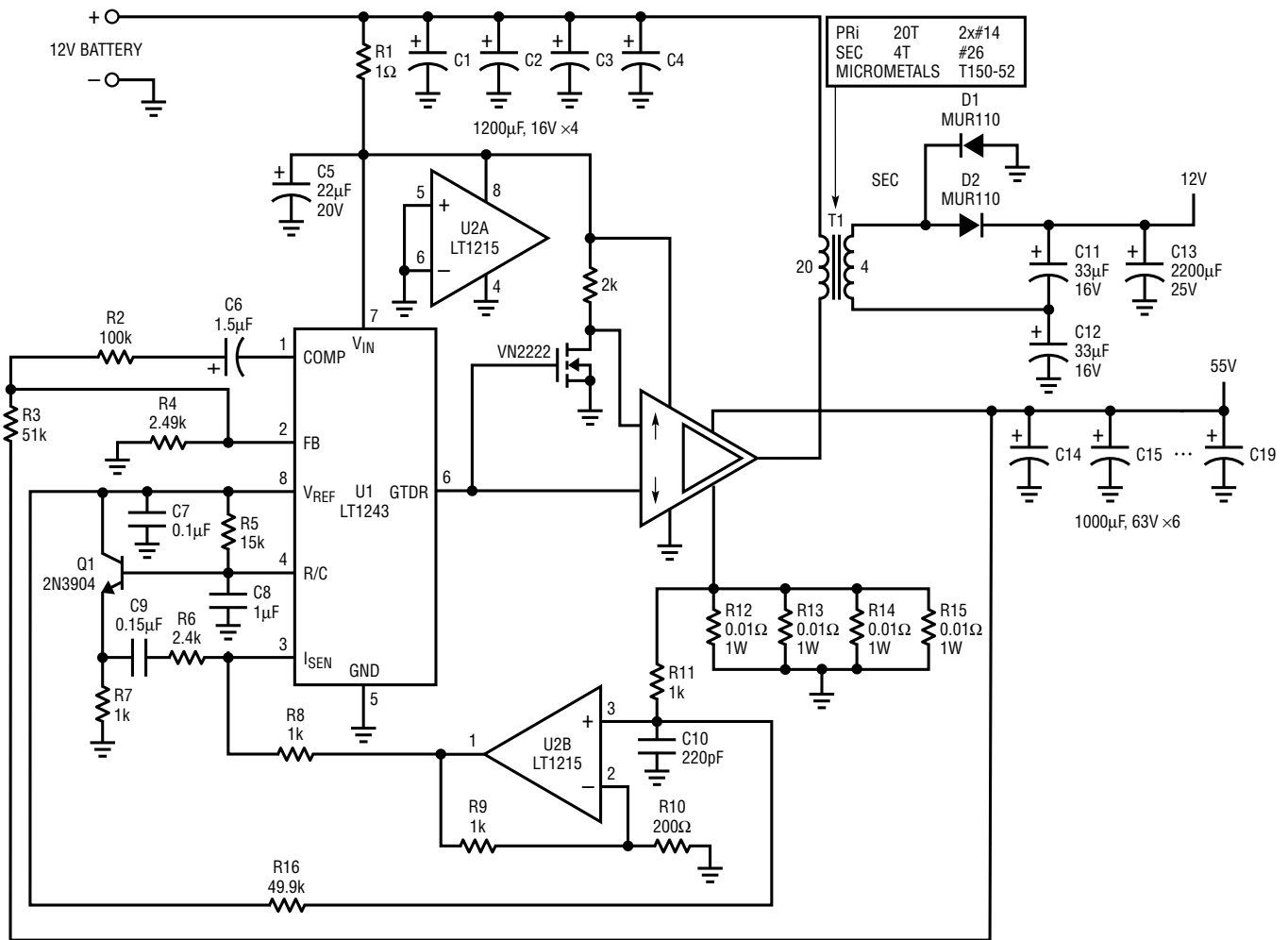**Figure 196. Class-D Motor Drive**

Figure 197. 200W, 2-Quadrant Front End for Automotive Applications

motor down by turning pot 1 back toward its center, disaster strikes. Rotational energy stored in the inertia of the motor is converted back into electrical energy by the motor and is presented to the output of the class-D amplifier. L1, X1 and X2 do their job by transferring the energy back into the 55V bus. The energy goes into C14–C19 of Figure 193, charging them to some voltage significantly above 55V, and something breaks. The problem here is that the circuit in Figure 193 is only a 1-quadrant class-D amplifier.

Managing the Negative Energy Flow

Sound like a course in management? The negative energy transferred through the class-D amplifier needs a home. One simple home is a 62V power Zener diode strapped across the 55V bus and bolted to a massive heat sink. One could easily imagine the heat sink as the brake shoes heating up as the electric vehicle winds down the mountain road. Another place to put the energy is back into the 12V battery. This will require upgrading the 12V to 55V front-end power converter from 1 quadrant to 2 quadrants.

The 2-Quadrant Class-D Converter

Converting Figure 193 to two quadrants involves replacing D2 with a switch and activating the switch out of phase with the switch formed by Q2 and Q3. The half-bridge power driver shown in Figure 195 is just such a switch. Refer to Figure 197. The I_{SENSE} signal (U1, pin 3) needs to be offset to accommodate negative current (add R16, Figure 197) The I_{SENSE} signal needs to be scaled for twice the range

(–30A to 30A rather than 0A to 30A); this is done by changing R10.

Now we are happily winding down the mountain road, watching the scenery unfold before us. We are happy in knowing that we are recycling the energy released from the descent by charging our batteries, while watching the mountain bikers burn their descent energy off in brake linings. Once again technology wins over sweat and brawn.

A Trip Over the Great Divide

Climbing the great divide in an electric vehicle requires some planning. Stops to recharge are necessary. Once on top, the whole scheme changes: descending the hill, charging our battery, all goes well until the battery is fully charged; then we have to stop. Further descent would overcharge our battery, boiling out the electrolyte. Not only would this ruin our battery, in the end we would have no place to put the energy and our class-D amplifier would find some way to fail. We need to stop and drain off some charge, trade batteries with someone climbing the other side or put a power Zener on our battery. Figure 198 details the active Zener circuit. Using the reference in U1 of Figure 197 and the unused half of U2 we are able to make a hysteretic clamp that puts all of the heat into a resistor, R5. This circuit will save the battery from destruction and drop our level of smugness back to that of the mountain bikers.

Conclusion

Class-D has been around for a long time: the venerable electric heater with its bang-bang controller is a remarkably efficient and reliable class-D amplifier. Class-D drives have been used for decades in golf carts, fork lifts, cranes and industry. The advent of the half-bridge driver greatly simplifies the Class-D Amplifier. Here at Linear Technology we have a family of half/full bridge MOSFET drivers. For further information, contact us at the factory or refer to the LT1158, LT1160, LT1162 or LT1336 data sheets.
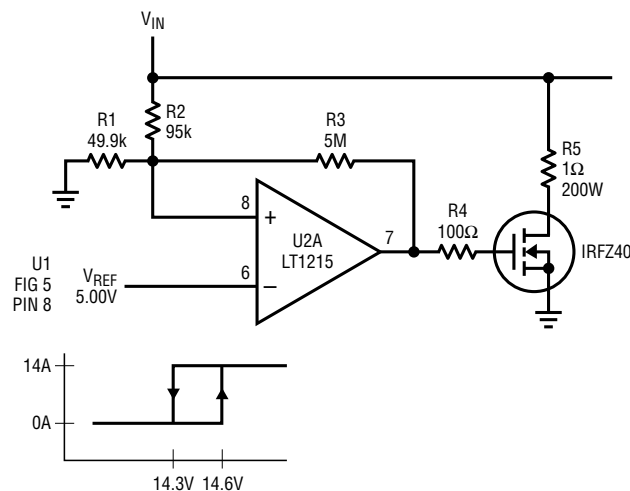
Figure 198. Wolf Creek Pass Adapter

SINGLE-SUPPLY RANDOM CODE GENERATOR
by Richard Markell

Presented here is a truly random code generator that operates from a single supply. The circuit allows operation from a single 5V supply with a minimum of adjustments.

The circuit produces random ones and zeroes by comparing a stream of random noise generated in a Zener diode to a reference voltage level. If the threshold is correctly set and the time period is long enough, the noise will consist of a random but equal number of samples above and below threshold.

That Fuzz is Noise

The circuit shown in Figure 199 is the random noise generator. Optimum noise performance is obtained from a 1N753A Zener diode, which has a 6.2 volt Zener "knee." The diode is used to generate random noise. We have found that optimum noise output for this diode occurs at the "knee" of the I-V curve, where the Zener just starts to limit voltage to 6.2 volts.

Operating a 6.2V Zener from a 5V supply required some thought. Obviously, some type of voltage boosting scheme was needed to provide the diode with the 8V or more that it requires in this circuit. U1, an LTC1340 low noise, voltage-boosted varactor driver, provides 9.2V at 20µA from an input of 5V. This Zener current is the optimal for noise output from the diode (at 20µA the output is about 20mV$_{P-P}$).

The 1M and 249k resistors bias the input to operational amplifier U2 to 1.25V to match the input common mode range of comparator U3. The 1µF capacitor provides an AC path for the noise. Note: be careful where you place any additional capacitors in this part of the circuit or the noise may be unintentionally rolled off. This is one circuit where noise is desirable.

U2 is an LT1215 23MHz, 50V/µs, dual operational amplifier that can operate from a single supply. It is used as a wideband, gain-of-eleven amplifier to amplify the noise from the Zener diode; the second op amp in U2 is unused. U3, an LT1116 high speed, ground-sensing comparator,

receives the noise at its positive input. A threshold is set at the negative comparator input and the output is adjusted via the 2k potentiometer for an equal number of ones and zeroes. The 5k resistor and the 10µF capacitor provide limited hysteresis so that the adjustment of the potentiometer is not as critical. Latch U4, a 74HC373, ensures that the output remains latched throughout one clock period. The circuit's output is taken from U4's Q0 output.

Some Thoughts on Automatic Threshold Adjustment

Several circuit designers have asked about threshold adjustment without manual knobs or potentiometers. One way to implement this would be to have the microprocessor count the number of ones and zeroes over a given time period and adjust the threshold (perhaps via a digital pot) to produce the required density of ones.

A more "analog" method of adjusting threshold might be to implement an integrator with reset. This circuit integrates the number of ones and zeroes over time to produce a zero result for an adjustment that produces equal numbers of ones and zeroes. Again, a digital pot could be used to adjust threshold, with the threshold being decreased for the case of "not enough ones" and increased for the case of "too many ones."

After many more conversations with the "cyber illuminati," the circuit in Figure 200 was devised. This circuit can be used to replace the pot shown in the dashed box in Figure 199. In operation, an LT1004-2.5 is used as a reference at the front end of a precision voltage divider string. A series of voltages is generated along the divider string and a jumper is used to connect this voltage to a buffer and then to the negative input of the LT1116 comparator. As was the case with the 2k pot, the voltage at pin 2 (the negative input of the comparator) sets the threshold for the comparator. The selection of voltage taps on the resistor string is arbitrary; they were selected to allow a good adjustment range (defined as allowing jumper adjustment to 50% ones and 50% zeros) for a sample of ten 1N753A Zener diodes used to produce noise. The jumper could (and probably should) be replaced with analog switches controlled by a microprocessor in medium- to high-volume applications.
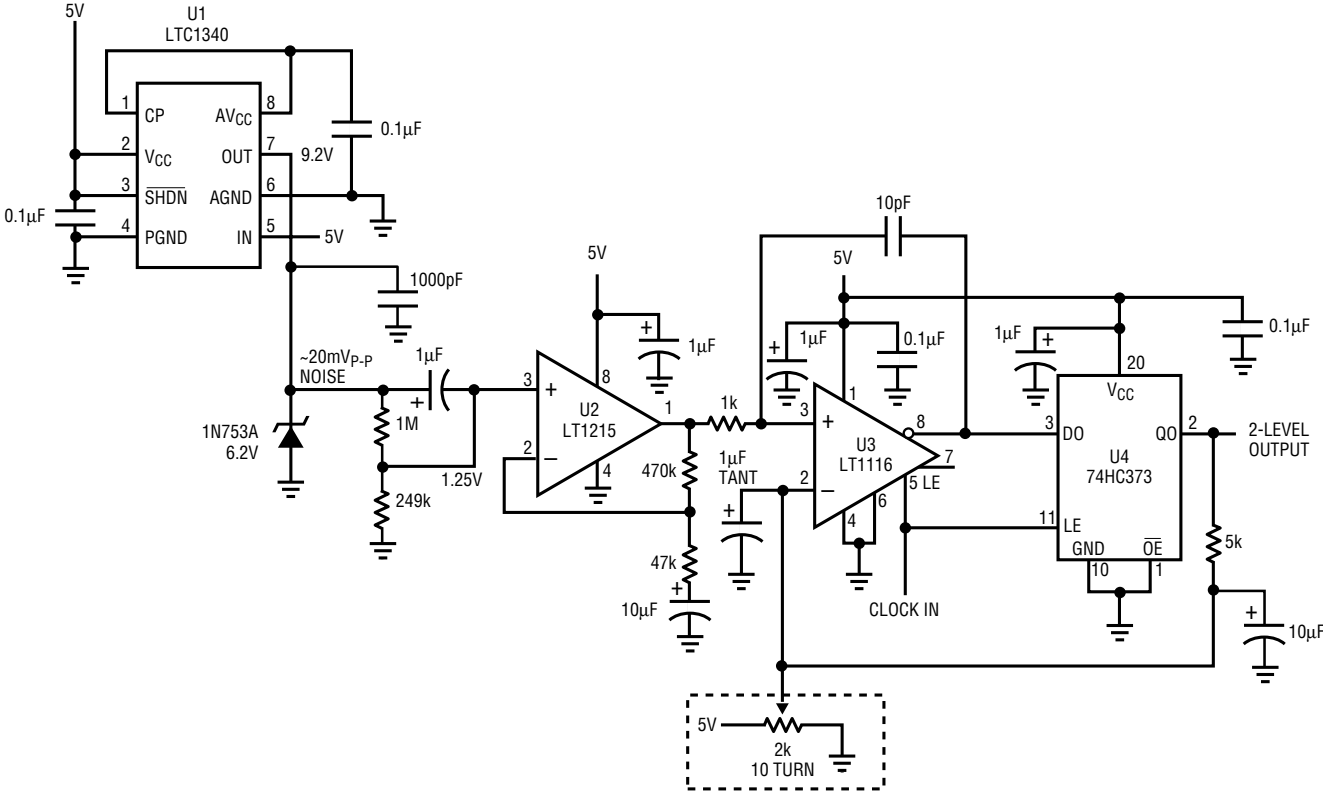
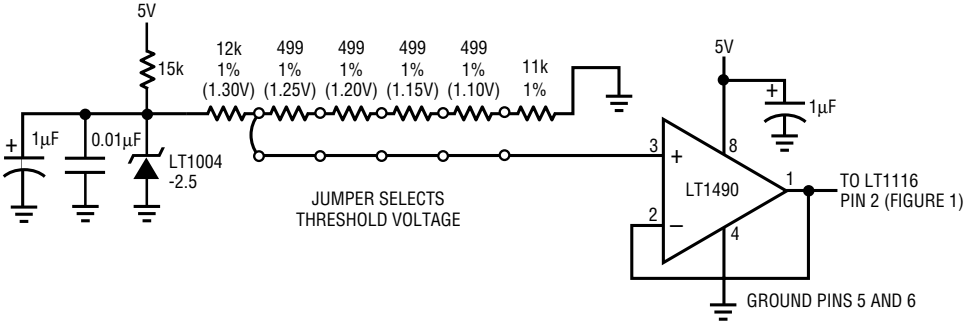**Figure 199. Single-Supply Random Code Generator**

Figure 200. Jumper Selects Threshold for Figure 199's Circuit

APPENDIX A: COMPONENT VENDOR CONTACTS

The tables on this and the following pages list contact information for vendors of non-LTC parts used in the application circuits in this publication. In some cases, components from other vendors may also be suitable. For information on component selection, consult the text of the respective articles and the appropriate LTC data sheets.

Capacitors			
Vendor	Product	Phone	URL
AVX	Chip Capacitors	(843) 946-0362	www.avxcorp.com/products/capacitors
AVX	Tantalum Capacitors	(207) 282-5111	
Electronic Concepts	400V Film Capacitors	(908) 542-7880	www.eci-capacitors.com
Kemet	Tantalum Capacitors	(408) 986-0424	www.kemet.com
Marcon	High C/V Capacitors	(847) 696-2000	www.chemi-con.com/main/company/marcon.html
Murata Electronics	Capacitors	(770) 436-1300	www.iijnet.or.jp/murata/products/english
Nichicon	Electrolytic Capacitors	(847) 843-7500	www.nichicon-us.com
Panasonic	Poly Capacitors	(714) 373-7334	www.panasonic.com/industrial_oem/electronic_components/electronic_components_capacitors_home.htm
Sanyo	Oscon Capacitors	(619) 661-6835	www.sanyovideo.com
Sprague	Capacitors	(207) 324-4140	www.comsprague.com
Taiyo Yuden	Chip Capacitors	(408) 573-4150	www.t-yuden.com
Tokin	Capacitors	(408) 432-8020	www.tokin.com
United Chemicon	Electrolytic Capacitors	(847) 696-2000	www.chemi-con.com/main
Vitramon	Ceramic Chip Capacitors	(203) 268-6261	www.vishay.com
Wima	Paper/Film Capacitors	(914) 347-2474	www.wimausa.com

Diodes			
Vendor	Product	Phone Number	URL
Agilent (formerly Hewlett Packard)	IR LEDs	(800) 235-0312	www.semiconductor.agilent.com/ir
Central Semiconductor	Small Signal Discretes	(516) 435-1110	www.centralsemi.com
Chicago Miniature Lamp	LEDs	(201) 489-8989	www.sli-lighting.com/cml
Data Display Products	LEDs	(800) 421-6815	www.ddp-leds.com
Fuji	Schottky Diodes	(201) 712-0555	www.fujielectric/co/jp/eng/index-e.html
General Semiconductor	Diodes	(516) 847-3000	www.gensemi.com
Motorola*	Discretes	(800) 441-2447	www.mot-sps.com/products/index.html
ON Semiconductor*	Discretes	(602) 244-6600	www.onsemi.com/home
Panasonic	LEDs	(201) 348-5217	www.panasonic.com/industrial_oem/semiconductors/semiconductor_home.htm
Temic	IR Photo Diodes	(408) 970-5700	www.temic.com
Vishay	Zener/Small Signal Diodes	(408) 241-4588	www.vishay.com
Zetex	Small Signal Discretes	(516) 543-7100	www.zetex.com

*Discretes formerly manufactured by Motorola are now manufactured by ON Semiconductor. Part numbers have not been changed as of January 2000

LINEAR
TECHNOLOGY

Inductors and Transformers

Vendor	Product	Phone Number	URL
API Delevan	Inductors	(716) 652-3600	www.delevan.com
BH Electronics	Inductors	(612) 894-9590	www.bhelectronics.com
BI Technologies	Transformers	(714) 447-2656	www.bitechnologies.com
Coilcraft	Inductors	(847) 639-6400	www.coilcraft.com
Cooper	Inductors/ Transformers	(561) 752-5000	www.coiltronics.com
Dale	Inductors/ Transformers	(605) 665-1627	www.vishay.com/fp/fp.html#inductors
Gowanda	Inductors	(716) 532-2234	www.gowanda.com
Midcom	Inductors/ Transformers	(605) 886-4385/ (800) 643-2661	www.midcom-inc.com
Murata Electronics	Inductors	(814) 237-1431	www.murata.com
Panasonic	Inductors/Transformers	(714) 373-7334	www.panasonic.com/industrial_oem/electronic_components/ electronic_components_inductors_coils_and_transformers.htm
Philips	Inductors	(914) 246-2811	www.acm.components.philips.com
Philips	Planar Inductors	(914) 247-2036	www.acm.components.philips.com
Pulse	Inductors	(619) 674-8100	www.pulseeng.com
Sumida	Inductors	(847) 956-0667	www.japanlink.com/sumida
Tokin	Inductors	(408) 432-8020	www.tokin.com

Logic

Vendor	Product	Phone Number	URL
Fairchild	Logic	(207) 775-4502	www.fairchildsemi.com
Intersil (formerly Harris)	Logic	(800) 442-7747	www.intersil.com
*Motorola	Logic	(800) 441-2447	www.mot-sps.com/products/index.html
*ON Semiconductor	Logic	(602) 244-6600	www.onsemi.com/home
Toshiba	Logic Single Gate Logic	(949) 455-2000/ (714) 455-2000	www.toshiba.com/taec

*Logic Devices formerly manufactured by by Motorola are now manufactured by ON Semiconductor; there have been no changes in part numbers as of January 2000

Resistors

Vendor	Product	Phone Number	URL
Allen Bradley	Carbon Resistors	(800) 592-4888	www.ab.com
AVX	Chip Resistors	(843) 946-0524	www.avxcorp.com/products/resistors/chiprstr.htm
BI Technologies	Resistors/Resistor Networks	(714) 447-2345	www.bitechnologies.com
Bourns	Potentiometers, SIPs	(801) 750-7253	www.bourns.com
Dale	Sense Resistors	(605) 665-9301	www.vishayfoil.com or www.vishay.com
IRC	Sense Resistors	(361) 992-7900	www.irctt.com
RG Allen	Metal Oxide Resistors	(818) 765-8300	www.rgaco.com
TAD	Chip Resistors	(800) 508-1521	www.tadcom.com
Taiyo Yuden	Chip Resistors	(408) 573-4150	www.t-yuden.com
Thin Film Technology	Thin Film Chip Resistors	(507) 625-8445	www.thin-film.com
Tocos	SMD Potentiometers	(847) 884-6664	www.tocos.com

Transistors			
Vendor	**Product**	**Phone Number**	**URL**
Central Semiconductor	Small Signal Discretes	(516) 435-1110	www.centralsemi.com
Fairchild	MOSFETs	(408) 822-2126	www.fairchildsemi.com
IR	MOSFETs	(310) 322-3331	www.irf.com
Motorola*	Discretes	(800) 441-2447	www.mot-sps.com/products/index.html
ON Semiconductor*	Discretes	(602) 244-6600	www.onsemi.com/home
Philips	Discretes	(401) 767-4427	www-us.semiconductors.philips.com
Siliconix	MOSFETs	(800) 554-5565	www.siliconix.com
Zetex	Small Signal Discretes	(631) 543-7100	www.zetex.com
*Discretes formerly manufacured by Motorola are now manufactured by ON Semiconductor; There are no changes in part numbers as of January 2000.			

Miscellaneous			
Vendor	**Product**	**Phone Number**	**URL**
Aavid	Heat Sinks	(714) 556-2665	www.aavid.com
Epson	Crystals	(310) 787-6300	www.eea.epson.com
Infineon (formerly Siemens Semiconductor)	Optoelectronics	(108) 257-7910	www.infineon.com/us/opto/content.htm
Magnetics, Inc.	Toroid Cores, etc.	(800) 245-3984	www.mag-inc.com
MF Electronics	Crystal Oscillators	(914) 576-6570	www.mfelec.com
Murata Electronics	RF Devices	(770) 433-5789	www.murata.com
QT Optoelectronics	RF Switches	(408) 720-1440	www.qtopto.com
Raychem	Fuses	(800) 227-4856	www.raychem.com
RF Micro Devices	RF Semiconductors	(336) 664-1233	www.rfmd.com
RTI/Ketema	Surge Suppressors	(714) 630-0081	www.rtie.rti-corp.com
Schurter	Fuses and Holders	(707) 778-6311	www.schurterinc.com
Thermalloy	Heat Sinks	(972) 243-4321	www.thermalloy.com
Toko	RF Products	(847) 699-3430	www.tokoam.com

Linear Technology Corporation		
Product	**Phone Number**	**URL**
High Performance Analog ICs	(408) 432-1900	www.linear-tech.com

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