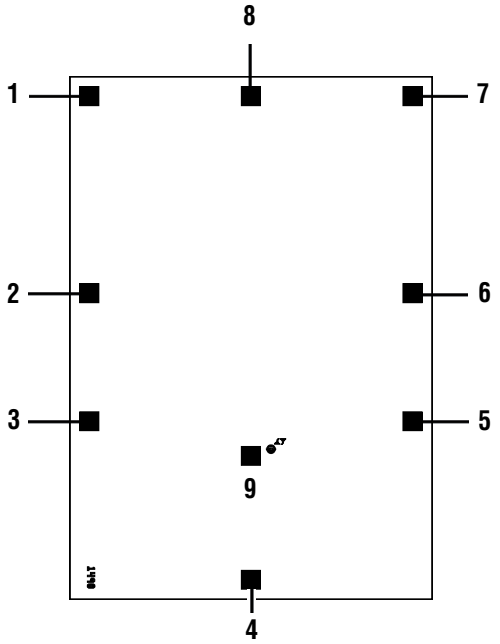
LT1498
10MHz, 6V/µs, Dual/Quad Rail-to-Rail Input and Output Precision C-Load Op Amps



117mils × 82mils,
12mils thick.
Connect Backside to V^+

PAD FUNCTION

1. OUTA
2. –INA
3. +INA
4. $V^–$
5. +INB
6. –INB
7. OUTB
8. V^+
9. V^+

117mils × 82mils,
12mils thick.
Connect Backside to V^+

LT1498 Die Pad Coordinates and Pad Opening Info Center of Die: 0,0 Coordinates

PAD NUMBER	PAD NAME	X-COORDINATE (µm)	Y-COORDINATE (µm)	X-COORDINATE (Mil)	Y-COORDINATE (Mil)	PAD OPENING (µm)	PAD FUNCTION
1	OUTA	–1339.50	–895.0	–52.74	–35.24	105x105	OutPut
2	–INA	–248.50	–895.00	–9.78	–35.24	105x105	Input
3	+INA	461.00	–895.00	18.15	–35.24	105x105	Input
4	$V^–$	1399.00	0.00	55.08	0.00	105x105	Supply
5	+INB	461.00	895.00	18.15	35.24	105x105	Input
6	–INB	–248.50	895.00	–9.78	35.24	105x105	Input
7	OUTB	–1339.5	895.00	–52.74	35.24	105x105	Output
8	V^+	–1339.5	0.00	–52.74	0.00	105x105	Supply
9	V^+	652.50	0.00	25.69	0.00	105x105	Supply

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to $V^–$) 36V
Input Current..... ±10mA
Output Short-Circuit Duration (Note 2) ..... Continuous

Junction Temperature ..... 150°C
Storage Temperature Range..... –65°C to 150°C

LT1498

DICE/DWF ELECTRICAL TEST LIMITS

T_A = 25°C, V_S = 5V, 0V; V_S = 3V, 0V; V_{CM} = V_{OUT} = half supply, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$ $V_{CM} = V^-$		475 475	µV µV
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^-$ to V^+		425	µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 3)	$V_{CM} = V^+, V^-$		750	µV
I_B	Input Bias Current	$V_{CM} = V^+$ $V_{CM} = V^-$	0 –650	650 0	nA nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^-$ to V^+		1300	nA
	Input Bias Current Match (Channel-to-Channel) (Note 3)	$V_{CM} = V^+$ $V_{CM} = V^-$	0 –100	100 0	nA nA
I_{OS}	Input Offset Current	$V_{CM} = V^+$ $V_{CM} = V^-$		65 65	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^-$ to V^+		130	nA
A_{VOL}	Large-Signal Voltage Gain	V_S = 5V, V_O = 75mV to 4.8V, R_L = 10k V_S = 3V, V_O = 75mV to 2.8V, R_L = 10k	600 500		V/mV V/mV
CMRR	Common Mode Rejection Ratio	V_S = 5V, $V_{CM} = V^-$ to V^+ V_S = 3V, $V_{CM} = V^-$ to V^+	81 76		dB dB
	CMRR Match (Channel-to-Channel) (Note 3)	V_S = 5V, $V_{CM} = V^-$ to V^+ V_S = 3V, $V_{CM} = V^-$ to V^+	75 70		dB dB
PSRR	Power Supply Rejection Ratio	V_S = 2.2V to 12V, $V_{CM} = V_O$ = 0.5V	88		dB
	PSRR Match (Channel-to-Channel) (Note 3)	V_S = 2.2V to 12V, $V_{CM} = V_O$ = 0.5V	82		dB
V_{OL}	Output Voltage Swing (Low) (Note 4)	No Load I_{SINK} = 0.5mA I_{SINK} = 2.5mA		30 70 200	mV mV mV
V_{OH}	Output Voltage Swing (High) (Note 4)	No Load I_{SOURCE} = 0.5mA I_{SOURCE} = 2.5mA		10 100 250	mV mV mV
I_{SC}	Short-Circuit Current	V_S = 5V V_S = 3V	±12.5 ±12.0		mA mA
I_S	Supply Current per Amplifier			2.2	mA
GBW	Gain-Bandwidth Product	V_S = 5V	6.8		MHz

DICE/DWF ELECTRICAL TEST LIMITS

T_A = 25°C, V_S = ±15V, V_{CM} = 0V, V_{OUT} = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{OS}	Input Offset Voltage	$V_{CM} = V^+$ $V_{CM} = V^-$		800 800	µV µV
ΔV_{OS}	Input Offset Voltage Shift	$V_{CM} = V^-$ to V^+		650	µV
	Input Offset Voltage Match (Channel-to-Channel) (Note 3)	$V_{CM} = V^+, V^-$		1400	µV
I_B	Input Bias Current	$V_{CM} = V^+$ $V_{CM} = V^-$	0 –715	715 0	nA nA
ΔI_B	Input Bias Current Shift	$V_{CM} = V^-$ to V^+		1430	nA
	Input Bias Current Match (Channel-to-Channel) (Note 3)	$V_{CM} = V^+$ $V_{CM} = V^-$	0 –120	120 0	nA nA
I_{OS}	Input Offset Current	$V_{CM} = V^+$ $V_{CM} = V^-$		70 70	nA nA
ΔI_{OS}	Input Offset Current Shift	$V_{CM} = V^-$ to V^+		140	nA
A_{VOL}	Large-Signal Voltage Gain	V_O = –14.5V to 14.5V, R_L = 10k V_O = –10V to 10V, R_L = 2k	1000 500		V/mV V/mV
	Channel Separation	V_O = –10V to 10V, R_L = 2k	116		dB
CMRR	Common Mode Rejection Ratio	$V_{CM} = V^-$ to V^+	93		dB
	CMRR Match (Channel-to-Channel) (Note 3)	$V_{CM} = V^-$ to V^+	87		dB
PSRR	Power Supply Rejection Ratio	V_S = ±5V to ±15V	89		dB
	PSRR Match (Channel-to-Channel) (Note 3)	V_S = ±5V to ±15V	83		dB
V_{OL}	Output Voltage Swing (Low) (Note 4)	No Load I_{SINK} = 0.5mA I_{SINK} = 10mA		30 80 500	mV mV mV
V_{OH}	Output Voltage Swing (High) (Note 4)	No Load I_{SOURCE} = 0.5mA I_{SOURCE} = 10mA		10 120 800	mV mV mV
I_{SC}	Short-Circuit Current		±15		mA
I_S	Supply Current per Amplifier			2.5	mA
SR	Slew Rate	A_V = –1, R_L = Open, V_O = ±10V Measure at V_O = ±5V	3.5		V/µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

Note 3: Matching parameters are the difference between the two amplifiers on the LT1498DICE.

Note 4: Output voltage swings are measured between the output and power supply rails.

LT1498

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

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