DEMO MANUAL DC136A
DESIGN-READY LINEAR REGULATOR

LT1575
UltraFast Linear Regulator for Microprocessor Power

DESCRIPTION

Demo circuit DC136A is an ultrahigh speed linear regulator designed to provide power for high performance microprocessors, such as the Intel Pentium® processor. These CPUs exhibit extreme dynamic loading of the core power supply and have very tight supply voltage tolerances. To date, the only way to maintain voltage tolerance in the face of large magnitude transient loads was to include several large value tantalum or aluminum electrolytic capacitors at the power supply output. In addition to the bulk capacitors, these systems require on the order of twenty-four 1µF ceramic capacitors. These parts are necessary to decouple the very high frequency components associated with the processor load. The LT®1575 changes these requirements dramatically.

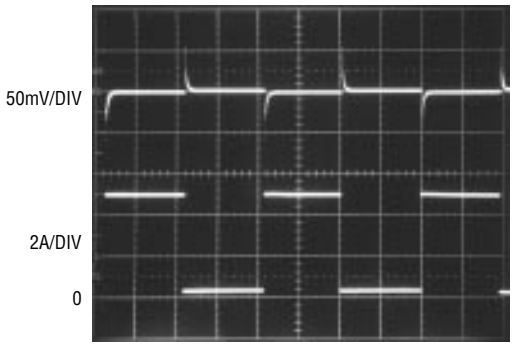
The LT1575 UltraFast™ linear regulator controller drives a power MOSFET pass transistor, forming a very wide bandwidth linear regulator. Loop crossover frequency is on the order of 1MHz. Total response time to a 5A load step is approximately 370ns. As a result of this extreme speed, the bulk capacitors may be entirely eliminated. The circuit provided here will power a 200MHz Pentium processor without a single bulk capacitor connected to the CPU core supply.

The demo board contains an LT1575 based linear regulator, a Pentium compatible socket and a load pulse generator circuit. The Pentium socket is included to permit the use of an Intel Power Validator to generate load steps that emulate a Pentium's load characteristics. If a Power Validator is not available, the board contains its own load step generator. Although not as flexible as a Power Validator, the step generator will produce loads that are adequate to evaluate the regulator's performance. There are a pair of connectors on the board to permit connection of a standard AT-type power supply. The regulator's output voltage may be jumper selected for 2.8V, 3.3V or 3.5V.

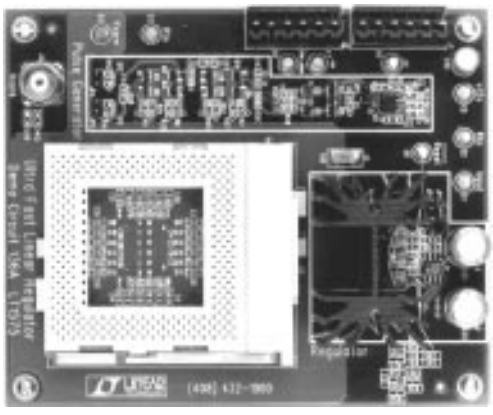
It is the intent of this demo board to show the layout techniques that should be employed to ensure proper operation of an LT1575 regulator circuit and microprocessor. **Gerber files for this circuit are available. Call LTC marketing.**

TYPICAL PERFORMANCE CHARACTERISTICS AND BOARD PHOTO

Transient Response

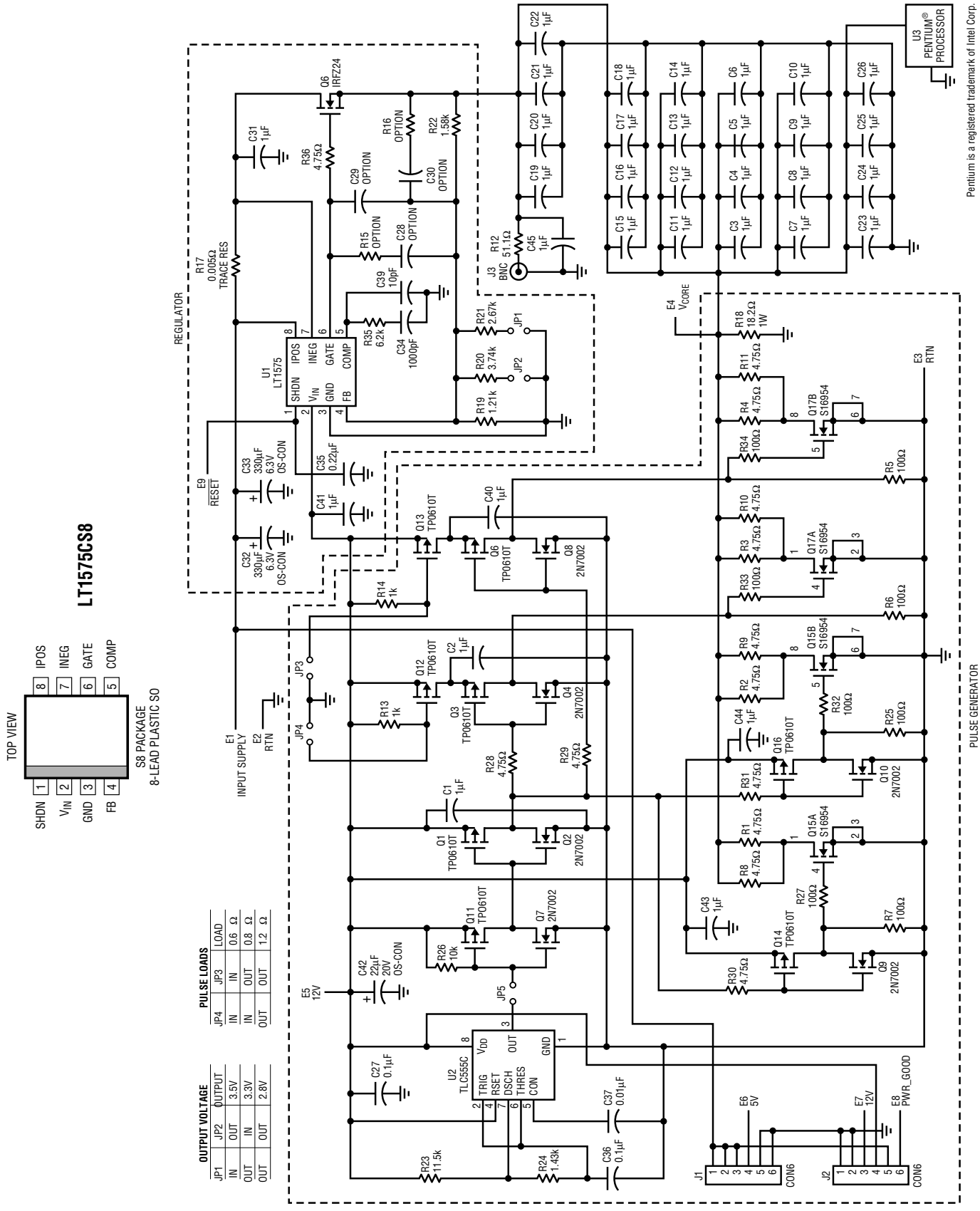


Completed Demo Board



DM 136A Bd Photo

PACKAGE A ND SCHEMATIC DIAGRAMS



PARTS LIST: Regulator and Decoupling Capacitors

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR	TELEPHONE
C3-C26, C31, C40, C41, C45	27	0805ZC105KAT3S	1µF 16V 20% X7R Chip Capacitor	AVX	(803) 946-0362
C28-C30	3	(Optional)	Chip Capacitor		
C32, C33	2	6SA330M, K	330µF 6.3V 20% OS-CON Electrolytic Capacitor	Sanyo	(619) 661-1055
C34	1	08055A102MAT3S	1000pF 50V 20% NPO Chip Capacitor	AVX	(803) 946-0362
C35	1	08053E223MAT3S	0.22µF 50V 20% Chip Capacitor	AVX	(803) 946-0362
C39	1	08051A100MAT3S	10pF 100V 20% NPO Chip Capacitor	AVX	(803) 946-0362
E9	1	2502-02	Turret Terminal	Mill-Max	(516) 922-6000
H1	1	533402/22	Heat Sink	Aavid	(714) 556-2665
J3	1	112404	Vertical BNC PC-Mount Connector	Connex	(805) 378-6464
JP1, JP2	2	3801S-2-G1	0.100 1 × 2 Header	Comm Con	(818) 301-4200
Q6	1	IRFZ24	Power MOSFET	IR	(310) 322-3331
R12	1	CR10-511J-T	51.1Ω 1/10W 1% Chip Resistor	TAD	(800) 508-1521
R15, R16	2	(Optional)	Chip Resistor		
R19	1	CR10-1211F-T	1.21k 1/10W 1% Chip Resistor	TAD	(800) 508-1521
R20	1	CR10-3741F-T	3.74k 1/10W 1% Chip Resistor	TAD	(800) 508-1521
R21	1	CR10-2671F-T	2.67k 1/10W 1% Chip Resistor	TAD	(800) 508-1521
R22	1	CR10-1581F-T	1.58k 1/10W 1% Chip Resistor	TAD	(800) 508-1521
R35	1	CR10-622J-T	6.2k 1/10W 1% Chip Resistor	TAD	(800) 508-1521
R36	1	CR10-4R75F-T	4.75Ω 1/0W 1% Chip Resistor	TAD	(800) 508-1521
U1	1	LT1575	UltraFast Linear Regulator Controller	LTC	(408) 432-1900
U3	1	214 320 3110	PGA 320 Pin ZIF Socket	Methode	(800) 323-6864
	2	CCIJ230-G	Shunt	Comm Con	(818) 301-4200
	1	115200	Kool-Klip	Aavid	(714) 556-2665
	4		4-40 1/4" Screw		
	4		4-40S 1/2" Nylon Stand-Off Screw		
	1		4-40 Nylon Washer		

OPERATION

The basic regulator circuit consists of U1, the LT1575, and power MOSFET Q6. The FET is operated in its saturated region (as opposed to its ohmic region), where it looks like a current source. The LT1575 adjusts its gate voltage as required to supply the desired load current and maintain output voltage regulation. Feedback is provided by R22, R19, R20 and R21. Installing JP1 or JP2 changes the feedback divider ratio to provide different output voltages. Loop compensation is provided by R35, C34 and C39. Trace resistor R17 is on internal layer 2 of the PCB and provides load current information to the LT1575. C35 determines the current limit time delay. In the event of a short circuit on the output, the current-limit circuitry will control the output current and start the timer. C35 is charged by a 15µA current source. When the voltage on C35 equals 1.21V, the LT1575 shuts down and latches the output off. To restore normal operation after removing the cause of the short, ground $\overline{\text{RESET}}$, E9, or recycle the input power to clear the latch.

The load pulser operation is straightforward. The TLC555C timer is configured as a low frequency oscillator with a duty factor of approximately 10%. The low duty factor is intended to minimize the dissipation in the load resistors. The output of the '555 can be disconnected from the rest of the circuit by removing JP5. The load is turned off in this

QUICK START GUIDE

Getting Demonstration Board DC136A up and running is really quite simple.

- Connect a standard off-line AT-type power supply to connector J1 and J2.
- If a Power Validator is available, it may be plugged into the processor socket and set up according to its manual's instructions. Nominal loads for this test circuit are 200mA minimum load and 5A maximum. Be sure to remove jumper JP5. This turns off the onboard load pulser.
- If a Power Validator is not available, use the onboard pulser. In this case, install JP5 to activate the pulser. There are three load levels possible: 50% load, 75% load and 100% load. Leave JP3 and JP4 off for 50%. Install JP3 only for 75% and install both JP3 and JP4 for 100% load.
- Connect a BNC cable from connector J3 to an oscilloscope input. Make sure the scope is set up for a high impedance input, not 50Ω. Set the scale for AC coupling, 50mV/div, and 200μs/div.
- Connect a DVM across E3 and E4 to measure the output voltage.
- Select the desired output voltage with jumper JP1 or JP2. With no jumpers installed, V_{CORE} equals 2.8V. Installing JP1 raises V_{CORE} to 3.5V. Installing JP2 gives an output of 3.3V.
- If using a Power Validator, apply power to it prior to powering up the AT supply. Next, turn on the AT supply. Verify that the output is as desired. The scope will show the transient response of the regulator.

OPERATION

case. Note that the 18Ω resistor, R18, is still in circuit to provide a small minimum load. When JP5 is installed, the output of the '555 is buffered by several inverting buffers, which consist of the N-channel/P-channel inverters. The pair of dual MOSFETs, Q15 and Q17, are driven to switch the array of 4.7Ω load resistors in and out of the circuit. The two sections of Q17 can be disabled by removing jumpers JP3 and JP4, allowing the load pulse amplitude to be altered. Removing the jumpers turns off Q12 and Q13, which, in turn, removes the drive to the load switch gates.

To apply a steady-state load to the regulator, remove JP5 and wire the desired load to E3 and E4. Note that it is not possible to power an actual processor board from this circuit because the lead inductance of the interconnect wiring is far above permissible levels and the transient response at the distant load would be unacceptable.

DESIGN CONSIDERATIONS

The basic circuit design is quite straightforward. Read Linear Technology Application Note AN69 for more detail.

The most important aspect of the power system design is the quality of the local decoupling of the microprocessor. The use of good quality X7R dielectric ceramic capacitors will produce good results if proper layout techniques are employed. These capacitors have extremely low ESR and ESL. To capitalize on these parameters, it is important not to introduce substantial parasitic impedance in the interconnect path. Keep connections to the capacitors extremely short. There should be two vias per end, per capacitor. They can be implemented as was done here on the demo board, where the capacitors are soldered to a floating power or ground island, which, in turn, is connected to the main internal power and ground layers by numerous vias.

Alternatively, the capacitors can have their own individual interconnects to the internal planes. Many designers will connect a trace "tail" of 2mm to 3mm length to a pad and then connect a via at the end of this trace. This is a poor practice for high frequency decoupling. The inductance of the pair of traces connected to a capacitor is approximately 1.6nH, compared to the 0.6nH of the capacitor

OPERATION

itself. Instead, place two vias nearly tangent to the edge of a pad and tie them into the pad with very short traces, less than 1mm in length. This will produce the lowest inductance connections possible (Figure 1).

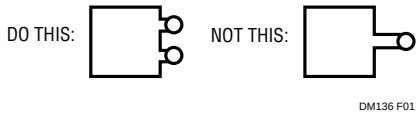


Figure 1

Mount the MOSFET as close to the load as possible. This will minimize the series inductance between the FET and the load. The LT1575 should also be mounted close to the FET to minimize the lengths of the interconnects, primarily the gate connection. Follow the layout shown here for grounding the frequency compensation and feedback divider (if using an adjustable part). It is preferable to make a separate connection from the LT1575's ground pin to the load ground, rather than connecting it to the ground plane locally. The interconnect trace should be fairly wide, at least 1mm.

If current limit is to be employed, calculate the sense resistor value as follows:

$$R_S = 30mV/I_{MAX}$$

See AN69 for details on how to use a small section of PCB trace for this resistor.

The time delay capacitor for the Shutdown pin will typically be in the range of 0.1µF to 1µF. Select a value that produces a delay time longer than the turn-on rise time of the regulator, because the regulator will probably come up in current limit if the input supply rise time is fast.

Heat sink requirements are no different than those for any linear regulator. The power dissipation is identical in all cases. Calculate the maximum power dissipation from the following equation:

$$P_{DIS(MAX)} = (V_{IN(MAX)} - V_{OUT(MIN)}) \bullet I_{MAX}$$

Calculate the required thermal resistance of the heat sink as follows:

$$R_{\theta SA} = [(T_{JMAX} - T_{AMB})/P_{DIS(MAX)}] - (R_{\theta CS} + R_{\theta JC})$$

where:

T_{JMAX} is the maximum allowable FET junction temperature,

T_{AMB} is the maximum expected ambient temperature,

$R_{\theta CS}$ is the case-to-sink thermal resistance (assume approximately 1°C/W), and

$R_{\theta JC}$ is the junction-to-case thermal resistance of the MOSFET.

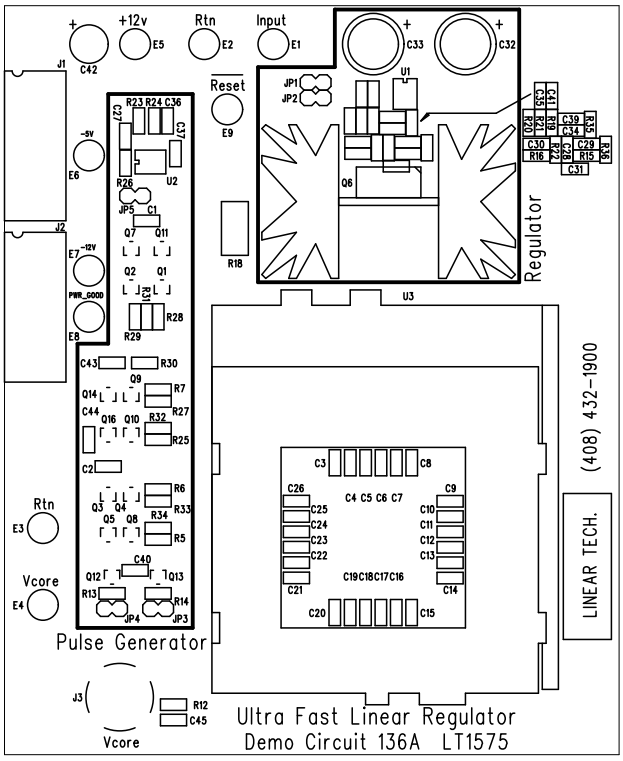
Select an appropriate heat sink from manufacturer's catalogs based on the number calculated above and the expected box airflow rate.

Note that the heat sink employed on the demo board is quite large compared to what will be required in most computer supplies. This was done because there will likely be no airflow during testing. Also, the power dissipation can become quite high if the board is operated with higher than normal input voltage and lower than normal output. Current limit is set to a nominal 10A.

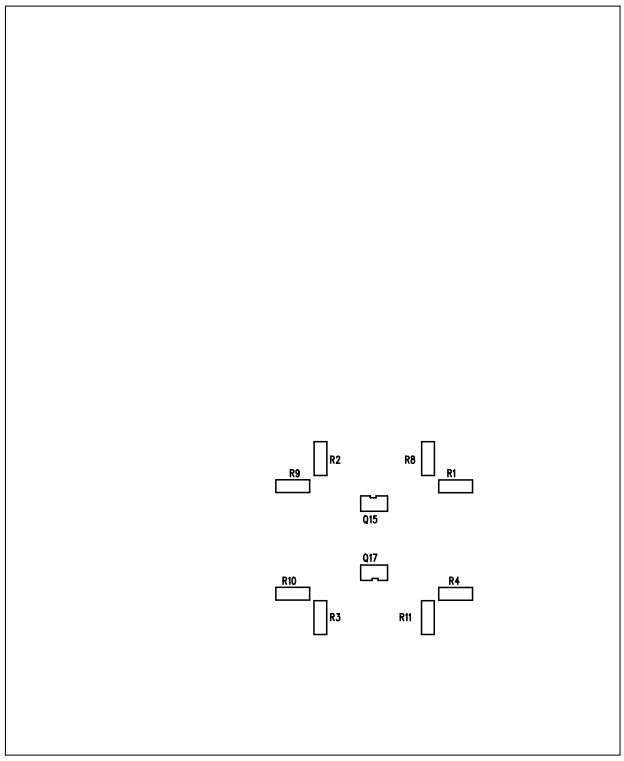
Input Capacitors

The OS-CON capacitors used on the demo board's input were chosen for convenience. Tantalum or aluminum electrolytic capacitors are viable alternatives. The single most important factor controlling the input capacitor selection is the off-line power supply's transient response. Monitor the 5V supply while subjecting the system to the maximum amplitude load transients that are anticipated. If the 5V supply is being pulled beyond specification limits, either add capacitors to the 5V supply or select a faster responding off-line supply. See AN69 for additional considerations.

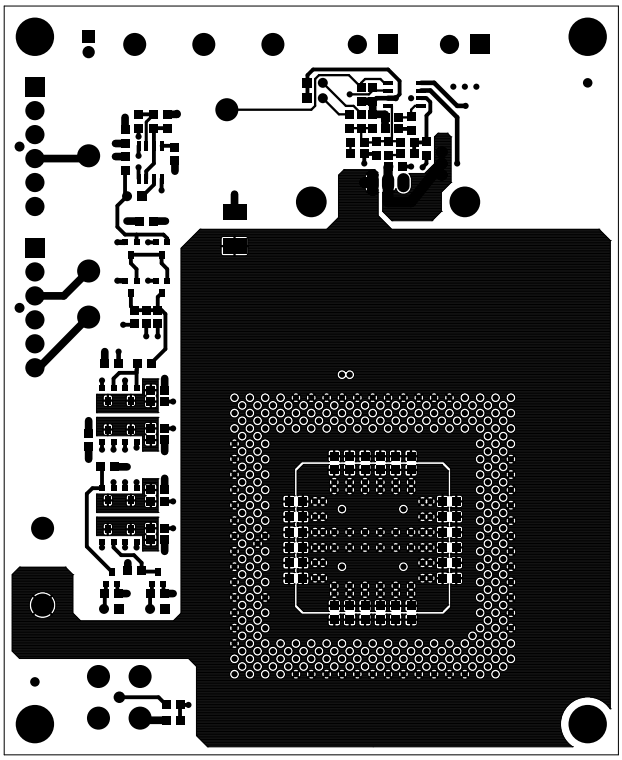
PCB LAYOUT AND FILM



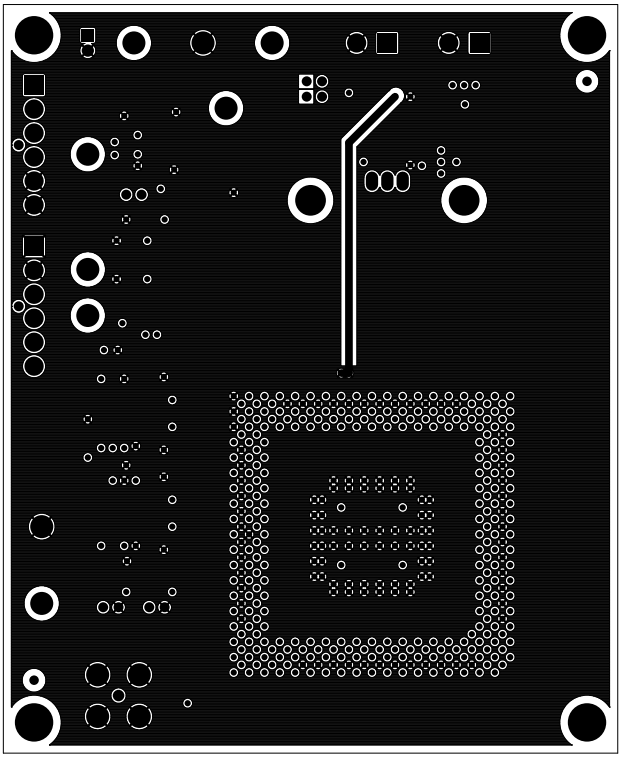
Component Silkscreen Top



Component Silkscreen Bottom

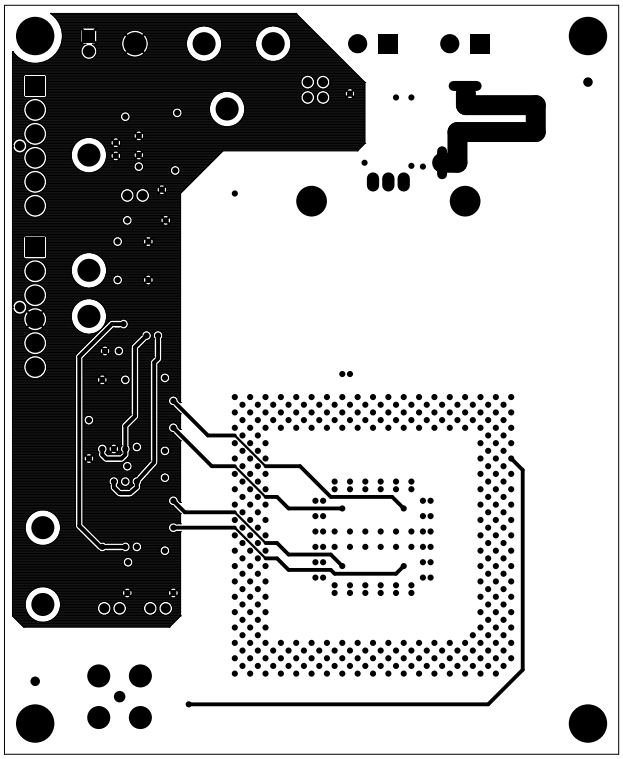


Copper Layer 1

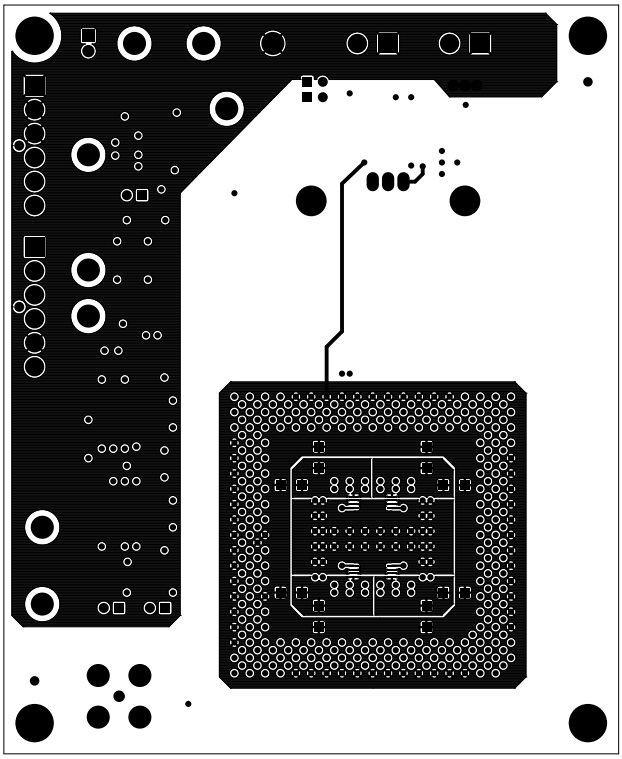


Copper Layer 2

PCB LAYOUT AND FILM

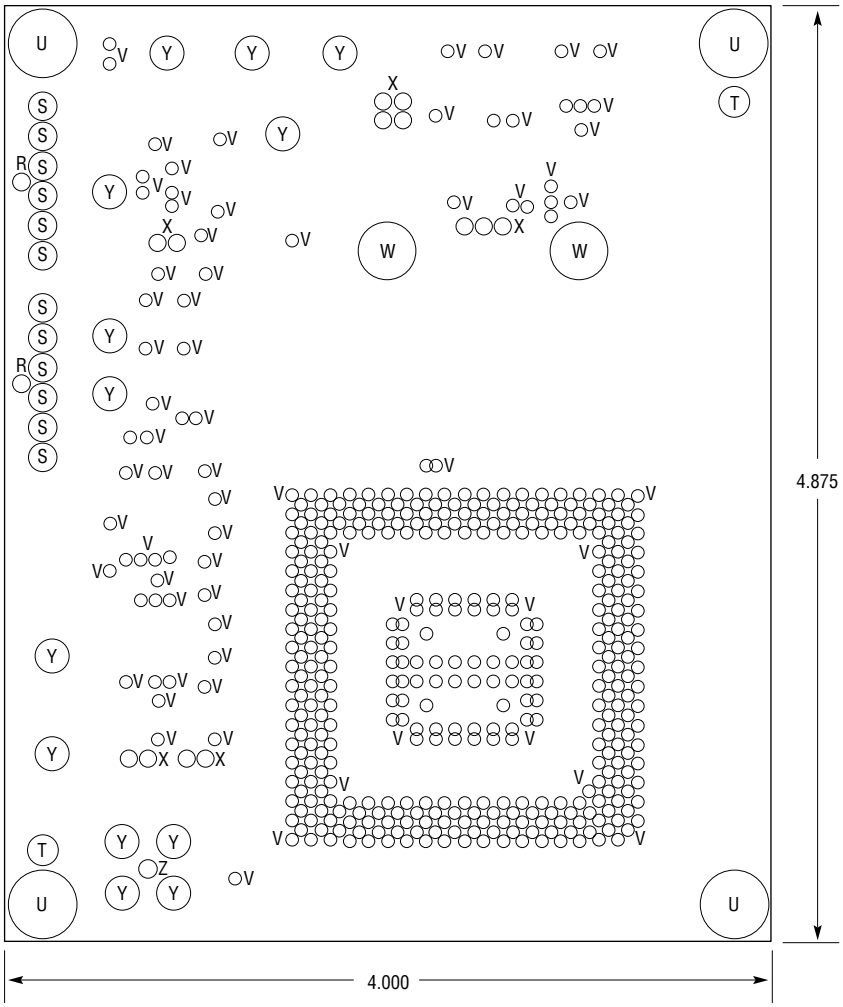


Copper Layer 3



Copper Layer 4

PC FAB DRAWING



NOTES:

1. MATERIAL: R4 OR EQUIVALENT EPOXY
   2 OZ COPPER CLAD FOR ALL OUTER LAYERS
   1 OZ COPPER CLAD FOR ALL INNER LAYERS
   THICKNESS 0.062" ± 0.006, TOTAL OF 4 LAYERS
2. FINISH: ALL PLATED HOLES 0.001 MIN/0.0015 MAX COPPER PLATE
   ELECTRODEPOSITED TIN-LEAD COMPOSITION
   BEFORE REFLOW, SOLDER MASK OVER BARE COPPER (SMOBC)
3. SOLDER MASK: BOTH SIDES USING GREEN SR1020 OR EQUIVALENT
4. SILKSCREEN: USING WHITE NONCONDUCTIVE EPOXY INK
5. ALL DIMENSIONS ARE INCHES

SYMBOL	DIAMETER (INCH)	NUMBER OF HOLES	PLATED
R	0.065	2	Yes
S	0.075	12	Yes
T	0.072	2	No
U	0.125	4	Yes
V	0.025	454	Yes
W	0.110	2	Yes
X	0.042	13	Yes
Y	0.096	13	Yes
Z	0.052	1	Yes
	TOTAL HOLES	662	

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