Minimizing Switching Regulator Residue in Linear Regulator Outputs

Banishing Those Accursed Spikes

Jim Williams

INTRODUCTION

Linear regulators are commonly employed to post-regulate switching regulator outputs. Benefits include improved stability, accuracy, transient response and lowered output impedance. Ideally, these performance gains would be accompanied by markedly reduced switching regulator generated ripple and spikes. In practice, all linear regulators encounter some difficulty with ripple and spikes, particularly as frequency rises. This effect is magnified at small regulator V_{IN} to V_{OUT} differential voltages; unfortunate, because such small differentials are desirable to maintain efficiency. Figure 1 shows a conceptual linear regulator and associated components driven from a switching regulator output.

The input filter capacitor is intended to smooth the ripple and spikes before they reach the regulator. The output capacitor maintains low output impedance at higher frequencies, improves load transient response and supplies frequency compensation for some regulators. Ancillary purposes include noise reduction and minimization of residual input-derived artifacts appearing at the regulators output. It is this last category–residual input-derived artifacts–that is of concern. These high frequency components, even though small amplitude, can cause problems in noise-sensitive video, communication and other types of circuitry. Large numbers of capacitors and aspirin have been expended in attempts to eliminate these undesired signals and their resultant effects. Although they are stubborn and sometimes seemingly immune to any treatment, understanding their origin and nature is the key to containing them.

Switching Regulator AC Output Content

Figure 2 details switching regulator dynamic (AC) output content. It consists of relatively low frequency ripple at the switching regulator's clock frequency, typically 100kHz to 3MHz, and very high frequency content "spikes" associated with power switch transition times. The switching regulator's pulsed energy delivery creates the ripple. Filter capacitors smooth the output, but not completely. The

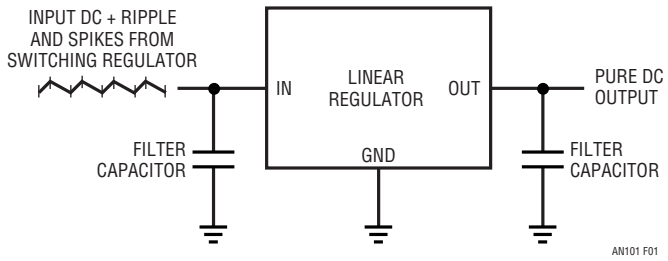


Figure 1. Conceptual Linear Regulator and Its Filter Capacitors Theoretically Reject Switching Regulator Ripple and Spikes

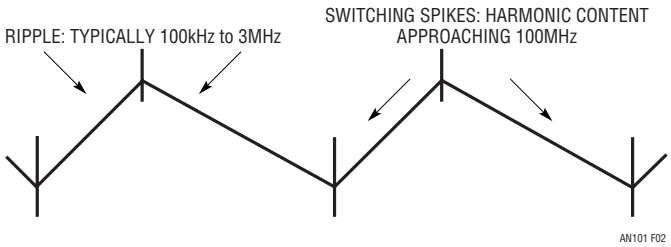


Figure 2. Switching Regulator Output Contains Relitively Low Frequency Ripple and High Frequency "Spikes" Derived From Regulators Pulsed Energy Delivery and Fast Transition Times

spikes, which often have harmonic content approaching 100MHz, result from high energy, rapidly switching power elements within the switching regulator. The filter capacitor is intended to reduce these spikes but in practice cannot entirely eliminate them. Slowing the regulator's repetition rate and transition times can greatly reduce ripple and spike amplitude, but magnetics size increases and efficiency falls[1]. The same rapid clocking and fast switching that allows small magnetics size and high efficiency results in high frequency ripple and spikes presented to the linear regulator.

Ripple and Spike Rejection

The regulator is better at rejecting the ripple than the very wideband spikes. Figure 3 shows rejection performance for an LT1763 low dropout linear regulator. There is 40db attenuation at 100KHz, rolling off to about 25db at 1MHz. The much more wideband spikes pass directly through the regulator. The output filter capacitor, intended to absorb the spikes, also has high frequency performance limitations. The regulator and filter capacitors imperfect response, due to high frequency parasitics, reveals Figure 1 to be overly simplistic. Figure 4 restates Figure 1 and includes the parasitic terms as well as some new components.

The figure considers the regulation path with emphasis on high frequency parasitics. It is important to identify these parasitic terms because they allow ripple and spikes to propagate into the nominally regulated output. Additionally, understanding the parasitic elements permits a measurement strategy, facilitating reduction of high frequency output content. The regulator includes high frequency parasitic paths, primarily capacitive, across its pass transistor and into its reference and regulation amplifier. These terms combine with finite regulator gain-bandwidth to limit high frequency rejection. The input and output filter capacitors include parasitic inductance and resistance, degrading their effectiveness as frequency rises. Stray layout capacitance provides additional unwanted feedthrough paths. Ground potential differences, promoted by ground path resistance and inductance, add additional error and also complicate measurement. Some new components, not normally associated with linear regulators, also appear. These additions include ferrite beads or inductors in the regulator input and output lines. These components have their own high frequency parasitic paths but can considerably improve overall regulator high frequency rejection and will be addressed in following text.

Note 1: Circuitry employing this approach has achieved significant harmonic content reduction at some sacrifice in magnetics size and efficiency. See Reference 1.

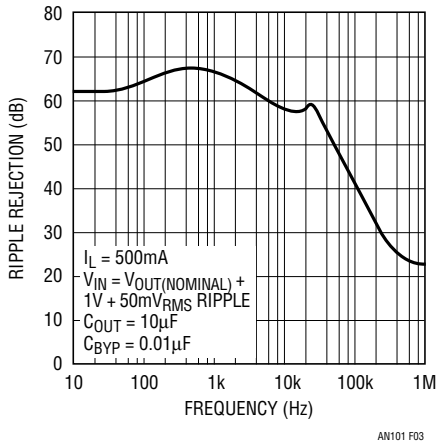


Figure 3. Ripple Rejection Characteristics for an LT1763 Low Dropout Linear Regulator Show 40dB Attenuation at 100kHz, Rolling Off Towards 1MHz. Switching Spike Harmonic Content Approaches 100MHz; Passes Directly From Input to Output

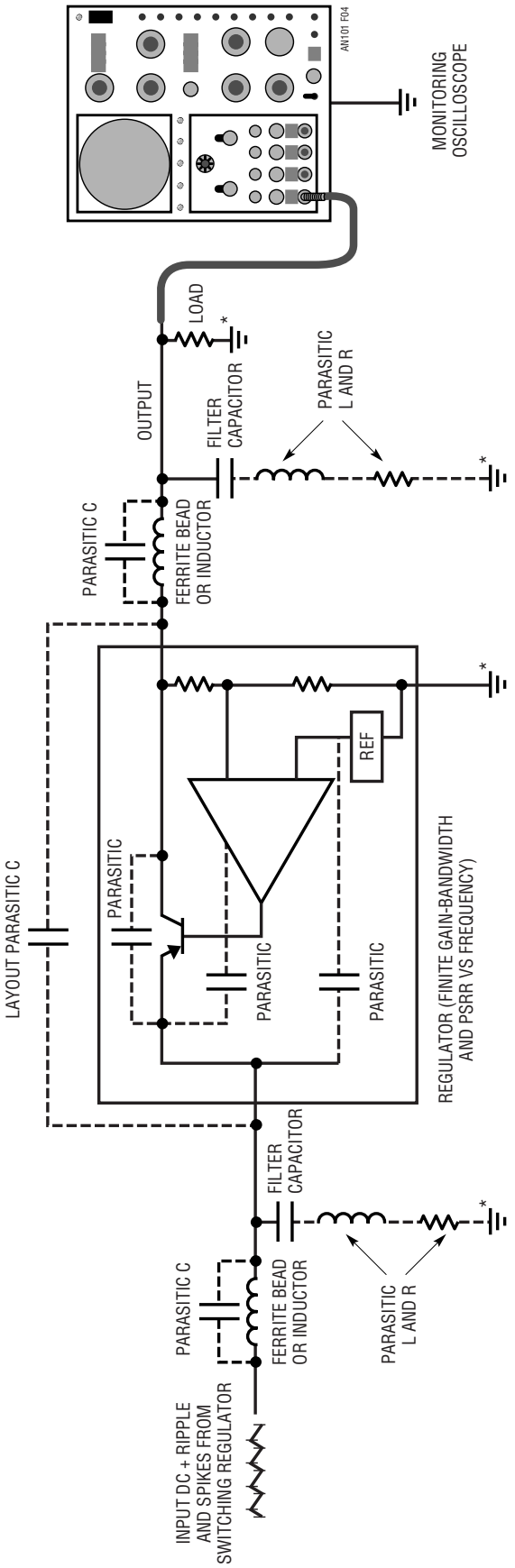
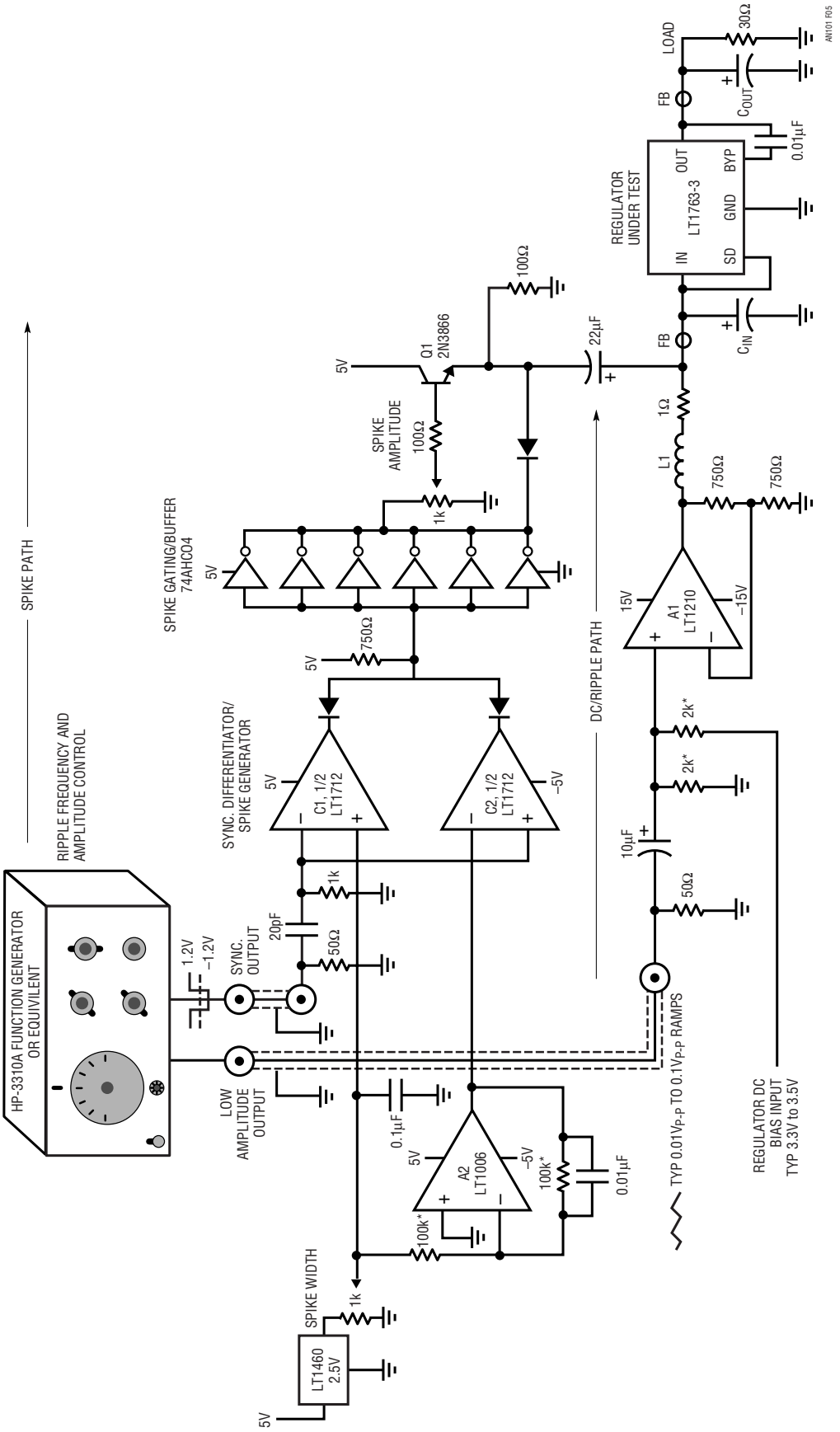


Figure 4. Conceptual Linear Regulator Showing High Frequency Rejection Parasitics. Finite GBW and PSRR vs Frequency Limit Regulator's High Frequency Rejection. Passive Components Attenuate Ripple and Spikes, But Parasitics Degrade Effectiveness. Layout Capacitance and Ground Potential Differences Add Errors, Complicate Measurement



* = 1% METAL FILM RESISTOR
L1 = 4 TURNS #26, 1/4" DIAMETER
FB = FERRITE BEAD. FAIR-RITE 2743002122. INDUCTORS OPTIONAL. SEE TEXT
= IN4148
C_{IN} = SEE TEXT
C_{OUT} = SEE TEXT

Figure 5. Circuit Simulates Switching Regulator Output. DC, Ripple Amplitude, Frequency and Spike Duration/Height are Independantly Settable. Split Path Scheme Sums Wideband Spikes with DC and Ripple, Presenting Linear Regulator with Simulated Switching Regulator Output. Function Generator Sources Waveforms to Both Paths

Ripple/Spike Simulator

Gaining understanding of the problem requires observing regulator response to ripple and spikes under a variety of conditions. It is desirable to be able to independently vary ripple and spike parameters, including frequency, harmonic content, amplitude, duration and DC level. This is a very versatile capability, permitting real time optimization and sensitivity analysis to various circuit variations. Although there is no substitute for observing linear regulator performance under actual switching regulator driven conditions, a hardware simulator makes surprises less likely. Figure 5 provides this capability. It simulates a switching regulator's output with independantly settable DC, ripple and spike parameters.

A commercially available function generator combines with two parallel signal paths to form the circuit. DC and ripple are transmitted on a relatively slow path while wideband spike information is processed via a fast path. The two paths are combined at the linear regulator input. The function generator's settable ramp output (trace A, Figure 6) feeds the DC/ripple path made up of power amplifier A1 and associated components. A1 receives the ramp input and DC bias information and drives the regulator under test. L1 and the 1Ω resistor allow A1 to drive the regulator at ripple frequencies without instability. The wideband spike path is sourced from the function generator's pulsed "sync" output (trace B). This output's edges are differentiated (trace C) and fed to bipolar comparator C1-C2. The comparator outputs (traces D and E) are spikes synchronized to the ramps inflection points. Spike width is controlled by complementary DC threshold potentials applied to C1 and C2 with the 1k potentiometer and A2. Diode gating and the paralleled logic inverters present trace F to the spike amplitude control. Follower Q1 sums the spikes with A1's DC/ripple path, forming the linear regulator's input (trace G).

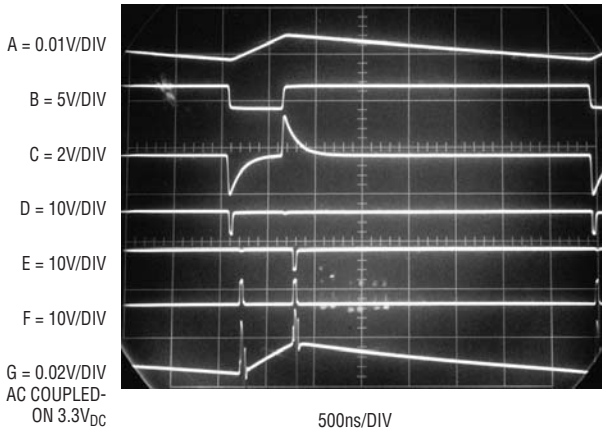


Figure 6. Switching Regulator Output Simulator Waveforms. Function Generator Supplies Ripple (Trace A) and Spike (Trace B) Path Information. Differentiated Spike Information's Bipolar Excursion (Trace C) is Compared by C1-C2, Resulting in Trace D and E Synchronized Spikes. Diode Gating/Inverters Present Trace F to Spike Amplitude Control. Q1 Sums Spikes with DC-Ripple Path From Power Amplifier A1, Forming Linear Regulator Input (Trace G). Spike Width Set Abnormally Wide for Photographic Clarity

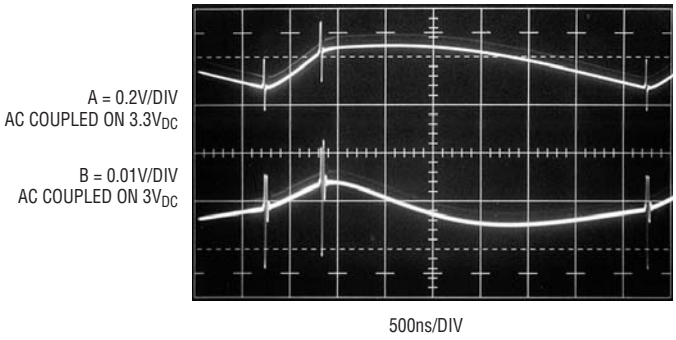


Figure 7. Linear Regulator Input (Trace A) and Output (Trace B) Ripple and Switching Spike Content for C_{IN} = 1μF, C_{OUT} = 10μF. Output Spikes, Driving 10μF, Have Lower Amplitude, But Risetime Remains Fast

Linear Regulator High Frequency Rejection Evaluation/Optimization

The circuit described above facilitates evaluation and optimization of linear regulator high frequency rejection. The following photographs show results for one typical set of conditions, but DC bias, ripple and spike characteristics may be varied to suit desired test parameters. Figure 7 shows Figure 5's LT1763 3V regulator response to a 3.3V DC input with trace A's ripple/spike contents, C_{IN} = 1μF and C_{OUT} = 10μF. Regulator output (trace B) shows ripple attenuated by a factor of ≈ 20. Output spikes see somewhat less reduction and their harmonic content remains high. The regulator offers no rejection at the spike rise time. The capacitors must do the job. Unfortunately, the capacitors are limited by inherent high frequency loss terms from completely filtering the wideband spikes; trace B's remaining spike shows no risetime reduction. Increasing capacitor value has no benefit at these rise times. Figure 8 (same trace assignments as Figure 7) taken with C_{OUT} = 33μF, shows 5× ripple reduction but little spike amplitude attenuation.

Figure 9's time and amplitude expansion of Figure 8's trace B permits high resolution study of spike characteristics, allowing the following evaluation and optimization. Figure 10 shows dramatic results when a ferrite bead immediately precedes C_{IN}[2]. Spike amplitude drops about 5×. The bead presents loss at high frequency, severely limiting spike passage[3]. DC and low frequency pass unattenuated to the regulator. Placing a second ferrite bead at the regulator output before C_{OUT} produces Figure 11's trace. The bead's high frequency loss characteristic further reduces spike amplitude below 1mV without introducing DC resistance into the regulator's output path[4].

Figure 12, a higher gain version of the previous figure, measures 900μV spike amplitude – almost 20× lower than without the ferrite beads. The measurement is completed by verifying that indicated results are not corrupted by common mode components or ground loops. This is done by grounding the oscilloscope input near the measurement point. Ideally, no signal should appear. Figure 13 shows this to be nearly so, indicating that Figure 12's display is realistic[5].

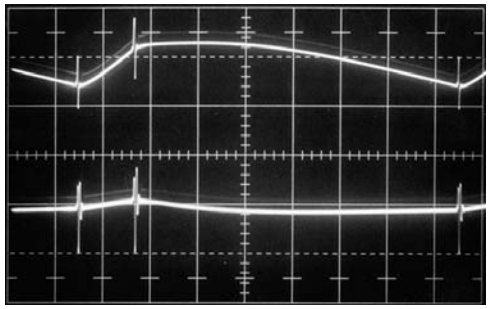


Figure 8. Same Trace Assignments as Figure 7 with C_{OUT} Increased to 33μF. Output Ripple Decreases By 5×, But Spikes Remain. Spike Risetime Appears Unchanged

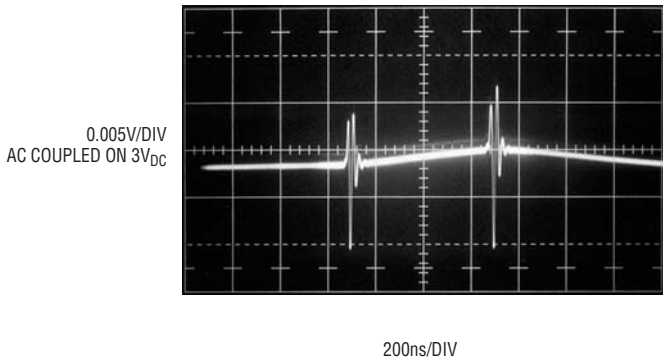


Figure 9. Time and Amplitude Expansion of Figure 8's Output Trace Permits Higher Resolution Study of Spike Characteristics. Trace Center-Screen Area Intensified for Photographic Clarity in This and Succeeding Figures

Note 2: "Dramatic" is perhaps a theatrical descriptive, but certain types find drama in these things.

Note 3: See Appendix A for information on ferrite beads

Note 4: Inductors can sometimes be used in place of beads but their limitations should be understood. See Appendix B.

Note 5: Faithful wideband measurement at sub-millivolt levels requires special considerations. See Appendix C.

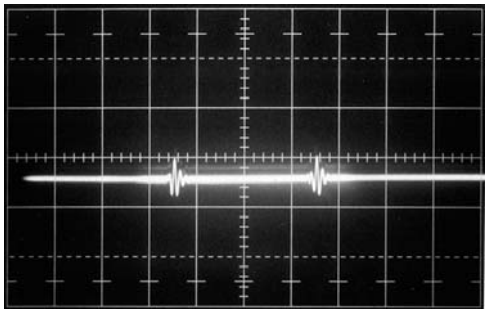


Figure 10. Adding Ferrite Bead to Regulator Input Increases High Frequency Losses, Dramaticlly Attenuating Spikes

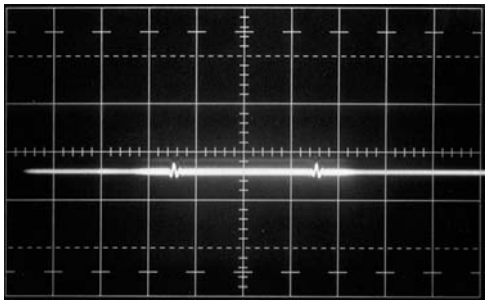


Figure 11. Ferrite Bead in Regulator Output Further Reduces Spike Amplitude

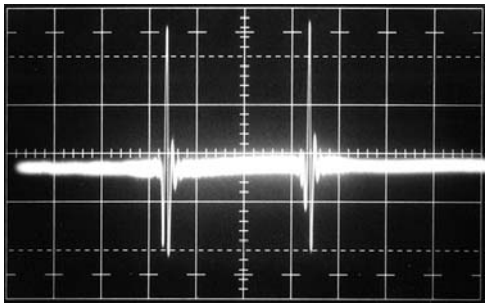


Figure 12. Higher Gain Version of Previous Figure Measures 900μV Spike Amplitude–Almost 20× Lower Than Without Ferrite Beads. Instrumentation Noise Floor Causes Trace Baseline Thickening

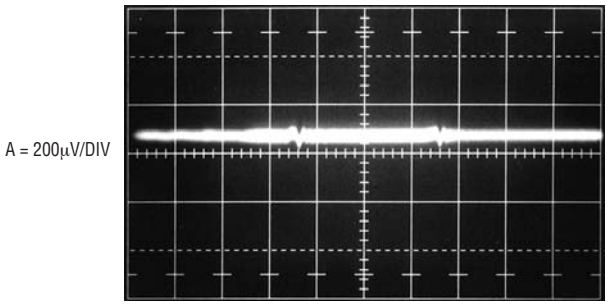


Figure 13. Grounding Oscilloscope Input Near Measurement Point Verifies Figure 12's Results Are Nearly Free of Common Mode Corruption

REFERENCES

1. Williams, Jim, "A Monolithic Switching Regulator with 100µV Output Noise," Linear Technology Corporation, Application Note 70, October 1997 (See Appendices B,C,D,H,I and J)

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3. Williams, Jim, "Component and Measurement Advances Ensure 16-Bit Settling Time," Linear Technology Corporation, Application Note 74, July 1998 (See Appendix G)

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5. Hurlock, Les, "ABCs of Probes," Tektronix Inc., 1990

6. McAbel, W.E., "Probe Measurements," Tektronix Inc., Concept Series, 1971

7. Morrison, Ralph, "Noise and Other Interfering Signals," John Wiley and Sons, 1992

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9. Fair-Rite Corporation, " Fair-Rite Soft Ferrites," Fair-Rite Corporation, 1998

APPENDIX A

About Ferrite Beads

A ferrite bead enclosed conductor provides the highly desirable property of increasing impedance as frequency rises. This effect is ideally suited to high frequency noise filtering of DC and low frequency signal carrying conductors. The bead is essentially lossless within a linear regulator's passband. At higher frequencies the bead's ferrite material interacts with the conductors magnetic field, creating the loss characteristic. Various ferrite materials and geometries result in different loss factors versus frequency and power level. Figure A1's plot shows this. Impedance rises from 0.01Ω at DC to 50Ω at 100MHz. As DC current, and hence constant magnetic field bias, rises, the ferrite becomes less effective in offering loss. Note that beads can be "stacked" in series along a conductor, proportionally increasing their loss contribution. A wide variety of bead materials and physical configurations are available to suit requirements in standard and custom products.

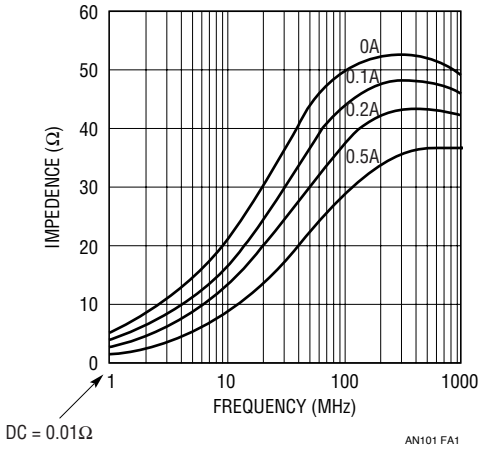

Figure A1. Impedance vs. Frequency at Various DC Bias Currents for a Surface Mounted Ferrite Bead (Fair-Rite 2518065007Y6). Impedance is Essentially Zero at DC and Low Frequency, Rising Above 50Ω Depending on Frequency and DC Current. Source: Fair-Rite 2518065007Y6 Datasheet.

APPENDIX B

Inductors as High Frequency Filters

Inductors can sometimes be used for high frequency filtering instead of beads. Typically, values of 2µH to10µH are appropriate. Advantages include wide availability and better effectiveness at lower frequencies, e.g., ≤100kHz. Figure B1 shows disadvantages are increased DC resistance in the regulator path due to copper losses, parasitic shunt capacitance and potential susceptibility to stray switching regulator radiation. The copper loss appears at DC, reducing efficiency; parasitic shunt capacitance allows unwanted high frequency feedthrough. The inductors circuit board position may allow stray magnetic fields to impinge its winding, effectively turning it into a transformer secondary. The resulting observed spike and ripple related artifacts masquerade as conducted components, degrading performance.

Figure B2 shows a form of inductance based filter constructed from PC board trace. Such extended length traces, formed in spiral or serpentine patterns, look inductive at high frequency. They can be surprisingly effective in some circumstances, although introducing much less loss per unit area than ferrite beads.

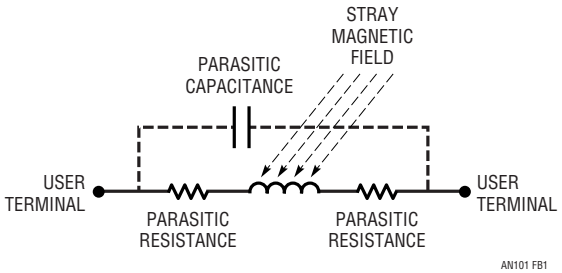

Figure B1. Some Parasitic Terms of an Inductor. Parasitic Resistance Drops Voltage, Degrading Efficiency. Unwanted Capacitance Permits High Frequency Feedthrough. Stray Magnetic Field Induces Erroneous Inductor Current

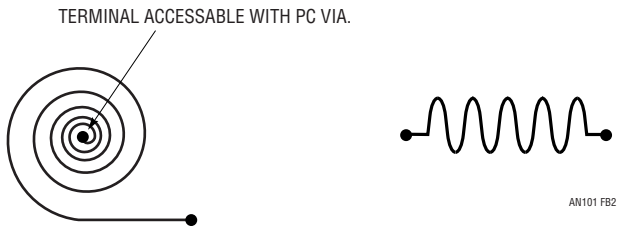

Figure B2. Spiral and Serpentine PC Patterns are Sometimes Used as High Frequency Filters, Although Less Effective Than Ferrite Beads

APPENDIX C

Probing Technique for Sub-Millivolt, Wideband Signal Integrity

Obtaining reliable, wideband, sub-millivolt measurements requires attention to critical issues before measuring anything. A circuit board layout designed for low noise is essential. Consider current flow and interactions in power distribution, ground lines and planes. Examine the effects of component choice and placement. Plan radiation management and disposition of load return currents. If the circuit is sound, the board layout proper and appropriate components used, then, and only then, may meaningful measurement proceed.

The most carefully prepared breadboard cannot fulfill its mission if signal connections introduce distortion. Connections to the circuit are crucial for accurate information extraction. Low level, wideband measurements demand care in routing signals to test instrumentation. Issues to consider include ground loops between pieces of test equipment (including the power supply) connected to the breadboard and noise pickup due to excessive test lead or trace length. Minimize the number of connections to the circuit board and keep leads short. Wideband signals to or from the breadboard must be routed in a coaxial environment with attention to where the coaxial shields tie into the ground system. A strictly maintained coaxial environment is particularly critical for reliable measurements and is treated here[1].

Figure C1 shows a believable presentation of a typical switching regulator spike measured within a continuous coaxial signal path. The spike's main body is reasonably well defined and disturbances after it are contained. Figure C2 depicts the same event with a 3 inch ground lead connecting the coaxial shield to the circuit board ground plane. Pronounced signal distortion and ringing occur. The photographs were taken at 0.01V/division sensitivity. More sensitive measurement requires proportionately more care.

Figure C3 details use of a wideband 40dB gain pre-amplifier permitting text Figure 12's 200µV/division measurement. Note the purely coaxial path, including the AC coupling capacitor, from the regulator, through the pre-amplifier and to the oscilloscope. The coaxial coupling capacitor's shield is directly connected to the regulator board's ground plane with the capacitor center conductor going to the regulator output. There are no non-coaxial measurement connections. Figure C4, repeating text Figure 12, shows a cleanly detailed rendition of the 900µV output spikes. In Figure C5 two inches of ground lead has been deliberately introduced at the measurement site, violating the coaxial regime. The result is complete corruption of the waveform presentation. As a final test to verify measurement integrity, it is useful to repeat Figure C4's measurement with the signal path input (e.g., the coaxial coupling capacitor's center conductor) grounded near the measurement point as in text Figure 13. Ideally, no signal should appear. Practically, some *small* residue, primarily due to common mode effects, is permissible.

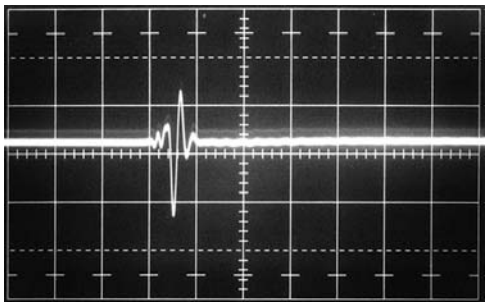

Figure C1. Spike Measured Within Continuous Coaxial Signal Path Displays Moderate Disturbance and Ringing After Main Event

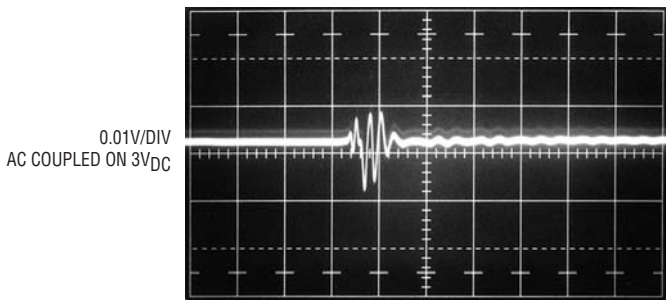

Figure C2. Introducing 3" Non-Coaxial Ground Connection Causes Pronounced Signal Distortion and Post-Event Ringing

Note 1: More extensive treatment of these and related issues appears in the appended sections of References 1 and 2. Board layout considerations for low level, wideband signal integrity appear in Appendix G of Reference 3.

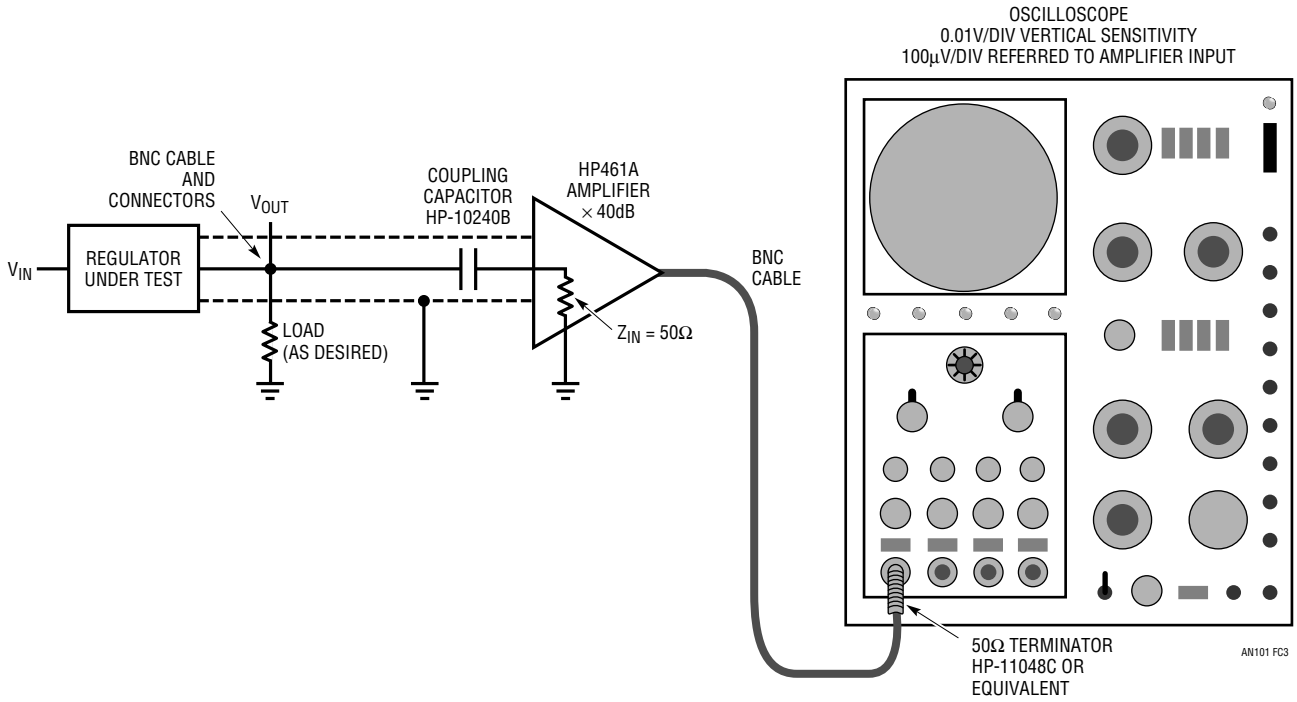

Figure C3. Wideband, Low Noise Pre-Amplifier Permits Sub-Millivolt Spike Observation. Coaxial Connections Must be Maintained to Preserve Measurement Integrity

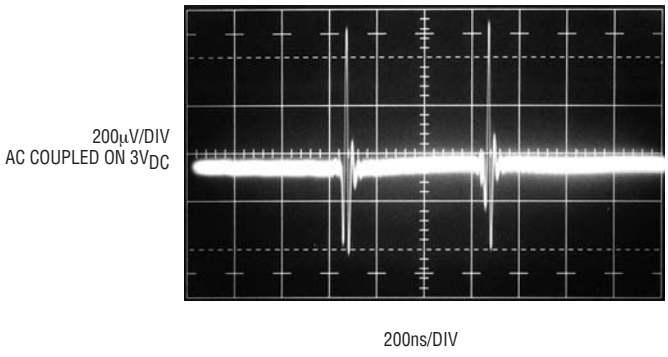

Figure C4. Low Noise Pre-Amplifier and Strictly Enforced Coaxial Signal Path Yield Text Figure 12's 900mVP-P Presentation. Trace Baseline Thickening Represents Pre-Amplifier Noise Floor

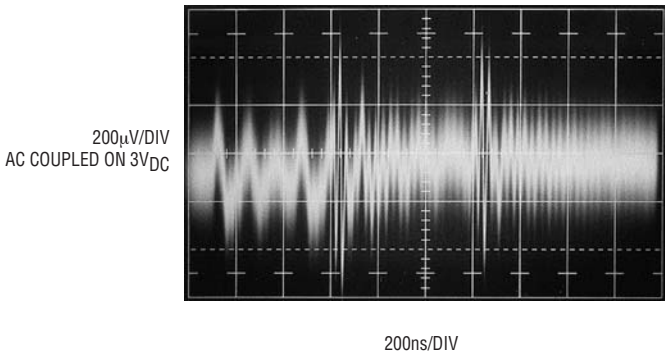

Figure C5. 2 Inch Non-Coaxial Ground Connection at Measurement Site Completely Corrupts Waveform Presentation

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