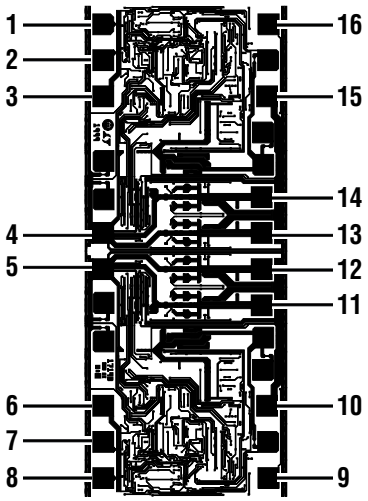
DICE SPECIFICATION

LT1714
Dual, 7ns, Low Power, 3V/5V/±5V Rail-to-Rail Comparator



90mils × 40mils,
12mils thick.
Backside metal: GOLD
Backside potential: V^-

PAD FUNCTION

1. –IN A
2. +IN A
3. V^-
4. V^+
5. V^+
6. V^-
7. +IN B
8. –IN B
9. LATCH ENABLE B
10. GND
11. Q B
12. $\overline{Q}$ B
13. $\overline{Q}$ A
14. Q A
15. GND
16. LATCH ENABLE A

DIE CROSS REFERENCE

Finished Part Number	Order Part Number
LT®1714	LT1714DICE

Please refer to ADI standard product data sheet for other applicable product information.

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage
- V^+ to V^- 12.6V
- V^+ to GND 12.6V
- V^- to GND ..... –10V to 0.3V

Differential Input Voltage ..... ±12.6V
Latch Pin Voltage 7V
Input and Latch Current ..... ±10mA
Output Current (Continuous) ..... ±20mA
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

DICE ELECTRICAL TEST LIMITS

T_A = 25°C. V^+ = 2.7V or V^+ = 5V, V^- = 0V, $V_{CM} = V^+/2$, V_{LATCH} = 0.8V, C_{LOAD} = 10pF, $V_{OVERDRIVE}$ = 20mV, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V^+	Positive Supply Voltage Range		2.4	7	V
V_{OS}	Input Offset Voltage (Note 3)	$R_S = 50\Omega$, $V_{CM} = V^+/2$		4	mV
I_{OS}	Input Offset Current			1	µA
I_B	Input Bias Current (Note 4)		–7	2	µA
V_{CM}	Input Voltage Range (Note 6)		–0.1	$V^+ + 0.1$	V
CMRR	Common Mode Rejection Ratio	$V^+ = 5V$, $0V \le V_{CM} \le 5V$ $V^+ = 2.7V$, $0V \le V_{CM} \le 2.7V$	60 57		dB dB
$PSRR^+$	Positive Power Supply Rejection Ratio	$2.4V \le V^+ \le 7V$, $V_{CM} = 0V$	65		dB
$PSRR^-$	Negative Power Supply Rejection Ratio	$-7V \le V^- \le 0V$, $V^+ = 5V$, $V_{CM} = 5V$	65		dB
A_V	Small-Signal Voltage Gain (Note 7)		1.5		V/mV
V_{OH}	Output Voltage Swing HIGH (Note 5)	I_{OUT} = 1mA, V^+ = 5V, $V_{OVERDRIVE}$ = 50mV I_{OUT} = 10mA, V^+ = 5V, $V_{OVERDRIVE}$ = 50mV	$V^+ – 0.5$ $V^+ – 0.7$		V V
V_{OL}	Output Voltage Swing LOW (Note 5)	I_{OUT} = –1mA, $V_{OVERDRIVE}$ = 50mV I_{OUT} = –10mA, $V_{OVERDRIVE}$ = 50mV		0.4 0.5	V V
I^+	Positive Supply Current (Per Comparator)	V^+ = 5V, $V_{OVERDRIVE}$ = 1V		6.5	mA
I^-	Negative Supply Current (Per Comparator)	V^+ = 5V, $V_{OVERDRIVE}$ = 1V		4.0	mA
V_{IH}	Latch Pin High Input Voltage		2.4		V
V_{IL}	Latch Pin Low Input Voltage			0.8	V
I_{IL}	Latch Pin Current	$V_{LATCH} = V^+$		10	µA

DICE ELECTRICAL TEST LIMITS

T_A = 25°C. V^+ = 5V, V^- = –5V, V_{CM} = 0V, V_{LATCH} = 0.8V, C_{LOAD} = 10pF, $V_{OVERDRIVE}$ = 20mV, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V^+	Positive Supply Voltage Range		2.4	7	V
V^-	Negative Supply Voltage Range (Note 2)		–7	0	V
V_{OS}	Input Offset Voltage (Note 3)	R_S = 50Ω, V_{CM} = 0V		3	mV
I_{OS}	Input Offset Current			1	µA
I_B	Input Bias Current (Note 4)		–7	2	µA
V_{CM}	Input Voltage Range (Note 6)		–5.1	5.1	V
CMRR	Common Mode Rejection Ratio	–5V ≤ V_{CM} ≤ 5V	62		dB
$PSRR^+$	Positive Power Supply Rejection Ratio	2.4V ≤ V^+ ≤ 7V, V_{CM} = –5V	68		dB
$PSRR^-$	Negative Power Supply Rejection Ratio	–7V ≤ V^- ≤ 0V, V_{CM} = 5V	65		dB
A_V	Small-Signal Voltage Gain (Note 7)	1V ≤ V_{OUT} ≤ 4V, R_L = ∞	1.5		V/mV
V_{OH}	Output Voltage Swing HIGH (Note 5)	I_{OUT} = 1mA, $V_{OVERDRIVE}$ = 50mV I_{OUT} = 10mA, $V_{OVERDRIVE}$ = 50mV	4.5 4.3		V V
V_{OL}	Output Voltage Swing LOW (Note 5)	I_{OUT} = –1mA, $V_{OVERDRIVE}$ = 50mV I_{OUT} = –10mA, $V_{OVERDRIVE}$ = 50mV		0.4 0.5	V V
I^+	Positive Supply Current (Per Comparator)	$V_{OVERDRIVE}$ = 1V		7.5	mA
I^-	Negative Supply Current (Per Comparator)	$V_{OVERDRIVE}$ = 1V		4.5	mA
V_{IH}	Latch Pin High Input Voltage		2.4		V
V_{IL}	Latch Pin Low Input Voltage			0.8	V
I_{IL}	Latch Pin Current	V_{LATCH} = V^+		10	µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The negative supply should not be greater than the ground pin voltages and the maximum voltage across the positive and negative supplies should not be greater than 12V.

Note 3: Input offset voltage (V_{OS}) is defined as the average of the two voltages measured by forcing first one output, then the other to $V^+/2$.

Note 4: Input bias current (I_B) is defined as the average of the two input currents.

Note 5: Output voltage swings are characterized and tested at V^+ = 5V and V^- = 0V. They are designed and expected to meet these same specifications at V^- = –5V.

Note 6: The input voltage range is tested under the more demanding conditions of V^+ = 5V and V^- = –5V. The LT1714 is designed and expected to meet these specifications at V^- = 0V.

Note 7: The LT1714 voltage gain is tested at V^+ = 5V and V^- = –5V only. Voltage gain at single supply V^+ = 5V and V^+ = 2.7V is guaranteed by design and correlation.

Wafer level testing is performed per the indicated specifications for dice. Considerable differences in performance can often be observed for dice versus packaged units due to the influences of packaging and assembly on certain devices and/or parameters. Please consult factory for more information on dice performance and lot qualifications via lot sampling test procedures.

Dice data sheet subject to change. Please consult factory for current revision in production.

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