Circuitry for Signal Conditioning and Power Conversion

Designs From a Once Lazy Sabbatical

Jim Williams

Introduction

Linear Technology has a sabbatical program. Every five years employees are granted sabbatical leave, which may last up to six weeks. You have 18 months from each five year employment anniversary to take the leave. Sabbatical is fully company paid and has no restrictions. The time is yours to do with as you please.

People exercise all degrees of freedom with their sabbaticals. They go sailing, they go to South Sea islands, they ski some mountain nobody ever heard of, they trek in Nepal. Houses get fixed, cars restored and children played with.

For my third sabbatical I resolved to do absolutely nothing. For the first time in my life I was really tired, and I knew it. A six week rest sounded just fine. I'd walk the dog and spend time with my wife and son. That's it. No transistors, no resistors, no op amps and, above all, *no writing*. I was so written out the thought of picking up a pencil produced an instant headache.

The first week I really did do nothing but sleep, walk the dog, read and hang around with my wife and kid. Later, on the weekend, I went for a long, cold (top down) ride in the countryside, which, via some convoluted route, ended up at an electronic junk store. There I found a wonderfully pristine, albeit nonfunctional, Hewlett-Packard 215A pulse generator. This instrument, utilizing an exotic, step recovery diode based output stage, has clean, sub-nanosecond transitions. After the requisite economic arm wrestling at the counter, I bought the thing for twenty-five bucks.

I took it home, repaired it, and used it to characterize a fast coincidence detector (Figures 14–18 and associated text) I had previously abandoned. This exercise proved fatally catalytic. Things rapidly proceeded in a predictable direction. The result was a three week binge in the middle of my formerly restful sabbatical. Many of the circuits presented here are refinements or adaptations of previous efforts, although some are new. Also included, and annotated as such, are other authors' works that seemed appropriate.

This publication's title is cursorily descriptive of its contents. A more studied accounting includes categories of data converters and signal conditioners, transducer circuits, oscillators and power converters. They begin immediately.

Micropower Voltage-to-Frequency Converters

Figure 1 is a voltage-to-frequency converter. A 0V to 5V input produces a 0Hz to 10kHz output, with a linearity of 0.02%. Gain drift is 60ppm/°C. Maximum current consumption is only 21µA, over 100 times lower than currently available monolithic ICs.

To understand circuit operation, assume that C1's negative input is slightly below its positive input (C2's output is low). The input voltage causes a positive-going ramp at C1's input (trace A, Figure 2). C1's output is high, allowing current flow from Q1's emitter, through C1's output stage to the 100pF capacitor. The 2.2µF capacitor provides high frequency bypass, maintaining low impedance at Q1's emitter. Diode connected Q6 provides a path to ground. The voltage to which the 100pF unit charges is a function of Q1's emitter potential and Q6's drop. C1's CMOS output, purely ohmic, contributes no voltage error. When the ramp at C1's negative input goes high enough, C1's output (trace B) goes low and the inverter switches high (trace C). This action pulls current from C1's negative input capacitor via the Q5 route (trace D). This current removal resets C1's negative input ramp to a potential slightly below ground. The 50pF capacitor furnishes AC positive feedback (C1's positive input is trace E) ensuring that C1's output remains negative long enough for a
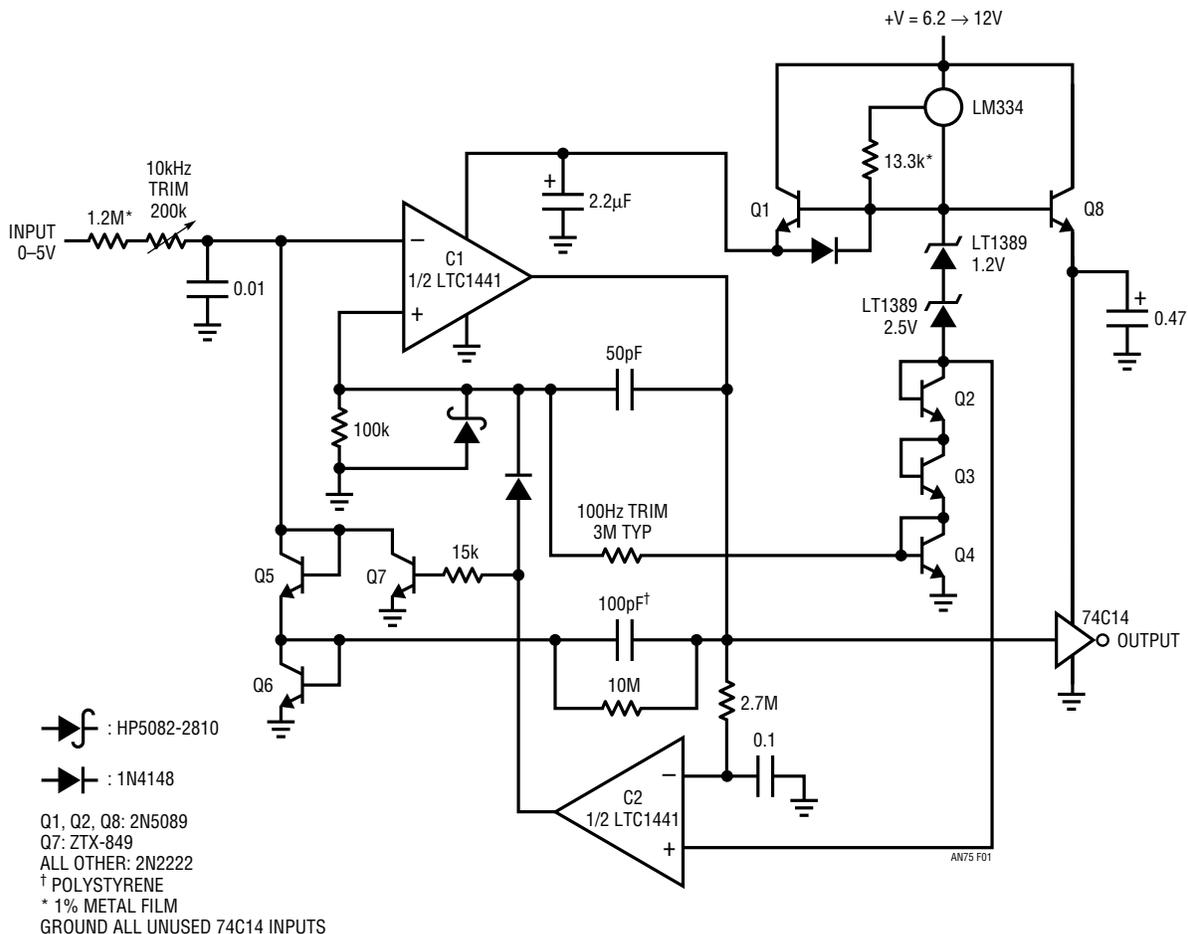
Figure 1. 0.02%, 0Hz to 10kHz Voltage-to-Frequency Converter Requires Only 21μA Supply Current

complete discharge of the 100pF capacitor. The Schottky diode prevents C1's input from being driven outside its negative common mode limit. When the 50pF units' feedback decays, C1 again switches high and the entire cycle repeats. The oscillation frequency depends directly on the input-voltage-derived current.

Q1's emitter voltage must be carefully controlled to get low drift. Q3 and Q4 temperature compensate Q5 and Q6 while Q2 compensates Q1's V_{BE}. The two LT1389s are the actual voltage reference and the LM334 current source provides 5μA bias to the stack. The current drive provides excellent supply immunity (better than 40ppm/V) and also aids circuit temperature coefficient. It does this by using the LM334's 0.3%/°C tempco to slightly temperature modulate the voltage drop in the Q2–Q4 trio. This correction's sign and magnitude directly oppose the –120ppm/°C 100pF polystyrene capacitor's drift, aiding overall circuit stability. Q8's isolated drive to the CMOS inverter prevents output loading from influencing Q1's

operating point. This makes circuit accuracy independent of loading.

The Q1 emitter-follower delivers charge to the 100pF capacitor efficiently. Both base and collector current end up in the capacitor. The 100pF capacitor, as small as desired performance permits, draws only small transient currents during its charge and discharge cycles. The 50pF–100k positive feedback combination draws insignificantly small switching currents. Figure 3, a plot of supply current vs operating frequency, reflects the low power design. At zero frequency, comparator quiescent current and the 5μA reference stack bias account for all current drain. There are no other paths for loss. As frequency scales up, the 100pF capacitor's charge-discharge cycle introduces the 1.1μA/kHz increase shown. A smaller value capacitor would cut power, but effects of stray capacitance and charge imbalance would introduce linearity and drift errors. Similarly, reduced reference stack drive would save current at the expense of drift.
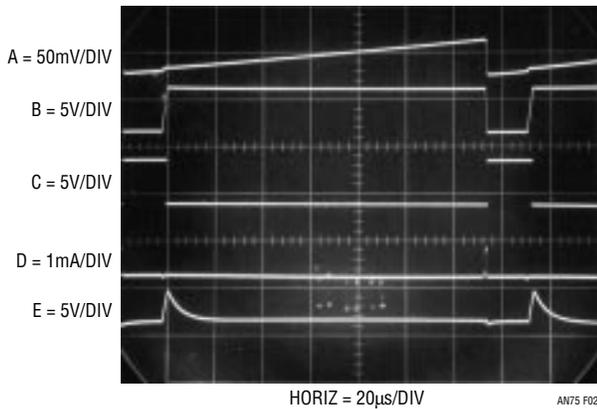
Figure 2. Waveforms for the Micropower Voltage-to-Frequency Converter. Charge-Based Feedback Provides Precision Operation with Extremely Low Power Consumption
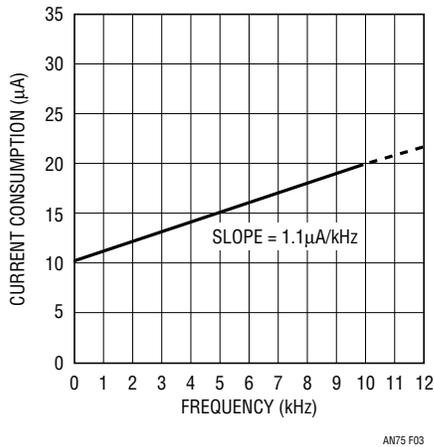

Figure 3. Current Consumption vs Frequency for the Voltage-to-Frequency Converter. Charge Dispensing Cycles Dominate 1.1μA/kHz Current Drain Increase

Circuit start-up or overdrive can cause the circuit's AC-coupled feedback to latch. If this occurs, C1's output goes low; C2, detecting this via the 2.7M–0.1μF lag, goes high. This lifts C1's positive input and grounds the negative input with Q7, initiating normal circuit action.

To calibrate this circuit, apply 50mV and select the indicated resistor at C1's positive input for a 100Hz output. Complete the calibration by applying 5V and trimming the input potentiometer for a 10kHz output.

Figure 4's circuit is quite similar, although a reworked reference cuts current drain to just 8.8μA and permits operation from a 5V supply (V_{IN} 3.4V to 36V). The penalty is degraded linearity and drift performance. A 0V to 2.5V input produces a 0Hz to 10kHz output, with 0.03% linearity, 250ppm/°C drift and 10ppm/V supply rejection. Maximum current consumption is only 8.8μA, 300 times lower than currently available ICs. Circuit AC operation is nearly identical to Figure 1, although a brief description follows.

Comparator C1 switches a charge pump comprising D1, D2 and the 33pF capacitor to maintain its negative input at 0V. A1 and associated components form a temperature compensating reference supply for the C1 based charge pump[1].

Note 1: Okay all you SPICE types out there, start your computers and model the charge pump drift and the reference compensation mechanism.
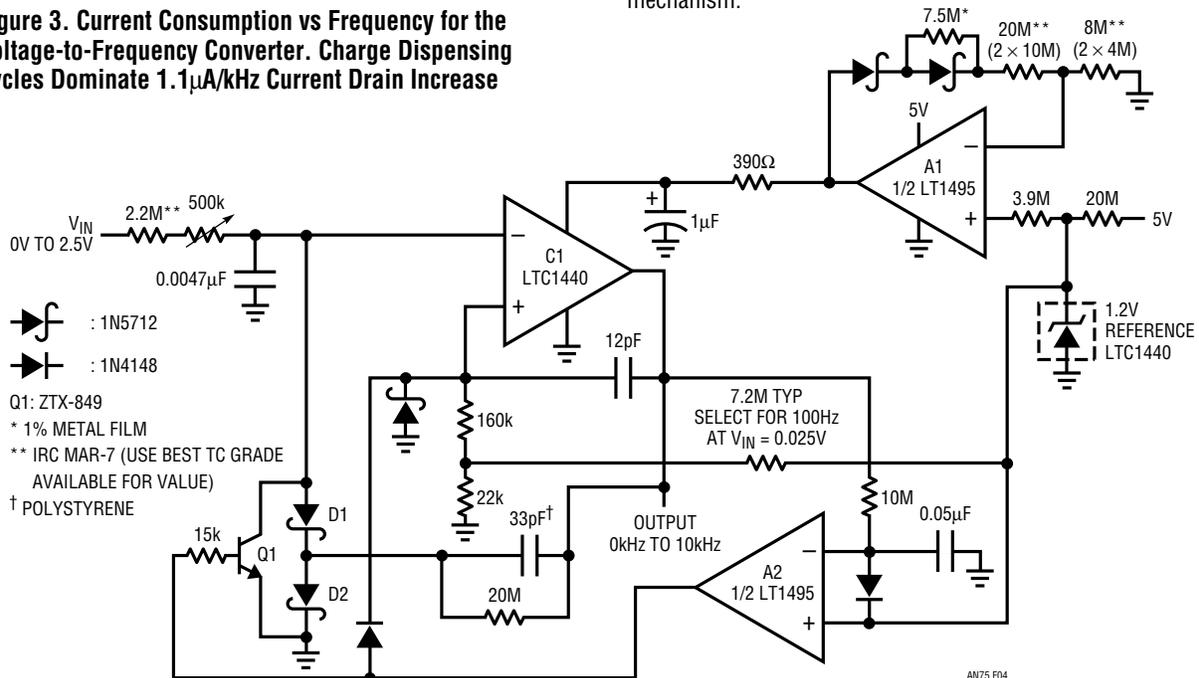

Figure 4. 0Hz to 10kHz Voltage-to-Frequency Converter Consumes Only 8.8μA. Circuit Is Similar to Figure 1. Reworked Reference Cuts Power, Although Linearity and Drift Degrade

The 1.2V reference biasing A1 is contained within C1's package. As such, a bootstrapped start-up is required. The 20M resistor provides this, while wasting less than 200nA.

The 33pF capacitor charges to a fixed voltage; hence, the switching repetition rate is the circuit's only degree of freedom to maintain feedback. Comparator C1 pumps uniform packets of charge to its negative input at a repetition rate precisely proportional to the input voltage derived current. This action ensures that circuit output frequency is strictly and solely determined by the input voltage.

Current consumption is extraordinarily low. Figure 4 shows only 5.4µA quiescent current, rising to 8.8µA at 10kHz. The 340nA/kHz slope directly relates to the charge dispensing losses.

Start-up or input overdrive can cause the circuit's AC-coupled feedback to latch. If this occurs, C1's output goes low; A2, detecting this via the 10M/0.05µF lag, goes high. This lifts C1's positive input and grounds the negative input with Q1, initiating normal circuit action.

It is worth noting that these voltage-to-frequency circuits are the beneficiaries of considerable attention over a protracted period of time. The evolution of these designs is detailed in Appendix A, "Some Guidelines for Micropower Design and an Example."
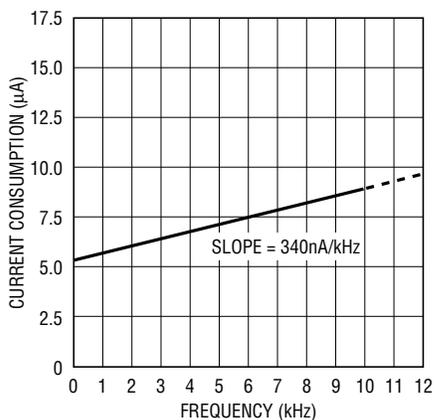

Figure 5. Current Consumption vs Frequency for Figure 4. Charge Dispensing Cycles Dictate 340nA/kHz Current Drain Increase

Micropower A/D Converters

In general, monolithic A/D converters have replaced discrete types. Occasionally, specific desirable circuit characteristics dictate a discrete design. Examples of such special cases include the need for a passive analog input, output data format, control protocol or economic constraints. Figure 6's 8-bit design consumes 12µA maximum, has 70ppm/°C drift (<1LSB 0°C to 70°C) and converts in 90ms. The circuit consists of a switched current source, an integrating capacitor, a comparator and a synchronized clock. When a pulse is applied to the convert command input (trace A, Figure 7) Q6 resets the 0.22µF capacitor to zero (trace B). Simultaneously, C1A goes low and Q5 conducts, biasing the LM334 based current source on. Additionally, Q4 conducts, causing the C1B based clock (trace D) to stop oscillating. During this interval the current source stabilizes, delivering its output to ground via Q6. When the convert command pulse falls the 0.22µF capacitor begins to ramp linearly. Concurrently, Q4 goes off, allowing the C1B clock to produce data output pulses (trace D). When the ramp voltage equals the E_X input, C1A switches high (trace C), biasing Q3 to stop the C1A clock. C1A's high state also cuts off Q5, shutting down the current source. Q5's gate going high bleeds a sub-microampere current through the 20M–Q1 path, maintaining ramp charging, but at a greatly reduced rate (this action is not readily discernible in Figure 7, but will be detailed). This insures overdrive for C1A while minimizing current source on-time, saving power. C1A's output pulse width (again, trace C) varies linearly with E_X's value. The Q3–Q4 gating of C1B prevents the convert command induced portion of C1A's output from allowing clock pulses. Thus, the clock bursts appearing at the data output (trace D) are directly and solely proportional to E_X. For the arrangement shown, 256 pulses appear for a 2.5V full-scale input.

Some subtleties are involved to achieve stated circuit performance. Q2 and associated biasing values combine with the LM334's inherent 3300ppm/°C temperature coefficient to keep current source drift inside 60ppm/°C. Q2, lacking gold doping, temperature tracks the LM334 more closely than a small signal diode would. The 0.22µF integrating and 220pF clock capacitors, both polystyrene, ratiometrically cancel their temperature coefficients to within 5ppm/°C. The specified resistors in the current
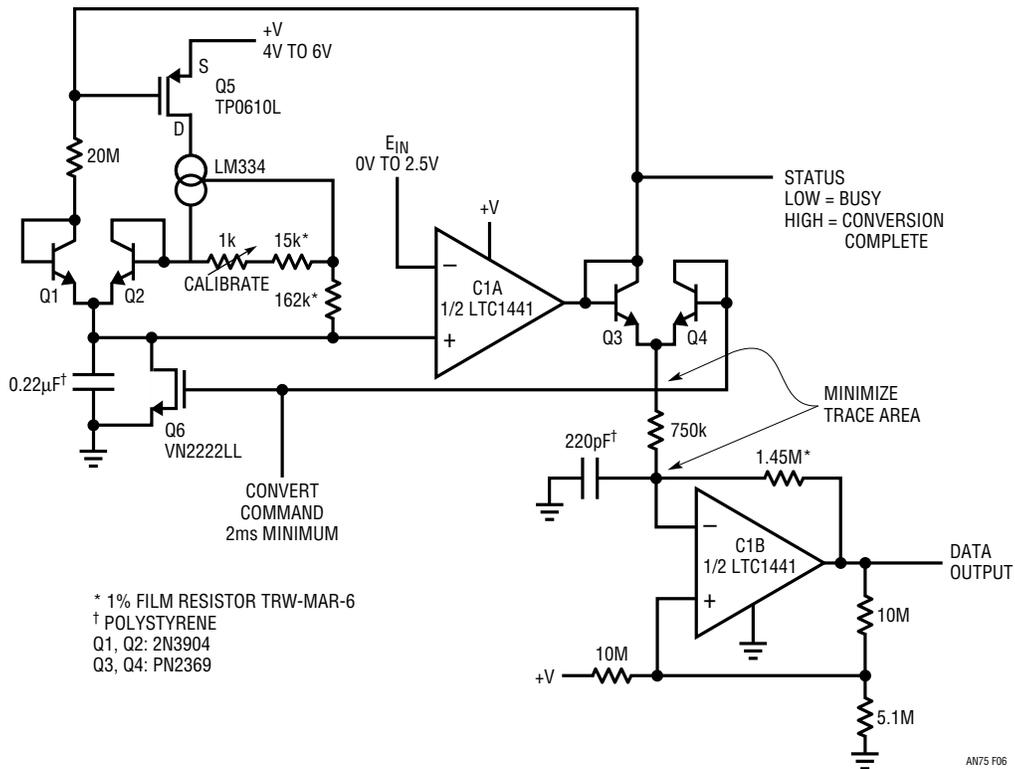
Figure 6. 8-Bit A/D Converter Consumes 12μA and Has Passive Input. Additional Features Include 7μA Quiescent Current, 70ppm/°C Drift and 90ms Conversion Time
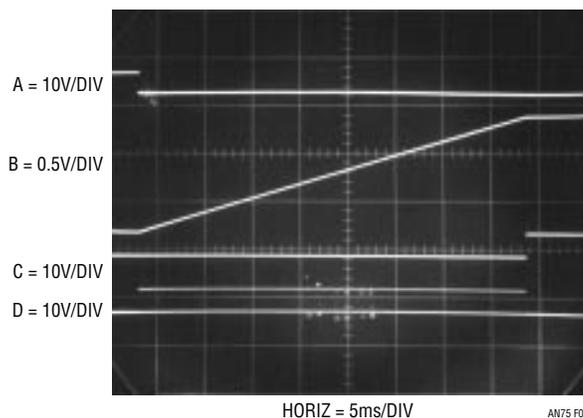

HORIZ = 5ms/DIV   AN75 F07

Figure 7. Waveforms for the 12μA A/D Converter (E_{IN} = 1.25V) Include Convert Command (A), Reference Ramp (B), Status Output (C) and Data Output (D). Segmented Ramp Slope Characteristic Is Not Discernable in Trace B

source and clock have very low drift. The biasing at C1B's negative input synchronizes the clock oscillator to the conversion sequence, eliminating a ±1 count error source. It also enforces predictable, optimum oscillator start-up, minimizing data jitter. Q3 and Q4 provide lower AC parasitics than diodes, enhancing clean oscillator gating. The converter typically holds 1LSB accuracy over 0°C to 70°C. Achievable conversion time varies with input. At tenth scale 16ms is possible, decreasing to 90ms at full scale.

Figure 8 details operation at E_X = 80mV. The segmented slope operation due to current source switching is easily seen under these conditions. Trace A is convert command, trace B Q5's drain, trace C the ramp, trace D C1A's output ("status" line), trace E C1B's negative input[2] and trace F the data output. Trace E shows the benefit of the aforementioned optimized biasing at C1B's negative input. Clock oscillations start immediately, with no untoward dynamics.

Figure 9 is a study of the segmented slope operation. The photograph, taken at a 180mV input, shows the ramp zero reset and clean switching. When Q5 is on, its drain (trace A, Figure 9) is high, turning on the current source. The current source linearly ramps the 0.22µF capacitor (trace

B) until C1A switches Q5 off. The current source then goes off, leaving the 20M–Q1 path to continue the charging at a sub-microampere rate. This continued charging ensures that C1A is overdriven, preventing spurious outputs.

The current source operates at almost 5µA. Turning it off after C1A switches saves considerable power, particularly at modest E_X values at high conversion rates. When Q5 switches the current source off, charging continues via the 20M–Q1 path, but far less than a microampere is lost.

A/D power consumption is extremely low, due to the low power components and circuit configuration. Current consumption is 12µA for E_X = 2.5V at a 10Hz conversion rate. Intermediate values of E_X and conversion rate result in less current drain, down to a minimum of 7µA at quiescence. Additional power savings are theoretically possible by running a lower current source value, but dynamics and temperature coefficient suffer. Further power economy is possible by shutting off the current source during capacitor reset, but accuracy degrades due to current source settling time requirements.

Note 2: Monitoring this high impedance AC node without incurring probe induced error involves special considerations. See Appendix B, "Parasitic Effects of Test Equipment in Micropower Circuits."
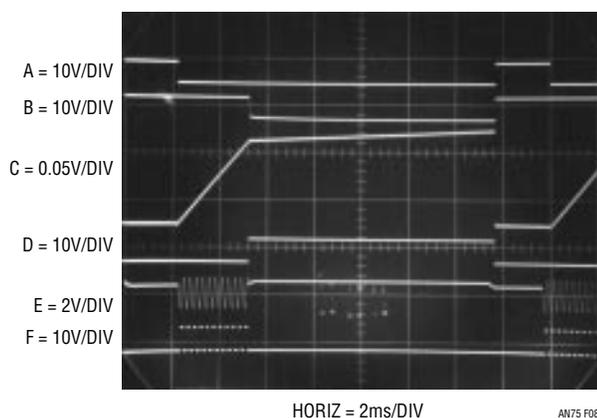

A = 10V/DIV
B = 10V/DIV
C = 0.05V/DIV
D = 10V/DIV
E = 2V/DIV
F = 10V/DIV

HORIZ = 2ms/DIV   AN75 F08

Figure 8. Detailed Operating Waveforms at E_{IN} = 80mV. Trace A Is Convert Command, B, Q5 Drain, C, Ramp, D, Status, E, Clock Capacitor and F, Data Out. Optimized Capacitor Biasing Ensures Immediate, Predictable Clock Start-Up. Segmented Ramp Slope is Viewable in Trace C
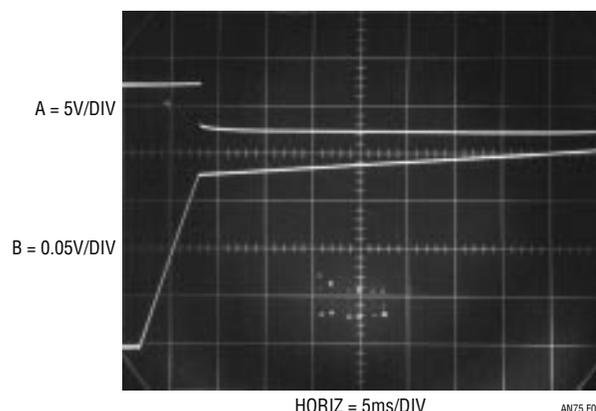

A = 5V/DIV

B = 0.05V/DIV

HORIZ = 5ms/DIV   AN75 F09

Figure 9. Expanded Detail of Segmented Slope Ramp (B) and Q5 Drain (A) at E_{IN} = 180mV. When Q5 Goes Off, Ramp Current Source Ceases, Saving Power. Ramp Capacitor Charging Continues at Greatly Reduced Rate Via 20M Resistor, Insuring Comparator Overdrive

10-Bit, Micropower A/D Converter

Figure 10 extends accuracy to 10 bits, while increasing conversion speed to 35ms. The trade off is current consumption, which increases to 29μA. The circuit's operation is nearly identical to the 8-bit version, although the current source and clock are redesigned for higher accuracy. The LT1389–2N3809 combination is the current source, with the 301k resistor specified to oppose the integrating capacitor's –120ppm/°C temperature coefficient. The clock employs a 32.768kHz "watch" crystal for stability[3]. The quartz crystal's high Q, resonant characteristic precludes direct oscillator gating as was done in the previous circuit. Instead, the clock is synchronized to the conversion sequence with a flip-flop, which in turn transmits the convert command to the converter.

These stability improvements allow 10-bit resolution with 1LSB of drift over 0°C to 70°C. At a 10Hz conversion rate with E_{IN} = 3V current drain is 29μA, decreasing to 21μA at quiescence. As in the previous circuit, different values of E_{IN} and conversion rate result in intermediate amounts of current consumption.

Differential Input, 10MHz RMS/DC Converter

Wideband, thermally based RMS/DC conversion has previously been described, utilizing single-ended inputs[4]. Figure 11's 10MHz RMS/DC converter has differential inputs while maintaining 1% accuracy beyond 10MHz. A $1V_{RMS}$ differential input produces 10V DC at the output.

The wideband LT1207 dual power op amp receives the differential inputs. The amplifiers, connected for a differential gain of 10, feed the LT1088 RMS/DC converter. The 24pF–5k trim provides a high frequency gain boost, preserving accuracy at the highest frequencies.

The LT1088 based RMS/DC converter is made up of matched pairs of heaters and diodes and a control amplifier. The A1–A2 amplifiers drive R1, producing heat which lowers D1's voltage. Differentially connected A3 responds by driving R2, via Q3, to heat D2, closing a loop around the amplifier. Because the diodes and heater resistors are matched, A3's DC output is related to the RMS value of the input, regardless of input frequency or waveshape. In practice, residual LT1088 mismatches necessitate a gain

Note 3: A detailed description of this clock circuit appears in the text associated with Figure 27.

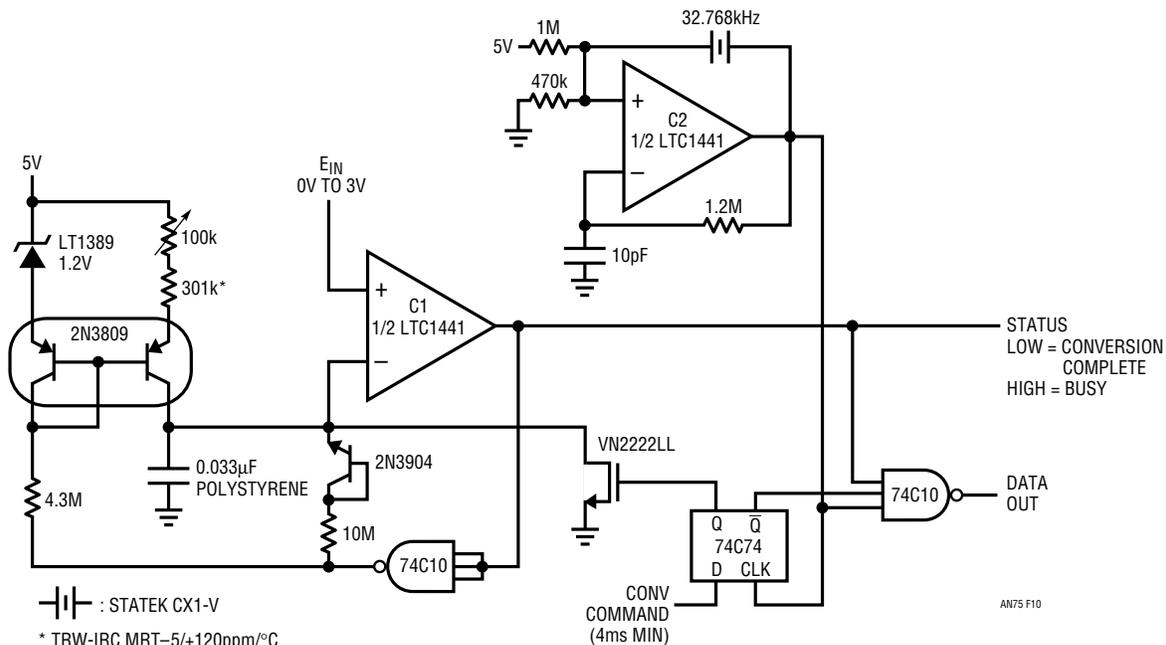**Note 4:** For examples, see references 10 through 13.

Figure 10. A 10-Bit Version of Figure 6. Improvements Include Higher Stability Clock and Current Source. Modifications Permit 1LSB Drift (0°C to 70°C) and 35ms Conversion Speed, Although Current Drain Increases to 29μA

trim, which is implemented at A4. A4's output is the circuit output. The LT1004 and associated components frequency compensate the loop and provide good settling time over wide ranges of operating conditions.

Start-up or input overdrive can cause A2 to deliver excessive current to the LT1088 with resultant damage. C1 and C2 prevent this. Overdrive forces D1's voltage to an abnormally low potential. C1 triggers low under these conditions, pulling C2's input low. This causes C2's output to go high, putting A1 and A2 into shutdown and terminating the overload. After a time determined by the RC at C2's input, A1 and A2 will be enabled. If the overload condition

still exists the loop will almost immediately shut A1 and A2 down again. This oscillatory action will continue, protecting the LT1088 until the overload condition is removed.

Performance for the circuit is quite impressive. Figure 12 plots error with one input driven at two different gain boost network trims. The graph (B) shows 1% error bandwidth to 11MHz. The slight peaking out to 5MHz is due to the A1–A2 gain boost network. This peaking is minimal compared to the total error envelope, and a small price to pay to get 1% accuracy to 11MHz. One percent accuracy to 14MHz is available if the gain trim and boost network are set to accentuate peaking at the expense of flatness (A).
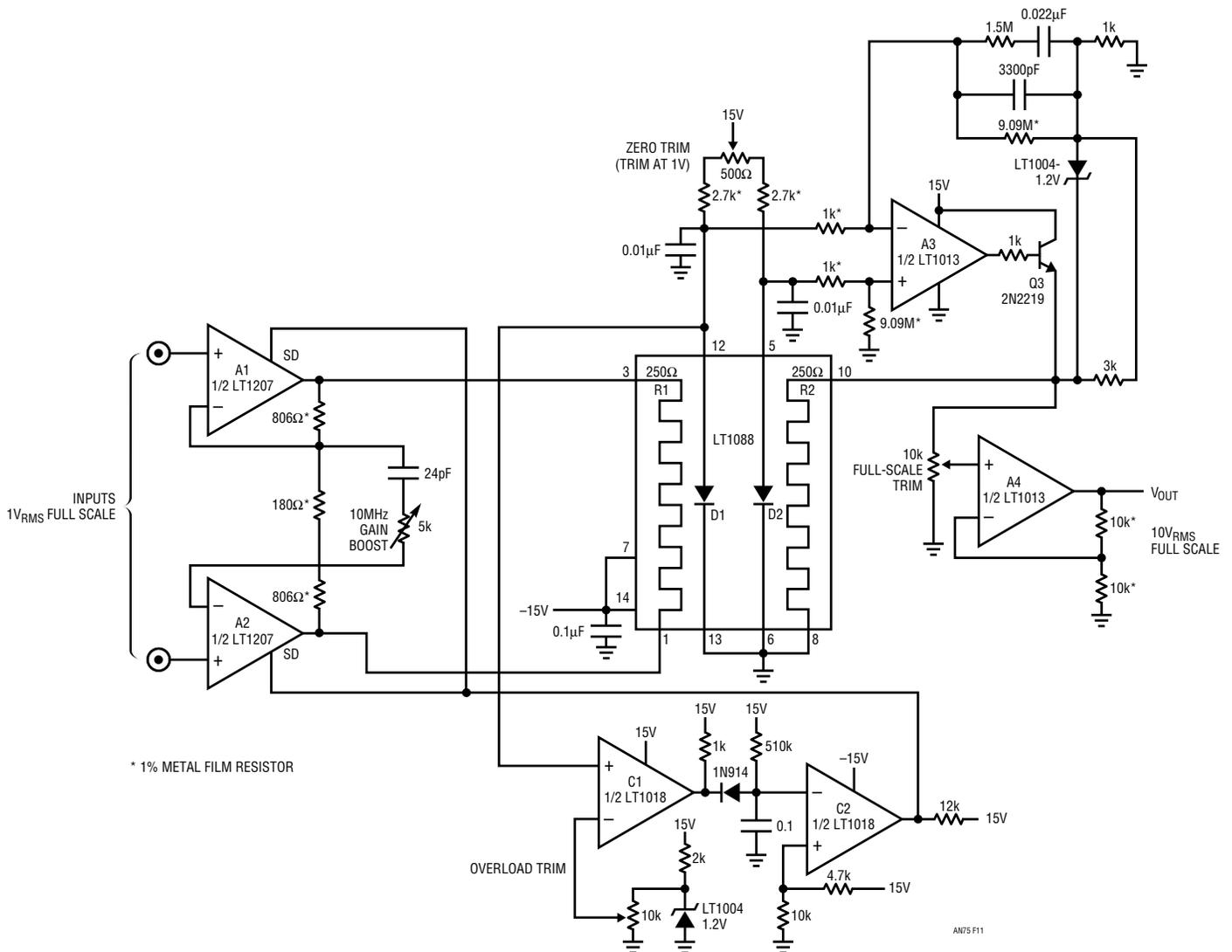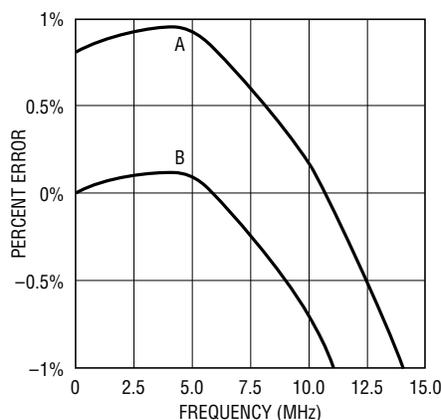

Figure 11. Differential Input 10MHz RMS/DC Converter Has 1% Accuracy, High Input Impedance and Overload Protection. Single-Ended Operation Extends 1% Error Bandwidth to 14MHz

Figure 13 shows effects of common mode signals on accuracy. This data was taken with a well shielded, carefully layed out breadboard. Common mode rejection ratio remains high as frequency scales, contributing negligible error until 10.2MHz. The indicated $5V_{RMS}$ common mode drive is a demanding test, with smaller values permitting better performance.

To trim this circuit put the $5k\Omega$ potentiometer at its maximum resistance position and apply a 100mV, 5MHz signal. Trim the 500Ω adjustment for exactly $1V_{OUT}$. Next, apply a 5MHz 1V input and trim the 10k potentiometer for $10.00V_{OUT}$. Finally, put in 1V at 10MHz and adjust the $5k\Omega$ trimmer for $10.00V_{OUT}$. Repeat this sequence until circuit output is within 1% accuracy for DC–10MHz inputs. Two passes should be sufficient. The overload trim is set at 10% below D1's voltage with the circuit operating at full scale.

AN75 F12

Figure 12. Error Plot for the Differential Input RMS/DC Converter with One Input Driven. Frequency Dependent Gain Boost Preserves 1% Accuracy, But Causes Slight Peaking Before Roll-Off. Boost Is Settable for Maximum Bandwidth (A) or Minimum Error (B)
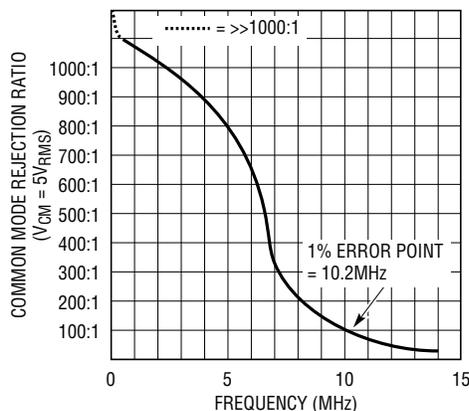
AN75 F13

Figure 13. Common Mode Rejection Ratio vs Frequency for the Differential Input RMS/DC Converter. Layout, Amplifier Bandwidth and AC Matching Characteristics Determine Curve

3 Nanosecond Coincidence Detector

Figure 14's circuit, detecting coincident voltage levels at its inputs, responds with a logical high at its output. The detection trigger level is settable between zero and 4.0V. The circuit will resolve coincidence down to 3ns and has a decision delay time of 4.5ns. The circuit is composed of a pair of fast level discrimination comparators and a sub-nanosecond AND gate. The comparators balance each input against a level threshold, in this case about 1V. The comparator outputs feed Q1 and associated components, which form a 300ps AND gate. Figure 15's waveforms show circuit operation. Trace A is one input, while trace B is the remaining input. Trace C is the circuit output. When trace B crosses the 1V recognition threshold the output goes high, remaining high until either input (in this case trace B) drops below 1V. The key to this circuit's speed is the fast comparators and the discrete AND gates extremely low delay.
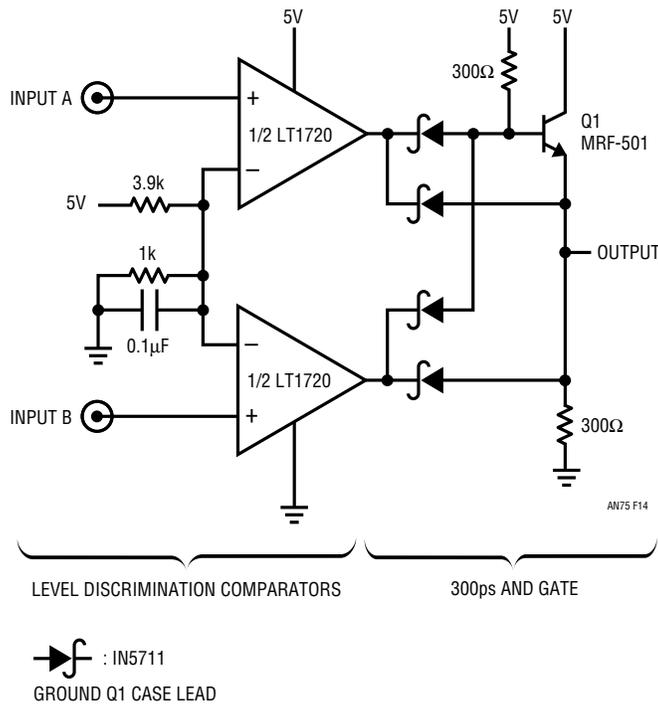

LEVEL DISCRIMINATION COMPARATORS   300ps AND GATE

➤⊣ϝ : IN5711

GROUND Q1 CASE LEAD

Figure 14. Coincidence Detector Has 3ns Recognition Threshold. Discrete Components Form 300ps AND Gate, Maintaining High Speed Signal Path
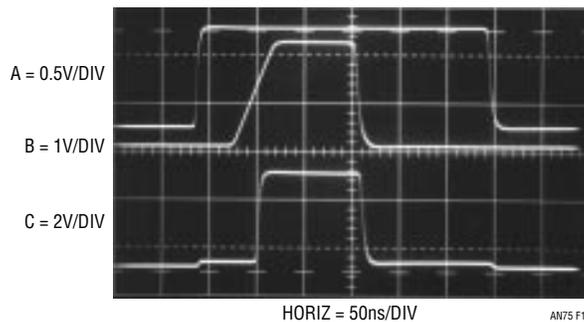

HORIZ = 50ns/DIV   AN75 F15

Figure 15. Coincidence Detector Waveforms. Trace A Is Input A, B Is Input B. Trace C Indicates Coincidence When A and B Are Both >1V

Evaluating circuit performance requires a sub-nanosecond rise-time pulse generator and a very fast oscilloscope[5]. Figure 16, taken in a 3.9GHz sampled bandpass, shows a comparator output (trace A) and the resultant circuit output (trace B). The Schottky diodes and gigahertz range transistor provide very fast response, and delay is inside 300ps.

Figure 17 shows circuit response in a 3.9GHz sampled bandpass with the inputs simultaneously driven by a 3ns, 2V pulse (trace A). This pulse width is just inside the recognition limit, and the output (trace B) responds cleanly.

The 4.5ns decision delay characteristic is also readily apparent. Further input pulse width reduction has dramatic results[6]. In Figure 18 input width (trace A) is shortened by 600ps. The output (trace B) is caught not quite fully responding. It rises about 2V before falling back in a noisy but controlled decay. The rise slope, degraded from Figure 17's, is additional evidence of circuit gain-bandwidth limitations.

Note 5: Refer to this publication's introduction.

Note 6: I offer no apology for the choice of verbiage. Nerds like me find drama in these things.

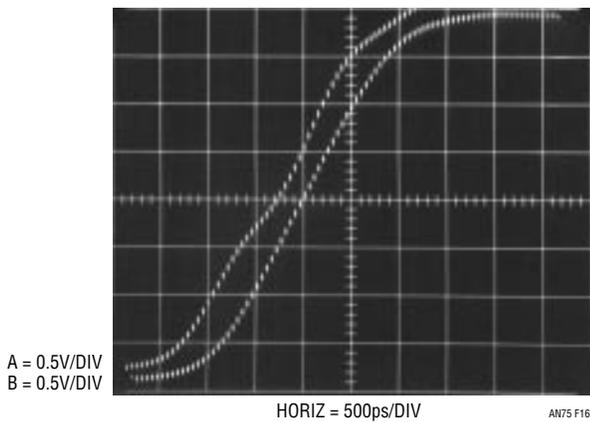A = 0.5V/DIV
B = 0.5V/DIV

HORIZ = 500ps/DIV   AN75 F16

Figure 16. 300ps AND Gate Delay Measured from Comparator Output (A) to Q1 Emitter (B). Fall Time Delay Is Similar. Sampling Oscilloscope Display Presents as a Series of Dots

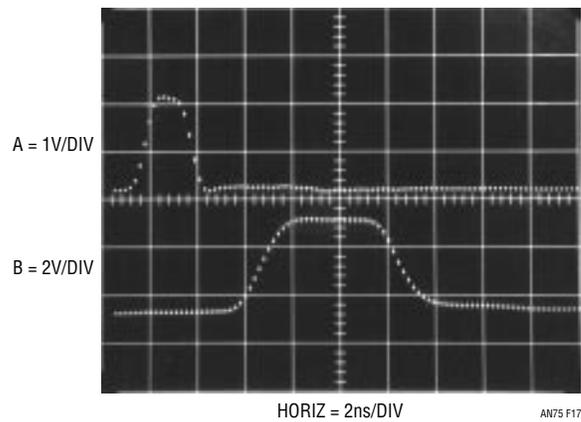A = 1V/DIV

B = 2V/DIV

HORIZ = 2ns/DIV   AN75 F17

Figure 17. Output (B) Recognizing a 3ns Coincident Pulse (A) at Inputs. Response Is Clean, with Decision Delay of 4.5ns. Segmented Display Is Characteristic of Sampling 'Scope Operation
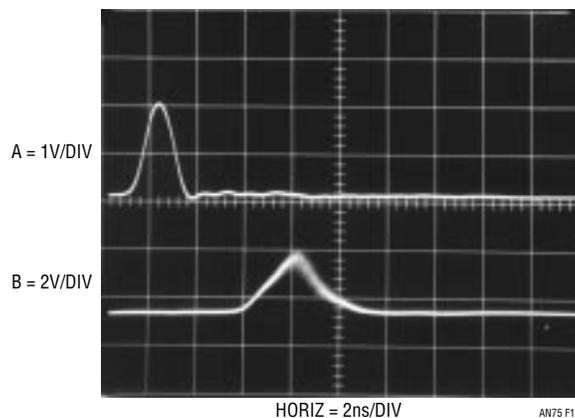

A = 1V/DIV

B = 2V/DIV

HORIZ = 2ns/DIV   AN75 F18

Figure 18. An Unrecognized Coincidence. Output (B) Cannot Fully Respond to ≈2.5ns Coincident Pulse (A). Additional 500ps of Coincidence Would Permit Valid Recognition (See Previous Figure)

15 Nanosecond Waveform Sampler

Figure 19 is another high speed circuit. This waveform sampler has 15ns response and a gain of 10. The circuit is made up of a fast, low parasitic switch, its drive components and an output amplifier. The switch is formed by the diode bridge. Borrowed from classical sampling oscilloscope circuitry, it is the key to circuit performance[7]. The diode bridge's inherent balance eliminates charge injection based errors in the output. It is far superior to other electronic switches in this characteristic. Any other high speed switch technology contributes excessive output spikes due to charge-based feedthrough. FET switches are not suitable because their gate-channel capacitance permits such feedthrough. This capacitance allows gate-drive artifacts to corrupt switch output. The diode bridge's balance, combined with matched, low capacitance monolithic diodes and complementary high speed switching, yields a cleanly switched output. Trims optimize switch performance. DC balance is achieved by trimming the bridge on-current for zero input-output offset voltage. Two AC trims are required. The "AC balance" corrects for diode and layout capacitive imbalances and the "skew compensation" corrects for any timing asymmetry in the nominally complementary bridge drive. These AC trims compensate small dynamic imbalances that could result in parasitic switch outputs.

Note 7: See references 14 and 15 for design details of diode bridge switches.
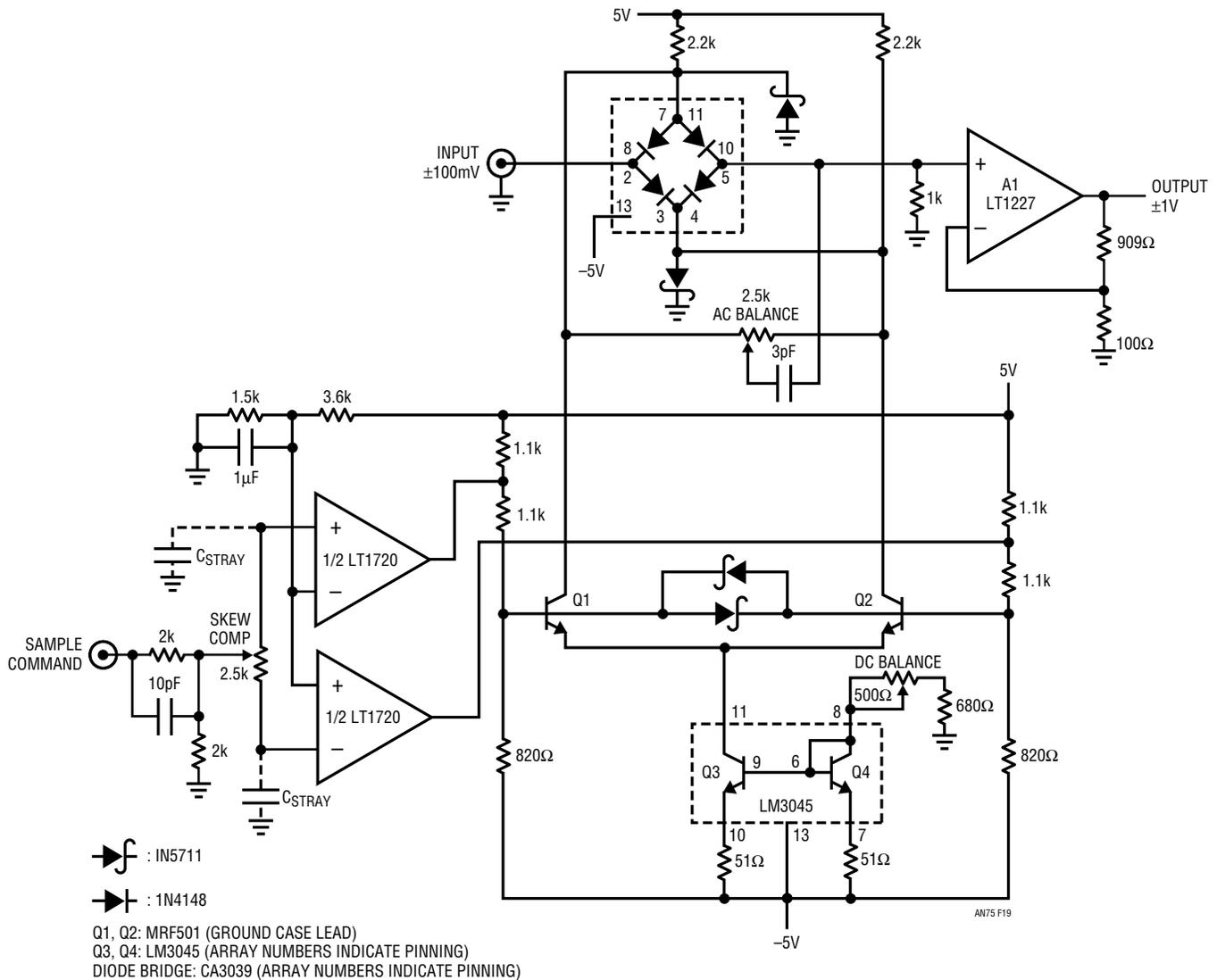

Figure 19. 15ns Waveform Sampler Utilizes Diode Bridge Switch and Wideband x10 Amplifier.
Comparators and Associated Components Provide Optimized Diode Bridge Switching

The sample command biases the LT1720 comparators, which furnishes complementary levels to the Q1–Q2 switch drivers. The "skew compensation" trim, working differentially against stray and device capacitance, provides a way to slightly time skew the comparators response. The comparator outputs bias current sink loaded Q1–Q2[8]. These devices provide level shifted drive to the bridge. Bridge output feeds A1, a wideband amplifier, operating at a gain of 10. Figure 20 presents waveforms. Trace A is the sample command, trace B and C complementary bridge drives at the Q1–Q2 collectors and trace D the output.

Figure 21, an amplitude and time expanded view, shows more detail. Trace assignments are identical, although scale factors are changed. A small delay occurs between the sample command (trace A) and the complementary bridge drives (traces B and C), although no drive time skewing is evident. Trace D, the output, responds cleanly, with some switch induced pre-shoot before falling.

Trimming is required to optimize sampler performance. DC balance is adjusted first. Ground the input and connect the sample command to the 5V supply. Monitor the output

and adjust the "DC balance" for 0V. The AC trims are made dynamically. Connect the input to a *well bypassed* 50mV DC source and drive the sample command with a 1MHz square wave. A typical pre-trim sampler output appears in Figure 22. The pre-shoot (waveform bottom) is due to poor AC balance. The mid-transition discontinuity is characteristic of untrimmed skew compensation. In general, poor AC balance shows up as pronounced pre or post transition events, while unadjusted skew compensation causes distortion during the transition. When properly trimmed, circuit output should be devoid of all such behavior. Figure 23 shows this; only very slight disturbances (probably due to residual AC imbalance) are visible.

Pertinent performance specifications include 100μV/$^\circ$C drift, 15ns delay time, 10MHz full-power bandwidth and a minimum sample window for full-power response of 30ns.

Note 8: The bridge drive scheme presented here is variant of a circuit developed by George Feliz (LTC). See LTC Application Note 74, "Component and Measurement Advances Ensure 16-Bit DAC Settling Time."
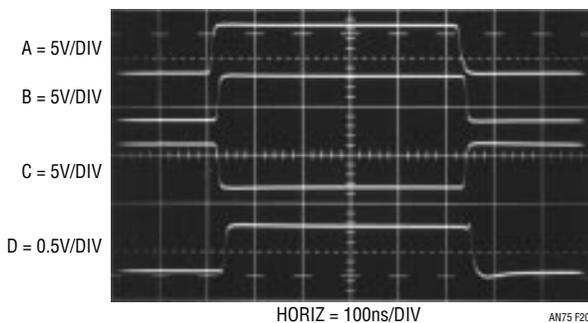

Figure 20. Sampler Operation at 50mV Input. Trace A Is Sample Command, B and C Complementary Bridge Drives. Trace D Is Output
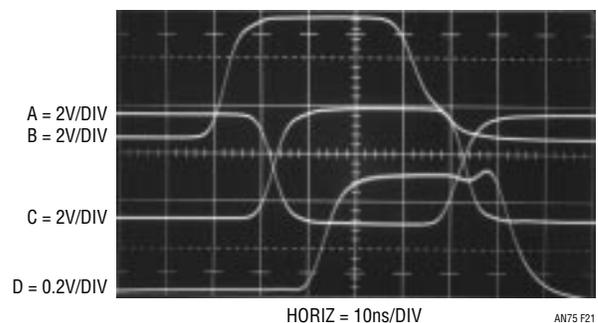

Figure 21. Highly Expanded View of Figure 20 Has Same Trace Assignments. Bridge Switching Appears Unskewed and Output Responds Cleanly
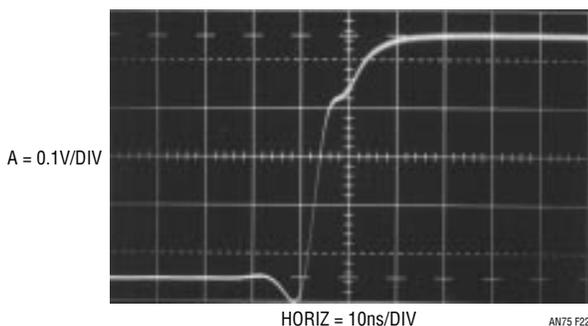

Figure 22. Sampler Output Before Trimming. Aberration at Bottom Is Due to Misadjusted AC Balance. Mid-Transition Discontinuity Derives from Untrimmed Skew Compensation
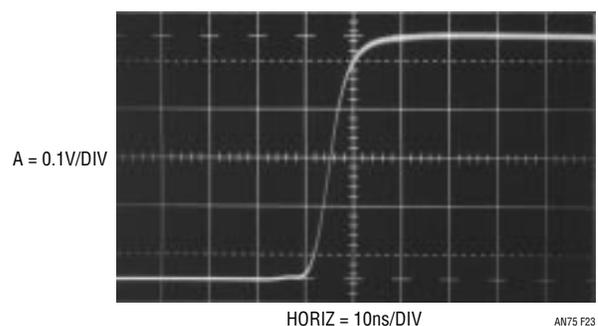

Figure 23. Sampler Output After Optimizing AC Balance and Skew Compensation

5.5μA Powered, 0.05μV/°C Chopped Amplifier

Figure 24 shows a chopped amplifier that requires only 5.5μA supply current. Offset voltage is 5μV, with 0.05μV/°C drift. A gain of 10^8 affords high accuracy, even at large closed-loop gains.

The micropower comparators form a biphase 5Hz clock. The clock drives the input related switches, causing an amplitude-modulated version of the DC input to appear at A1A's input. AC-coupled A1A takes a gain of 1000, presenting its output to a switched demodulator similar to the aforementioned modulator.

The demodulator output, a reconstructed, DC-amplified version of the circuit's input, is fed to A1B, a DC gain stage. A1B's output is fed back, via gain setting resistors, to the input modulator, closing a feedback loop around the entire amplifier. The configuration's DC gain is set by the feedback resistor's ratio, in this case 1000.

The circuit's internal AC coupling prevents A1's DC characteristics from influencing overall DC performance, accounting for the extremely low offset uncertainty noted. The high open-loop gain permits 10ppm gain accuracy at a closed-loop gain of 1000.

The desired micropower operation and A1's bandwidth dictate the 5Hz clock rate. As such, resultant overall bandwidth is *low*. Full-power bandwidth is 0.05Hz with a slew rate of about 1V/s. Clock-related noise, about 5μV, can be reduced by increasing C_{COMP}, with commensurate bandwidth reduction.
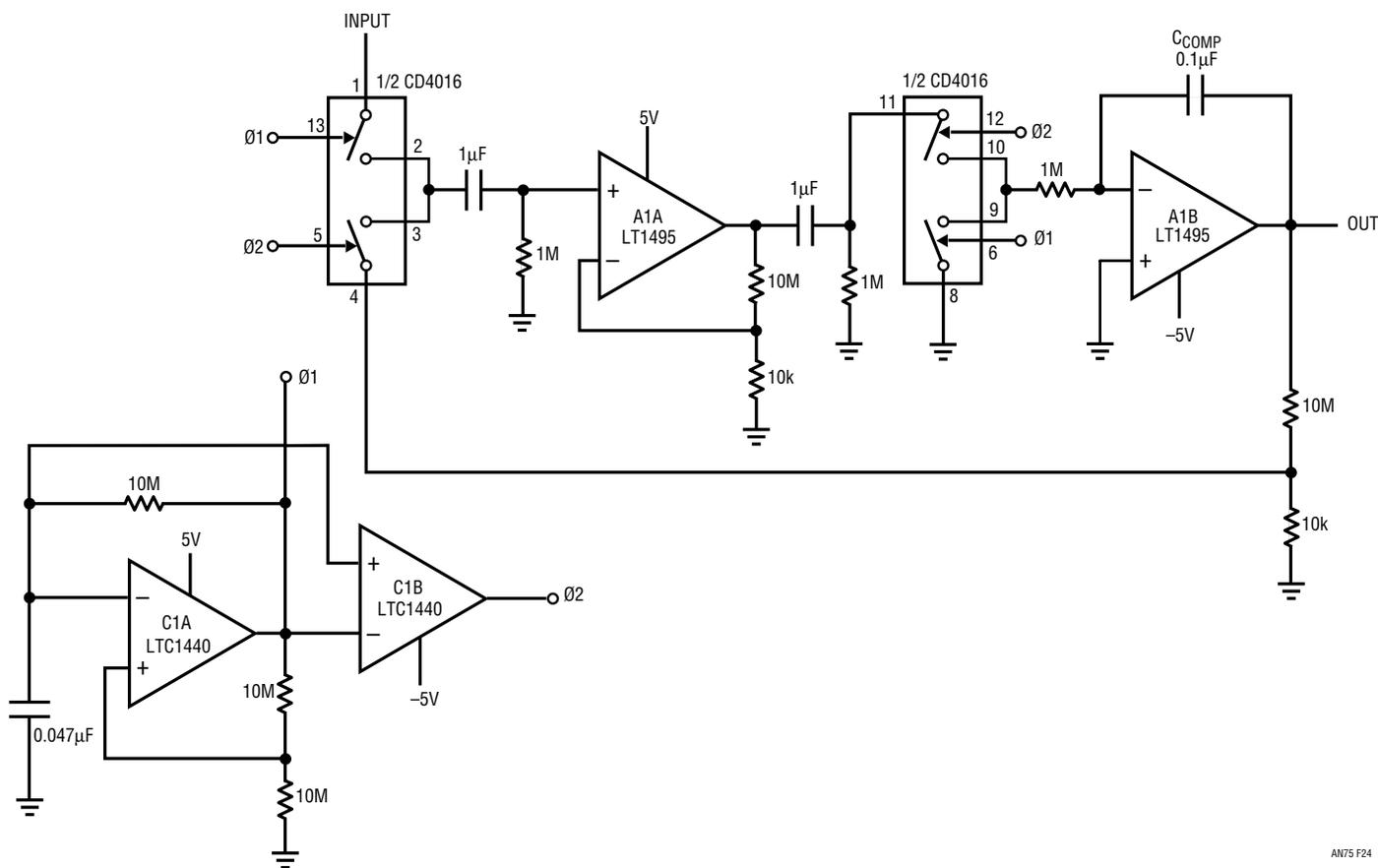

Figure 24. 0.05μV/°C Chopped Amplifier Consumes Only 5.5μA Supply Current

Pilot Light Flame Detector with Low-Battery Lockout

Figure 25 shows a pilot light flame detector with low-battery lockout. The amplifier ("A"), running open loop, compares a small portion of the reference with the thermocouple-generated voltage. When the thermocouple is hot, the amplifier's output swings high, biasing Q1 on. Hysteresis, provided by the 10M resistor, ensures clean transitions, while the diodes clamp static generated voltages to the rails. The 100k–2.2μF RC filters the signal to the amplifier.

The comparator ("C") monitors the battery voltage via the 2M–1M divider and compares it to the 1.2V reference. A battery voltage above 3.6V holds C's output high, biasing Q2 on and maintaining the small potential at A's negative input. When the battery voltage drops too low, C goes low, signaling a low-battery condition. Simultaneously, Q2 goes off, causing A's negative input to move to 1.2V. This biases A low, shutting off Q1. The low outputs alert downstream circuitry to shut down gas flow.
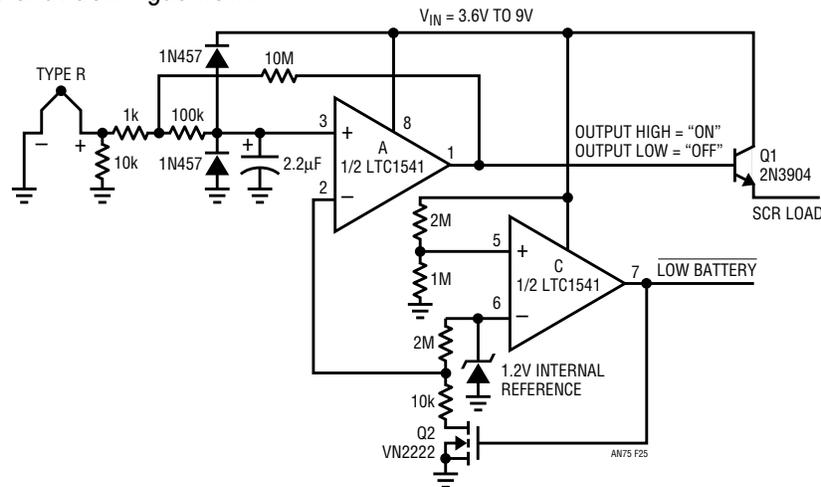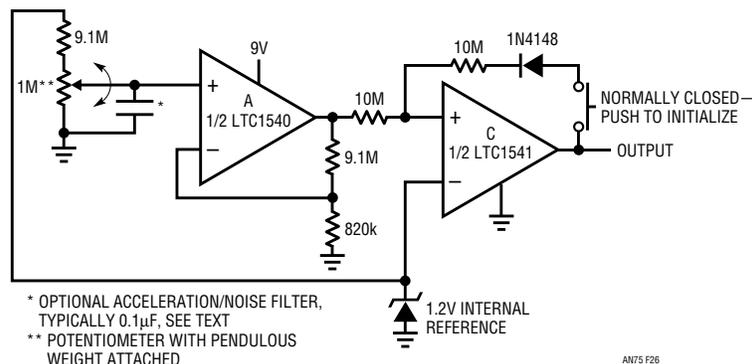
Tip-Acceleration Detector for Shipping Containers

Figure 26's circuit is a tip-acceleration detector for shipping containers. It detects if a shipping container has been subjected to excessive tipping or acceleration and retains the detected output. The sensitivity and frequency response are adjustable. A potentiometer with a small pendulous mass biases the amplifier ("A"), operating at a gain of 12. Normally, A's output is below C's trip point and circuit output is low. Any tip-acceleration event that causes A's output to swing beyond 1.2V will trip C high. Positive feedback around C will latch it in this high state, alerting the receiving party that the shipped goods have been mishandled. Sensitivity is variable with potentiometer mechanical or electrical biasing or A's gain. Bandwidth is settable by selection of the capacitor at A's input. The circuit is prepared for use by applying power and pushing the button in C's output.

Figure 25. Pilot Light Flame Detector with Low-Battery Lockout

Figure 26. Tip-Acceleration Detector for Shipping Containers Retains Output If Triggered. Sensitivity Is Adjustable Via Amplifier Feedback Values. Capacitor Sets Acceleration Response Bandwidth

32.768kHz "Watch Crystal" Oscillator

Figure 27's quartz oscillator, using a standard 32.768kHz "watch crystal," starts under all conditions with no spurious modes. Current draw is only 9μA at a 2V supply.

The circuit is best understood by initially ignoring the crystal. Resistors at the positive input establish a DC bias point. The 1.2M–10pF path sets up phase shifted negative feedback and the circuit looks like a marginally stable unity gain follower at DC. When the crystal is realized, positive feedback occurs and oscillation commences at the crystal's resonant frequency.

Power consumption is low. The LTC1441's output stage design eliminates "totem" currents, maintaining low drain even as supply increases. Figure 28's plot shows 9μA drain at 2V supply, increasing linearly to 18μA at 5V supply. Current drain is reducible by altering component values, but erratic crystal start-up or parasitic modes may result. This is particularly the case if various brands of crystal are employed. The values given represent a compromise between minimized current drain and assured operation.
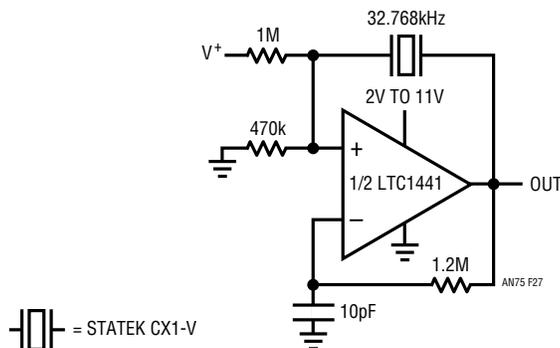

Figure 27. 32.768kHz "Watch Crystal" Oscillator Has No Spurious Modes. Circuit Pulls 9μA at V$_S$ = 2V
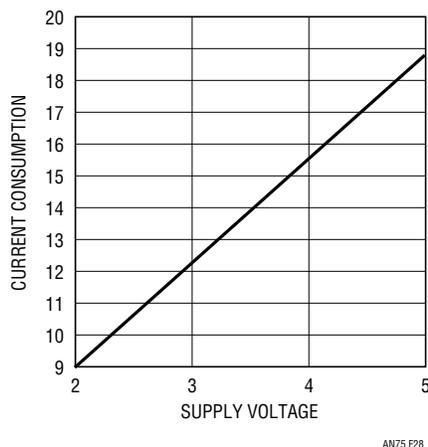

Figure 28. Current Consumption vs Supply Voltage for the 32.768kHz Crystal Oscillator. Characteristic Is Essentially Linear

Complementary Output, 50% Duty Cycle Crystal Oscillator

Figure 29's circuit, developed jointly by Joe Petrofsky (LTC) and the author, uses the LT1720 dual comparator in a 50% duty cycle crystal oscillator. Output frequencies to 10MHz are practical.

Resistors at C1's positive input set a DC bias point. The 2k–0.068µF path furnishes phase-shifted feedback and C1 acts like a wideband, unity-gain follower at DC. The crystal's path provides resonant positive feedback and stable oscillation occurs. C2, sensing C1's input, provides a delay matched, low skew, complementary output. A1 compares band limited versions of the outputs and biases C1's negative input.

Because frequency is fixed, C1's only degree of freedom to respond is variation of pulse width; hence, the outputs are forced to 50% duty cycle.

The circuit operates with AT-cut fundamental crystals from 1MHz to 10MHz, over a 2.7V to 6V power supply range. All biasing is supply derived, and hence ratiometric. As such, 50% duty cycle is maintained at all supply voltages, with output skew below 800ps. Figure 30 plots skew, which is seen to vary by about 800ps over a 2.7V to 6V supply excursion.

It is noteworthy that any desired duty cycle may be obtained by summing current into either of A1's inputs. If this is done, the current should derive directly from the supply or supply rejection will be compromised.
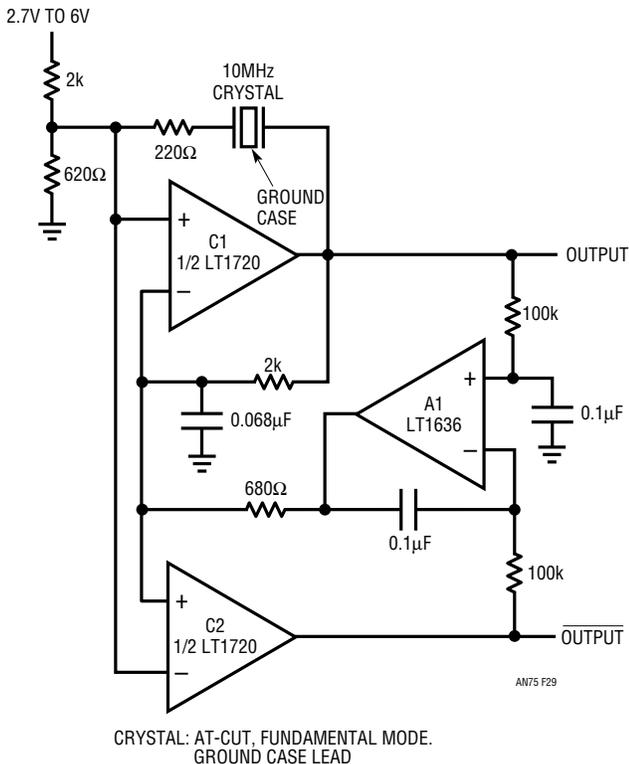

Figure 29. Crystal Oscillator Has Complementary Outputs and 50% Duty Cycle. A1's Feedback Maintains Output Duty Cycle Despite Supply Variations
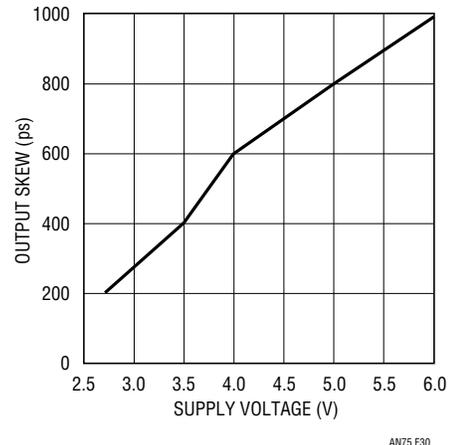

Figure 30. Output Skew vs Supply for 10MHz Clock. Skew Varies Only 800ps Over 2.7V to 6V Supply Excursion

Nonoverlapping, Complementary Output Crystal Oscillator

Figure 31, an extension of the previous design, generates a nonoverlapping, complementary output crystal clock. The circuit is essentially identical to Figure 29, with the exception that C2 receives attenuated bias. This causes the outputs to have a nonoverlapping characteristic. Under these conditions, the only way A1 can balance its inputs is if the circuit outputs have identical output duty. The nonoverlapping operation is verified in Figure 32, which shows the circuit's output. The outputs transition crisply, with no detectable overlap. This circuit shares the previous version's supply immunity due to ratiometric biasing. If the A1 network is deleted output duty will be unequal, but nonoverlapping operation retained.
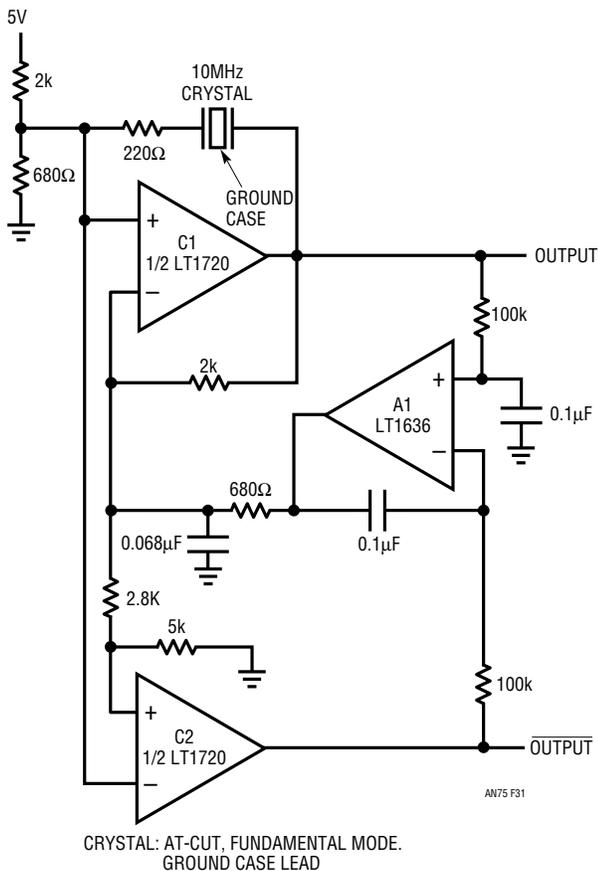

A = 5V/DIV

B = 5V/DIV

HORIZ = 10ns/DIV   AN75 F23

Figure 32. Nonoverlap Characteristic Verified in a 275MHz Bandpass

CRYSTAL: AT-CUT, FUNDAMENTAL MODE.
GROUND CASE LEAD

Figure 31. Rearranging Figure 29's Comparator Biasing Provides Nonoverlapping Complementary Outputs

High Power CCFL Backlight Inverter for Desktop Displays

Large LCD (liquid crystal display) displays designed to replace CRTs (cathode ray tubes) in desktop computer applications are becoming available. The LCD's reduced size and power requirements allow much smaller product size, a highly desirable feature.

CRT replacement requires a 10W to 20W inverter to drive the CCFL (cold cathode fluorescent lamp) that illuminates the LCD. Additionally, the inverter must provide the wide dimming range associated with CRTs, and it must have safety features to prevent catastrophic failures.

Figure 33's circuit meets these requirements. It is a modified, high power variant of an approach employed in laptop computer displays[9]. T1, Q1, Q2 and associated components form a current fed, resonant Royer converter that produces high voltage at T1's secondary. Current flows through the CCFL tubes and is summed, rectified and filtered, providing a feedback signal to the LT1371 switching regulator. The LT1371 delivers switched mode power to the L1–D1 node, closing a control loop around the Royer converter. The 182Ω resistor provides current-to-voltage conversion, setting the lamp current operating
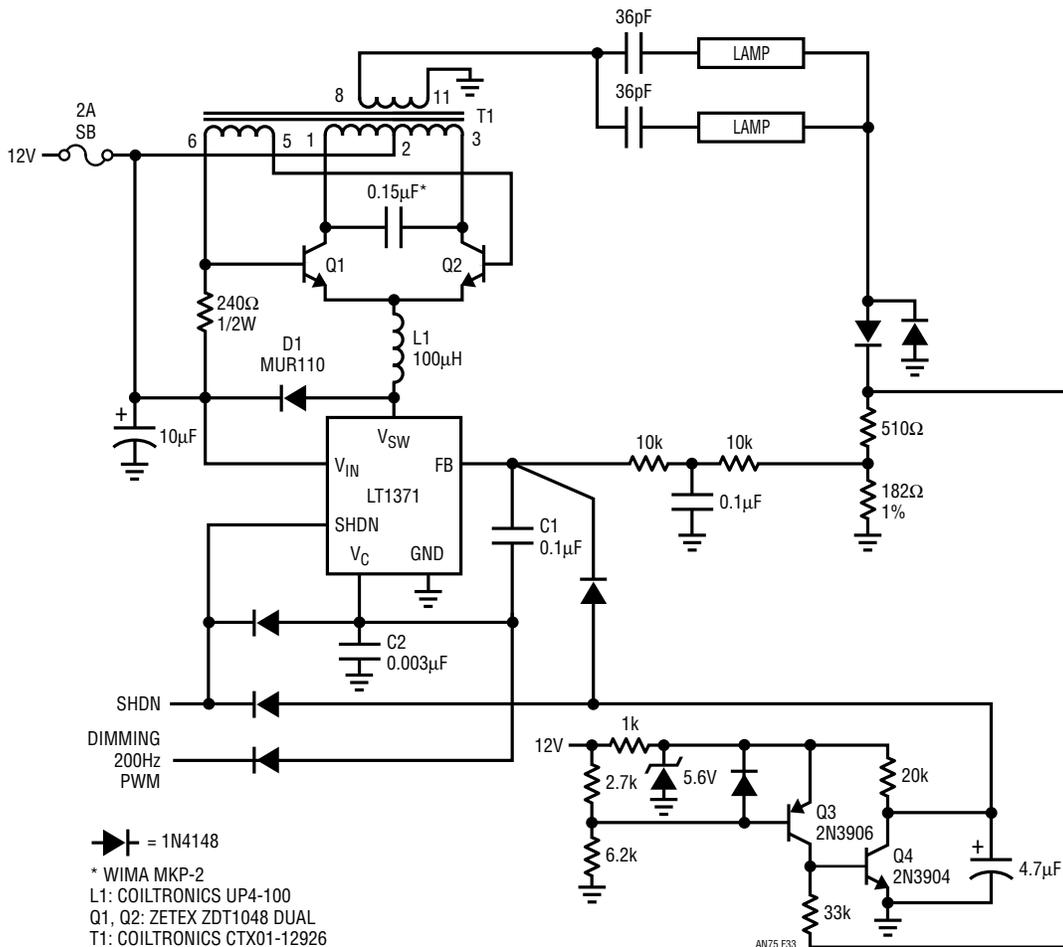
Note 9: See reference 21.

Figure 33. 12W CCFL Backlight Inverter for Desktop Displays Provides Wide Range Dimming and Safety Features

point. The loop stabilizes lamp current against variations in time, supply, temperature and lamp characteristics. The LT1371's frequency compensation is set by C1 and C2. The compensation responds quickly enough to permit the 200Hz PWM input to control dimming over a 30:1 range with no degradation in loop regulation. Applicable waveforms appear in Figure 34.

Q3 and Q4 shut down the circuit if lamp current ceases (open or shorted lamps or leads, T1 failure or similar malfunction). Normally, Q4's collector is held near ground by the lamp-current-derived base biasing. If lamp current ceases, Q4's collector voltage increases, overdriving the feedback node and shutting down the circuit. Q3 prevents unwanted shutdown during power supply turn-on by driving Q4's base until supply voltage is above about 7V.

Figure 35 shows the shutdown circuit reacting to the loss of lamp feedback. When lamp feedback ceases, the voltage across the 182Ω current sense resistor drops to zero (visible between Figure 35's third and fourth vertical graticule lines, trace A). The LT1371 responds to this open-loop condition by driving the Royer converter to full power (Q1's collector is trace B). Simultaneously, Q4's collector (trace C) ramps up, overdriving the LT1371's feedback node in about 50ms. The LT1371 stops switching, shutting off the Royer converter drive. The circuit remains in this state until the failure has been rectified.

This circuit's combination of features provides a safe, simple and reliable high power CCFL lamp drive. Efficiency is in the 85% to 90% range. The closed-loop operation ensures maximum lamp life while permitting extended dimming range. The safety feature prevents excessive heating in the event of malfunction and the use of off-the-shelf components allows ease of implementation.

Ultralow Noise Power Converters[10]

Today's circuit designer is often challenged to assemble a high performance system by combining sensitive analog electronics with potentially noisy power converters. Requirements for a small, efficient, cost effective solution are in conflict with acceptable noise performance—noisy switching regulators call for filtering, shielding and layout revisions that add bulk and expense. Most electromagnetic interference (EMI) problems associated with DC/DC converters are due to high speed switching of large currents and voltages. To maintain high efficiency, these switch transitions are designed to occur as quickly as possible. The result is input and output ripple that contains very high harmonics of the switching frequency. These fast edges also couple through stray magnetic and electric fields to nearby signal lines, making efforts to filter the supply lines ineffective.

The LT1534 ultralow noise switching regulator provides an effective and flexible solution to this problem. Using two external resistors, the user can program the slew rates of the current through the internal 2A power switch and the voltage on it. Noise performance can be evaluated and improved with the circuit operating in the final system. The system designer need sacrifice only as much efficiency as is necessary to meet the required noise performance. With the controlled slew rates, system performance is less sensitive to layout, and shielding requirements can be greatly reduced; expensive layout and mechanical revisions can be avoided.

Note 10: Figures 36 to 39 and all associated text are authored by Jeff Witt of LTC. Their original presentation is annotated in reference 22.

A = 5V/DIV
B = 50mA/DIV
C = 0.5V/DIV
(0.4V/DC LEVEL)
D = 0.5V/DIV
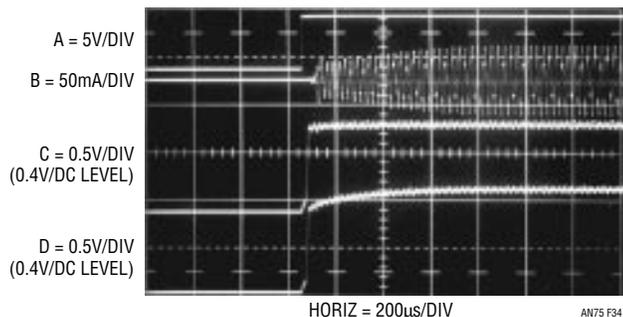(0.4V/DC LEVEL)
HORIZ = 200μs/DIV
AN75 F34

Figure 34. Fast Loop Response Maintains Regulation at 200Hz PWM Rate. Waveforms Include PWM Command (A), Lamp Current (B), LT1371 Feedback (C) and Error Amplifier V_C (D) Pins. Loop Settling Occurs in 500μs

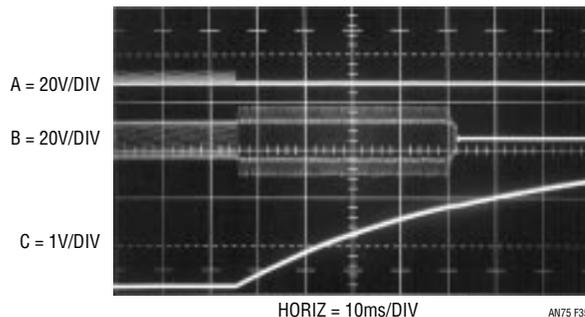A = 20V/DIV
B = 20V/DIV
C = 1V/DIV
HORIZ = 10ms/DIV
AN75 F35

Figure 35. Safety Feature Reacts to Lamp Feedback Loss by Shutting Down Power. Lamp Current Dropout (A) Allows Monitoring Circuit to Ramp Up (C), Shutting Off Drive (B)

The LT1534's internal oscillator can be programmed over a broad frequency range (20kHz to 250kHz) with good initial accuracy. It can also be synchronized to an external signal placing the switching frequency and its harmonics away from sensitive system frequencies.

Low Noise Boost Regulator

In Figure 36, the LT1534 boosts 3.3V to supply 650mA at 5V with its oscillator synchronized to an external 50kHz clock. The circuit relies on the low ESR of capacitor C2 to keep the output ripple low at the fundamental frequency; slew rate control reduces the high frequency ripple. Figure 37 shows waveforms of the circuit as it delivers 500mA. The top trace shows the voltage on the collector of the internal bipolar power switch (the COL pins), and the middle trace shows the switch current. The lowest trace is

the output ripple. The slew rates are programmed to their fastest here, resulting in good efficiency (83%), but also generating excessive high frequency ripple. Figure 38 shows the same waveforms with the slew rates reduced. The large high frequency transients have been eliminated.

Low Noise Bipolar Supply

Many high performance analog systems require quiet bipolar supplies. This circuit (Figure 39) will generate ±5V from a wide input range of 3V to 12V, with a total output power of 1.5W. By using a 1:1:1 transformer, the primary and secondary windings can be coupled using capacitors C2 and C3, allowing the LT1534 to control the switch transitions at the output rectifiers as well as at the switch collector. Secondary damping networks are not required.
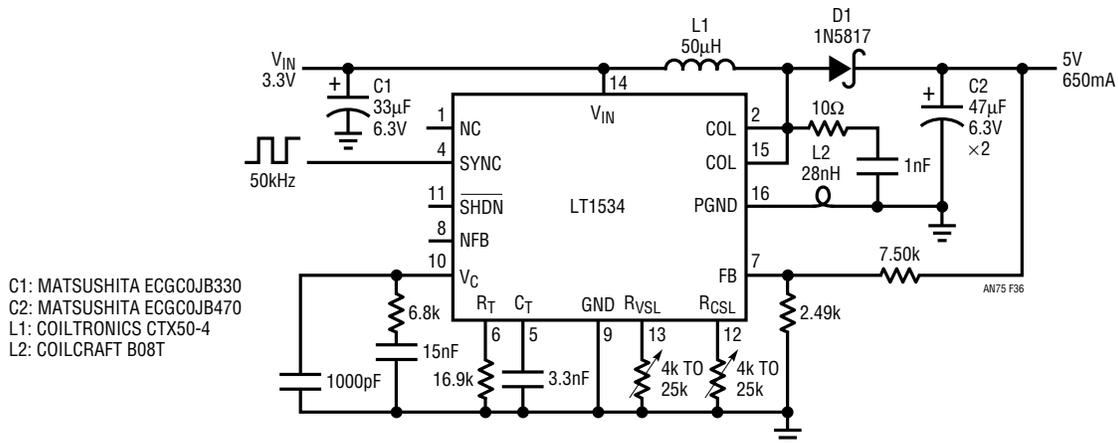

Figure 36. The LT1534 Boosts 3.3V to 5V. The Resistors On the R_{VSL} and R_{CSL} Pins Program the Slew Rates of the Voltage On the Power Switch (COL Pins) and the Current Through It
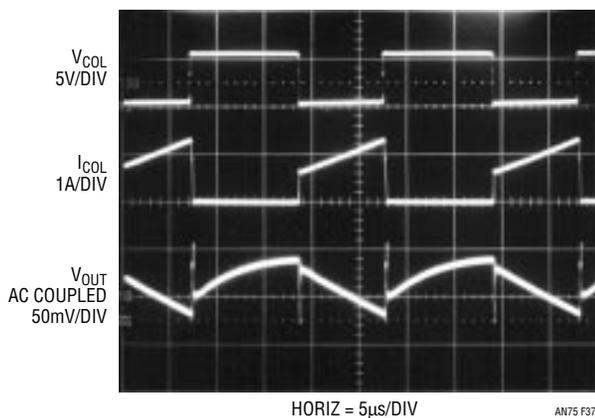

Figure 37. High Slew Rates (R_{CSL} = R_{VSL} = 4k) Result in Good Efficiency But Excess High Frequency Ripple
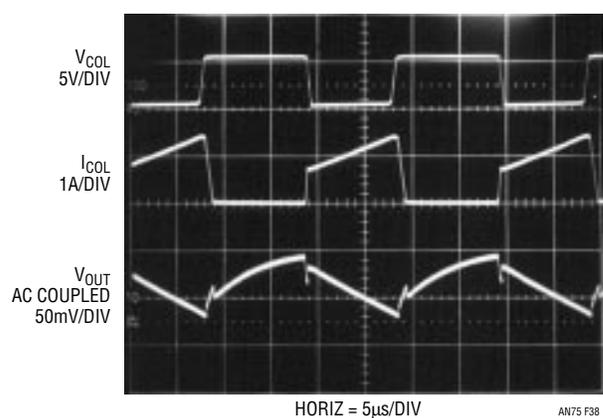

Figure 38. Low Slew Rates (R_{CSL} = R_{VSL} = 24k) Result in an Output Without Troublesome High Frequency Transients
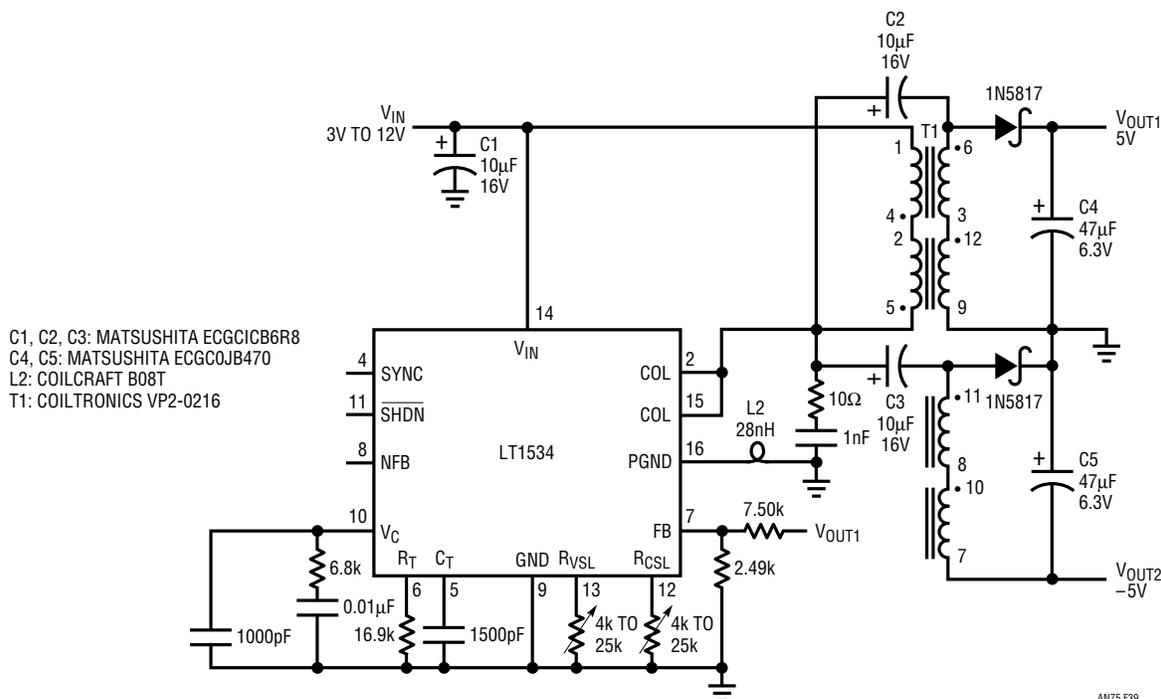
Figure 39. A Low Noise, Wide Input Range ±5V Supply

Ultralow Noise Off-Line Power Supply

Off-line power supplies require input filtering components to meet FCC emission requirements. Additionally, board layout is usually quite critical, requiring considerable experimentation even for experienced off-line supply designers. These considerations derive from the wideband harmonic energy generated by the fast switching of traditional off-line supplies. A new device, the LT1533 low noise switching regulator, eliminates these issues by continuous, closed-loop control of voltage and current switching times.[11] Additionally, the device's push-pull output drive eliminates the flyback interval of conventional approaches. This further reduces harmonics and smoothes input current drain characteristics. Although intended for DC/DC conversion, the LT1533 adapts nicely to off-line service, while eliminating emission, filtering, layout and noise concerns.

Figure 40 shows the supply. Q5 and Q6 drive T1, with a rectifier-filter, the LT1431 and the optocoupler closing an isolated loop back to the LT1533. The LT1533 drives Q5 and Q6 in cascode fashion to achieve high voltage switching capability. It also continuously controls their current and voltage switching times, using the resistors at the I_{SLEW} and V_{SLEW} pins to set transition rates. FET current

information is directly available, although FET voltage status is derived via the 360k–10k dividers and routed to the gates via the NPN-PNP followers. The source wave shapes, and hence the voltage slewing information at the LT1533 collector terminals, are nearly identical in shape to the drain waveforms.

Q1, Q2 and associated components provide a bootstrapped bias supply, with start-up transistor Q1 turning off once T1 begins supplying power to Q2. The resistor string at Q2's emitter furnishes various "housekeeping" bias potentials. The LT1533's internal 1A current limit is too high for effective overcurrent protection. Instead, current is sensed via the 0.8Ω shunt at the LT1533's emitter pin (E). C1, monitoring this point, goes low when current limit is exceeded. This pulls the V_C pin low and also accelerates voltage slew rate, resulting in fast limiting while minimizing instantaneous FET stress. Prolonged short-circuit conditions result in C2 going low, putting the circuit into shutdown. Once this occurs, the C1–C2 loop oscillates in a controlled manner, sampling current for about a millisecond every second or so. This action forms a power limit, preventing FET heating and eliminating heat sink requirements.

Note 11: In depth coverage of this device, its use and performance verification appears in reference 23.

Figure 40. 10W Off-Line Power Supply Passes FCC Emission Requirements Without Filter Components

L1: COILTRONICS UP-4
L2: COILCRAFT B07T
NPN: 2N3904 UNLESS OTHERWISE NOTED
PNP: 2N3906
T1: COILTRONICS CTX02-13978-X3

→ƒ : 20CJQ045(I.R.) UNLESS OTHERWISE NOTED
→ : 1N4148

: AC(HOT) RETURN
: OUTPUT COMMON

Figure 41 shows waveforms for the power supply. Trace A is one FET source; traces B and C are its gate and drain waveforms, respectively. FET current is trace D. The cascoded drive maintains waveshape fidelity, even as the LT1533 tightly regulates voltage and current transition rates. The wideband harmonic activity typical of off-line supply waveforms is entirely absent. Power delivery to T1 (center screen, trace C) is particularly noteworthy. The waveshapes are smoothly controlled, and no high frequency content is observable. Figure 42 increases sweep speed by a factor of 5, but high frequency components are still undetectable. Figure 43 shows supply input monitored with a wideband current probe at the "HV" node. The current drain profile is smooth, with complete absence of high frequency content.
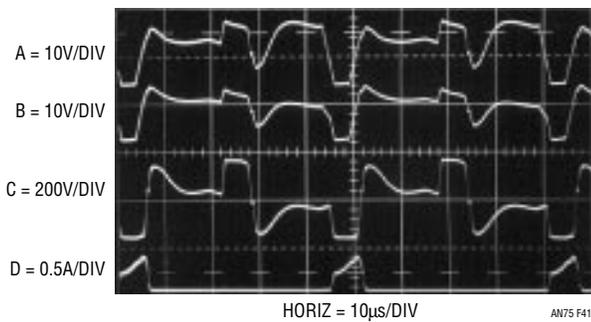

Figure 41. Waveforms for One of the Power Supplies' FETs Show No Wideband Harmonic Activity. LT1533 Provides Continuous Control of Voltage and Current Slewing. Result Is Smoothly Controlled Waveshapes for FET Source (A), Gate (B) and Drain (C). FET Current is Trace D
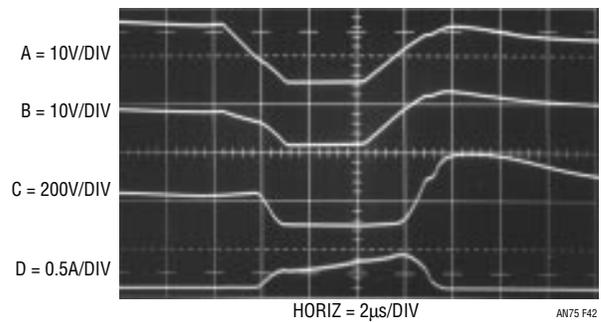

Figure 42. Time Expanded Version of Figure 41, with Same Trace Assignments. No Wideband Components Are Detectable
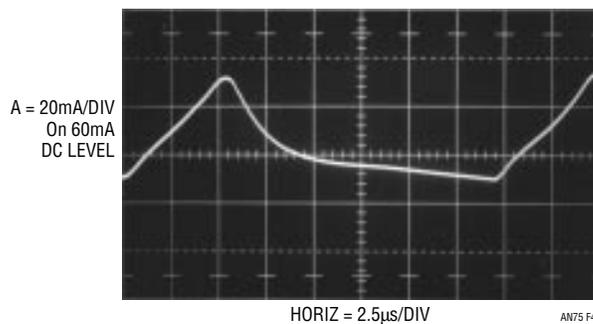

Figure 43. Circuit's Input Current Drain Profile Is Smooth, with No High Frequency Content

Figure 44, a 30MHz wide spectral plot, shows circuit emissions well below FCC requirements. This data was taken with no input filtering LC components and a nominally nonoptimal layout.

Output noise is composed of fundamental ripple residue, with essentially no wideband components. Typically, the low frequency ripple is below 50mV. If additional ripple attenuation is desired a 100µH–100µF LC section permits <100µV output noise. Figure 45 shows this in a 100MHz bandpass. Ripple and noise are so low that the oscilloscope requires a 40dB low noise preamplifier to even register a display (see Note 11).
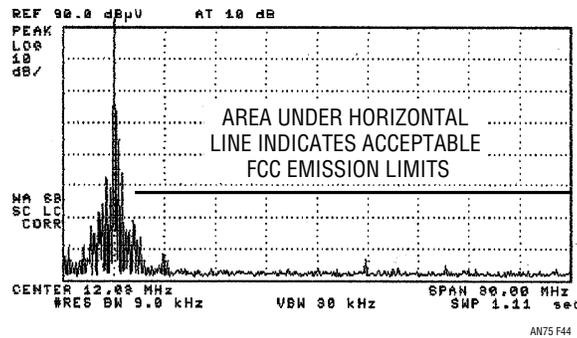

Figure 44. 30MHz Wide Spectral Plot Shows Circuit Emissions Well Below FCC Requirements Despite Lack of Conventional Filter Components
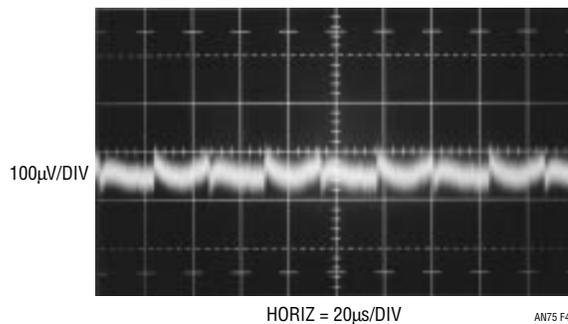

HORIZ = 20µs/DIV

Figure 45. Power Supply Output Noise Below 100µV (100MHz Measurement Bandwidth) Is Obtainable Using Additional Output LC Section. Without LC Section Wideband Harmonic Is Still Absent, Although Fundamental Ripple Is 50mV

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24. Hunt, F. V., and Hickman, R. W., "On Electronic Voltage Stabilizers," "Cascode," Review of Scientific Instruments, January 1939, pp. 6–21, p. 16.[12]

25. Williams, J., "High Speed Amplifier Techniques," Linear Technology Corporation, Application Note 47, 1991, pp. 96–97.

Note 12: Veterans of LTC Application Notes, a weary brigade, may recognize this reference as the object of Application Note 70's (Footnote 14) champagne prize offer. The mystery solved, the messenger was compensated as specified (Veuve Clicquot Ponsardin).

APPENDIX A

SOME GUIDELINES FOR MICROPOWER DESIGN AND AN EXAMPLE

As with all engineering, micropower circuitry requires attention to detail, awareness of trade-offs and an opportunistic bent towards achieving the design goal.

The most obvious way to save power is to choose components which require little energy. Additional savings require more effort.

Circuits should be examined in terms of current flow. Consider such flow in all DC and AC paths. For example, do DC base currents go where they can do some useful work, or are they thrown away? Try to keep AC signal swings down, particularly if capacitors (parasitic or intended) must be continually charged and discharged. Examine the circuit for areas where power strobing may be allowable.

Consider quiescent vs dynamic power requirements of components to avoid unpleasant surprises. Data sheets usually specify quiescent power because the manufacturer doesn't know what the user's circuit conditions are. For example, everyone "knows" that "MOS devices draw no current." Unfortunately, Mother Nature dictates that as frequency and signal swings go up, the capacitances associated with MOS devices begin to require more power. It is often a mistake to automatically associate low power operation with a process technology. While it's likely that CMOS will provide lower power operation for a given function than 12AX7s, a bipolar approach may be even better. Consider individual situations on the basis of their specific requirements before committing to a technology. Very often, circuits require several technologies (i.e., CMOS, bipolar and discrete) for best results.

Usually, achieving low power operation requires performance trade-offs. Minimizing signal swings and current saves power, but moves circuit operation closer to the noise floor. Offsets, drift, bias currents and noise become increasingly significant error factors as signal amplitudes are constricted to save power. This is a fundamental trade-off and must be carefully considered. Circuits employing power strobing can sometimes get around this problem by utilizing low duty cycles.

Text Figures 1 and 4, voltage-to-frequency converters, furnish an example of the evolution of a low power design. Design goals included a 10kHz maximum output, low drift, fast step response, linearity inside 0.05% and minimum supply current. Other specifications appear in the text.

Figure A1 shows an early (1986) version of this circuit. Operation is similar to the text described for Figure 1, but a brief description follows. When the input current-derived ramp at C1's negative input crosses zero, C1's output drops low, pulling charge through C1. This forces the negative input below zero. C2 provides positive feedback, allowing a complete discharge for C1. When C2 decays, C1A's output goes high, clamping at the level set by D1, D2 and V_{REF}. C1 receives charge and recycling occurs when C1A's negative input again arrives at zero. The frequency of this action is related to the input voltage. Diodes D3 and D4 provide steering, and are temperature compensated by D1 and D2. C1A's sink saturation voltage is uncompensated, but small. C1B is a start-up loop.

Although the LT1017 and LT1034 have low operating currents, this circuit pulls almost 400μA. The AC current paths include C1's charge-discharge cycle, and C2's branch. The DC path through D2 and V_{REF} is particularly costly. C1's charging must occur quickly enough for 10kHz operation, meaning the clamp seen by C1A's output must have low impedance at this frequency. C3 helps, but significant current still must come from somewhere to keep impedance low. C1A's current limited output cannot do the job unaided, and the resistor from the supply is required. Even if C1A could supply the necessary current, V_{REF}'s settling time would be an issue. Dropping C1's value will reduce impedance requirements proportionally, and would seem to solve the problem. Unfortunately, such reduction magnifies the effects of stray capacitance at the D3–D4 junction. It also mandates increasing R_{IN}'s value to keep scale factor constant. This lowers operating currents at C1A's negative input, making bias current and offset more significant error sources.

Figure A2 shows an initial attempt at dealing with these issues. This scheme is similar to Figure A1, except that Q1 and Q2 appear. V_{REF} receives switched bias via Q1, instead of being on all the time. Q2 provides the sink path for C1. These transistors invert C1A's output, so its input pin assignments are exchanged. R1 provides a light current from the supply, improving reference settling time. This

arrangement decreases supply current to about 300μA, a significant improvement. Several problems do exist, however. Q1's switched operation is really effective only at higher frequencies. In the lower ranges, C1A's output is low most of the time, biasing Q1 on and wasting power. Additionally, when C1A's output switches, Q1 and Q2 simultaneously conduct during the transition, effectively shunting R2 across the supply. Finally, the base currents of both transistors flow to ground and are lost. The basic temperature compensation is as before, except that Q2's saturation term replaces the comparator's.

Figure A3 is better. Q1 is gone, Q2 remains but Q3, Q4 and Q5 have been added. V_{REF} and its associated diodes are biased from R1. Q3, an emitter-follower, is used to source current to C1. Q4 temperature compensates Q3's V_{BE}, and Q5 switches Q3.

This method has some distinct advantages. The V_{REF} string can operate at greatly reduced current because of Q3's current gain. Also, Figure A2's simultaneous conduction problem is largely alleviated because Q5 and Q2 are switched at the same voltage threshold out of C1A. Q3's base and emitter currents are delivered to C1. Q5's currents are wasted, although they are much smaller than Q3's. Q2's small base current is also lost. The values for C2 and R3 have been changed. The time constant is the same, but some current reduction occurs due to R3's increase.

If C1 cannot be reduced, then its AC currents cannot be avoided. This leaves only the aforementioned Q5 and Q2 currents as significant wasted terms, along with R3's now smaller loss. Current drain for this circuit is about 200μA maximum.

Figure A4 (1987) is very similar, but eliminates Q5 and Q2's losses to get maximum operating current below 150μA with quiescent current under 80μA. The basic improvement is the use of CMOS inverters for reference switching—the inverters supply pin is driven by the reference buffer NPN and their paralleled outputs switch between V_{REF} and ground. Other enhancements provide better temperature compensation and improved power supply rejection. The modified LM334 driven reference stack begins to look very similar to Figure 1's arrangement. This circuit provided excellent precision—0.02% linearity, 40ppm/°C drift and 40ppm/V PSRR.

A variant (1991) of this circuit, Figure A5, reduced supply current to only 90μA maximum, by minimizing the number of CMOS inverters, eliminating their AC input currents. The charge dispensing capacitor was also reduced to 100pF, necessitating a larger input resistance value. The price for the current saving was degradation of drift and linearity by factors of 2 and 3, respectively.

Text Figures 1 and 4 (1997 and 1999, respectively) are direct extensions of the last two circuits. Their markedly decreased operating currents are obtained with minimal performance compromises by utilizing contemporary components. The LTC1440/LTC1441 comparators and the LT1389 reference are the heroes. Some other refinements are involved, but the text's voltage-to-frequency circuits are the final (for now) iteration of the five versions shown here.
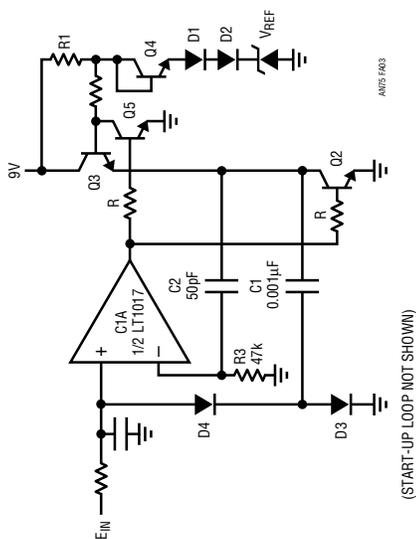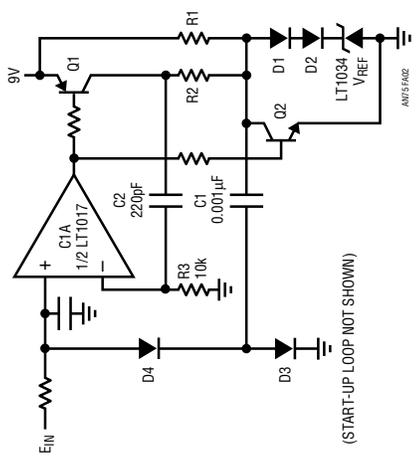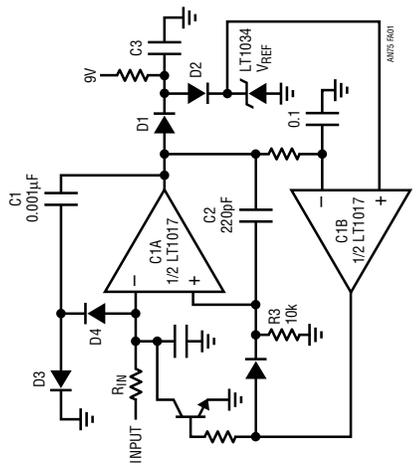
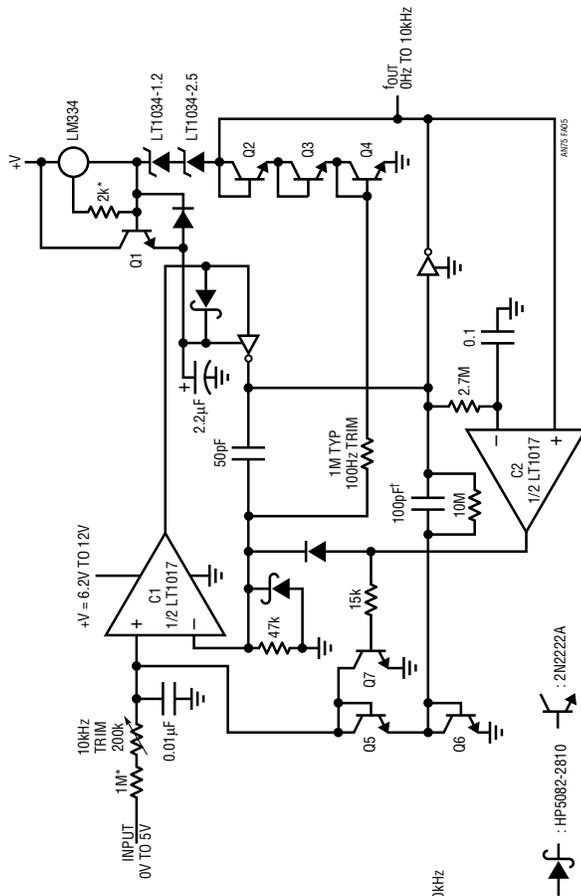**Figure A1**
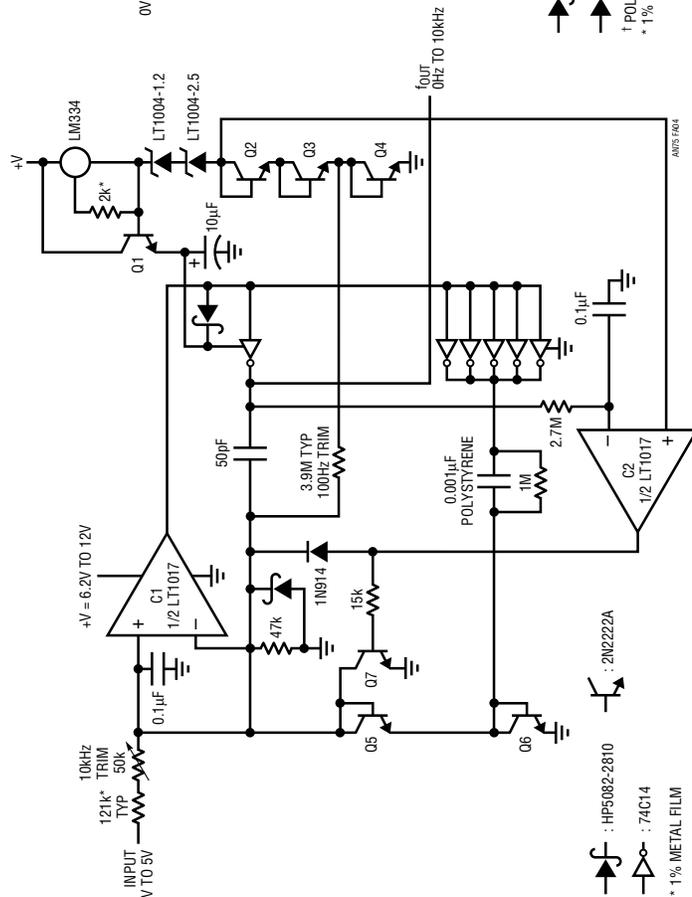
Figure A2

Figure A3

Figure A4

Figure A5

APPENDIX B

PARASITIC EFFECTS OF TEST EQUIPMENT ON MICROPOWER CIRCUITS

The energy absorbed by test equipment connections to micropower circuits can be significant. Under normal circumstances test equipment and probes have negligible power drain, but microampere level operating currents mandate care. Test instrumentation should be regarded as an integral part of the circuit. DC and AC loading and parasitic effects must be kept in mind to avoid unpleasant surprises. Such instrument connection errors can make the circuit under test look unfairly bad or good.

The DC resistance of oscilloscope probes varies from hundreds of ohms (1X types) to 10MΩ (10X), with some 10X types as low as 1MΩ. Contrary to some expectations, FET probes do not have high input resistance—some types are as low as 100kΩ, although most are about 10MΩ. The DC loading of a 10X 1M probe could introduce as much as 5μA of loss, almost 60% of Figure 4's total! The AC loading of a 10pF probe looking at Figure 27's 30kHz clock will cause apparent circuit consumption of 1μA, a significant loss in a low power circuit. 1X type probes present about 50pF of loading, with 1MΩ DC resistance when connected to the 'scope. This kind of probe loading can cause large errors in micropower circuits, while virtually disabling some. Such a probe, introduced at C1B's negative input in text Figure 6, would stop the circuit's oscillator. If placed across the supply of Figure 6 it would consume almost as much current as the circuit.

Probe AC and DC loading are not the only effects. Some DVMs produce "charge spitting" at their inputs. Such parasitic charge, introduced into high impedance nodes, can cause substantial errors. It's also worth remembering that DVM DC loading may change with range. Lower ranges may have very high input impedance, but higher ranges are typically 10MΩ. A 10MΩ DVM reading Figure 6's supply introduces almost 10% supply current error.

Figure B1 shows a way test equipment can make the circuit look too good, instead of too bad. If the pulse generator is adjusted more than a diode drop above the regulator's output, the bypass capacitor peak detects the charge delivered through the IC's internal diode. The regulator can't sink current, and with its output forced high it won't source anything. Under these conditions the circuit functions while the current meter reads zero…a very low power circuit indeed[1]!

Figure B2 shows a very simple, but useful circuit which greatly aids probe loading problems in micropower circuits. The LT1022 high speed FET op amp drives an LT1010 buffer. The LT1010's output allows DVM cable and probe driving and also biases the circuit's input shield. This bootstraps the input capacitance, reducing its effect. DC and AC errors of this circuit are low enough for almost all work, with enough bandwidth for just about any low power circuit. Built into a small enclosure with its own power supply, it can be used ahead of a 'scope or DVM with good results. Pertinent specifications appear in the diagram.

Figure B3 is a very fast high impedance probe for those occasions which require it. A1, a hybrid FET buffer, forms the electrical core of the probe. This device is a low input capacitance, wideband FET source follower driving a fast bipolar output stage. The input of the probe goes to this device via a 51Ω resistor, reducing the possibility of oscillations in the follower input stage when the probe sees low AC impedance. A1's output drives a guard shield around the probe's input line, reducing effective input capacitance to about 4pF. A ground referred shield encircles the guard shield, reducing pickup and making high quality ground connections to the circuit under test easy. Back-terminated A1 drives the output BNC cable, feeding a 50Ω termination at the oscilloscope. Specifications are noted in the figure. Note that the back termination mandates an attenuation of 2, while the buffer's open-loop architecture introduces a small gain error. The probe's physical construction is critical to achieving stated performance. See reference 25 for details.

Note 1: Practically speaking, most regulators and power supplies can sink small amounts of current. Because of this, the current meter may actually read negative.
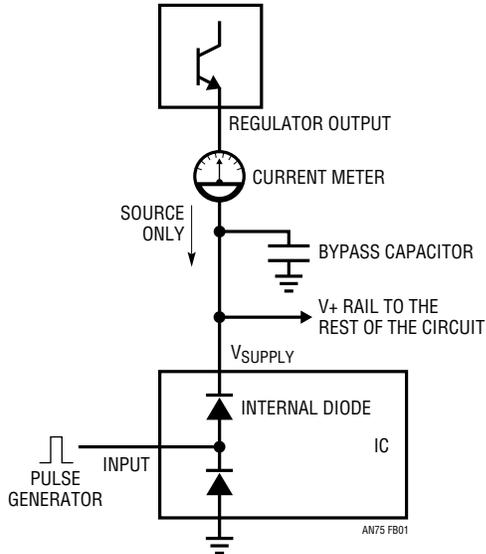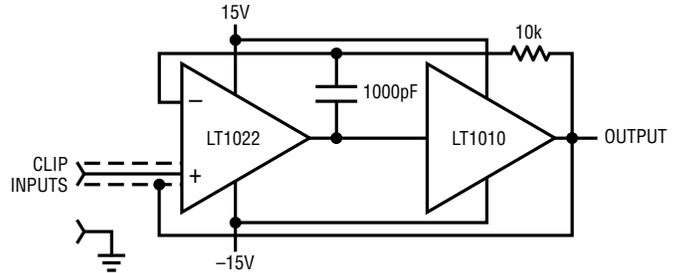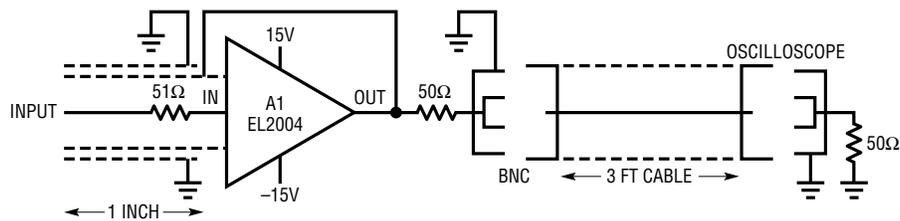
Figure B1. **Parasitic Currents Flowing Into Circuit From Pulse Generator Produce Misleading Current Meter Indications**

A = 1
INPUT CAPACITANCE ≈ 8pF
I_B = 50pA
GBW = 8.5MHz
SLEW = 23V/μs
E_{OS} = 250μV
$E_{OS}\Delta TC$ = 5μV/°C

AN75 FB02

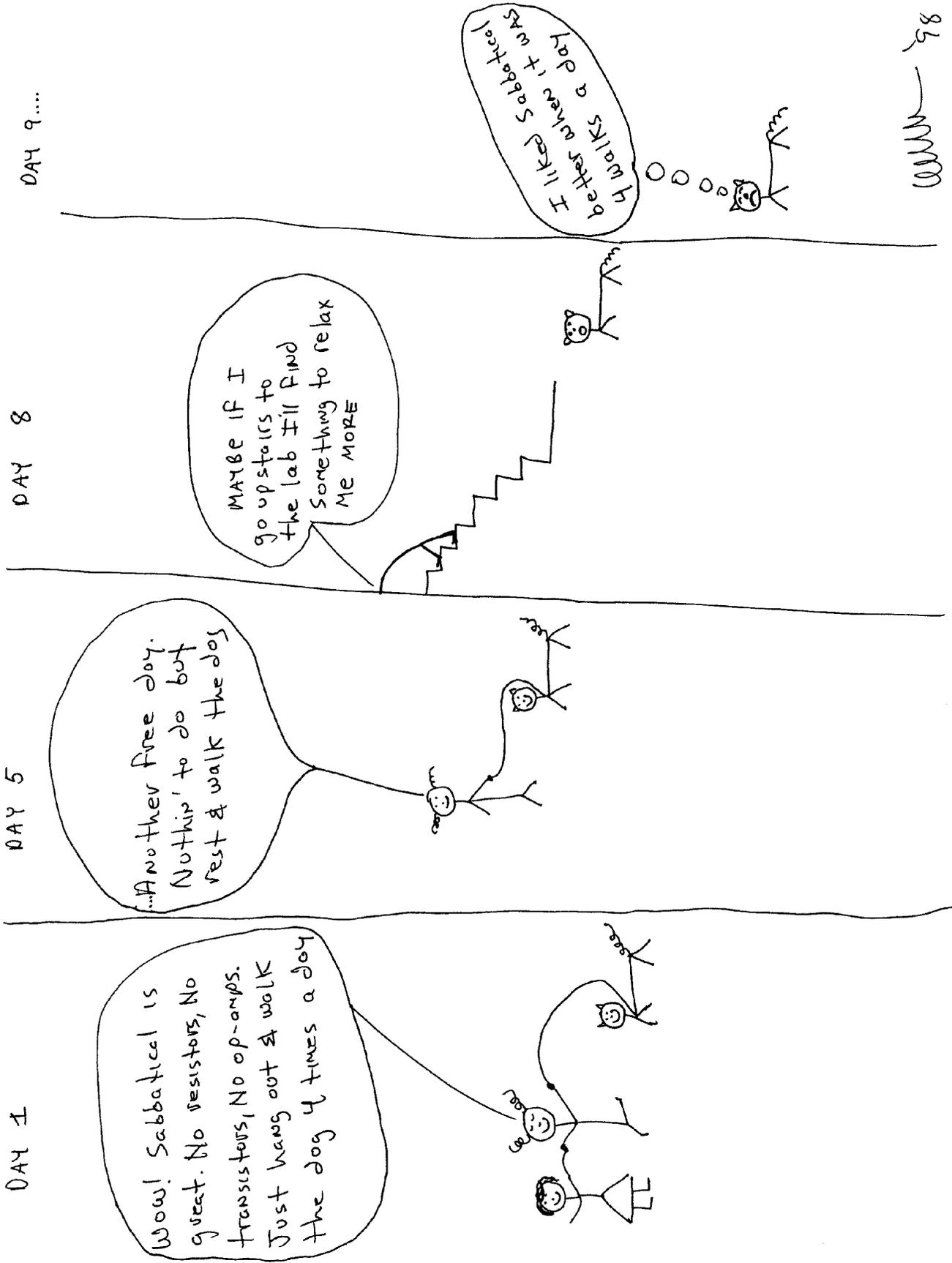Figure B2. **High Impedance Probe Introduces Minimal Loading. Speed Is Adequate for Most Micropower Circuits**

ATTN = NOMINAL 2, TYPICAL 2.1 (SEE TEXT)
INPUT CAPACITANCE = 4pF
I_B = 400pA
GBW = 50MHz
SLEW = 1000V/μs
E_{OS} = 10MV
$E_{OS}\Delta TC$ = 50μV/°C

AN75 FB03

Figure B3. **Ultrafast Buffer Probe Maintains Minimal Loading with 50MHz Bandwidth**