DC279 INTRODUCTION

DESCRIPTION

Demo board DC279 is a low cost three output power supply designed to meet Intel VRM specifications. It features the LTC1736, LTC1772 and LT1762 providing the core, I/O and clock voltages required by the latest Pentium™ mobile processors. The LTC1736 regulates the 5-bit-VID selectable, 14A, Core voltage output from a 7.5V-24V input. The LTC1772 provides the 1.5V, I/O voltage output with the nominal 0.12A or the maximum 2.5A load current required by Intel. The 2.5V, 0.15A Clock output is provided by the LT1762.

DC279 was designed for use on the latest Intel MPDK, mobile Pentium development platform. It can also be evaluated on a user supplied interface board. This demo board is intended for power supply designers of mobile products that use the latest Pentium processors.

QUICK START GUIDE

When using an Intel evaluation platform, plug the DC279 into the CPU Bridge board and follow normal startup procedures.

When using an interface board to evaluate DC279, verify that the mating connector on the interface board has the same pinout as the connector shown in the schematic diagram of DC279. Connect an adjustable 24V, 4A power supply to $+V_{IN}$, a 5V, 0.1A supply to the 5V input and a 3.3V, 2A supply to the 3.3V input.

For static load testing, connect loads to the CPU Core, CPU I/O, and CPU Clock output terminals. Select the desired VID code to program the CPU Core voltage. Output voltage ripple can be viewed with an oscilloscope.

For dynamic load testing, connect the load pulser to the CPU core output terminals. Local decoupling capacitors need to be added to the interface board as close to the output terminals as possible. Either add low ESR capacitors to the interface board near the output terminals or move C12 and C13 from the DC279 to the interface board near the output terminals. Set the load pulser to switch from 0.2A to 12A at a 20A/μs rate. Measure the transient response across the nearest capacitor to the output terminals.

Ground the VRON terminal and observe that all three outputs turn off.

The power good signal at the V_GATE pin can be observed by applying an overcurrent condition to force each output low. The V_GATE voltage should go low when any output drops below about 90% of nominal.