LT3072
Dual, Low Noise, 2.5A Programmable Output, Low Dropout Linear Regulator

DESCRIPTION

Demonstration Circuit 1938A features the LT3072 dual, low noise, 2.5A programmable output, low dropout linear regulator. The input voltages V_{IN1} and V_{IN2} are independent and can range from 0.8V to 3.45V. Each channel has jumpers to set a three-bit code that determines output voltages V_{OUT1} and V_{OUT2} at pre-programmed levels with a range from 0.6V to 2.5V and a maximum output current of 2.5A. DC1938A requires a single external BIAS voltage that is higher than V_{IN1} and V_{IN2}, between 2.375V and 5.25V and is at least 1.2V higher than the highest output voltage.

Each output is decoupled by a 1µF + 2.2µF + 6.8µF capacitor network and each input is decoupled with a 22µF capacitor. The internal reference of each channel is bypassed with a 0.1µF capacitor to reduce output noise and program the soft-start. 1500µF aluminum electrolytic capacitors and 220µF tantalum polymer capacitors hold up VIN1 and VIN2 but the aluminum electrolytic capacitors are cabling dependent and are not required on customer circuits. The BIAS voltage is bypassed at each channel's BIAS pin with a 2.2µF capacitor and there is a single terminal for the BIAS input.

The positions of the VOUT1 and VOUT2 ENABLE jumpers either pull up the EN1 and EN2 pins to the BIAS voltage by a 100k resistor, short EN1 and EN2 to ground or float EN1 and EN2 so they can be driven directly by a signal applied to the EN1 and EN2 terminals. Each channel has a terminal for PWRGD that is pulled up to BIAS by a 51kΩ resistor. Resistors program a 3A output current limit and a 333mV/A output current monitoring voltage that is available at the IMON/LIM terminals. The TEMP terminal allows monitoring of die temperature. VOIC allows automatic control of a pre-regulation voltage and the VOIC pins are bypassed with 1nF capacitors. MARGA1 and MARGA2 terminals for margining allow an optional external voltage to program an adjustment to each channel's output voltage.

Banana jacks minimize voltage drops on VIN and VOUT connections. Each channel's SENSE pin terminates at a 10µF capacitor near the VOUT banana jacks. The PCB design minimizes parasitic SENSE to GND and SENSE to OUT trace capacitance. VO1+, VO1-, VO2+ and VO2- terminals Kelvin-connect to the 10µF VOUT capacitors and are the optimal place to observe output voltage regulation and load transient response. Each output has a 560Ω pre-load so the minimum load requirement is met over the VOUT programming range.

DC1938A has placeholders identified on the schematic as optional (Opt) components that make it convenient to add capacitance, add filtering, parallel references or use the VOIC function – check the schematic for placeholder locations.

The LT3072 is well suited to microprocessor systems and instrumentation applications with stringent performance requirements for output noise and load transient response. Systems with high efficiency requirements will benefit from the low dropout of the LT3072. DC1938A features the LT3072 in a thermally enhanced 36-lead 4mm × 7mm QFN package. The LT3072 data sheet must be read in conjunction with this demo manual to properly use or modify demo circuit DC1938A.

Design files for this circuit board are available.

PERFORMANCE SUMMARY

Specifications are at T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Input Voltage, V_{IN1} or V_{IN2}				0.8	V
Maximum Input Voltage, V_{IN1} or V_{IN2}		3.45			V
Minimum Bias Voltage, V_{BIAS}	$V_{BIAS} > V_{IN1}$, $V_{BIAS} > V_{IN2}$, $V_{BIAS} \geq V_{OUT1} + 1.2V$, and $V_{BIAS} \geq V_{OUT2} + 1.2V$			2.375	V
Maximum Bias Voltage, V_{BIAS}		5.25			V
Output Voltage, V_{OUT1} or V_{OUT2}	V_{OUT} = 0.6V, 10mA ≤ I_{OUT} ≤ 2.5A, 0.90V ≤ V_{IN} ≤ 1.05V V_{OUT} = 1.0V, 10mA ≤ I_{OUT} ≤ 2.5A, 1.3V ≤ V_{IN} ≤ 1.45V V_{OUT} = 1.2V, 10mA ≤ I_{OUT} ≤ 2.5A, 1.5V ≤ V_{IN} ≤ 1.65V V_{OUT} = 1.5V, 10mA ≤ I_{OUT} ≤ 2.5A, 1.8V ≤ V_{IN} ≤ 1.95V V_{OUT} = 1.8V, 10mA ≤ I_{OUT} ≤ 2.5A, 2.1V ≤ V_{IN} ≤ 2.25V V_{OUT} = 2.5V, 10mA ≤ I_{OUT} ≤ 2.5A, 2.8V ≤ V_{IN} ≤ 2.95V	0.59 0.98 1.18 1.48 1.77 2.46		0.61 1.02 1.22 1.52 1.83 2.54	V V V V V V
Maximum Output Current, I_{OUT1} or I_{OUT2}		2.5			A
Output Current Limit, I_{OUT1} or I_{OUT2}	R1 = R2 = 1kΩ		3		A

QUICK START PROCEDURE

To use DC1938A to evaluate the performance of the LT3072, refer to Figure 1 for the proper equipment setup and follow the procedure below:

1. With the input supplies and loads off and turned down, make all connections according to Figure 1. Make sure the jumpers to set VOUT1 and VOUT2 are in the proper positions for the desired output voltage according to Table 1 of the LT3072 data sheet. Make sure the VOUT1 ENABLE and VOUT2 ENABLE jumpers are in the ON position.
2. Turn on the input and bias supplies and increase them to the desired voltages. The BIAS voltage must be higher than V_{IN1} and V_{IN2}, between 2.375V and 5.25V and at least 1.2V higher than the highest output voltage.

NOTE: WHEN SETTING THE INPUT AND BIAS VOLTAGES: An input or bias voltage that is too close to the programmed output voltage (too low) may cause dropout operation and a loss of output voltage regulation. Also, an input voltage that is too high above the output may increase power dissipation to an unacceptable level.

3. Increase the load to the desired output current. Verify that VOUT1 and VOUT2 are as programmed by the jumpers.

NOTE: If the output voltage is low, temporarily disconnect the load to make sure that it is not set too high.

4. Once the proper output voltages are established, adjust the input voltages and loads within the operating ranges and observe the output voltage regulation, load transient response and other parameters.

QUICK START PROCEDURE

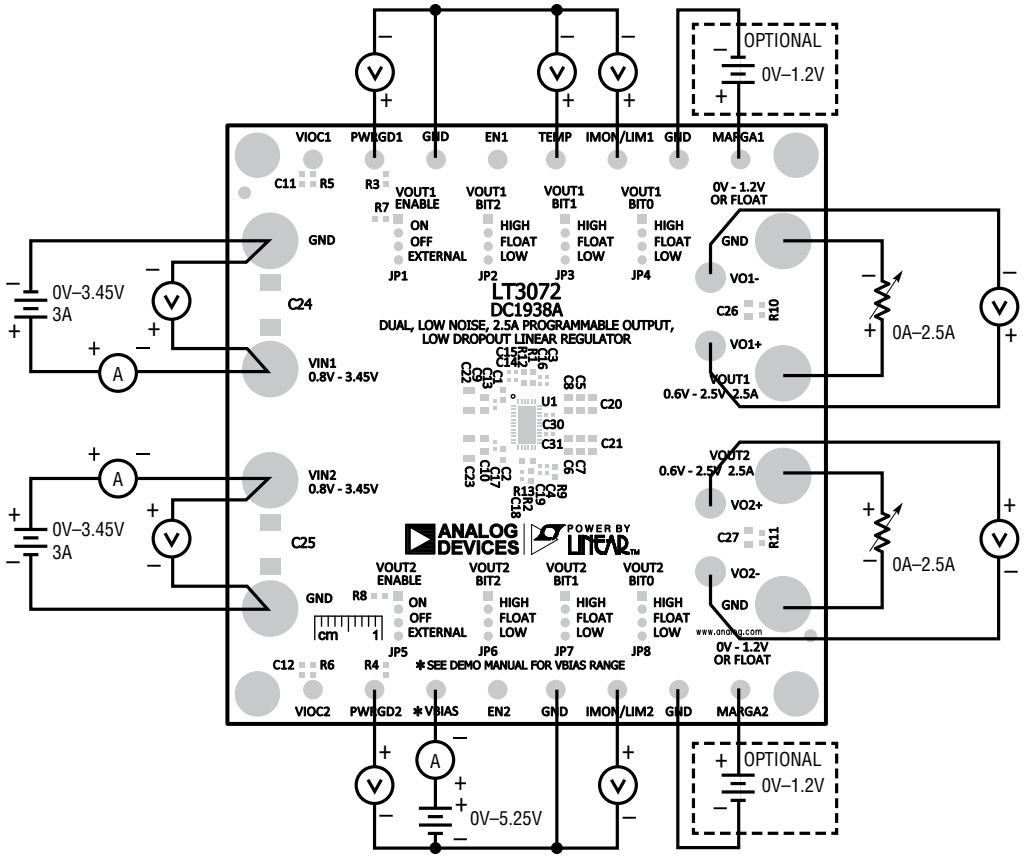


Figure 1. Proper Equipment Setup for DC1938A.

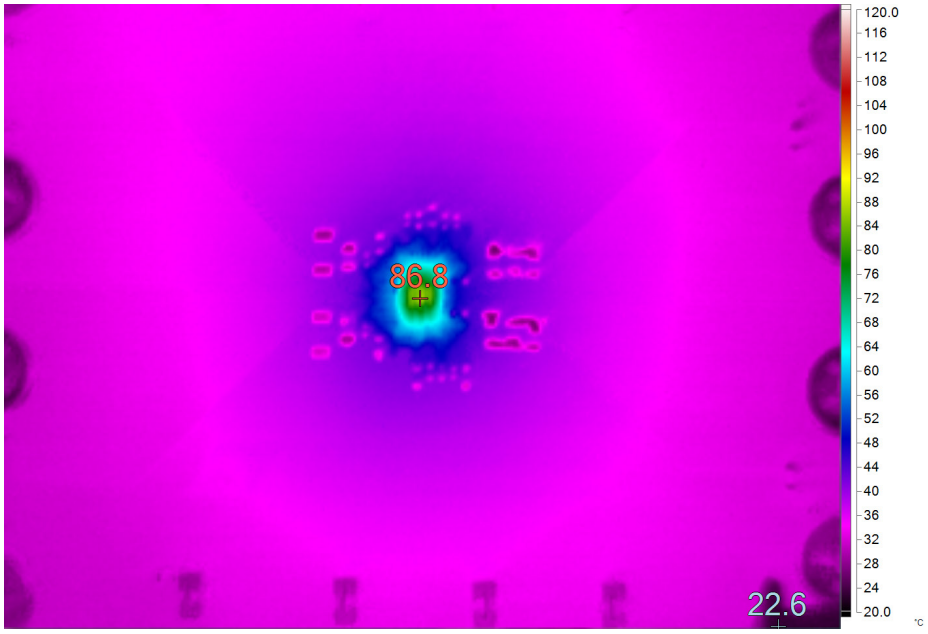
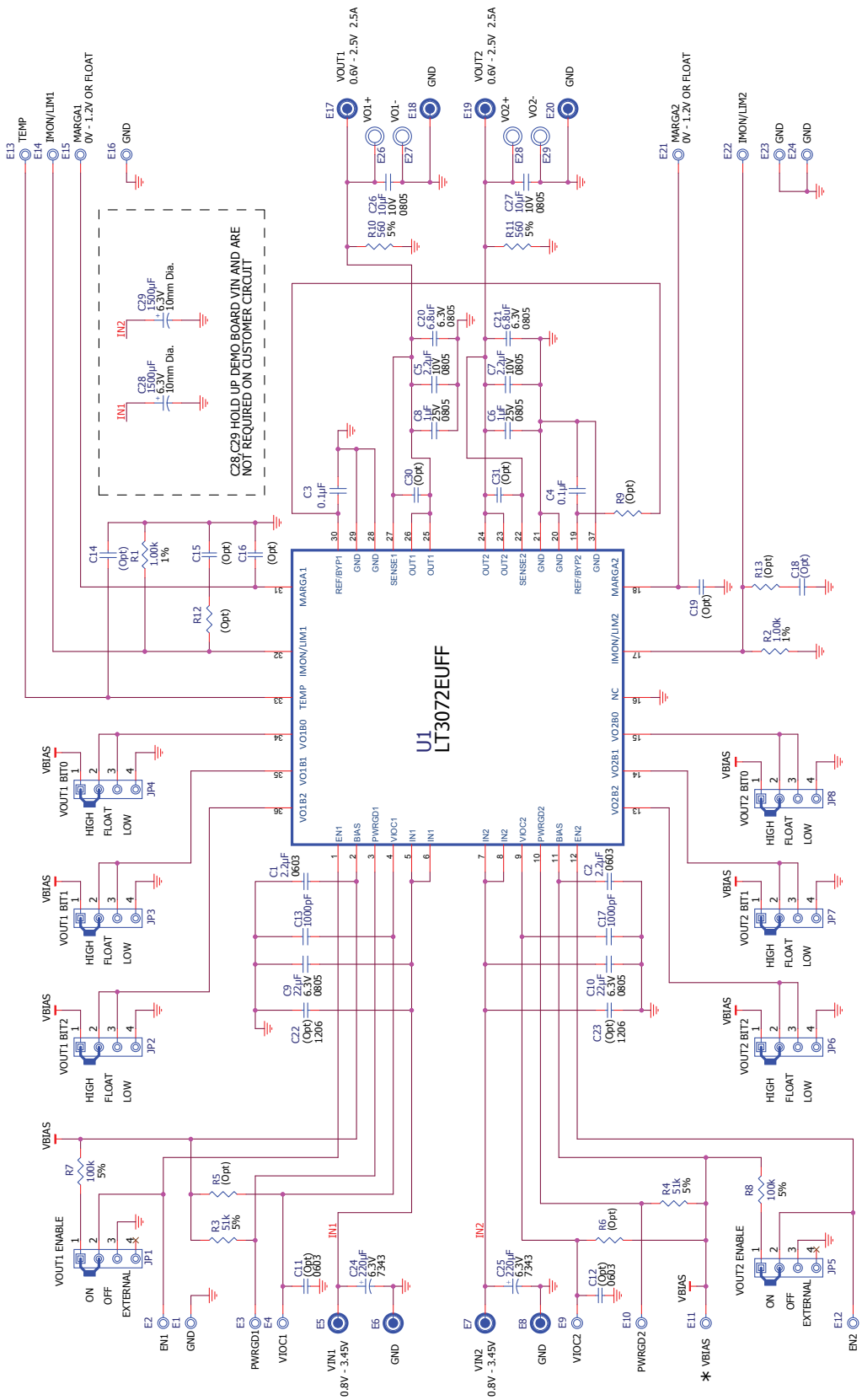


Figure 2. Thermal Image with $3.1V_{IN1}$, $3.1V_{IN2}$, $2.5V_{OUT1}$ at 2.5A and $2.5V_{OUT2}$ at 2.5A. Vertical Orientation with No Forced Air.

PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
Required Circuit Components				
1	2	C1, C2	Cap., X5R, 2.2µF, 10V, 20%, 0603	Taiyo Yuden LMK107BJ225MA-T
2	2	C3, C4	Cap., X5R, 0.1µF, 25V, 10%, 0402	AVX, 04023D104KAT2A
3	2	C5, C7	Cap., X5R, 2.2µF, 10V, 20%, 0805	AVX, 0805ZD225MAT2A
4	2	C6, C8	Cap., X7R, 1.0µF, 25V, 10%, 0805	AVX, 08053C105KAT2A
5	2	C9, C10	Cap., X5R, 22µF, 6.3V, 20%, 0805	TDK C2012X5R0J226M
6	2	C13, C17	Cap., X7R, 1000pF, 25V, 20%, 0402	AVX 04023C102MAT2A
7	2	C20, C21	Cap., X5R, 6.8µF, 6.3V, 10%, 0805	AVX, 08056D685KAT2A
8	2	C24, C25	Cap., Tant. Polymer 220µF, 6.3V, 20%, 7343	AVX TCJY227M006R0025
9	2	R1, R2	Res., Chip 1.00k, 0.06W, 1%, 0603	Vishay CRCW06031K00FKEA
10	2	R10, R11	Res., Chip 560, 0.06W, 5%, 0603	Vishay CRCW0603560RJNEA
11	1	U1	I.C., LDO Reg. QFN-UFF-36-4X7-1863-RV0	Analog Devices., LT3072EUFF#PBF
Optional Demo Circuit Components				
1	0	C11, C12 (Opt)	Cap., 0603	
2	0	C14, C15, C16, C18, C19, C30, C31 (Opt)	Cap., 0402	
3	0	C22, C23 (Opt)	Cap., 1206	
4	2	C26, C27	Cap., X5R, 10µF, 10V, 10%, 0805	AVX 0805ZD106KAT2A
5	2	C28, C29	Cap., Al Elect. 1500µF, 6.3V, 20%, 10mm/DIA	Panasonic EEEFK0J152P
6	2	R3, R4	Res., Chip 51k, 0.06W, 5%, 0603	Vishay CRCW060351K0JNEA
7	0	R5, R6, R9, R12, R13 (Opt)	Res., 0603	
8	2	R7, R8	Res., Chip 100k, 0.06W, 5%, 0603	Vishay CRCW0603100KJNEA
Hardware				
1	16	E1, E2, E3, E4, E9, E10, E11, E12, E13, E14, E15, E16, E21, E22, E23, E24	Turret, Testpoint 0.063"	Mill Max 2308-2-00-80-00-00-07-0
2	8	E5, E6, E7, E8, E17, E18, E19, E20	Connector, Banana Jack	Keystone 575-4
3	4	E26, E27, E28, E29	Testpoint, Turret, .094" pbf	Mill-Max, 2501-2-00-80-00-00-07-0
4	8	JP1, JP2, JP3, JP4, JP5, JP6, JP7, JP8	Headers, 4 Pins 2mm Ctrs.	Sullin, NRPN041PAEN-RC
5	8	XJP1, XJP2, XJP3, XJP4, XJP5, XJP6, XJP7, XJP8	Shunt, 2mm Ctrs.	Samtec 2SN-BK-G
6	4	MH1-MH4	Standoff, Nylon, 0.5, 1/2" SNAP ON	Keystone, 8833

SCHEMATIC DIAGRAM



ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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