# 2-Wire Virtual Remote Sensing for Voltage Regulators
## Clairvoyance Marries Remote Sensing

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## Introduction

Wires and connectors have resistance. This simple, unavoidable truth dictates that a power source's remote load voltage will be less than the source's output voltage. Figure 1 shows this, and implies that intended load voltage can be maintained by raising regulator output. Unfortunately, line resistance and load variations introduce uncertainties, limiting achievable performance.

Figure 2 illustrates one compensatory approach. Locally positioned regulation stabilizes load voltage against line drops but is inefficient due to regulator losses. Figure 3, the classical approach, utilizes "4-wire" remote sensing to eliminate line drop effects. The power supply sense inputs are fed from load referred sense wires. The sense inputs are high impedance, negating sense line resistance effects. This scheme works well, but requires dedicated sense wires, a significant disadvantage in many applications.

## "Virtual" Remote Sensing

Figure 4 retains the advantages of classical 4-wire remote sensing while eliminating the sense leads. Here, the LT4180 Virtual Remote Sense™ (VRS) IC alternates output current between 95% and 105% of the nominal required output current. The LT4180 forces the power supply to provide a DC current plus a small square wave current with peak-to-peak amplitude equal to 10% of the DC current. Decoupling capacitor $C_{LOAD}$, normally required for low impedance under transient conditions in non-VRS systems, takes an additional role by filtering out the VRS square wave excursions.
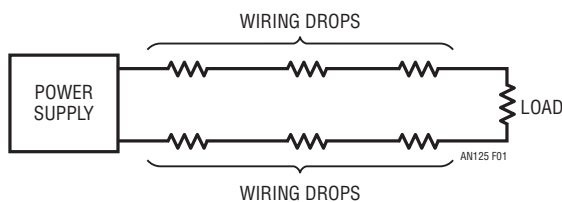


Figure 1. Unavoidable Wiring Drops Cause Low Load Voltage. Line and Load Resistance Variations Introduce Additional Load Voltage Uncertainty, Mitigating Against Compensation by Raising Supply Voltage
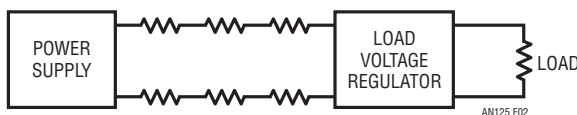


Figure 2. Local Regulation Stabilizes Load Voltage But is Inefficient
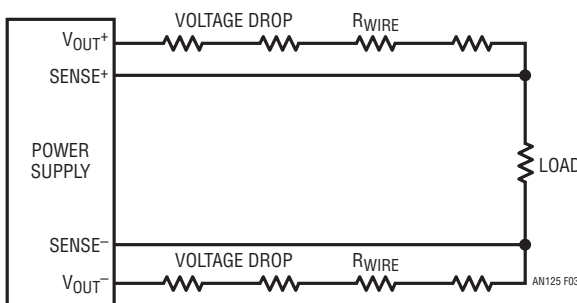


Figure 3. Classical "4-Wire" Remote Sensing. $V_{OUT}$ Line Voltage Drops Are Compensated by Regulator Sensing at Load. High Impedance Sense Inputs Negate Sense Wire Resistance. Approach Requires Four Wires

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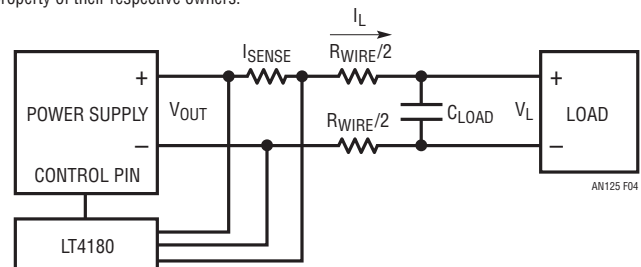


$V_{OUT}$ = DC + SQUAREWAVE FROM WIRING VOLTAGE DROP
$C_{LOAD}$ REMOVES SQUAREWAVE, SO $V_L$ CONTAINS ONLY DC.
$I_L$ = DC + SQUAREWAVE

Figure 4. LT4180 2-Wire Virtual Remote Sense Estimates Wiring Voltage Drops, Compensates by Adjusting Supply Output Voltage. Wiring Loss Is Determined by Measuring Small Signal Square Wave Carrier Induced Voltage Drop. Load Capacitor Absorbs Square Wave; Load Is at DC

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Because C is sized to produce an "AC short" at the square wave frequency, a square wave voltage is produced at the power supply equal to $V_{OUTAC} = 0.1 \cdot I_{DC} \cdot R_{WIRE}V_{P-P}$. The square wave voltage at the power supply has a peak-to-peak amplitude equal to one tenth the DC wiring drop. This is a direct measurement of wiring drop, not an estimate, accurate over all load currents. Signal processing produces a DC voltage from this AC signal which is introduced into the supply feedback loop to provide accurate load regulation[1]. Note that the "power supply" may be an IC linear or switching regulator, a module or any other power source capable of variable output. Power supplies can be synchronized to the LT4180 and VRS operating frequency is adjustable over more than three decades. Optional spread spectrum operation provides partial immunity from single-tone interference and a 3V to 50V input range simplifies design. Because this technique is based on an estimate of load voltage, not a direct measurement, the resultant correction is an approximation, but a very good one.

Typical LT4180 load regulation is plotted in Figure 5. In this example, load current increases from zero until it produces a 2.5V wiring drop. Load voltage drops only 73mV at maximum current. A voltage drop equivalent to 50% of load voltage results in only a 1.5% shift in load voltage value. Smaller wiring drops produce even better results.

**Note 1.** Readers finding their intellectual prowess unsatiated by this admittedly cursory description will find more studious coverage in Appendix A, "A Primer on LT4180 VRS Operation."
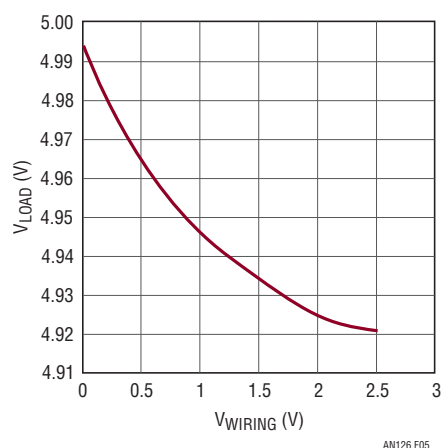


**Figure 5. Typical LT4180 Virtual Remote Sense Performance Shows 1.6% Regulation vs 0V → 2.5V Wiring Drop**

## Applications

The following applications are all VRS augmented voltage regulators of various descriptions. The power regulation stages employed are, with one exception, generic LTC designs and are spared exhaustive commentary, permitting emphasis on the LT4180 VRS role. Additionally, the similarity of the VRS associated circuitry across the broad array of applications shown should be noted, and is indicative of the relative ease of implementation. Surprisingly little change is needed to use the VRS in the different situations presented.

### VRS Linear Regulators

Figure 6 adds a simple stage to the LT4180 to implement a complete VRS aided linear regulator. The LT4180 senses current via the 0.2Ω shunt and feedback controls Q1 with Q2, completing a control loop. Cascoded Q2 permits the ICs 5V capable open drain output to control a high voltage at Q1's gate. Components at the compensation pin furnish loop stability, promoting good transient response[2]. Figure 7 shows Figure 6's load step waveforms. They include $V_{SENSE}$ (trace A), $V_{LOAD}$ (B) and $I_{LOAD}$ (C). Transient response is determined by loop compensation, load capacitance and remote sense sample rate. Figure 8 shows response with $C_{LOAD}$ increased to 1100μF. Load voltage transient excursion reduces and duration increases.

Figure 9, employing a monolithic regulator, adds current limiting and simplifies loop compensation. Transient response approximates Figure 6's. As before, the LT4180's low voltage drain pin requires a cascode transistor to control the high voltage at the LT3080 set pin.

**Note 2.** Value selection procedure for LT1480 VRS circuits is detailed in Appendix B, "Design Guidelines for LT4180 VRS Circuits."

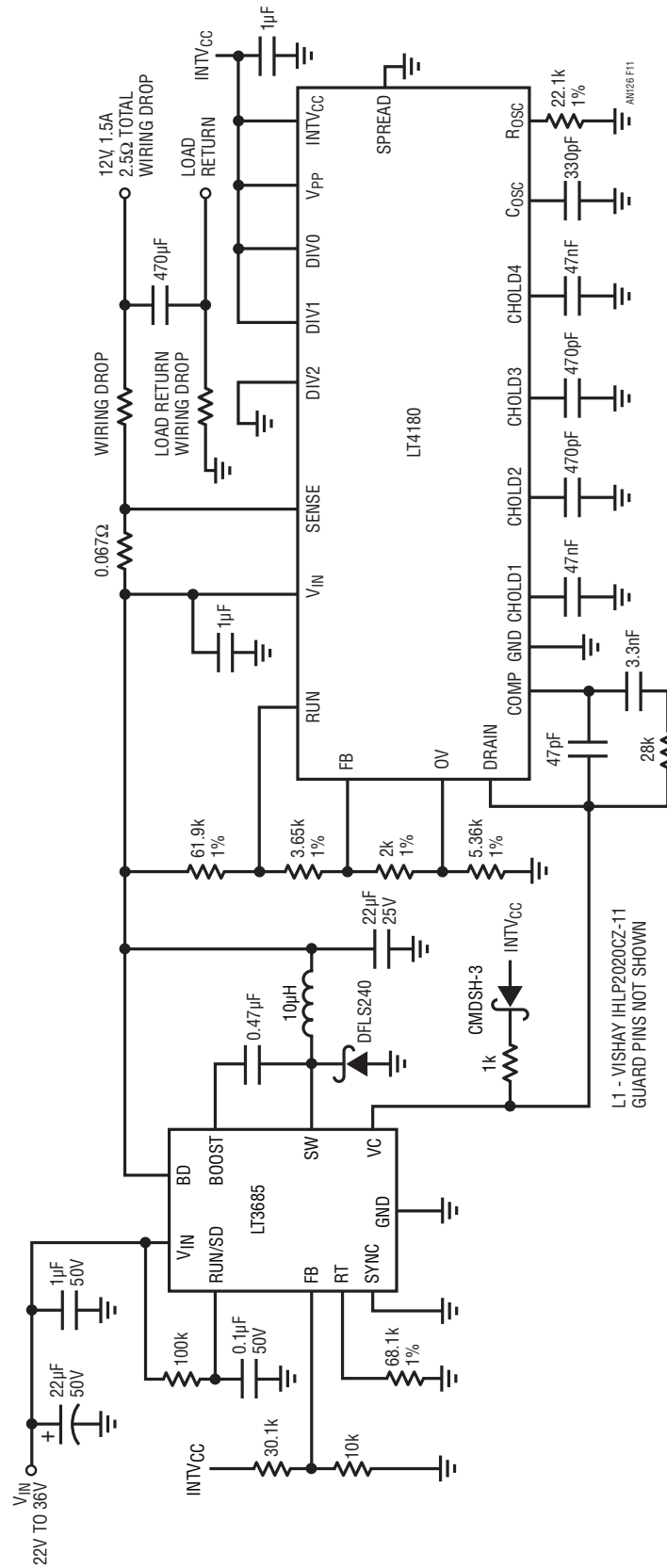**Figure 6. Virtual Remote Sense Controls Discrete Linear Regulator. Q2 Cascodes Drain Output, Buffering High Voltage Q1 Gate Drive. COMP Pin Associated Components Stabilize Loop**



**Figure 7. Figure 6's Load Step Waveforms with 100µF Load Capacitor Include $V_{SENSE}$ (Trace A), $V_{LOAD}$ (B) and $I_{LOAD}$ (C). Transient Response is Determined by Loop Compensation, Load Capacitance and Remote Sense Sample Rate**



**Figure 8. Same Conditions as Figure 7 with $C_{LOAD}$ Increased to 1100µF. $V_{LOAD}$ Transient Excursion Reduces, Duration Extends**

**Figure 9. Figure 6's Approach Utilizing IC Regulator Adds Current Limiting, Simplifies Loop Compensation. Transient Response Approximates Figure 6's**

## VRS Equipped Switching Regulators

VRS based switching regulators are readily constructed. Figure 10's flyback voltage boost configuration has similar architecture to the linear examples although output voltage is above the input. In this case, the LT4180 open drain output is directly compatible with the LT3581 boost regulator low voltage $V_C$ pin—no cascode stage is necessary.

Step down ("Buck") VRS equipped switching regulators are similarly easily achieved. Figure 11's scheme, reminiscent of the previously described linear regulators, substitutes an LT3685 step down regulator which is directly controlled from the LT4180 open drain output. A single pole roll-off stabilizes the loop and a 12V, 1.5A output is maintained from a 22V to 36V input despite a 0Ω to 2.5Ω wiring drop loss. Figure 11A is similar, except that it provides a 5V, 3A output from a 12V to 36V input.

## VRS Based Isolated Switching Supplies

The VRS approach is adaptable to isolated output supplies. Figure 12's 24V output converter utilizes an approach similar to the previous examples except that it supplies a fully isolated output. The virtual remote sense feature accommodates a 10Ω wire resistance. The LT3825 and T1 form a transformer coupled power stage. Opto-coupled feedback maintains output isolation.

Figure 13's 48V → 3.3V, 3A design also has a fully isolated output, facilitated by power delivery through a transformer and optically coupled feedback loop closure. The LT3758 drives T1 via Q1. T1's rectified and filtered secondary supplies output power which is corrected for line drops by the LT4180. Isolation is maintained by transmitting the feedback signal with an opto-isolator. The opto-isolators output collector ties back to the LT3578 $V_C$ pin, closing the control loop.

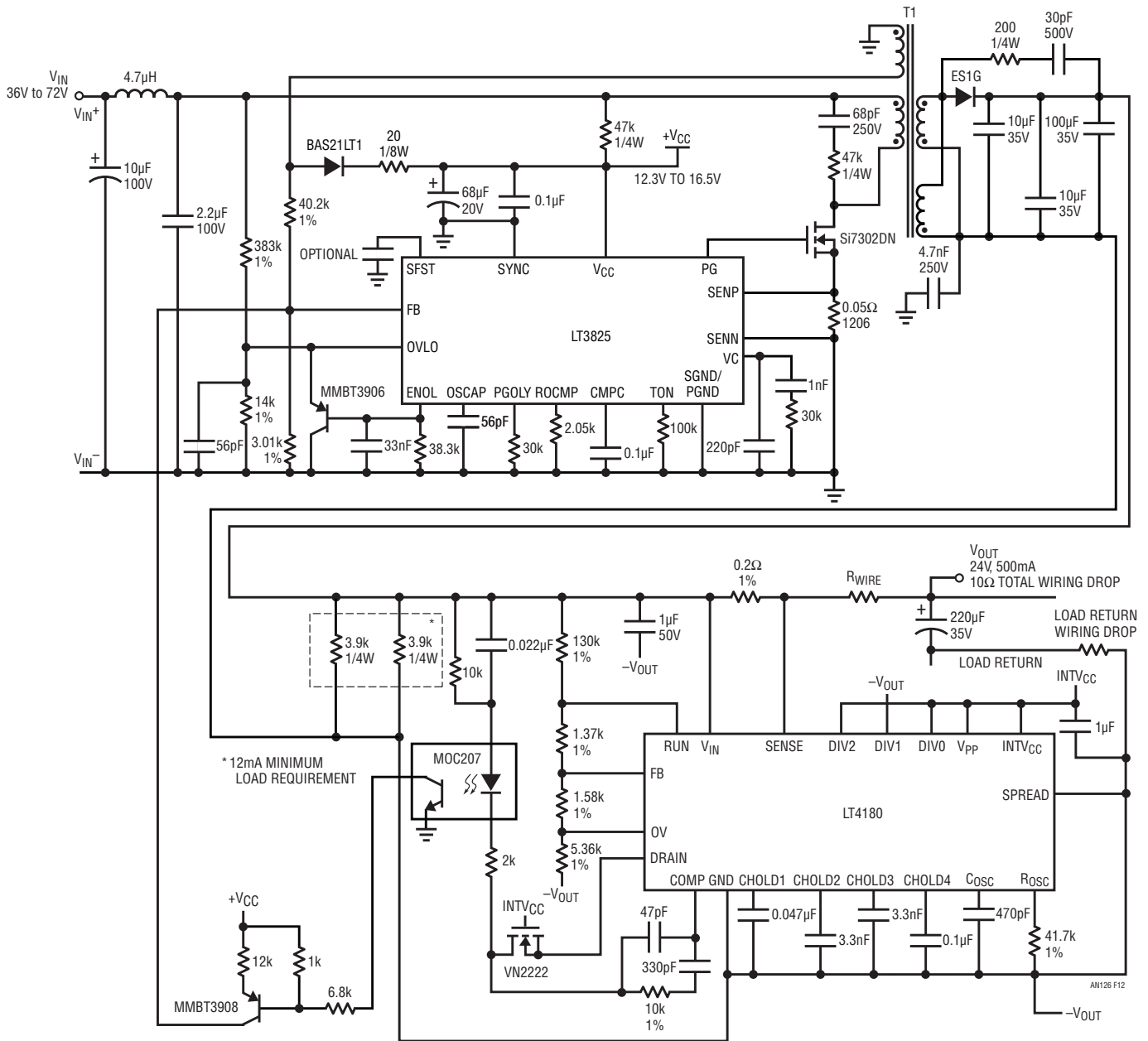**Figure 10. Virtual Remote Sensed Voltage Boost Configuration. LT4180 Drain Output Controls Flyback Regulator via LT3581 $V_C$ Pin**

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Figure 11. Remote Sense Corrected 22V$_{IN}$ to 36V$_{IN}$ Step-Down Regulator Maintains 12V Output Despite Wiring Losses

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**Figure 11A. 12V$_{IN}$ → 36V$_{IN}$ to 5V$_{OUT}$ Step-Down Remote Sensed Regulator Has Similar Architecture to Figure 11**

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**Figure 12. Virtual Remote Sensed, Isolated 36V$_{IN}$ → 72V$_{IN}$ to 24V$_{OUT}$ Converter Accommodates 10Ω Lead Wire Resistance. LT3825/T1 Form Transformer Coupled Power Stage. LT4180 Provides Virtual Remote Sense, Opto-Coupled Feedback Maintains Output Isolation**

10µF TANYO YUDEN GMK325BJ106KN 1210
100µF 36V NICHICON PL (M)
10µF 100V SANYO 100CE10FS
68µF 20V KEMET T491D686K020AS
4.7nF 250V MURATA GA343DR7GD472KW01L
4.7µH COOPER BUSSMANN SO3814-4R7-R
1/4W RESISTORS ARE 1206
1/8W RESISTORS ARE 0805
T1 PULSE PA2925NL
GUARD PINS NOT SHOWN

⏚ = INPUT COMMON

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**Figure 13. 48V → 3.3V Isolated Step-Down, Remote Sensed Regulator. T1 Delivers Isolated Power, LT4180 Remotely Senses Output, Supplies Feedback via Opto-Isolator**

T1 = PULSE ENGINEERING PA1277NL
GUARD PINS NOT SHOWN
* C_LOAD = 4×, 470μF
AVXTPSE477M010R0050

⏚ = INPUT COMMON

▽ = OUTPUT COMMON

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Figure 14, also a VRS isolated step-down supply, uses a commercially produced 48V isolated input module augmented with virtual remote sensing. The module sense terminals are unused. The LT4180 wiring drop correction is introduced at the module trim pin. Compon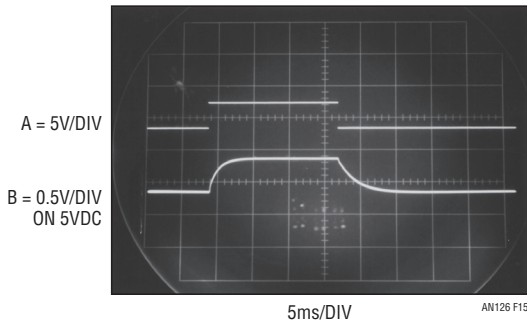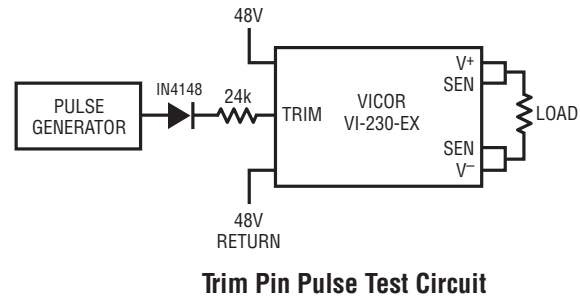ent values are shown for 3.3 and 5V outputs. The "black box" Vicor module trim pin transient response defines available control bandwidth. Figure 15, trace A, is the trim pin input step (see test circuit A), trace B, the module output. The trim pin directed dynamics set practical expectations for VRS equipped loop response around the module. Figures 16 and 17 do not disappoint. Figure 14's load step response appears in Figure 16. Trace A is load step current, trace B, the resultant output voltage transient. The response envelope, bounded by module trim pin dynamics, is clean and well controlled. Figure 17 shows Figure 14's turn-on into a 2.5Amp load. LT4180 activation arrests the initial abrupt rise at the 3rd vertical division. The ascent's conclusion is controlled to the regulation point in damped fashion.

LT4180 sampling square wave residue is just discernible in the waveforms settled portion.

**BEFORE PROCEEDING ANY FURTHER, THE READER IS WARNED THAT CAUTION MUST BE USED IN THE CONSTRUCTION, TESTING AND USE OF THIS CIRCUIT. HIGH VOLTAGE, AC LINE CONNECTED POTENTIALS ARE PRESENT IN THIS CIRCUIT. EXTREME CAUTION MUST BE USED IN WORKING WITH AND MAKING CONNECTIONS TO THIS CIRCUIT. REPEAT: THIS CIRCUIT CONTAINS DANGEROUS, AC LINE CONNECTED HIGH VOLTAGE POTENTIALS. USE CAUTION.**

Figure 18's VRS aided "Off-Line" isolated output supply has a 5V output with 2A capacity. The schematic appears complex, but inspection reveals it to be essentially an AC line powered variant of Figure 13's isolated approach. The LT4180 provides remote sensing and closes an isolated feedback loop with optical transmission.
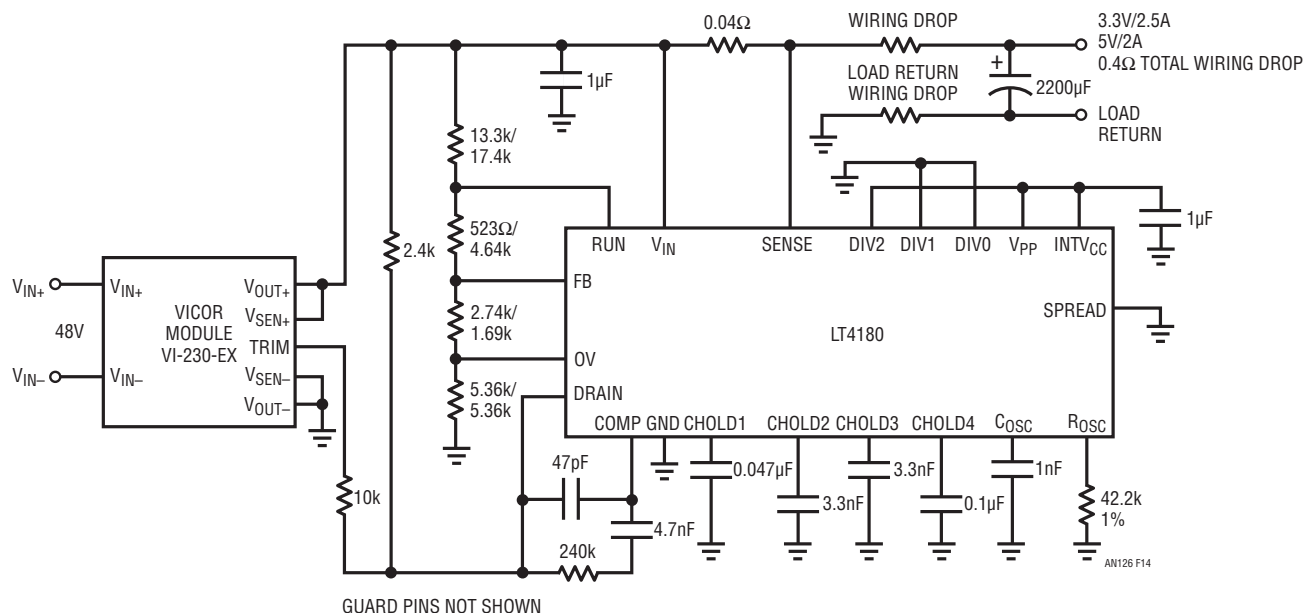


**Figure 14. Commercially Produced, Isolated 48V Input Module Augmented with Virtual Remote Sense. Module Sense Terminals Are Unused. Wiring Drop Correction Introduced at Module Trim Pin. Component Values Shown for 3.3V/5V Outputs**

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Trim Pin Pulse Test Circuit

**Figure 15.Vicor Module Trim Pin Transient Response Defines Available Control Bandwidth. Trace A is Trim Pin Input Step (See Test Circuit), Trace B, Module Output**
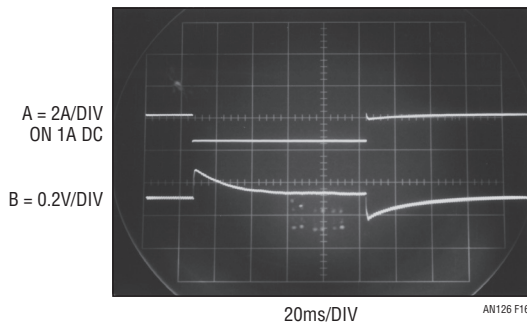


**Figure 16. Figure 14's Load Step Response. Trace A is Load Step Current, Trace B Resultant Output Voltage Transient. Response Envelope, Bounded by Module Trim Pin Dynamics, is Well Controlled**
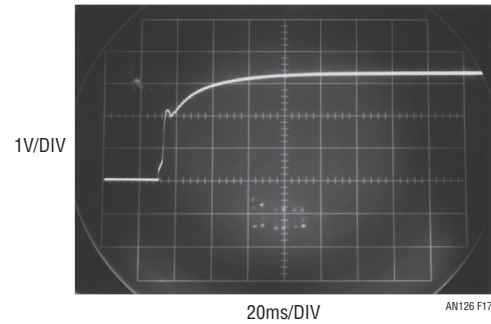


**Figure 17. Figure 14's Turn-On into a 2.5A Load. LT4180 Activation Arrests Initial Abrupt Rise at Third Vertical Division. Ascent Conclusion is Controlled to Regulation Point. LT4180 Sampling Square Wave Residue is Discernible**

## VRS Halogen Lamp Drive Circuit

A final circuit, Figure 19, uses the VRS to stabilize drive to a halogen lamp, in this case a 12V, 30W automotive type. Lamp output power remains constant despite 9V to 15V input variation and line resistance/connection uncertainties. Additional benefits include constant color output and extended lamp life. The circuit, a step up/down ("SEPIC") converter, maintains 12V at the lamp despite the 9V to 15V input range[3]. The VRS functions in the manner previously described. Line resistance losses due to switches, wiring and connectors are obviated by VRS action. Figure 20 plots unaided vs remote sensed and regulated halogen lamp light output. VRS equipped luminosity is flat over the 9 to 15V input range while unregulated performance

**Note 3.** SEPIC operation is described in Reference 2.

suffers dramatically. The regulation also benefits lamp life by greatly reducing lamp turn-on current. Figure 21 shows unregulated lamp turn-on exceeding 20A without regulation. In Figure 22, regulation cuts current peaking to 7A, a 3x reduction. This soft turn-on and constant 12V drive under high/low line conditions optimizes illumination and improves lamp life.

### References

1. LT4180 Data Sheet, Linear Technology Corporation, 2010.

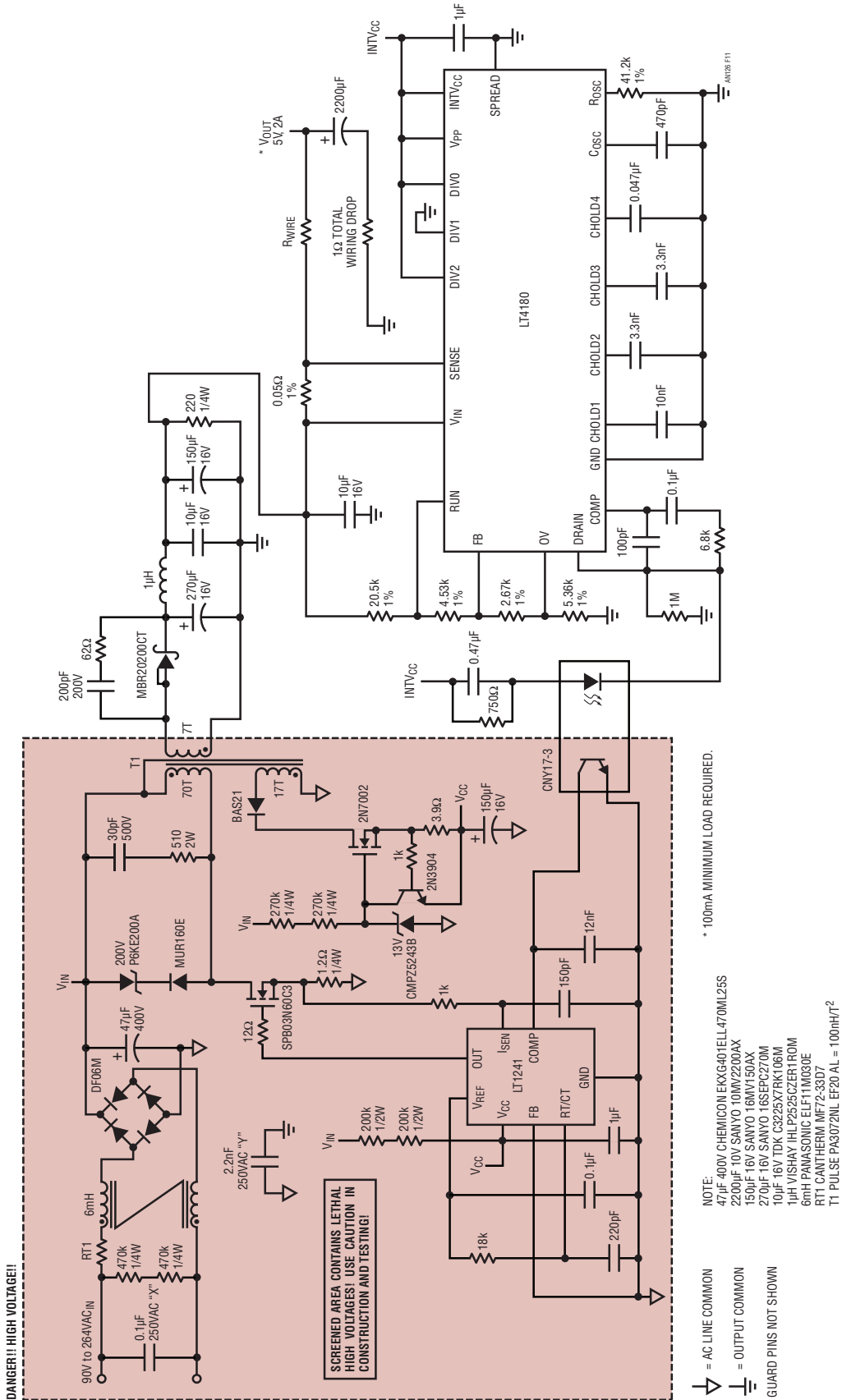2. Ridley, R. "Analyzing the Sepic Converter", Power Systems Design Europe, November, 2006.

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Figure 18. A 5V Output "Off-Line" Converter Equipped with Virtual Remote Sense.
LT4180 Provides Remote Sensing, Closes Isolated Feedback Loop via Opto-Isolator

WARNING! SCREENED AREA CONTAINS LETHAL AC LINE CONNECTED HIGH VOLTAGES. USE CAUTION IN CONSTRUCTION AND TESTING.
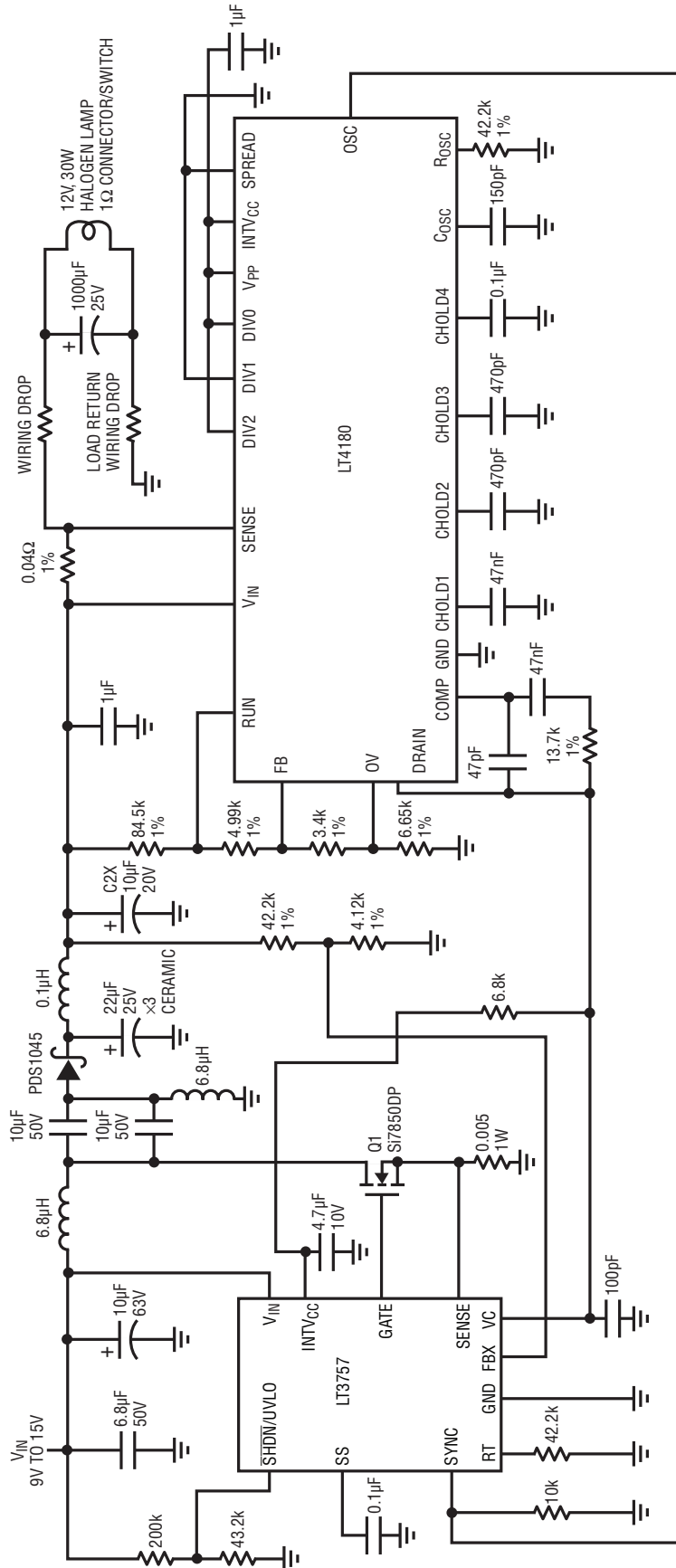
**Figure 19. LT4180 Step Up/Down Converter Stabilizes 12V Drive to 30W Halogen Automotive Lamp Despite 9V → 15V Input Variation and Line Resistance Uncertainties**

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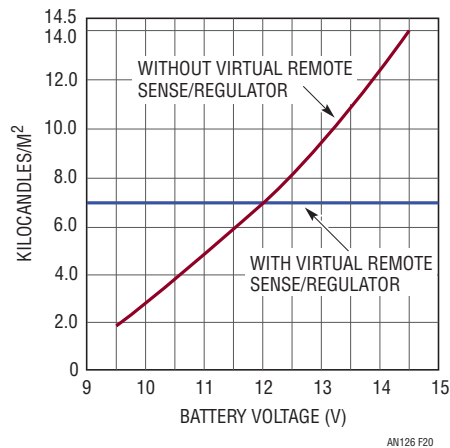
Figure 20. Unaided vs Remote Sensed/Regulated Halogen Lamp Light Output. Regulation Benefits Include Stable Illumination, Constant Color Output and Extended Lamp Life
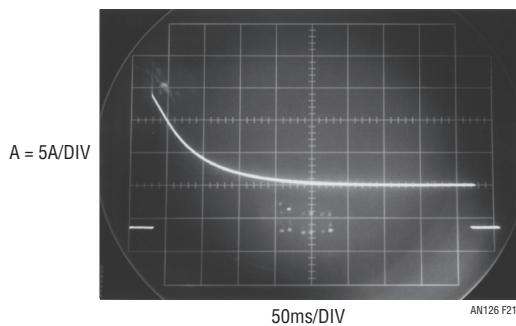


Figure 21. Lamp Turn-On Current Exceeds 20A Without Regulation, Degrading Lifetime
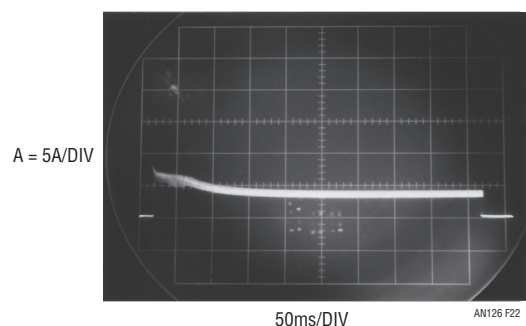


Figure 22. Regulation Promotes Soft Turn-On, 12V Drive Under High/Low Line Conditions, Optimizing Illumination and Improving Lamp Life

## APPENDIX A

### A Primer on LT4180 VRS Operation

Voltage drops in wiring can produce considerable load regulation errors in electrical systems (Figure A1). As load current $I_L$ increases, voltage drop in the wiring ($I_L \cdot RW$) increases and the voltage delivered to the system ($V_L$) drops. The traditional approach to solving this problem, remote sensing, regulates the voltage at the load, increasing the power supply voltage ($V_{OUT}$) to compensate for voltage drops in the wiring. While remote sensing works well, it does require an additional pair of wires to measure at the load, which may not always be practical.

The LT4180 eliminates the need for a pair of remote sense wires by creating a virtual remote sense. Virtual remote sensing is achieved by measuring the incremental change in voltage that occurs with an incremental change in current in the wiring (Figure A2). This measurement can be used to infer the total DC voltage drop in the wiring, which can then be compensated for. The Virtual Remote Sense takes over control of the power supply via its feedback pin ($V_{FB}$), maintaining tight regulation of load voltage $V_L$.

Figure A3 shows the timing diagram for Virtual Remote Sensing (VRS). A new cycle begins when the power supply and VRS close the loop around $V_{OUT}$ (Regulate $V_{OUT}$ = H). Both $V_{OUT}$ and $I_{OUT}$ slew and settle to a new value, and these values are stored in the Virtual Remote Sense (Track $V_{OUTHIGH}$ = L and Track $I_{OUT}$ = L). The $V_{OUT}$ feedback loop is opened and a new feedback loop is set up commanding the power supply to deliver 90% of the previously measured current (0.9 $I_{OUT}$). $V_{OUT}$ drops to a new value as the power supply reaches a new steady state, and this information is also stored in the Virtual Remote Sense. At this point, the change in the output voltage ($\Delta V_{OUT}$) for a –10% change in output current has been measured and is stored in the Virtual Remote Sense. This voltage is used during the next VRS cycle to compensate for voltage drops due to wiring resistance.
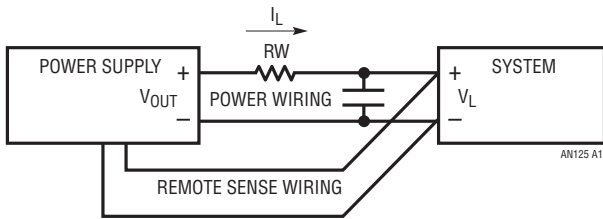


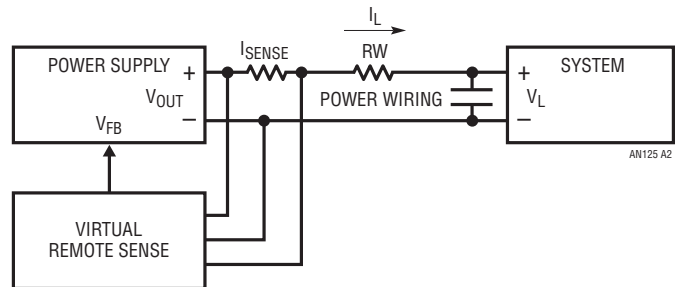**Figure A1. Traditional Remote Sensing Works Well But Requires Two Sense Wires**



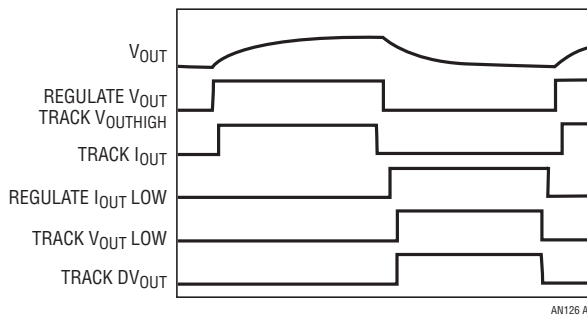**Figure A2. Virtual Remote Sensing Eliminates Sense Wires**



**Figure A3. Simplified Virtual Remote Sense Timing Diagram. State Machine Driven Sequence Samples and Stores Information Necessary to Set Appropriate Power Supply Voltage to Correct for Wiring Losses**

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## APPENDIX B

### Design Guidelines for LT4180 VRS Circuits

#### INTRODUCTION

The LT4180 is designed to interface with a variety of power supplies and regulators having either an external feedback or control pin. In Figure B1, the regulator error amplifier (which is a $g_m$ amplifier) is disabled by tying its inverting input to ground. This converts the error amplifier into a constant-current source which is then controlled by the drain pin of the LT4180. This is the preferred method of interfacing because it eliminates the regulator error amplifier from the control loop which simplifies compensation and provides best control loop response.

For proper operation, increasing control voltage should correspond to increasing regulator output. For example, in the case of a current mode switching power supply, the control pin ITH should produce higher peak currents as the ITH pin voltage is made more positive.

Isolated power supplies and regulators may also be used by adding an opto-coupler (Figure B2). LT4180 output voltage $INTV_{CC}$ supplies power to the opto-coupler LED. In situations where the control pin $V_C$ of the regulator may exceed 5V, a cascode may be added to keep the DRAIN pin of the LT4180 below 5V (Figure B3). Use a Low VT MOSFET for the cascode transistor.
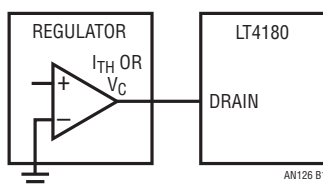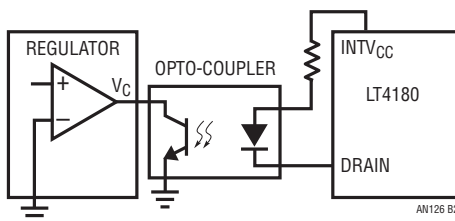


**Figure B1. Nonisolated Regulator Interface**



**Figure B2. Isolated Power Supply Interface**
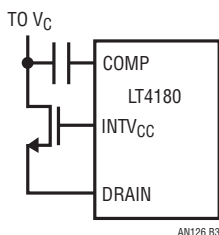


**Figure B3. Cascoded DRAIN Pin for Isolated Supplies**

## DESIGN PROCEDURE

The first step in the design procedure (Figure B4) is to determine whether the LT4180 will control a linear or switching supply/regulator. If using a switching power supply or regulator, it is recommended that the supply be synchronized to the LT4180 by connecting the OSC pin to the SYNC pin (or equivalent) of the supply.

If the power supply is synchronized to the LT4180, the power supply switching frequency is determined by:

$$f_{OSC} = \frac{4}{R_{OSC} \cdot C_{OSC}}$$

Recommended values for $R_{OSC}$ are between 20k and 100k (with 30.1k the optimum for best accuracy) and greater than 100pF for $C_{OSC}$. $C_{OSC}$ may be reduced to as low as 50pF, but oscillator frequency accuracy will be somewhat degraded.

The following example synchronizes a 250kHz switching power supply to the LT4180. In this example, start with $R_{OSC} = 30.1k$:
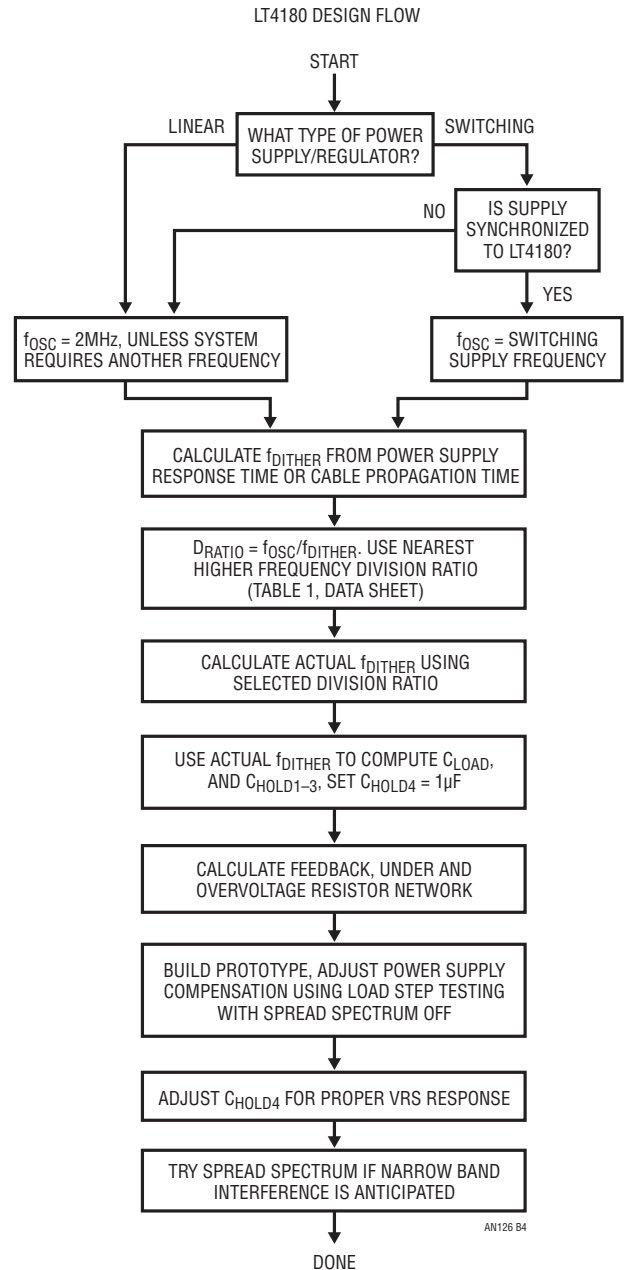
$$C_{OSC} = \frac{4}{250kHz \cdot 30.1k} = 531pF$$

This example uses 470pF. For 250kHz:

$$R_{OSC} = \frac{4}{250kHz \cdot 470pF} = 34.04k$$

The closest standard 1% value is 34k.

The next step is to determine the highest practical dither frequency. This may be limited either by the response time of the power supply or regulator, or by the propagation time of the wiring connecting the load to the power supply or regulator.



LT4180 DESIGN FLOW

START

WHAT TYPE OF POWER SUPPLY/REGULATOR?

LINEAR — SWITCHING

IS SUPPLY SYNCHRONIZED TO LT4180? — NO — YES

$f_{OSC}$ = 2MHz, UNLESS SYSTEM REQUIRES ANOTHER FREQUENCY

$f_{OSC}$ = SWITCHING SUPPLY FREQUENCY

CALCULATE $f_{DITHER}$ FROM POWER SUPPLY RESPONSE TIME OR CABLE PROPAGATION TIME

$D_{RATIO} = f_{OSC}/f_{DITHER}$. USE NEAREST HIGHER FREQUENCY DIVISION RATIO (TABLE 1, DATA SHEET)

CALCULATE ACTUAL $f_{DITHER}$ USING SELECTED DIVISION RATIO

USE ACTUAL $f_{DITHER}$ TO COMPUTE $C_{LOAD}$, AND $C_{HOLD1-3}$, SET $C_{HOLD4}$ = 1µF

CALCULATE FEEDBACK, UNDER AND OVERVOLTAGE RESISTOR NETWORK

BUILD PROTOTYPE, ADJUST POWER SUPPLY COMPENSATION USING LOAD STEP TESTING WITH SPREAD SPECTRUM OFF

ADJUST $C_{HOLD4}$ FOR PROPER VRS RESPONSE

TRY SPREAD SPECTRUM IF NARROW BAND INTERFERENCE IS ANTICIPATED

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DONE

**Figure B4. Design Flow Chart**

First determine the settling time (to 1% of final value) of the power supply. The settling time should be the worst-case value (over the whole operating envelope: $V_{IN}$, $I_{LOAD}$, etc.).

$$F1 = \frac{1}{2 \cdot t_{SETTLING}} \; Hz$$

For example, if the power supply takes 1ms to settle (worst-case) to within 1% of final value:

$$F1 = \frac{1}{2 \cdot 1e-3} = 500Hz$$

Next, determine the propagation time of the wiring. In order to ignore transmission line effects, the dither period should be approximately twenty times longer than this. This will limit dither frequency to:

$$F2 = \frac{V_F}{20 \cdot 1.017ns/ft \cdot L} \; Hz$$

where $V_F$ is the velocity factor (or velocity of propagation), and L is the length of the wiring (in feet).

For example, assume the load is connected to a power supply with 1000ft of CAT5 cable. Nominal velocity of propagation is approximately 70%.

$$F2 = \frac{0.7}{20 \cdot 1.017e-9 \cdot 1000} = 34.4kHz$$

The maximum dither frequency should not exceed F1 or F2 (whichever is less):

$$f_{DITHER} < min \; (F1, F2).$$

Continuing this example, the dither frequency should be less than 500Hz (limited by the power supply).

With the dither frequency known, the division ratio can be determined:

$$D_{RATIO} = \frac{f_{OSC}}{f_{DITHER}} = \frac{250,000}{500} = 500$$

The nearest division ratio is 512 (set DIV0 = L, DIV1 = DIV2 = H). Based on this division ratio, nominal dither frequency will be:

$$f_{DITHER} = \frac{f_{OSC}}{D_{RATIO}} = \frac{250,000}{512} = 488Hz$$

After the dither frequency is determined, the minimum load decoupling capacitor can be determined. This load capacitor must be sufficiently large to filter out the dither signal at the load.

$$C_{LOAD} = \frac{2.2}{R_{WIRE} \cdot 2 \cdot f_{DITHER}}$$

where $C_{LOAD}$ is the minimum load decoupling capacitance, $R_{WIRE}$ is the minimum wiring resistance of one conductor of the wiring pair, and $f_{DITHER}$ is the minimum dither frequency.

Continuing the example, our CAT5 cable has a maximum 9.38Ω/100m conductor resistance.

Maximum wiring resistance is:

$$R_{WIRE} = 2 \cdot 1000ft \cdot 0.305m/ft \cdot 0.0938\Omega/m$$

$$R_{WIRE} = 57.2\Omega$$

With an oscillator tolerance of ±15%, the minimum dither frequency is 414.8Hz, so the minimum decoupling capacitance is:

$$C_{LOAD} = \frac{2.2}{57.2\Omega \cdot 2 \cdot 414.8Hz} = 46.36\mu F$$

This is the minimum value. Select a nominal value to account for all factors which could reduce the nominal, such as initial tolerance, voltage and temperature coefficients and aging.

**CHOLD Capacitor Selection and Compensation**

**CHOLD1**

A 47nF capacitor will suffice for most applications. A smaller value might allow faster recovery from a sudden load change, but care must be taken to ensure full load p-p ripple at this node is kept within 5mV:

$$CHOLD2 = CHOLD3 = \frac{2.5nF}{f_{DITHER}(kHz)}$$

For a dither frequency of 488Hz:

$$CHOLD2 = CHOLD3 = \frac{2.5nF}{0.488(kHz)} = 5.12nF$$

NPO ceramic or other capacitors with low leakage and dielectric absorption should be used for all HOLD capacitors.

Set CHOLD4 to 1µF. This value will be adjusted later.

## Compensation

Start with a 47pF capacitor between the COMP and DRAIN pins of the LT4180. Add an RC network in parallel with the 47pF capacitor, 10k and 10nF are good starting values. Once the output voltage has been confirmed to regulate at the desired level at no load, increase the load current to the 100% level and monitor the wire current (dither current) with a current probe. Verify the dither current resembles a square-wave with the desired dither frequency.

If the output voltage is too low, increase the value of the 10k resistor until some overshoot is observed at the leading edge of the dither current waveform. If the output voltage is still too low, decrease the value of the 10nF capacitor and repeat the previous step. Repeat this process until the full load output voltage increases to within 1% below the no load level. Refer to Figures B5a, B5b and B5c, which show compensation of the 12V 1.5A Buck Regulator Application on the data sheet. Check for proper voltage drop correction over the load range. The "dither current" should have good half-wave symmetry. Namely, waveform should have similar rise and fall times, enough settling time at top and bottom and minimum to no over/undershoot.
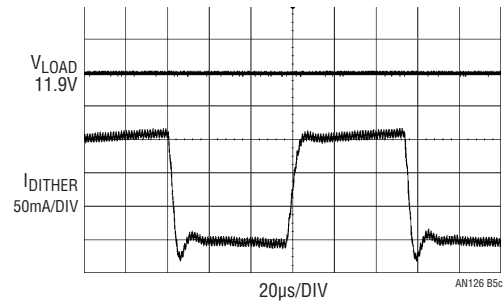


**Figure B5c. Dither Current and V$_{OUT}$ with 3.3nF, 28k Compensation 1.5A Load**

## Set Final Value of CHOLD4

Set the minimum value for CHOLD4, by performing a transient load test of 30% to 60% of the load and set the value of CHOLD4 to where a nicely damped waveform is observed. Refer to Figures B6a and B6b for an illustration.

After all the CHOLD values have been finalized, check for proper voltage drop correction and converter behavior (start-up, regulation etc.), over the load and input voltage ranges.
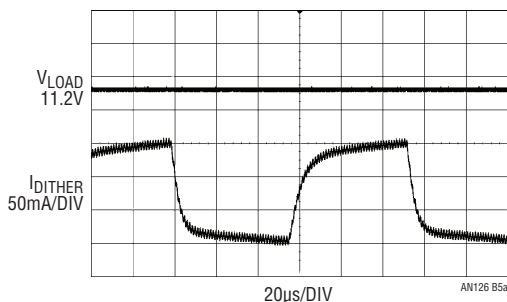


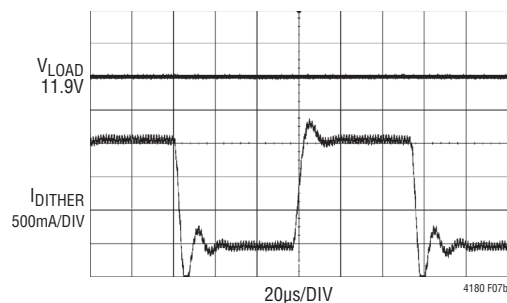**Figure B5a. Dither Current and V$_{OUT}$ with 10nF, 10k Compensation 1.5A Load**



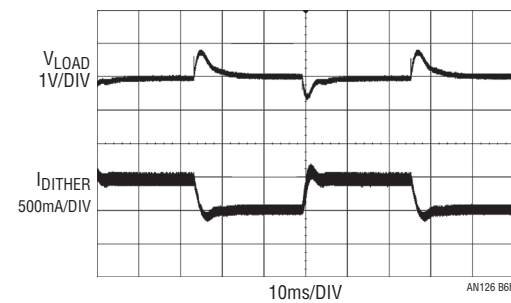**Figure B6a. 500mA to 1A Transient Response Test with CHOLD4 = 25nF CHOLD4 Too Small**



**Figure B5b. Dither Current and V$_{OUT}$ with 10nF, 37k Compensation 1.5A Load**



**Figure B6b. 500mA to 1A Transient Response Test with CHOLD4 = 47nF Nicely Damped Behaviour**

an126fa

## Setting Output Voltage, Undervoltage and Overvoltage Thresholds

The RUN pin has accurate rising and falling thresholds which may be used to determine when Virtual Remote Sense operation begins. Undervoltage threshold should never be set lower than the minimum operating voltage of the LT4180 (3.1V).

The overvoltage threshold should be set slightly greater than the highest voltage which will be produced by the power supply or regulator:

$$V_{OUT(MAX)} = V_{LOAD(MAX)} + V_{WIRE(MAX)}$$

$V_{OUT(MAX)}$ should never exceed $1.5 \cdot V_{LOAD}$

Since the RUN and OV pins connect to MOSFET input comparators, input bias currents are negligible and a common voltage divider can be used to set both thresholds (Figure B7).
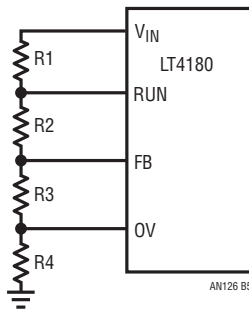


**Figure B7. Voltage Divider for UVL and OVL**

The voltage divider resistors can be calculated from the following equations:

$$R_T = \frac{V_{OV}}{200\mu A}, \quad R4 = \frac{1.22V}{200\mu A}$$

where $R_T$ is the total divider resistance and $V_{OV}$ is the overvoltage set point.

Find the equivalent series resistance for R2 and R3 ($R_{SERIES}$). This resistance will determine the RUN voltage level.

$$R_{SERIES} = \left( \frac{1.22 \cdot R_T}{V_{UVL}} \right) - R4$$

$$R1 = R_T - R_{SERIES} - R4$$

$$R3 = \frac{1.22V - \left( V_{OUT(NOM)} \cdot \dfrac{R4}{R_T} \right)}{\dfrac{V_{OUT(NOM)}}{R_T}}$$

$$R2 = R_{SERIES} - R3$$

Where $V_{UVL}$ is the RUN voltage and $V_{OUT(NOM)}$ is the nominal output voltage desired.

For example, with $V_{UVL} = 4V$, $V_{OV} = 7.5V$ and $V_{OUT(NOM)} = 5V$,

$$R_T = \frac{7.5V}{200\mu A} = 37.5k$$

$$R4 = \frac{1.22V}{200\mu A} = 6.1k$$

$$R_{SERIES} = \left( \frac{1.22V \cdot 37.5k}{4V} \right) - 6.1k = 5.34k$$

$$R1 = 37.5k - 5.34k - 6.1k = 26.06k$$

$$R3 = \frac{1.22V - \left( \dfrac{5V \cdot 6.1k}{37.5k} \right)}{\dfrac{5V}{37.5k}} = 3.05k$$

$$R2 = R_{SERIES} - R3 = 2.29k$$

## $R_{SENSE}$ SELECTION

Select the value of $R_{SENSE}$ so that it produces a 100mV voltage drop at maximum load current. For best accuracy, $V_{IN}$ and SENSE should be Kelvin connected to this resistor.

## Soft-Correct Operation

The LT4180 has a soft-correct function which insures orderly start-up (Figure B8). When the RUN pin rising threshold is first exceeded (indicating $V_{IN}$ has crossed its undervoltage lockout threshold), power supply output voltage is set to a value corresponding to zero wiring voltage drop (no correction for wiring). Over a period of time (determined by $C_{HOLD4}$), the power supply output voltage ramps up to account for wiring voltage drops, providing best load-end voltage regulation. A new soft-correct cycle is also initiated whenever an overvoltage condition occurs.
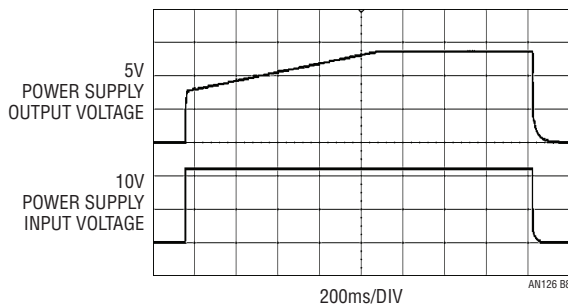


**Figure B8. Soft-Correct Operation, $C_{HOLD4}$ = 1µF**

## Using Guard Rings

The LT4180 includes a total of four track/holds in the Virtual Remote Sense path. For best accuracy, all leakage sources on the CHOLD pins should be minimized.

At very low dither frequencies, the circuit board layout may include guard rings which should be tied to their respective guard ring drivers.

To better understand the purpose of guard rings, a simplified model of hold capacitor leakage (with and without guard rings) is shown in Figure B9. Without guard rings, a large difference voltage may exist between the hold capacitor (Pin 1) node and adjacent conductors (Pin 2) producing
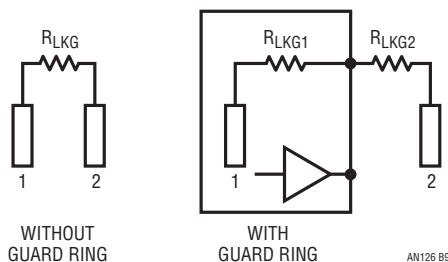


**Figure B9. Simplified Leakage Models
(with and without Guard Rings)**

substantial leakage current through the leakage resistance ($R_{LKG}$). By adding a guard ring driver with approximately the same voltage as the voltage on the hold capacitor node, the difference voltage across $R_{LKG1}$ is reduced substantially thereby reducing leakage current on the hold capacitor.

## Synchronization

Linear and switching power supplies and regulators may be used with the LT4180. In most applications regulator interference should be negligible. For those applications where accurate control of interference spectrum is desirable, an oscillator output has been provided so that switching supplies may be synchronized to the LT4180 (Figure B10). The OSC pin was designed so that it may directly connect to most regulators, or drive opto-isolators (for isolated power supplies).
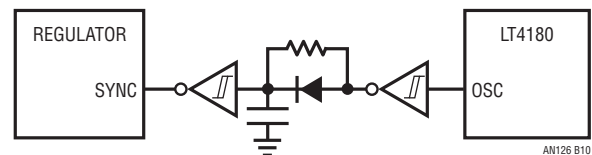


**Figure B10. Clock Interface for Synchronization**

## Spread Spectrum Operation

Virtual remote sensing relies on sampling techniques. Because switching power supplies are commonly used, the LT4180 uses a variety of techniques to minimize potential interference (in the form of beat notes which may occur between the dither frequency and power supply switching frequency). Besides several types of internal filtering, and the option for VRS/power supply synchronization, the LT4180 also provides spread spectrum operation.

By enabling spread spectrum operation, low modulation index pseudo-random phasing is applied to Virtual Remote Sense timing. This has the effect of converting any remaining narrow-band interference into broadband noise, reducing its effect.

## Increasing Voltage Correction Range

Correction range may be slightly improved by regulating $INTV_{CC}$ to 5V. This may be done by placing an LDO between $V_{IN}$ and $INTV_{CC}$. Contact Linear Technology Applications for more information.
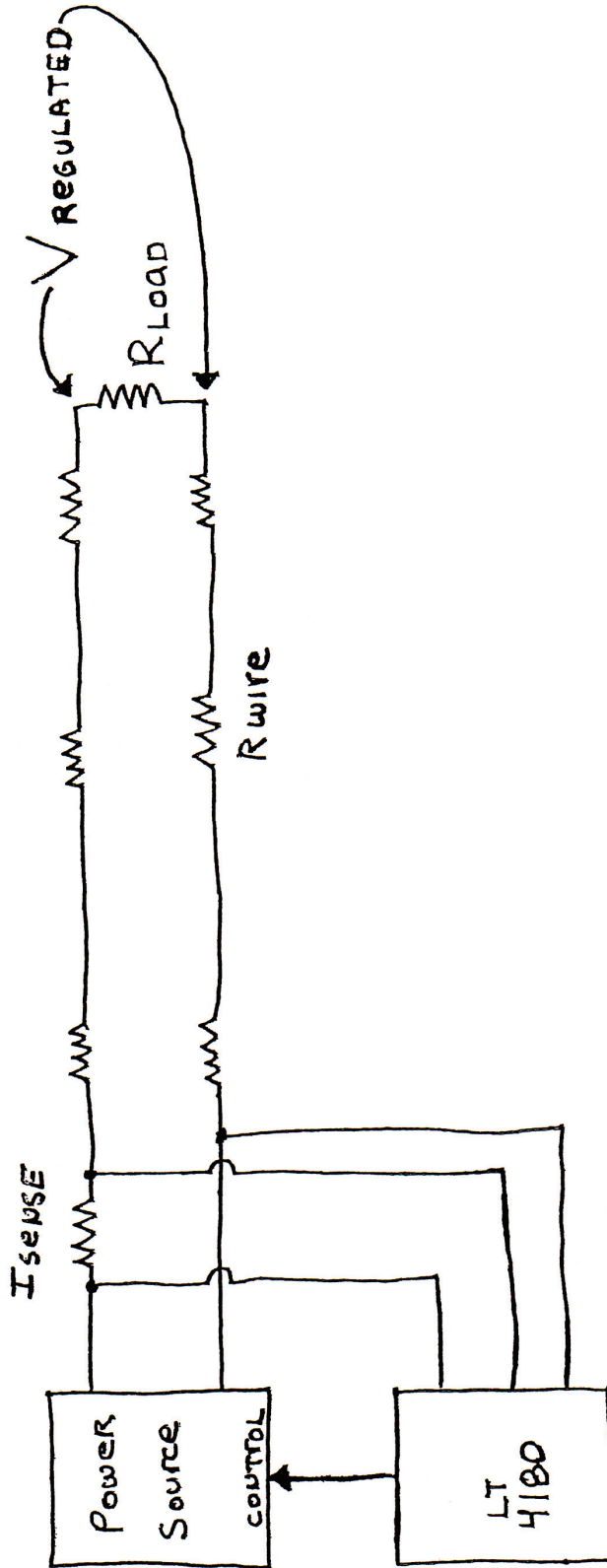
"Any sufficiently advanced technology is indistinguishable from magic."

~ Arthur C. Clarke

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