February 24, 2005

LT5515 board level design issues and considerations.

The LT5515 Direct Conversion Receiver is a high performance radio frequency integrated circuit. The actual product design and implementation requires optimum placement of the LT5515 and its external components, as well as good RF layout for the printed circuit board (PCB) in order to maximize the receiver performance. In general, direct conversion receivers are sensitive to leakage of the Local Oscillator signal to the Baseband (BB) and the RF ports, and also leakage of the RF signal to the BB and LO ports. Such leakages result in degradation of important receiver parameters.

Board level issues with direct conversion receivers.

1. LO leakage to the Baseband outputs.

LO leakage to the BB outputs (as well as 2nd harmonic of LO at the BB outputs) may degrade the phase balance of the baseband I/Q signals.
Suggested actions:

- Provide high frequency terminations to ground with small value shunt capacitors at the BB outputs, placed close to the BB pins.
- The BB output signal lines should be routed on the bottom side of the PCB for improved isolation.
- Use good conservative layout with solid ground plane on the 1st and 2nd PCB layers. Use lots of ground vias, especially in the areas separating the LO signal lines from the BB signal lines, as well as in areas separating RF signal lines from BB signal lines and RF signal lines from LO signal lines.

2. RF leakage to BB outputs.

RF, as well as LO leakage to Baseband, produces static and dynamic DC offset at the BB outputs. This may lead to IP2 performance degradation.
Suggested actions: Refer to suggested actions in item 1.

3. LO leakage to the RF input.

LO leakage to the RF input may result in a LO “self-mixing” which produces static DC offset at the BB outputs.
Suggested actions: Refer to suggested actions in item 1.

4. RF leakage to the LO port.

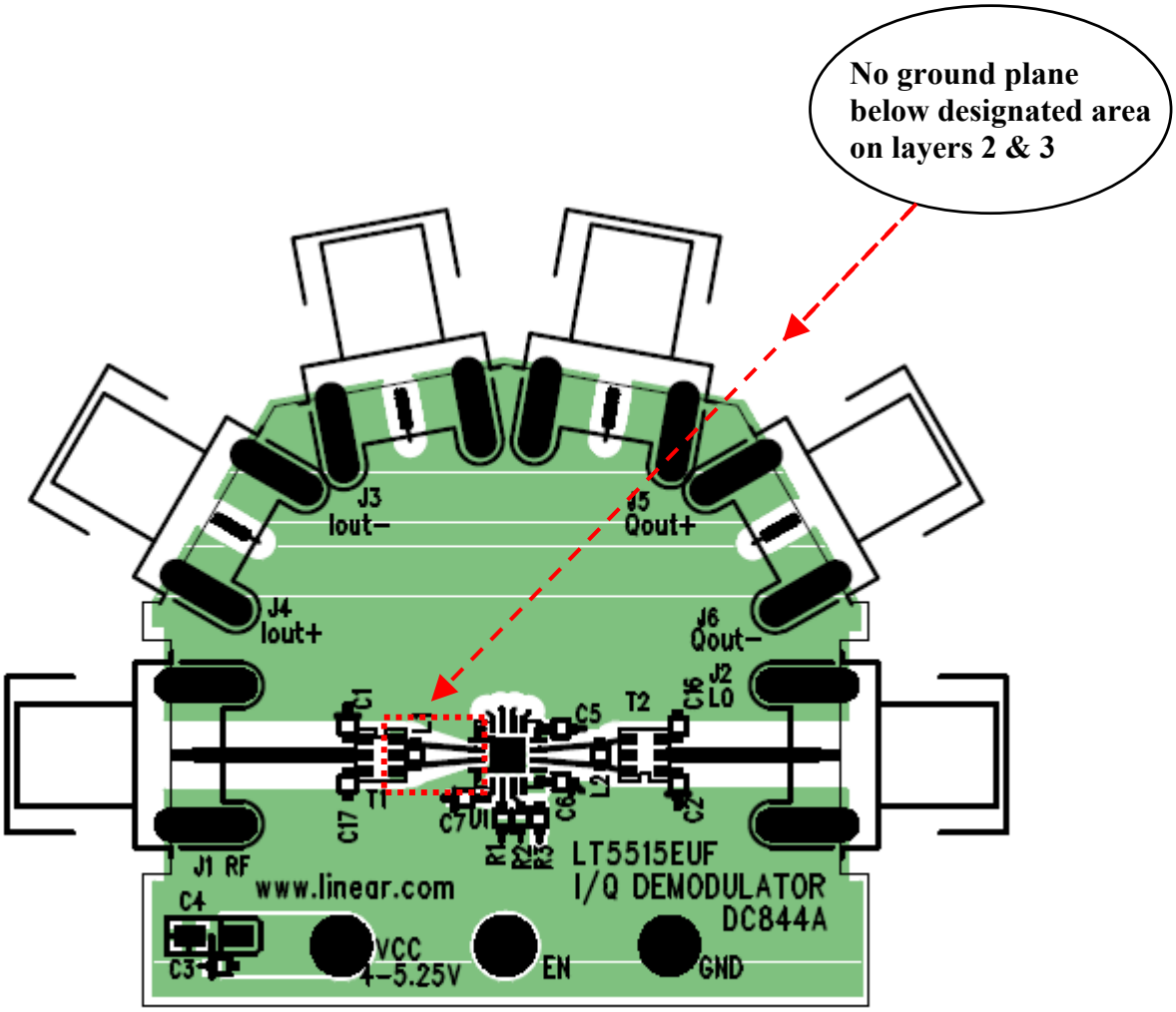
RF leakage to the LO port may result in IP2 degradation. If a large signal interferer leaks from the RF input to the LO port, it can thereby mix with itself. This may produce dynamic DC offset at the BB outputs. Additionally, large signal interferers in the receive band leaking to the LO port can change the phase and/or pull the LO VCO off frequency, degrading the receiver performance.
Suggested actions: Refer to suggested actions in item 1.

5. LT5515 board level considerations & parts placement issues:

- Bypass capacitors (from V_{CC} to ground) should be placed as closely as possible to the designated V_{CC} pins of the IC.
- To minimize coupling between the RF input transformer and LO port transformer, the RF input transformer should be placed about 4.0mm away from the side of the LT5515 package where the RF input pins 2 & 3 are located (measured from the edge of the landing pads of the secondary winding of RF input transformer to the edge of landing pads for pins 2 & 3 of the LT5515 IC). The secondary of the RF input transformer should be connected to the RF input pins with narrow microstrip lines, 0.2mm wide. This minimizes the coupling between the RF input transformer and the external transformer used at the LO input port. The differential shunt inductor at pins 2 & 3 of the LT5515 should be placed as close as possible to the landing pads of the secondary winding of the RF input transformer.
- Depending on the PCB structure, the landing pads of the secondary winding of the RF transformer and the landing pads of the LT5515 differential RF input may have some parasitic shunt capacitance to ground. In conjunction with the LT5515 package's RF input bond wires, this can form a very high frequency tank circuit, which may result in an out-of-band (5GHz – 9GHz) self-oscillation of the LT5515's RF input buffer stage. Such an oscillation would degrade important parameters of the LT5515 including IP2 and IP3. The area surrounding the IC's RF inputs (including input solder pads) and their connecting traces to the RF input transformer, should not have any ground plane on layers 2 and 3 (4-layer printed circuit board, 0.062-inch total PCB thickness), refer to Figure 1 and demo board layout. Additionally the ground plane on the top layer of the PCB should have a keep-out of about 0.5 to 0.7mm for the area from the IC's RF inputs to the RF transformer (also refer to Figure 1 and demo board layout). This will effectively minimize the parasitic shunt capacitance of the landing pads of the secondary winding of the RF transformer and the landing pads of LT5515 differential RF input.

  Note: The LTC LT5515 demo board is a 4-layer PCB structure, 62 mils thick total. Layer 1 and layer 2 are separated by 17 mils. PCB material is FR-4.

For advice about particular PCB layout questions involving the LT5515, consult the factory.


No ground plane
below designated area
on layers 2 & 3
J3
Iout–
J5
Qout+
J4
Iout+
J6
Qout–
J2
LO
C1
C5
T2
C16
L1
L2
C2
T1
C17
C7
U1
C6
R1
R2
R3
J1 RF
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LT5515EUF
I/Q DEMODULATOR
DC844A
C4
C3
VCC
4–5.25V
EN
GND

Figure 1