AN-1599
APPLICATION NOTE

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IEC 61000-4-x and CISPR 11 Tested Analog Output Design with the AD5758 for Industrial Process Control Applications

by Li Ke

INTRODUCTION

The AD5758 is a single-channel, 16-bit, voltage and current output digital-to-analog converter (DAC) with on-chip dynamic power control (DPC) and HART® connectivity. The AD5758 is designed to work with programmable logic controller (PLC) and distributed control system (DCS) modules of the industrial process control applications.

This application note describes an electromagnetic compatibility (EMC) tested solution of the AD5758 output voltage (V_{OUT}) and output current (I_{OUT}) for industrial process control with dynamic power control. The IEC 61000-4-x set of standards cover the evaluation of the immunity of electrical and electronic equipment at a system level.

The AD5758 EMC test board is characterized to ensure that the circuit performance is not affected by radiated RF or conducted RF disturbances, and has sufficient immunity against electrostatic discharge (ESD), electrical fast transients (EFT), and surge. The EMC test board was also tested per the CISPR 11 standard, in which the radiated emissions of the board fell well below the Class A limits.

Refer to the AN-2046 Application Note, *IEC 61000-4-x and CISPR 11 Tested Analog Output Design with the AD5758 and ADP1031 for Industrial Process Control Applications*, for comparable AD5758 immunities and improved electromagnetic interference (EMI) performance. The AN-2046 application note describes testing the AD5758 EMC test board (EVAL-AD5758EMCZ) with the ADP1031, and provides a bill of materials variant of the AD5758 that implements power and digital isolation with the ADP1031, which passes the CISPR 11 Class B limits with a greater than 9 dB margin.

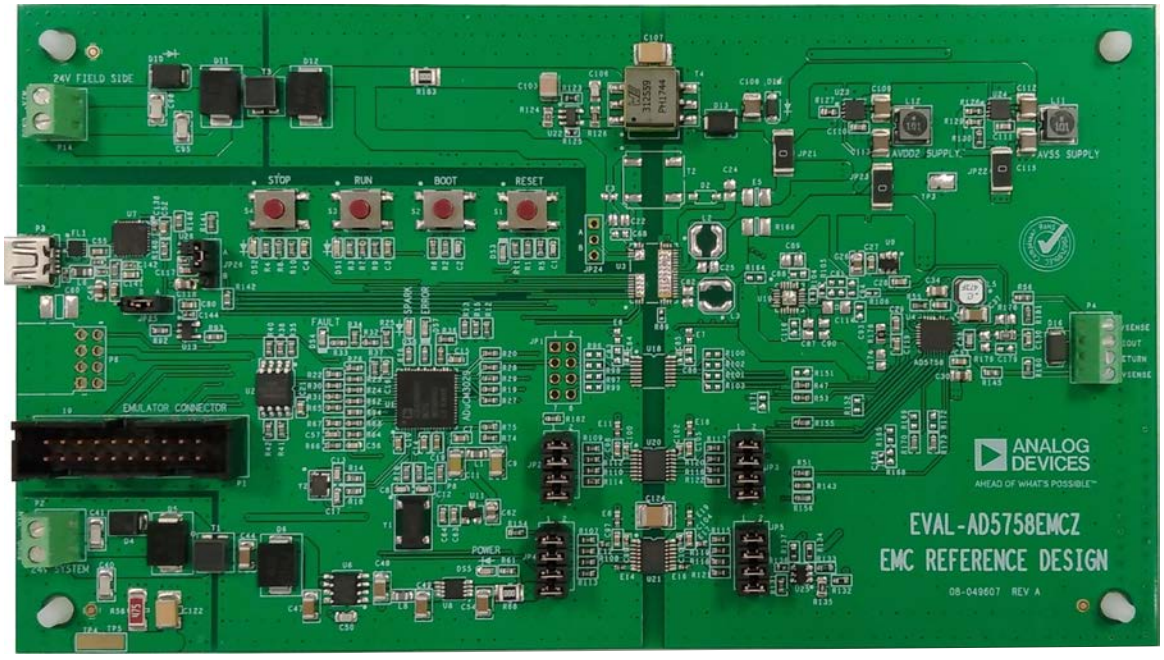

Figure 1. AD5758 EMC Test Board Photograph

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6/2019—Rev. 0 to Rev. A

Changed AD5758 ADC Description Section to AD5758 DAC Description Section 3
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3/2019—Revision 0: Initial Version

SYSTEM DESIGN

AD5758 DAC DESCRIPTION

The AD5758 is a single-channel, voltage and current output DAC that operates with a 60 V maximum operating voltage between the AV_{SS} and AV_{DD1} rails. The on-chip DPC minimizes package power dissipation, which is achieved by regulating the supply voltage (V_{DPC+}) to the VI_{OUT} output driver circuitry from 5 V to 27 V using a buck dc-to-dc converter. The C_{HART} pin enables a HART signal to couple to the current output.

The device uses a versatile, 4-wire serial peripheral interface (SPI) that operates at clock rates of up to 50 MHz and is compatible with standard SPI, QSPI™, MICROWIRE™, DSP, and microcontroller interface standards. The interface also features an optional SPI cyclic redundancy check (CRC) and a watchdog timer (WDT). The AD5758 offers diagnostic features, such as output current monitoring and an integrated 12-bit diagnostic analog-to-digital converter (ADC). Additional robustness is provided by the inclusion of a fault protection switch on the VI_{OUT}, $+V_{SENSE}$, and $-V_{SENSE}$ pins.

For full details, refer to the AD5758 data sheet.

CIRCUIT DESCRIPTION

This circuit is a single-channel, isolated, industrial voltage and current output module for harsh EMI/EMC environments featuring the AD5758 DAC. This design is targeted for PLC and DCS applications. The AD5758 EMC test board is designed to satisfy the IEC 6100-4-x and CISPR 11 standards intended for use in harsh industrial environments that is stated in the IEC 61000-6-2 generic standard.

The AD5758 EMC test board is a bill of materials variant of the AD5758 EMC test board with the ADP1031. See the AN-2046 application note for more information. These two boards are assembled on the same blank printed circuit board (PCB). The only difference with the AD5758 EMC test board in this application note is that the functions of the ADP1031 is replaced with the discrete power and digital isolation implementation from the LT8300, ADP2360, ADuM141D, ADuM142D, and ADM6339.

Powering the Design

The AD5758 EMC test board is powered by two separate supplies. The first 24 V input is supplied to the LT8300, which generates an isolated 20 V and powers the AV_{DD1} pin of the AD5758. The output from the LT8300 also supplies two ADP2360 devices, which supply the voltage for the AV_{DD2} and AV_{SS} pins of the AD5758. The second 24 V supply powers the circuits on the system side domain, including the microprocessor and digital isolator. The ADP7142 steps the 24 V supply down to 5 V, which supplies the circuits where 5 V logic or 5 V power is required. A low dropout (LDO) regulator, the ADP124, further regulates the 5 V supply to 3 V for low power components, including the ADuCM3029. The AD5758 EMC test board can operate from a single 24 V supply, but the two 24 V supplies must be isolated from each other to demonstrate that the system power and the field power are separate power supplies. The two 24 V supplies are meant to mimic the typical use case, where the system power and the field power are supplied separately within the system.

Isolation Considerations

A properly placed isolation barrier is often the first method used to improve EMC robustness. The ADuM141D and ADuM142D provide electrical isolation between the field side AD5758 and the system side microcontroller unit (MCU). Take precautions to achieve optimal EMC and EMI performance. For optimum radiated emission performance, it is recommended to connect an inductor and capacitor (LC) filter consisting of a ferrite bead and 100 nF and 10 nF capacitors in parallel to each other, decoupling the VDD1 and VDD2 pins. A 0.001 µF ceramic capacitor across the isolation barrier also reduces the radiated emission. See the AN-1109 Application Note, *Recommendations for Control of Radiated Emissions with iCoupler Devices*, for more details.

The LT8300 isolated flyback converter drives a flyback transformer. A 3.3 nF, 3 kV capacitor across the primary and secondary side provides a return path for the image current. The LTspice® software simulates the LT8300 circuit if component substitutions are needed and is available for download from the LTspice page on the Analog Devices, Inc., website.

The ADuCM3029 ultra low power Arm® Cortex®-M3 MCU provides local control and data communication for the AD5758 EMC test board. The ADuCM3029 has an acceptable emission profile and has adequate immunity in the IEC 61000-4-x tests.

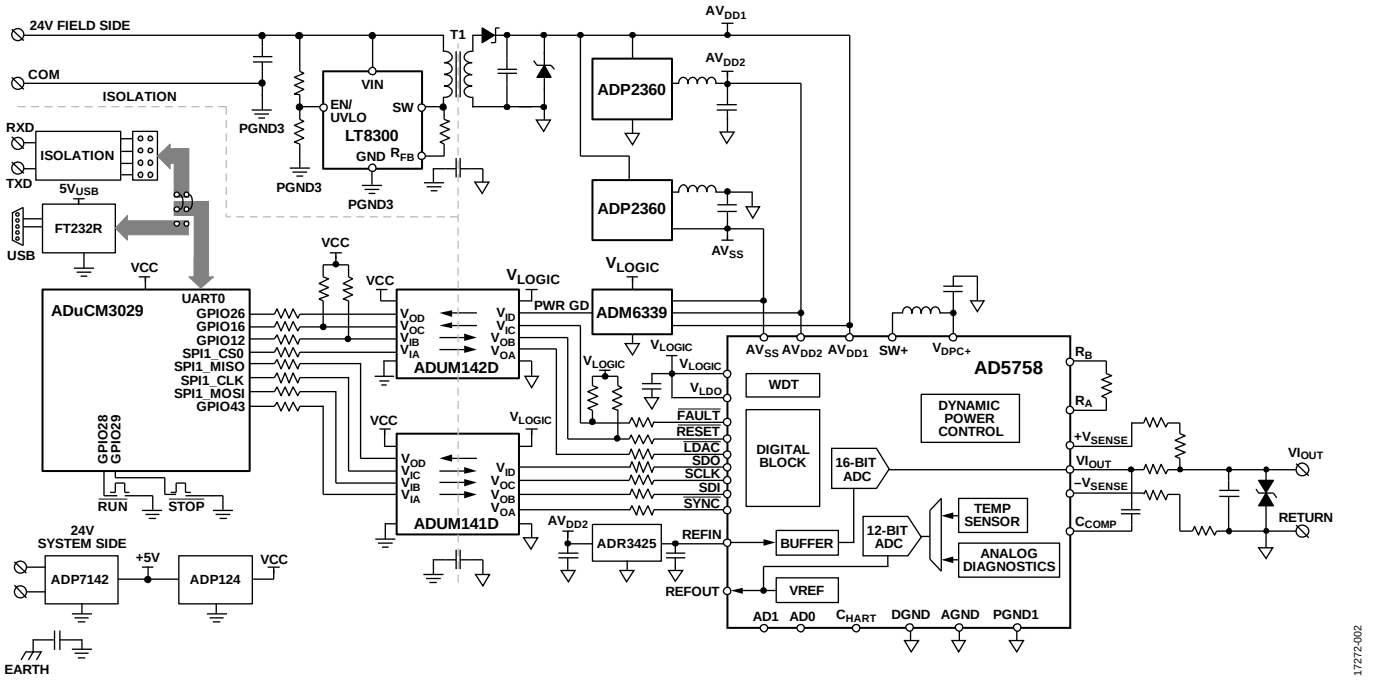

Figure 2. AD5758 EMC Test Board in Circuit

PRINTED CIRCUIT BOARD

The AD5758 EMC test board is built on a FR4 4-layer printed circuit board (PCB). The primary side and the secondary side of the PCB have 0.5 oz copper foil, and the internal layers are on 1 oz copper. The PCB stack is illustrated in Figure 3.

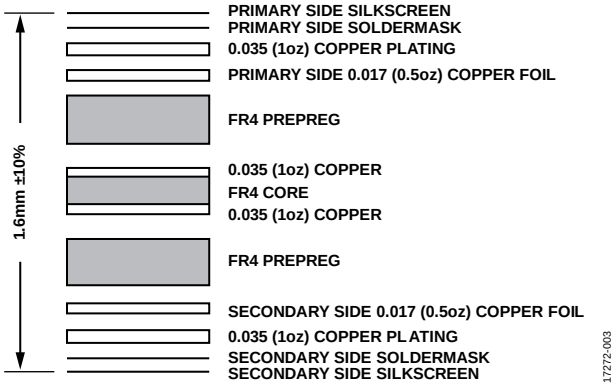

Figure 3. PCB Stack

COMPONENT PLACEMENT AND LAYOUT CONSIDERATIONS

This section describes design considerations for optimal EMC and EMI performance of the AD5758 with the minimum mandatory components (general recommendations on component placement, and distances from connector).

Place the digital interface side of AD5758 close to the isolators. The damping resistors (around a few tens of ohms to hundreds of ohms) on the digital lines attenuate the electrical transients due to the CMOS switching on and off, which helps to reduce EMI. The VI_{OUT} side of the AD5758 must be close to the 4-pin output terminal block on the edge of the AD5758 EMC test board.

Other Component Considerations

The AD5758 EMC test board uses 0.1 µF, 50 V, X7R, 10%, low equivalent series resistance (ESR) ceramic capacitors in the C0603 footprint for the decoupling capacitors, which is a trade-off among considerations for performance, derating, cost, and space saving. In some cases, when a closer decoupling is required, a 1 nF, 25 V, X7R capacitor in the C0402 footprint is applied.

Voltage Supply Protection

The scope of EMC or EMI evaluation and demonstration focuses on the AD5758 and the companion parts. The two 24 V power supply circuits on the AD5758 EMC test board provide the necessary voltages for the function of the board. The supply circuits are not intended to match the robustness of the power supply module or the backplane supply in the automation control system of a user. Therefore, only basic protections are implemented for these supply circuits. In the 24 V supply for the system side, a 1 nF capacitor is placed next to each pin of the power input terminal to the protected ground, where transient energy can be discharged to the earth ground through a 3.3 nF, 3 kV capacitor.

The 4.7 MΩ resistor bleeds energy to the earth, which can accumulate on the protected ground. A transient voltage suppression (TVS) diode is inserted to prevent miswiring to the power supply input. The TVS diode clamps the transient voltage from going higher than 33 V (nominal). A common-mode inductor attenuates the emissions escaping from the downstream circuits. A second TVS diode is inserted after the inductor to provide further clamping for the transient. The 24 V power supply for the field side has a similar protection scheme.

ESD Protection

The AD5758 EMC test board must have the appropriate ESD protection circuitry. The protection consists of a current-limiting resistor, a transient voltage clamp, and a transient energy diverting capacitor.

There are three minimum mandatory components for the AD5758 EMC and EMI. A 10 Ω resistor, a TVS diode, and a 10 nF, 50 V, X7R capacitor.

The 10 Ω resistor is on the trace between the AD5758 VI_{OUT} pin and the terminal block, which limits the transient current to and from the device. The TVS diode is crucial to clamp the electrical transient on the EVAL-AD5758EMCZ during the EMC events. A TVS diode is inserted between the AD5758 and the output terminal block. The pins of the TVS diode are directly routed to the VIOUT and RETURN screws (on the P4 terminal) with short and heavy traces. A 10 nF, 50 V, X7R capacitor located in parallel to the TVS diode diverts the small amount of high frequency transient to the RETURN screw. Optional clamp diodes connected to the AV_{DD1} and AV_{SS} rails can be added to the VI_{OUT} line to further improve the robustness. However, these diodes are unnecessary for the AD5758 EMC test board because the EMC and EMI performance objectives are met without them.

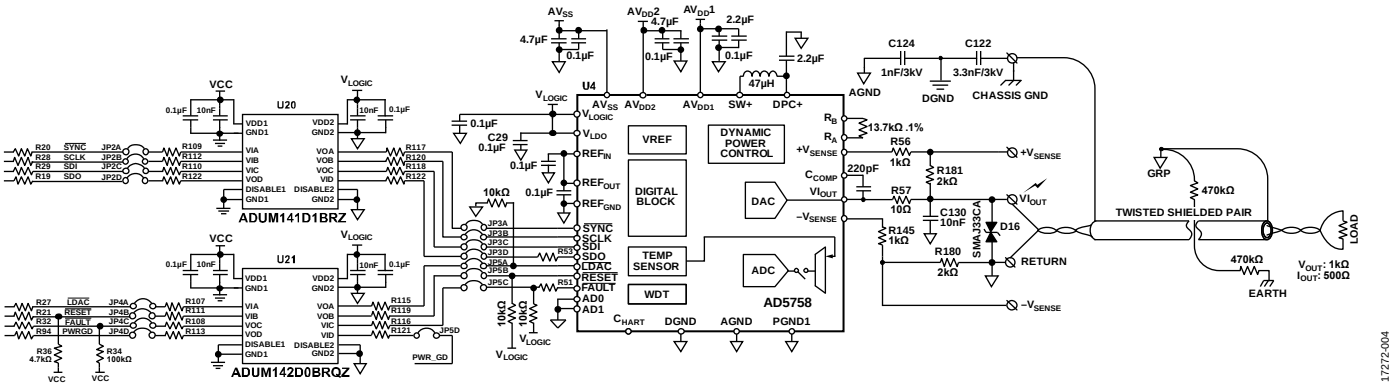

Figure 4. AD5758 Bypass and Peripheral Circuit

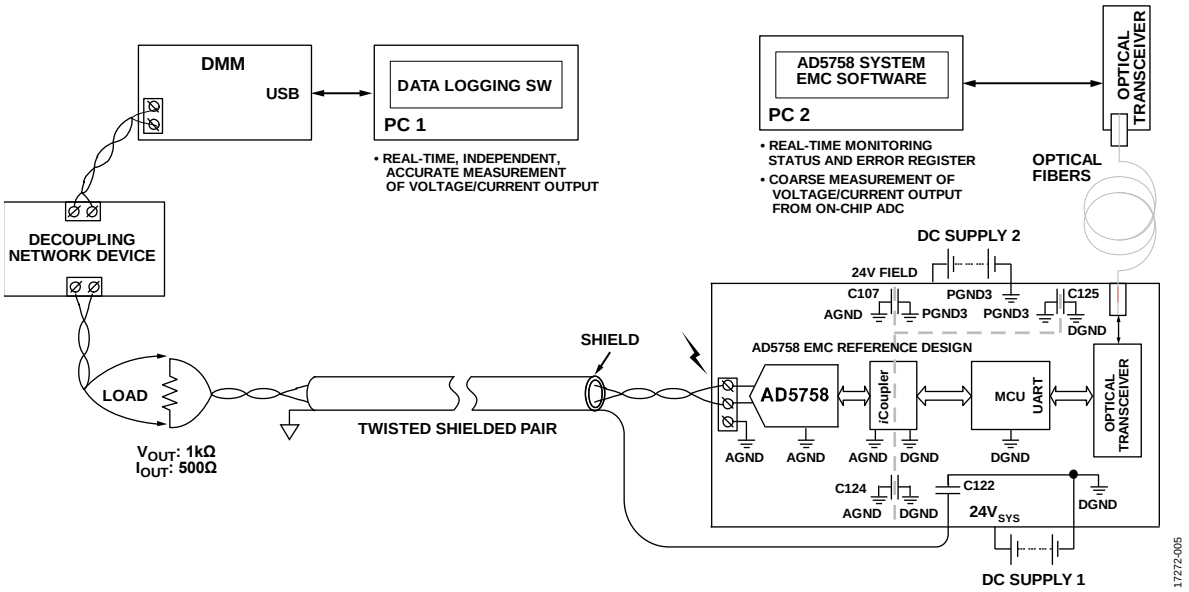

Figure 5. General EMC Test Setup

CIRCUIT EVALUATION AND TEST

The AD5758 reference design is run by being connected to a PC or run in standalone mode. The graphic user interface (GUI) on the PC configures the running parameters, such as DAC output range, output code, and ADC sequencing. The GUI displays the fault flag map and plots the reading from the AD5758 on-chip, diagnostic ADC nodes.

When the operational parameters are programmed in the on-board flash memory, the board can be disconnected from the PC or controller board when the software is operating. To operate the board, power up the board and press the RUN or STOP buttons on the AD5758 EMC test board.

Figure 5 shows the general setup of the AD5758 EMC test board for EMC tests. Before and after each potentially destructive EMC test, the precision bench digital multimeter (DMM) takes 500 measurements of the AD5758 output on the load resistor. The deviation between the two sets of DMM measurements must stay within the predefined range to meet the performance criterion. The maximum allowable deviation is 0.1% of full scale, which aligns with the common requirements of the industrial automation applications.

During the nondestructive EMC tests, the bench DMM continuously measures the AD5758 output on the load resistor. The measurements taken during and after the EMC event are compared to the average of the DMM measurement before the EMC event for judging the performance criterion.

In the emissions test, the AD5758 is configured to output the full-scale voltage or current that is being refreshed at 1 kHz. The AD5758 EMC test board runs in standalone mode. The only auxiliary devices in this setup are two 24 V battery packs that power the AD5758 EMC test board. These battery packs are assumed to not contribute EMI.

SOFTWARE NEEDED

To perform EMC testing on the AD5758, the following software is required:

- Firmware, Revision 57-58-E0-01 on the AD5758 EMC test board
- AD5758 system EMC GUI software, Revision 1.0.0.1
- Keysight Technologies BenchVue™ software, Version 2.6

EQUIPMENT NEEDED

To perform EMC testing on the AD5758, the following equipment is required:

- Optical USB transceiver board
- Industrial fiber optic cable
- PC running Windows® 7, 64-bit version, image model: V3.0.2011.10.14
- DC power supply: Agilent 3630A
- Digital multimeter: Keysight 33470A
- 2 m (1 pair twisted) conductor multiconductor cable: Belden 8761
- Line filter: Schaffner FN353Z-30-33

A load resistor is connected to the AD5758 by a 2 m cable (Belden 8761, twisted, shielded pair). In current output mode, the load is a radial leaded, 500 Ω, ±0.005%, ±0.8 ppm/°C, 600 mW, 300 V foil resistor. In voltage output mode, the load is a radial leaded, 1 kΩ, ±0.01%, ±0.8 ppm/°C, 600 mW, 300 V foil resistor.

A pair of twisted leads, followed by a low-pass filter, probes the voltage across the load resistor. The filter output is wired to the Keysight 33470A DMM with a pair of twisted leads. The DMM integration time is set to a 0.02 power line cycle (400 µs). A USB cable connects the DMM to the PC. The AD5758 GUI software monitors the AD5758 status register every 1 ms via the electrically isolated data link.

The AD5758 system EMC GUI software sends parameters to the local microprocessor to write to the AD5758. For each EMC and EMI test item, the AD5758 EMC test board is tested in voltage output mode and current output mode.

Two output conditions are checked in each output mode. The first condition is an alternated write of 0xFFFF and 0x8000 to the AD5758 every 2 sec to verify that the AD5758 output is actively updated according to the input code during the EMC tests. The second condition is a fixed write of 0xFFFF to the AD5758 every 1 ms for the simplified calculation of the AD5758 output deviation, during and after EMC events.

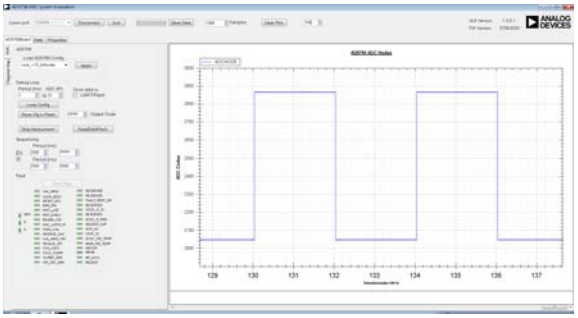

Figure 6. AD5758 System EMC GUI, Toggling Output

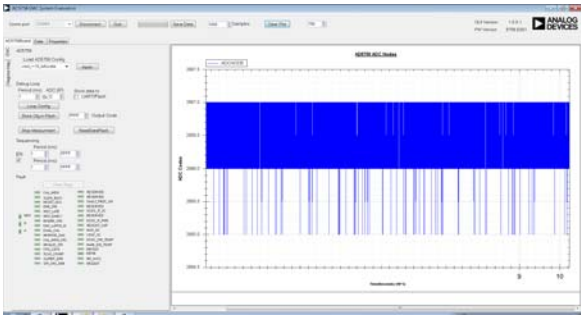

Figure 7. AD5758 System EMC GUI, Stable Output

The AD5758 EMC test board is tested to and meets the CISPR 11 and IEC 61000-4-x standards described in Table 1 and Table 2. Table 3 describes the performance criteria listed in Table 2.

Table 1. Emissions Performance Summary

Test	Basic Standard	Frequency Range (MHz)	Limits	Measured Minimum Margin (dBµV/m)	Result
Radiated Emissions	CISPR 11, Class A	30 to 1000	See Table 11 and Table 12	13.70	Pass

Table 2. Immunity Performance Summary

Test	Basic Standard	Test Levels	Performance Criterion	Measured Minimum Margin	Result
Conducted Immunity	IEC 61000-4-6	10 V/m	A	See Table 4	Pass
Radiated Immunity	IEC 61000-4-3	10 V/m	A	See Table 10	Pass
ESD	IEC 61000-4-2	±6 kV contact	B	See Table 5	Pass
	IEC 61000-4-2	±12 kV air	B	See Table 6	Pass
	IEC 61000-4-2	±30 kV coupling	B	See Table 7	Pass
EFT	IEC 61000-4-4	±4 kV	B	See Table 8	Pass
Surge	IEC 61000-4-5	±4 kV	B	See Table 9	Pass

Table 3. Performance Criteria

Performance Criterion	Description
A	Normal performance within an error band specified by the manufacturer.
B	Temporary loss of function or degradation of performance, which ceases after the disturbance is removed. The equipment under test (EUT) recovers its normal performance without operator intervention.
C	Temporary loss of function or degradation of performance, correction of performance requires operator intervention, such as manual restart, power off, or power on.
D	Loss of function or degradation of performance, which is not recoverable. Permanent damage to hardware or software, or loss of data.

STANDARDS AND PERFORMANCE CRITERIA

The AD5758 EMC test board is designed to pass the EMC and EMI test items and limits, and to meet the performance criteria. The AD5758 EMC test board limits and performance criteria are defined according to the IEC 61000-6-2 and the IEC 61131-2 standards.

According to these standards, the following six applicable tests were selected:

- IEC 61000-4-2
- IEC 61000-4-3
- IEC 61000-4-4
- IEC 61000-4-5
- IEC 61000-4-6
- CISPR 11

EMC AND EMI MEASUREMENT RESULTS OF THE AD5758 EMC TEST BOARD

CONDUCTED IMMUNITY

As per IEC 61000-4-6, the EUT is placed on an insulating support that is 0.1 m high above a ground reference plane. All cables exiting the EUT are supported at a height of at least 30 mm above the ground reference plane. The interference is injected with a coupling and decoupling network (CDN), 801A. The cable is decoupled by an attenuation clamp, KEMZ 801A. The frequency range is swept from 150 kHz to 80 MHz (10 V/m) with the disturbance signal of 80% amplitude modulated with a 1 kHz sine wave. The step size is 1% of the start and thereafter 1% of the preceding frequency value where the frequency is swept incrementally. The dwell time of the amplitude modulated carrier at each frequency is 1 sec.

Table 4. IEC 61000-4-6 Test Levels and Results

Output Mode	Average Before Zap	During Zap		Average After Zap	Deviation of Full Scale (ppm)	Pass or Fail
		Minimum	Maximum			
V_{OUT} = 10 V	10.006514 V	10.006716 V	10.006716 V	10.006529 V	−29, +20	Pass, Criterion A
I_{OUT} = 20 mA	19.969723 mA	19.969090 mA	19.970795 mA	19.969397 mA	−32, +54	Pass, Criterion A

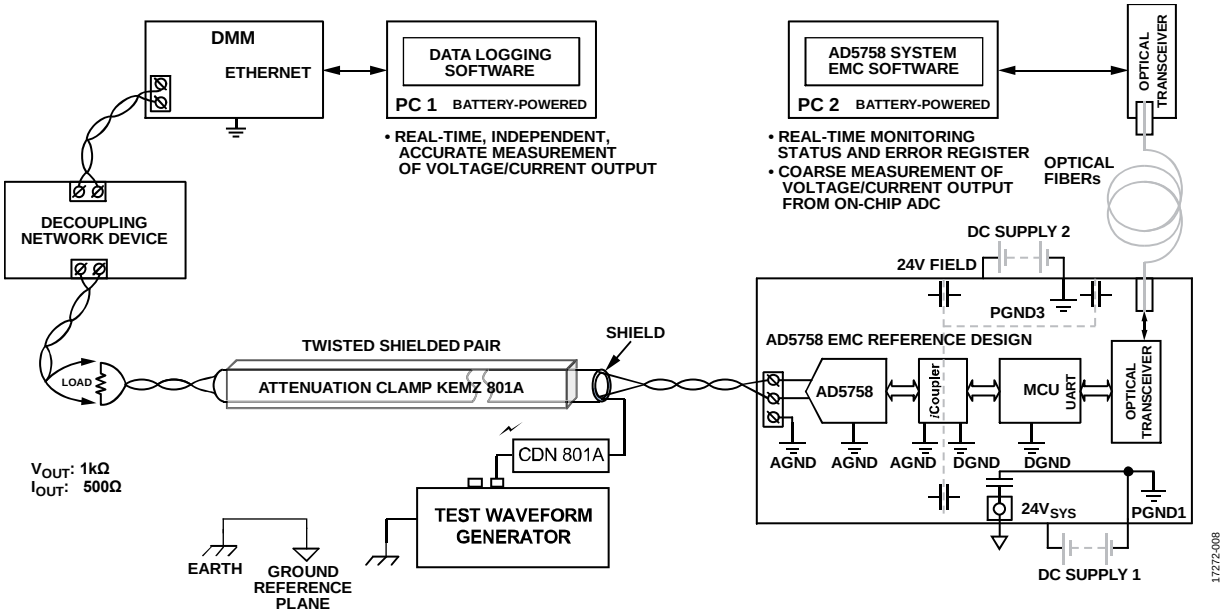

Figure 8. IEC 61000-4-6 Test Setup Connection Diagram

Figure 9. IEC 61000-4-6 Test Setup Photograph

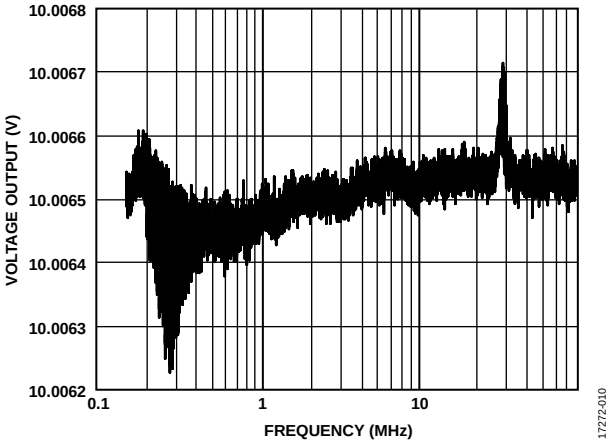

Figure 10. Voltage Output vs. Frequency, Below 10 V/m

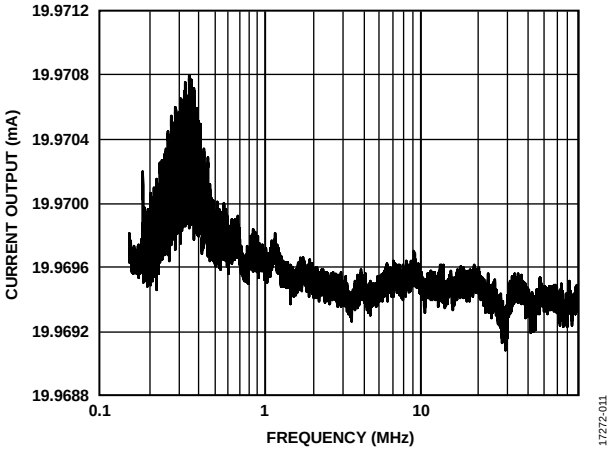

Figure 11. Current Output vs. Frequency, Below 10 V/m

IMMUNITY TO ESD

The test setup consists of a nonconductive table with a height of 0.8 m, standing on the ground reference plane. A 1.6 m × 0.8 m horizontal coupling plane (HCP) is placed on the table. The EUT and its cable are isolated from the coupling plane by an insulating mat that is 0.5 mm thick.

The contact discharges are applied to the VIOUT and RETURN terminal screws of the AD5758 output terminal block (P4). For the contact ESD tests, the EUT is exposed to at least 20 discharges at each rating, 10 each at the negative and positive polarity. The discharges are repeated at a rate of one discharge per second.

The air discharges are applied to the AD5758 output terminal block. For the air ESD tests, the EUT is exposed to at least 20 discharges at each rating, 10 each at the negative and positive polarity. The discharges are repeated at a rate of one discharge per second.

The coupling discharge are applied to the horizontal and vertical coupling planes. For the coupling EST tests, the EUT is exposed to at least 20 discharges at each rating, 10 each at negative and positive polarity. The discharges are repeated at a rate of one discharge per second. The coupling plane has two 470 kΩ bleeding resistors to earth ground.

Table 5. IEC 61000-4-2 Test Levels and Results of ±6 kV Contact ESD

Test Level	Output Mode	Zap Point on P4	Before Zap	After Zap	Deviation of Full Scale (ppm)	Pass or Fail
6 kV Contact Discharge	V_{OUT} = 10 V	VIOUT terminal screw	10.001216 V	10.001293 V	8	Pass, Criterion B
	V_{OUT} = 10 V	RETURN terminal screw	10.001147 V	10.001239 V	9	Pass, Criterion B
	I_{OUT} = 20 mA	VIOUT terminal screw	19.956612 mA	19.957161 mA	28	Pass, Criterion B
	I_{OUT} = 20 mA	RETURN terminal screw	19.956419 mA	19.957038 mA	31	Pass, Criterion B
−6 kV Contact Discharge	V_{OUT} = 10 V	VIOUT terminal screw	10.000819 V	10.001363 V	54	Pass, Criterion B
	V_{OUT} = 10 V	RETURN terminal screw	10.000869 V	10.001367 V	50	Pass, Criterion B
	I_{OUT} = 20 mA	VIOUT terminal screw	19.956516 mA	19.957777 mA	63	Pass, Criterion B
	I_{OUT} = 20 mA	RETURN terminal screw	19.956556 mA	19.957870 mA	66	Pass, Criterion B

Table 6. IEC 61000-4-2 Test Levels and Results of ±12 kV Air ESD

Test Level	Output Mode	Zap Point on P4	Before Zap	After Zap	Deviation of Full Scale (ppm)	Pass or Fail
12 kV Air Discharge	V_{OUT} = 10 V	VIOUT terminal block	10.001441 V	10.001436 V	−1	Pass, Criterion B
	I_{OUT} = 20 mA	VIOUT terminal block	19.956336 mA	19.956245 mA	−5	Pass, Criterion B
−12 kV Air Discharge	V_{OUT} = 10 V	VIOUT terminal block	10.001404 V	10.001504 V	10	Pass, Criterion B
	I_{OUT} = 20 mA	VIOUT terminal block	19.956207 mA	19.956125 mA	−4	Pass, Criterion B

Table 7. IEC 61000-4-2 Test Levels and Results of ±30 kV Coupling ESD

Test Level	Output Mode	Zap Point	Before Zap	After Zap	Deviation of Full Scale (ppm)	Pass or Fail
30 kV Coupling Discharge	V_{OUT} = 10 V	Horizontal plane	9.964192 V	9.964155 V	−4	Pass, Criterion B
	V_{OUT} = 10 V	Vertical plane	9.963320 V	9.963781 V	46	Pass, Criterion B
	I_{OUT} = 20 mA	Horizontal plane	19.824776 mA	19.824814 mA	2	Pass, Criterion B
	I_{OUT} = 20 mA	Vertical plane	19.824891 mA	19.824977 mA	4	Pass, Criterion B
−30 kV Coupling Discharge	V_{OUT} = 10 V	Horizontal plane	9.964175 V	9.964150 V	−3	Pass, Criterion B
	V_{OUT} = 10 V	Vertical plane	9.963687 V	9.963443 V	−48	Pass, Criterion B
	I_{OUT} = 20 mA	Horizontal plane	19.825065 mA	19.825120 mA	3	Pass, Criterion B
	I_{OUT} = 20 mA	Vertical plane	19.824974 mA	19.824703 mA	−14	Pass, Criterion B

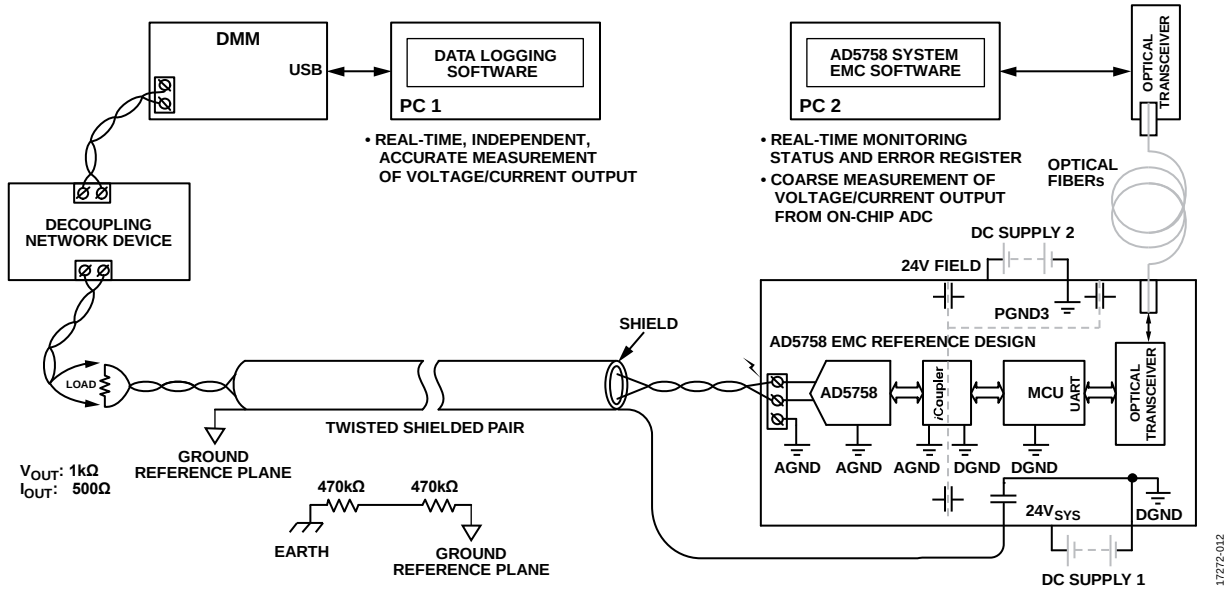

Figure 12. IEC 61000-4-2 Test Setup Connection Diagram, Contact Discharge or Air Discharge

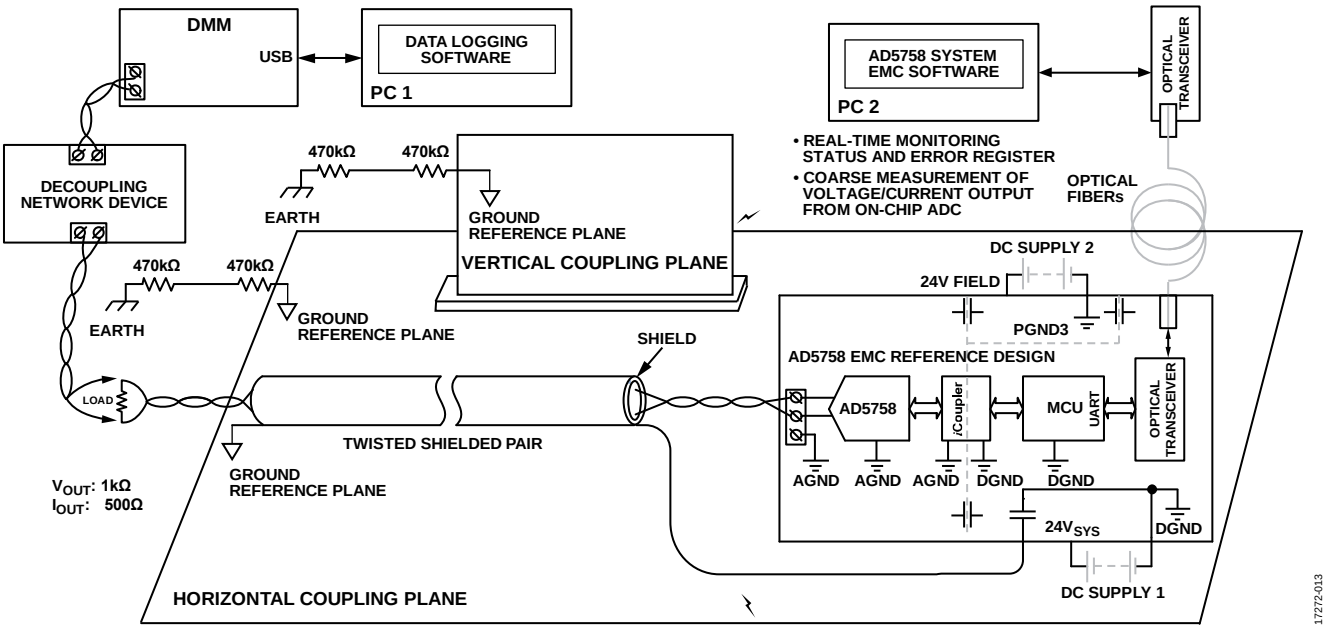

Figure 13. IEC 61000-4-2 Test Setup Connection Diagram, Coupling Discharge

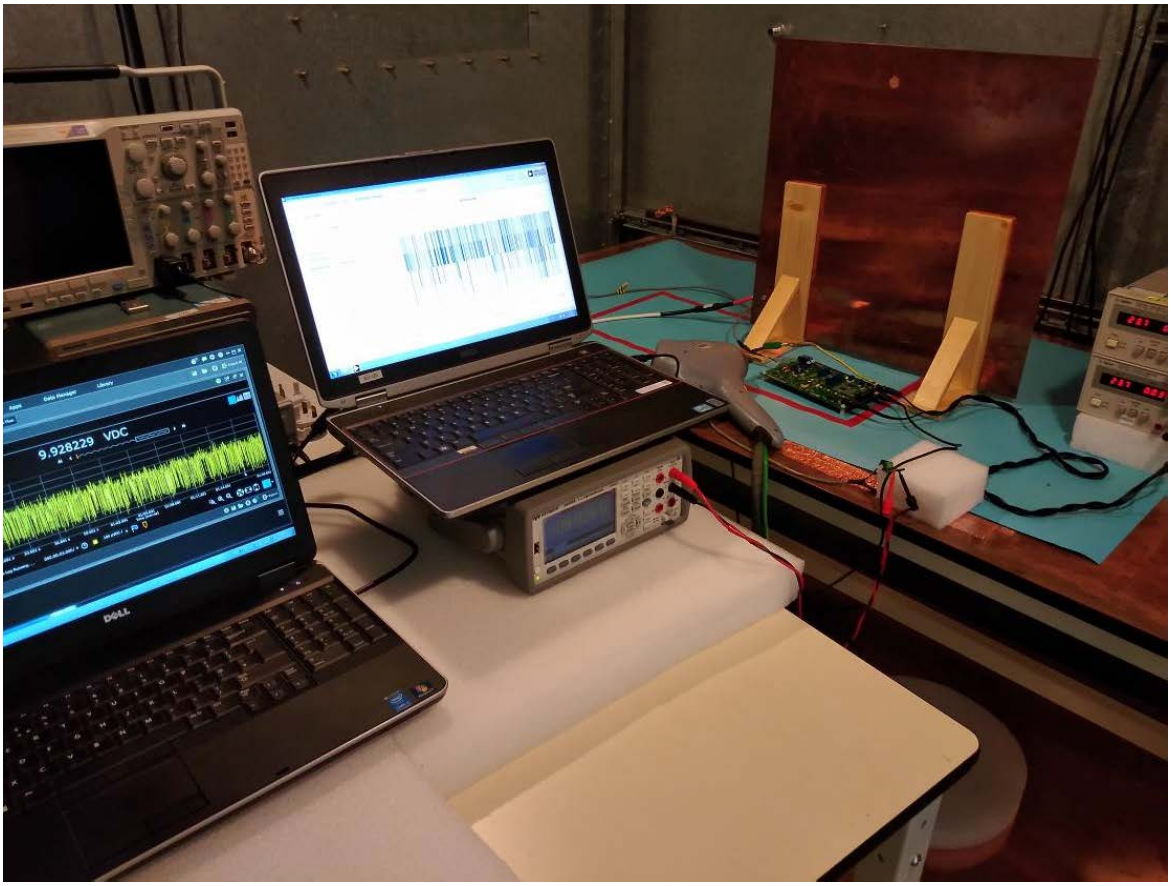

Figure 14. IEC 61000-4-2 Test Setup Photograph

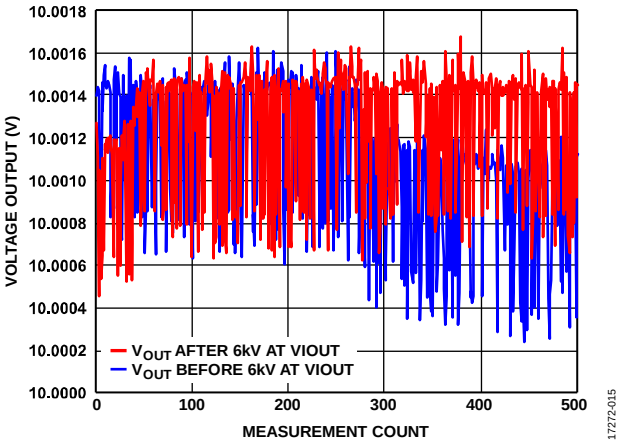

Figure 15. Voltage Output vs. Measurement Count, 6 kV ESD at VIOUT Terminal Screw

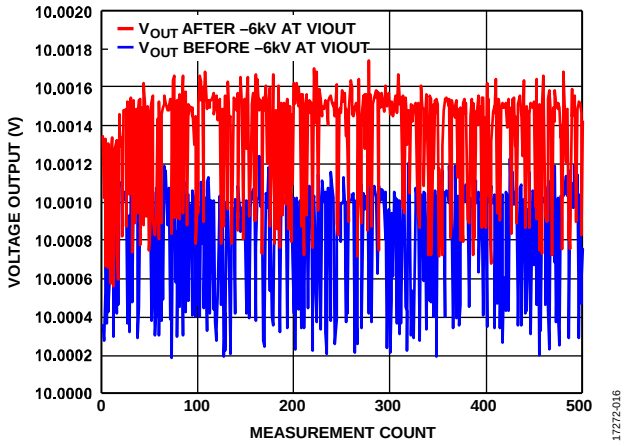

Figure 16. Voltage Output vs. Measurement Count, –6 kV ESD at VIOUT Terminal Screw

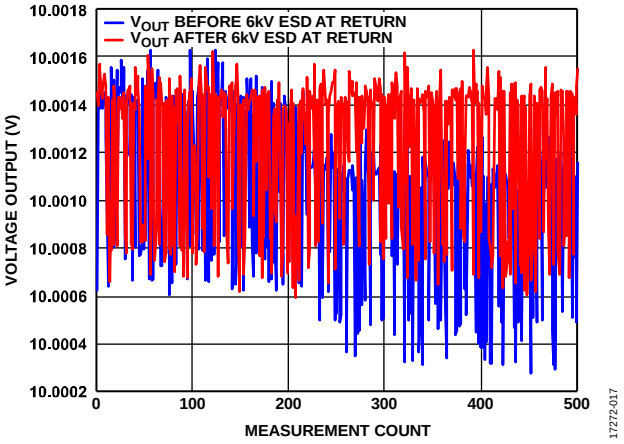

Figure 17. Voltage Output vs. Measurement Count, 6 kV ESD at RETURN Terminal Screw

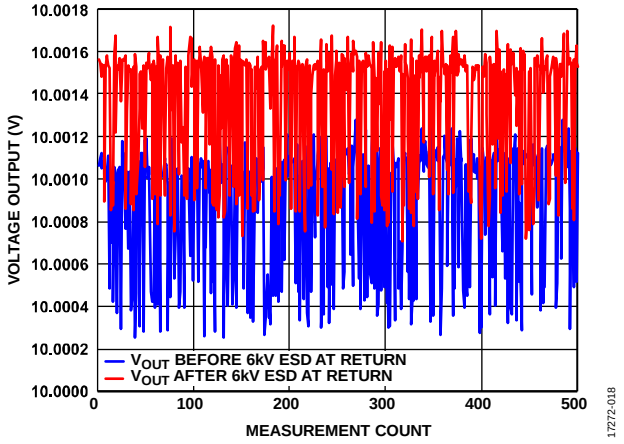

Figure 18. Voltage Output vs. Measurement Count, −6 kV ESD at RETURN Terminal Screw

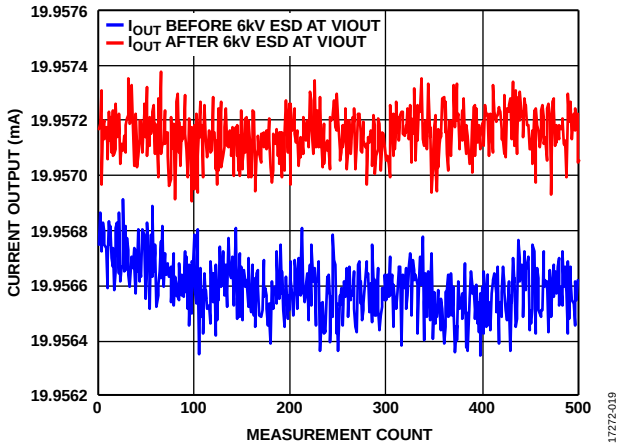

Figure 19. Current Output vs. Measurement Count, 6 kV ESD at VIOUT Terminal Screw

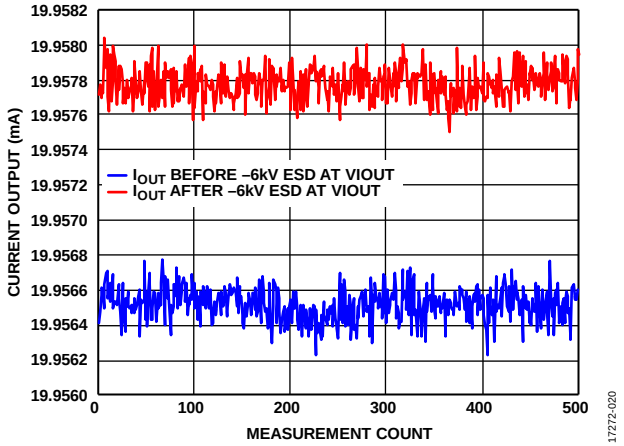

Figure 20. Current Output vs. Measurement Count, −6 kV ESD at VIOUT Terminal Screw

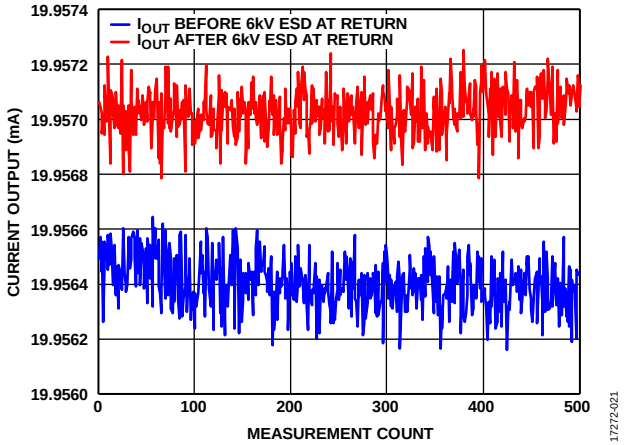

Figure 21. Current Output vs. Measurement Count, 6 kV ESD at RETURN Terminal Screw

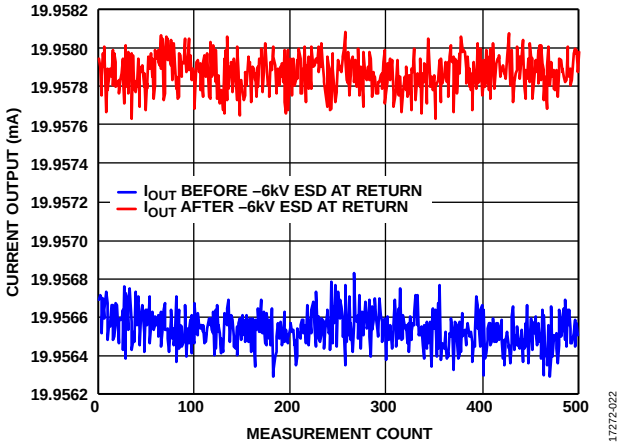

Figure 22. Current Output vs. Measurement Count, −6 kV ESD at RETURN Terminal Screw

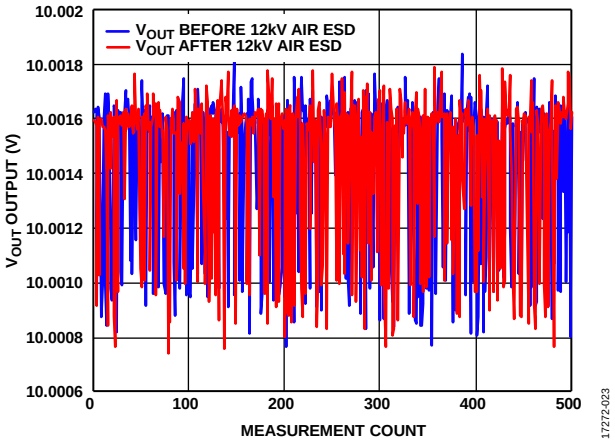

Figure 23. Voltage Output vs. Measurement Count, 12 kV Air ESD

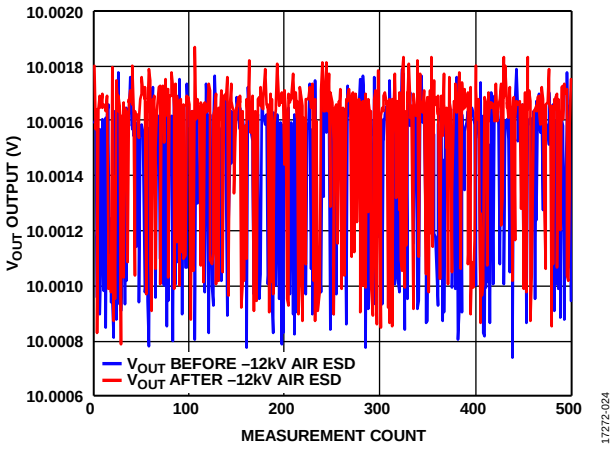

Figure 24. Voltage Output vs. Measurement Count, –12 kV Air ESD

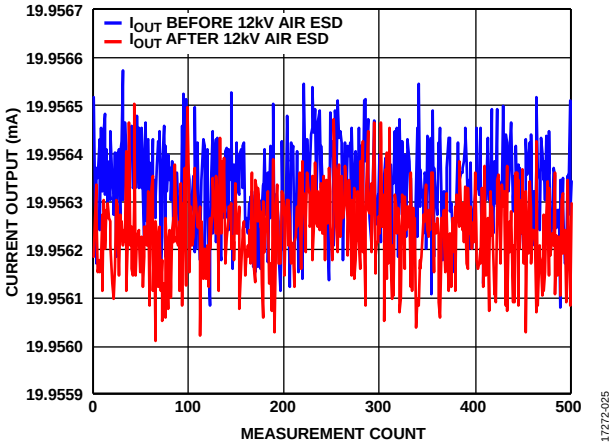

Figure 25. Current Output vs. Measurement Count, 12 kV Air ESD

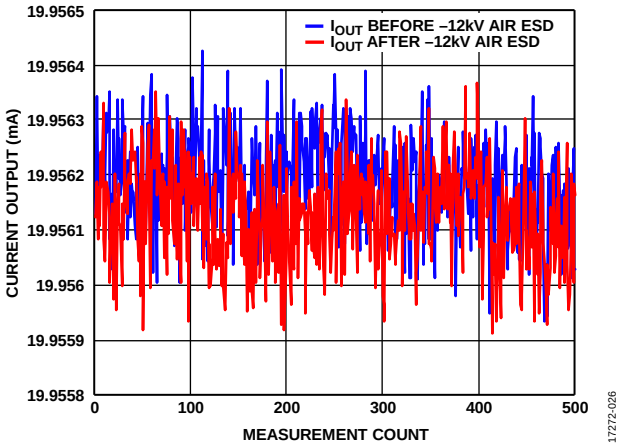

Figure 26. Current Output vs. Measurement Count, –12 kV Air ESD

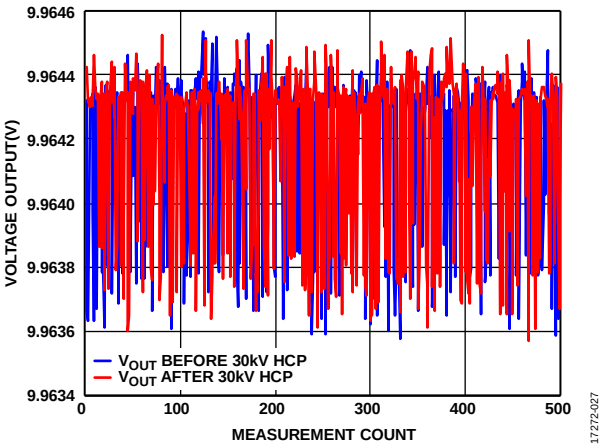

Figure 27. Voltage Output vs. Measurement Count, 30 kV HCP ESD

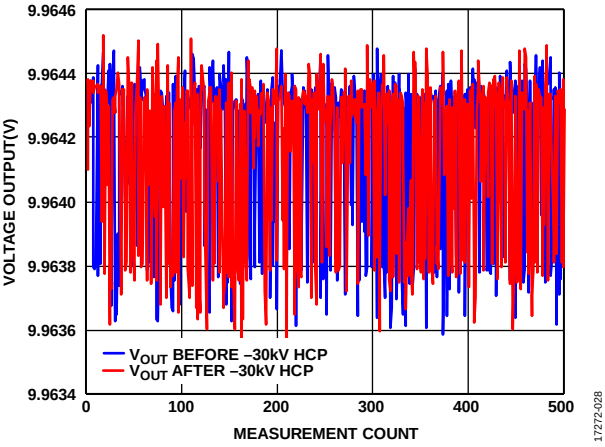

Figure 28. Voltage Output vs. Measurement Count, –30 kV HCP ESD

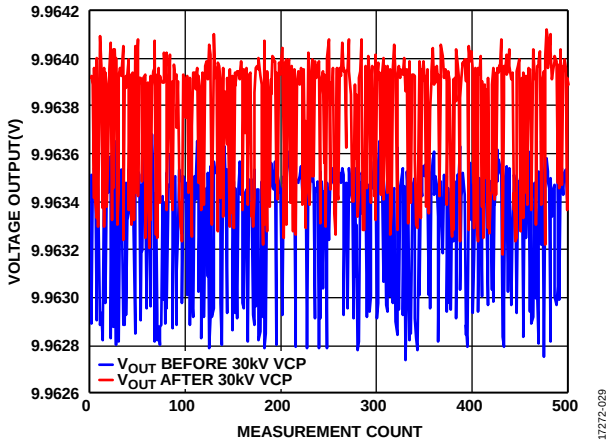

Figure 29. Voltage Output vs. Measurement Count, 30 kV Vertical Coupling Plane (VCP) ESD

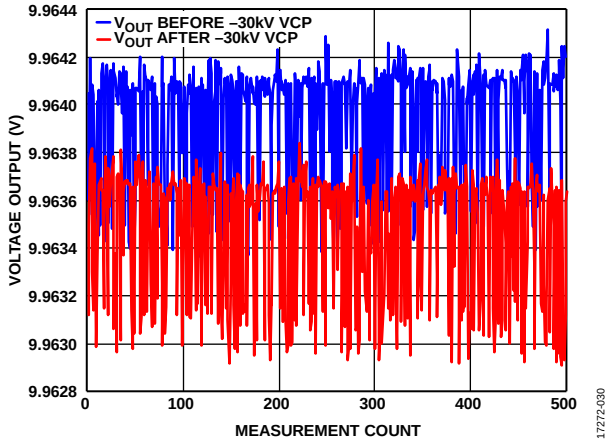

Figure 30. Voltage Output vs. Measurement Count, –30 kV VCP ESD

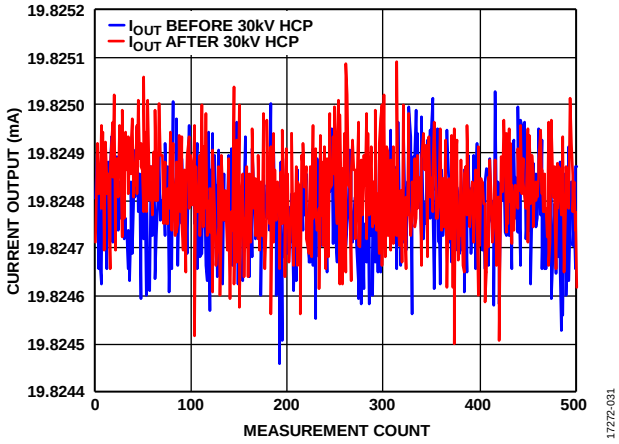

Figure 31. Current Output vs. Measurement Count, 30 kV HCP ESD

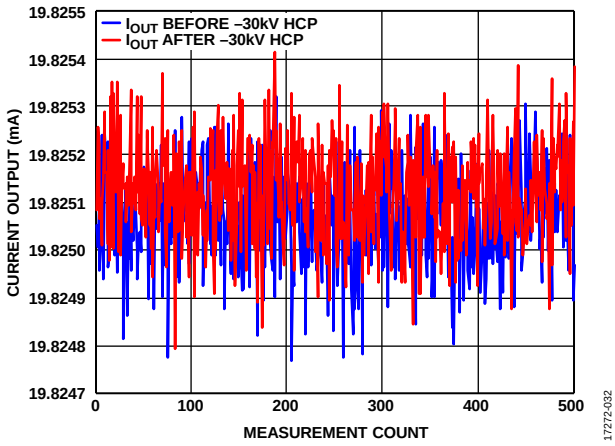

Figure 32. Current Output vs. Measurement Count, –30 kV HCP ESD

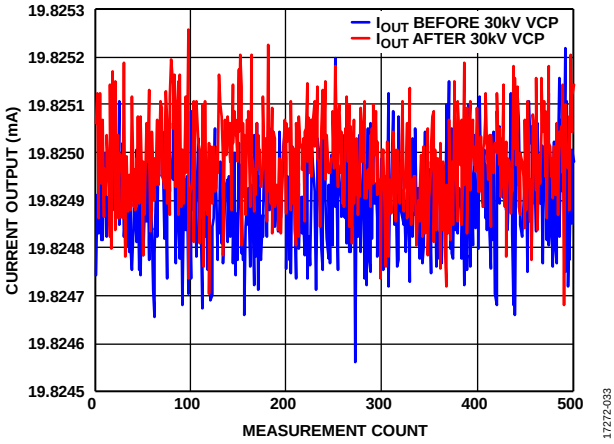

Figure 33. Current Output vs. Measurement Count, 30 kV VCP ESD

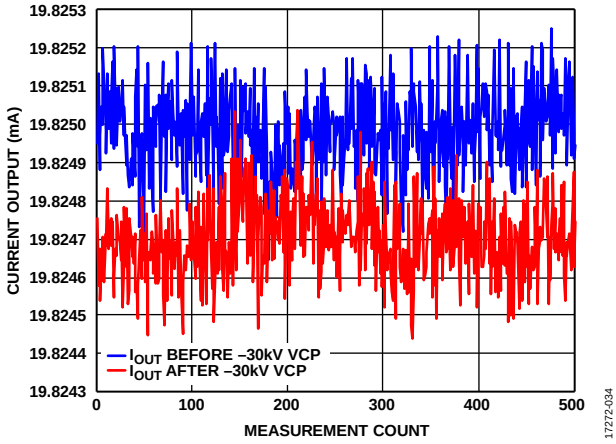

Figure 34. Current Output vs. Measurement Count, –30 kV VCP ESD

IMMUNITY TO ELECTRICAL FAST TRANSIENTS

Per the IEC 61000-4-4 standard, the EUT is tested with 4000 V discharges on the analog input cable. Positive and negative polarity discharges are applied. The length of the hot wire from the coaxial output of the EFT generator to the terminals on the EUT must not exceed 1 m. The duration time of each test sequential is 1 min. The transient and burst waveform is in accordance with IEC 61000-4-4, 5 ns rising time with 50 ns pulse width.

The configuration consists of a 0.8 m high wooden table, covered with a sheet of copper that is at least 0.25 mm thick, and connected to the protective grounding system. The EUT is placed on a 0.1 m thick isolating support. A minimum distance of 0.5 m is provided between the EUT and the walls of the laboratory.

Table 8. IEC 61000-4-4 Test Levels and Results of ±4 kV EFT

Test Level	Output Mode	Before Zap	After Zap	Deviation of Full Scale (ppm)	Pass or Fail
4 kV EFT	V_{OUT} = 10 V	9.964647 V	9.964702 V	6	Pass, Criterion B
	I_{OUT} = 20 mA	19.825442 mA	19.825494 mA	3	Pass, Criterion B
−4 kV EFT	V_{OUT} = 10 V	9.964628 V	9.964722 V	9	Pass, Criterion B
	I_{OUT} = 20 mA	19.825397 mA	19.825398 mA	1	Pass, Criterion B

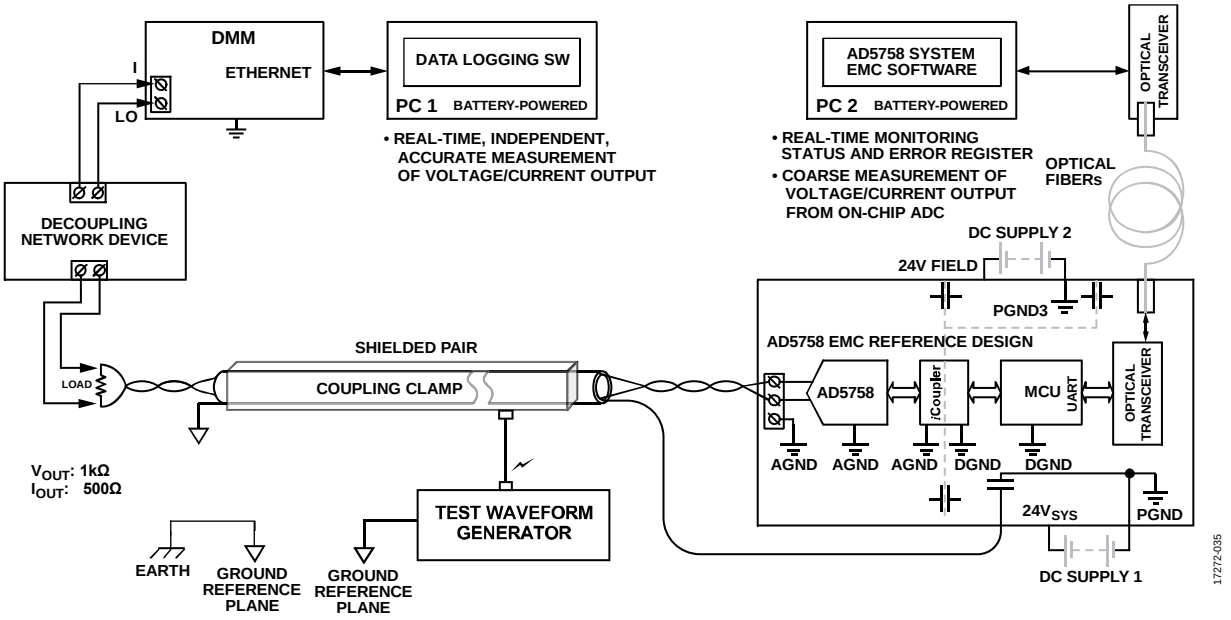

Figure 35. IEC 61000-4-4 Test Setup Connection Diagram

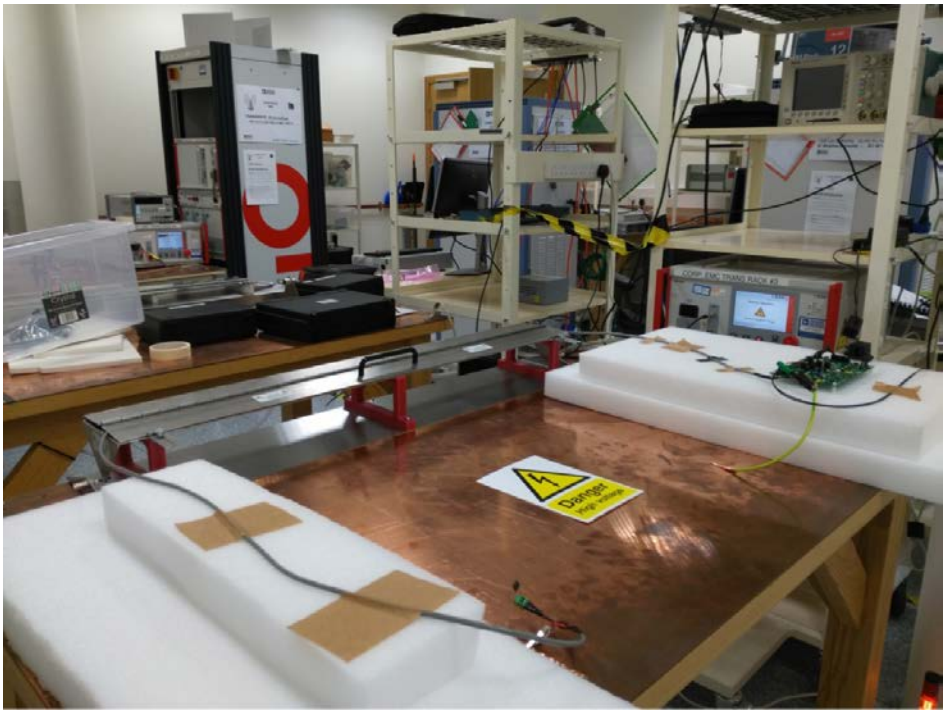

Figure 36. IEC 610004-4 Test Setup Photograph

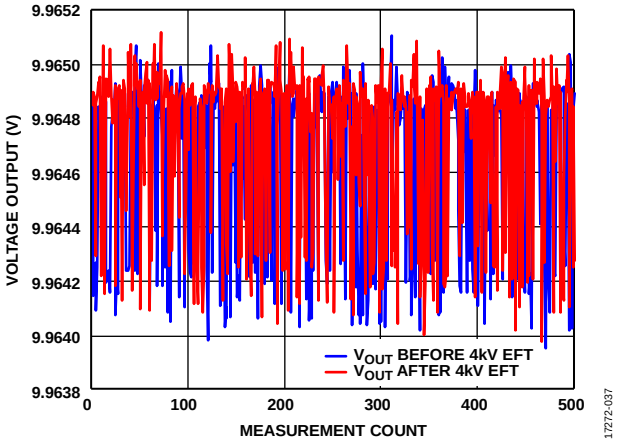

Figure 37. Voltage Output vs. Measurement Count, 4 kV EFT

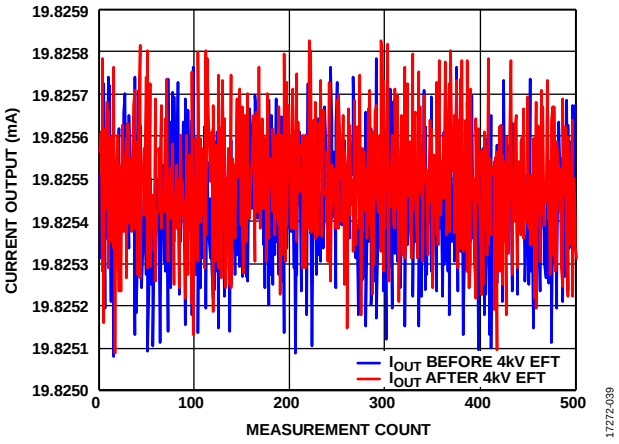

Figure 39. Current Output vs. Measurement Count, 4 kV EFT

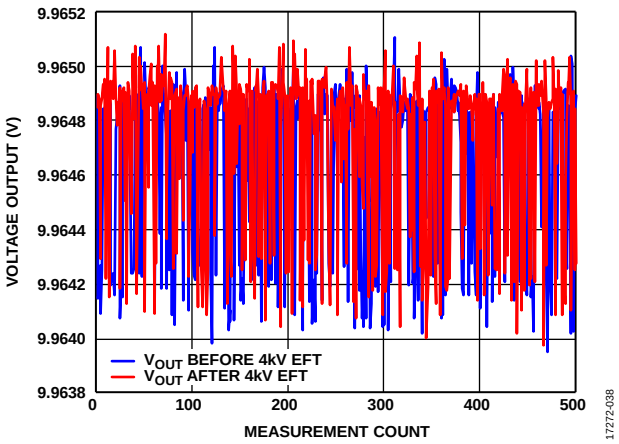

Figure 38. Voltage Output vs. Measurement Count, –4 kV EFT

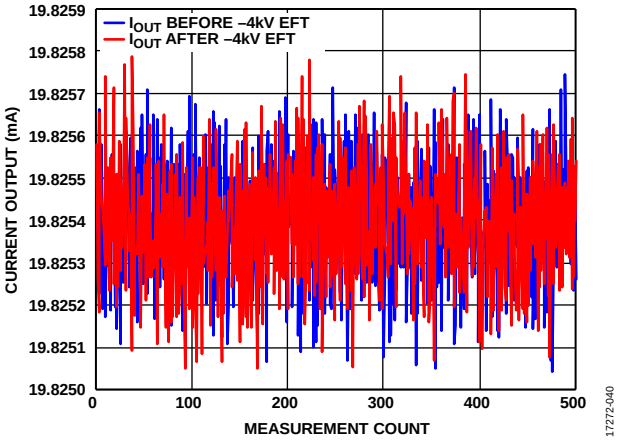

Figure 40. Current Output vs. Measurement Count, –4 kV EFT

IMMUNITY TO SURGE

Per the IEC 61000-4-5 standard for industrial environments, the surge is a combination wave of 1.2 µs rising time with 50 µs pulse width open circuit voltage and 8 µs rising time with 20 µs pulse width short-circuit current. The EUT is subject to five positive and five negative surges at each rating. The interval between each surge is 1 min. The surge is tested to the AD5758 output cable, which is treated as unshielded asymmetrically operated interconnection lines of the EUT. The surge is applied to the lines via capacitive coupling. The CDNs do not influence the specified functional conditions of the EUT. The interconnection line between the EUT and the CDN are 2 m in length or shorter.

Table 9. IEC 61000-4-5 Test Levels and Results

Test Level	Output Mode	Before Zap	After Zap	Deviation of Full Scale (ppm)	Pass or Fail
4 kV Surge	V_{OUT} = 10 V	9.965415 V	9.965475 V	6	Pass, Criterion B
	I_{OUT} = 20 mA	19.825555 mA	19.825508 mA	−2	Pass, Criterion B
−4 kV Surge	V_{OUT} = 10 V	9.965426 V	9.965486 V	6	Pass, Criterion B
	I_{OUT} = 20 mA	19.825489 mA	19.825532 mA	2	Pass, Criterion B

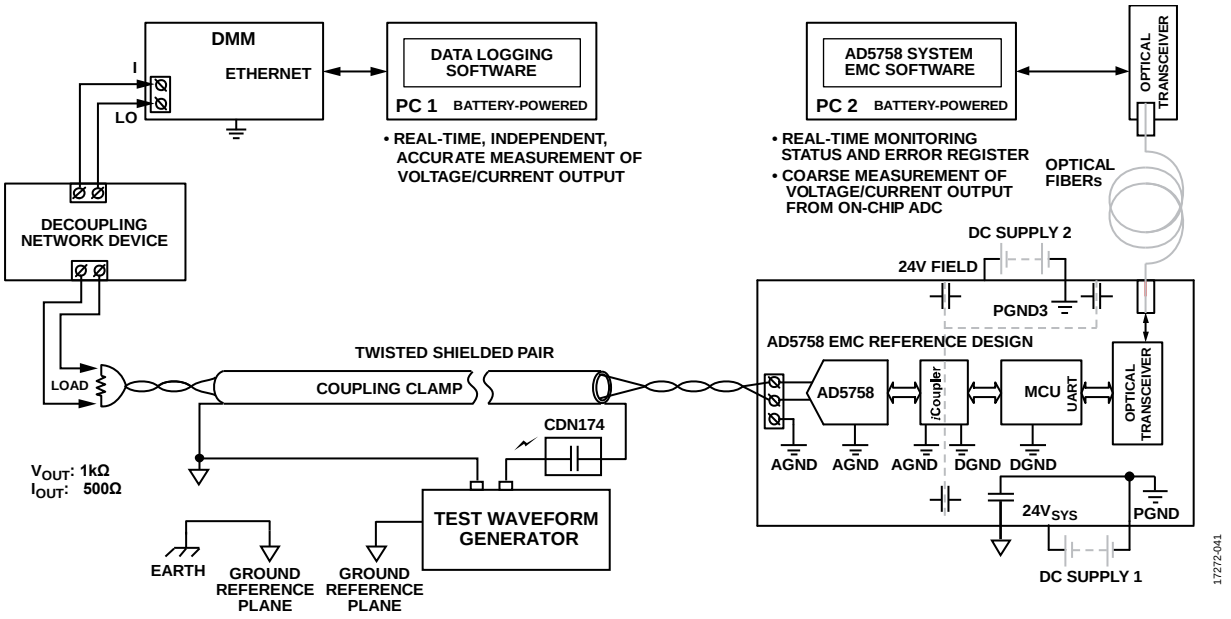

Figure 41. IEC 61000-4-5 Test Setup Connection Diagram

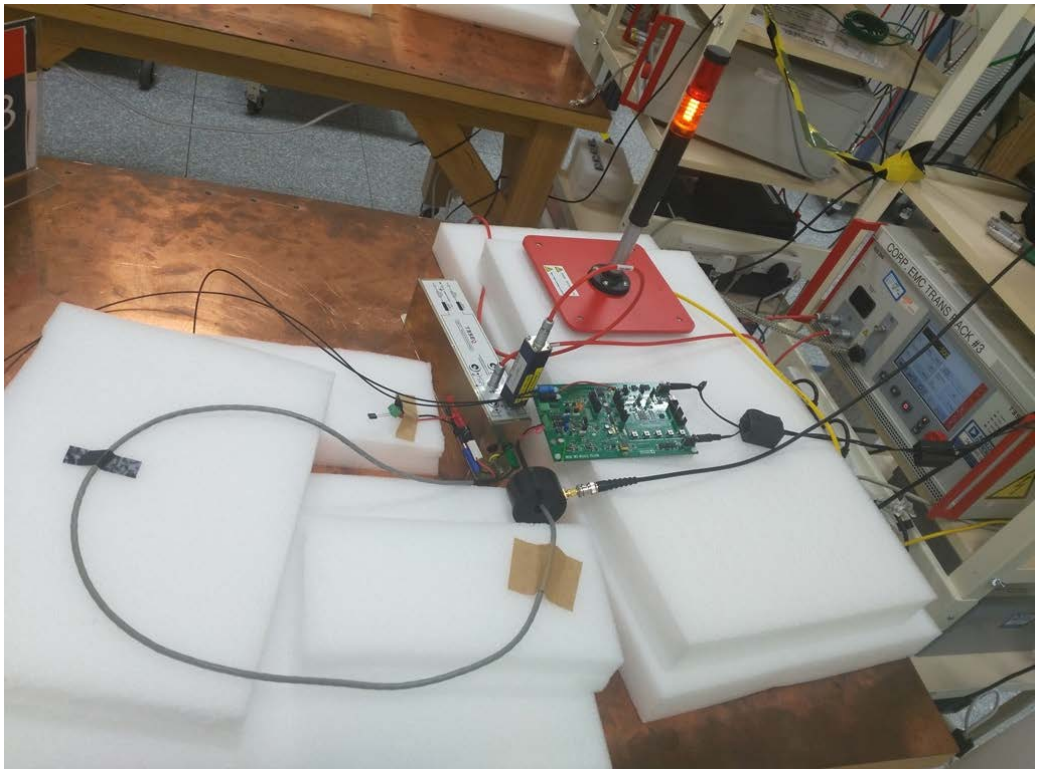

Figure 42. IEC 61000-4-5 Test Setup Photograph

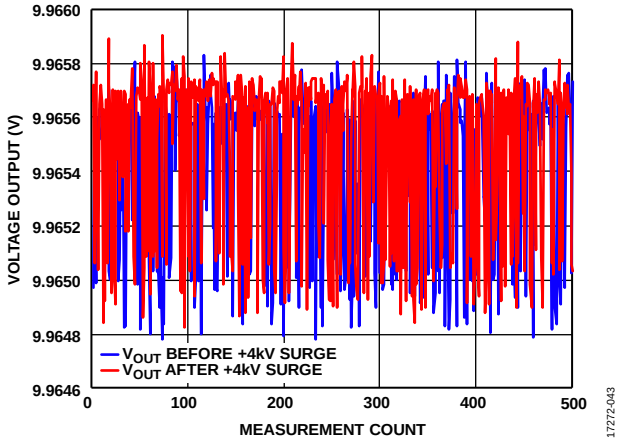

Figure 43. Voltage Output vs. Measurement Count, Below 4 kV Surge

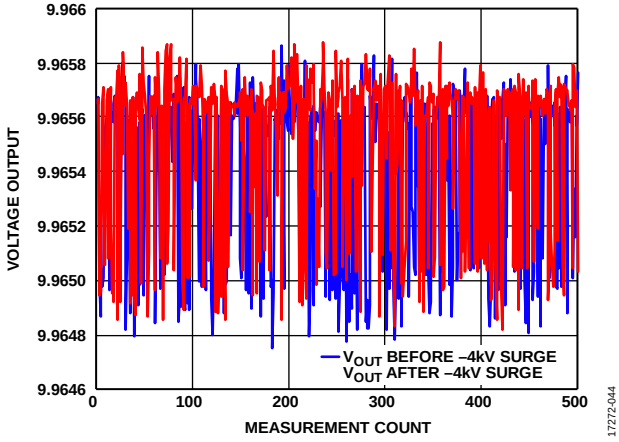

Figure 44. Voltage Output vs. Measurement Count, Below –4 kV Surge

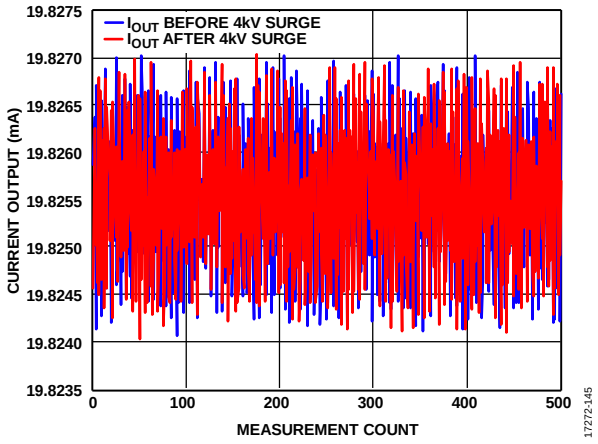

Figure 45. Current Output vs. Measurement Count, Below 4 kV Surge

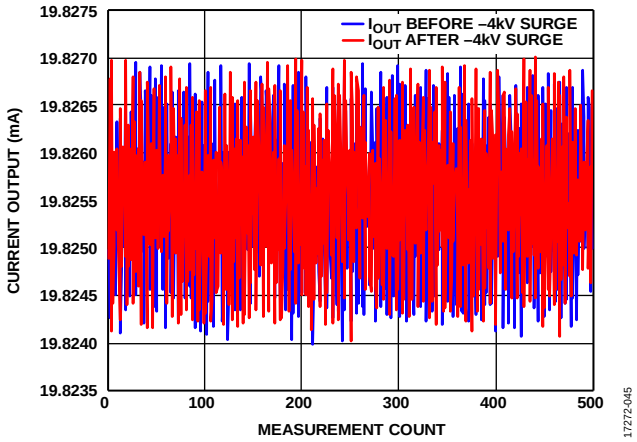

Figure 46. Current Output vs. Measurement Count, Below –4 kV Surge

RADIATED IMMUNITY

Per the IEC 61000-4-3 standard for industrial environments, the test is performed in a fully anechoic chamber. The EUT is placed on a 0.8 m high nonconductive table. A DMM, used as auxiliary equipment, is put in a shielded box under the table and probes the AD5758 output at the load resistor. The DMM measurement data is sent to the PC outside the chamber via an Ethernet cable. The transmit antenna is located 3 m from the EUT. The frequency range was swept from 80 MHz to 1000 MHz, and from 1000 MHz to 6000 MHz with the 80% signal amplitude modulated with a 1 kHz sinewave. The frequency range is swept incrementally, and the step size is 1% of the preceding frequency value. The dwell time at each frequency is 1 sec, which is not less than the time necessary for the EUT to respond. The field strength is 20 V/m in the 80 MHz to 1000 MHz range. The field strength for the 1000 MHz to 6000 MHz range is 10 V/m. The test is performed with the EUT exposed to a vertically and horizontally polarized field.

Table 10. IEC 61000-4-3 Test Levels and Results

Frequency Range	Test Level	Antenna Polarization	Output Mode	Average	During Zap (Maximum)	During Zap (Minimum)	Deviation 0f Full Scale (%)	Pass or Fail
80 MHz to 1000 MHz	20 V/m	Horizontal	V_{OUT} = 10 V	9.967239 V	9.968194 V	9.964191 V	−0.03, +0.01	Pass, Criterion A
	20 V/m	Vertical	V_{OUT} = 10 V	9.9672123 V	9.968163 V	9.965935 V	−0.01, +0.01	Pass, Criterion A
	20 V/m	Horizontal	I_{OUT} = 20 mA	19.879439 mA	19.881228 mA	19.873851 mA	−0.03, +0.01	Pass, Criterion A
	20 V/m	Vertical	I_{OUT} = 20 mA	19.879657 mA	19.881962 mA	19.877793 mA	−0.01, +0.01	Pass, Criterion A
1000 MHz to 6000 MHz	10 V/m	Horizontal	V_{OUT} = 10 V	9.967296 V	9.968218 V	9.966069 V	−0.01, +0.01	Pass, Criterion A
	10 V/m	Vertical	V_{OUT} = 10 V	9.967441 V	9.968302 V	9.966203 V	−0.01, +0.01	Pass, Criterion A
	10 V/m	Horizontal	I_{OUT} = 20 mA	19.879407 mA	19.881070 mA	19.877572 mA	−0.01, +0.01	Pass, Criterion A
	10 V/m	Vertical	I_{OUT} = 20 mA	19.879212 mA	19.880868 mA	19.877303 mA	−0.01, +0.01	Pass, Criterion A

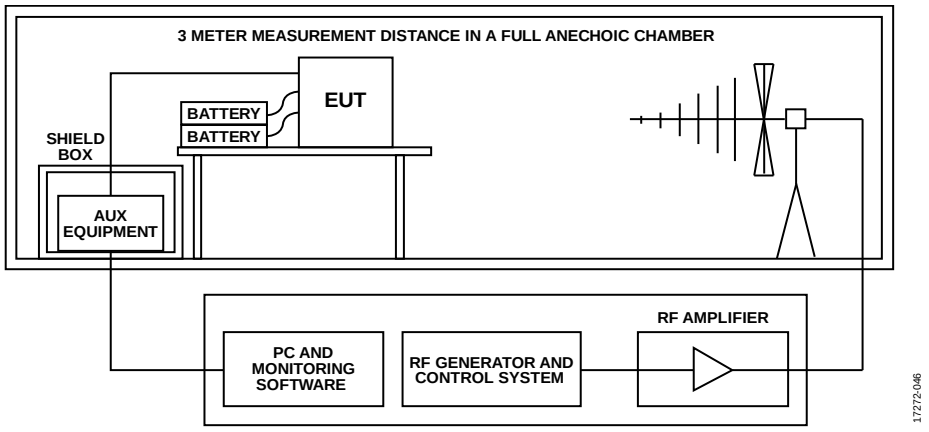

Figure 47. IEC 61000-4-3 Test Setup Configuration Diagram

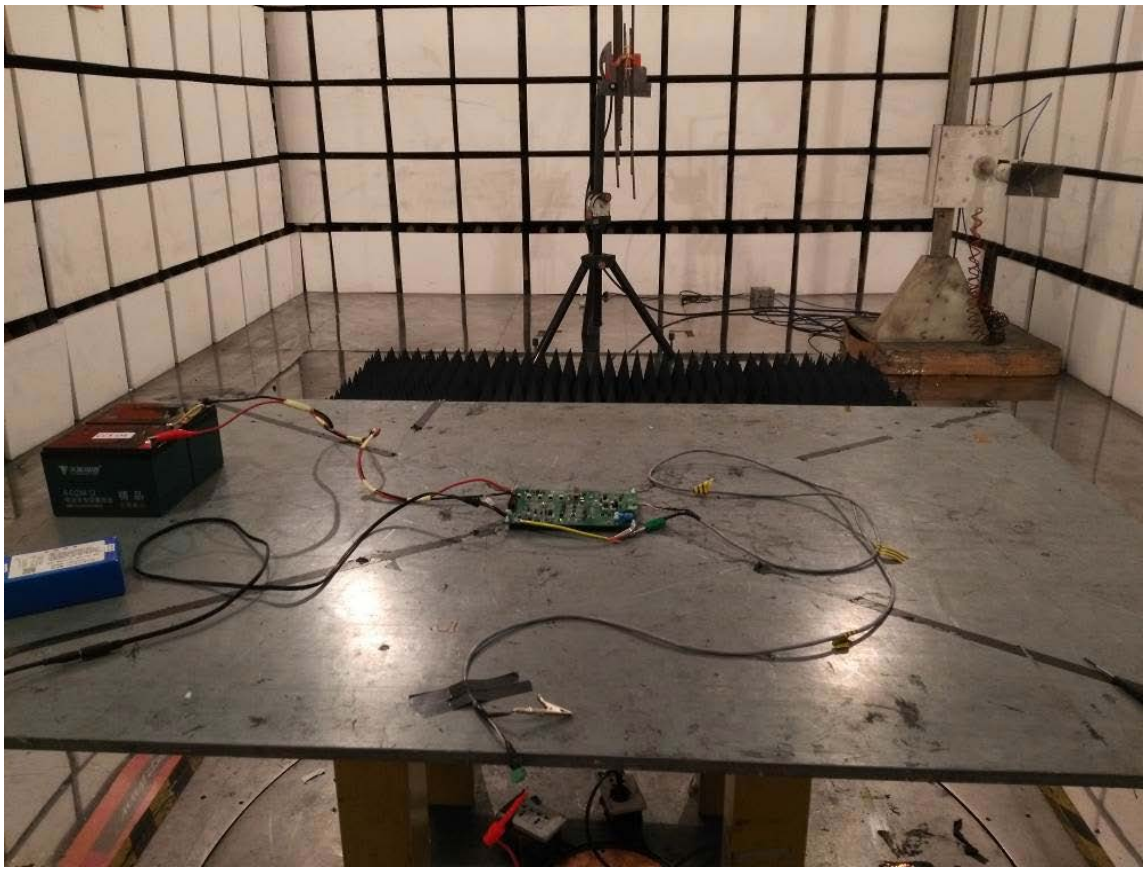

Figure 48. IEC 61000-4-3 Test Setup Photograph

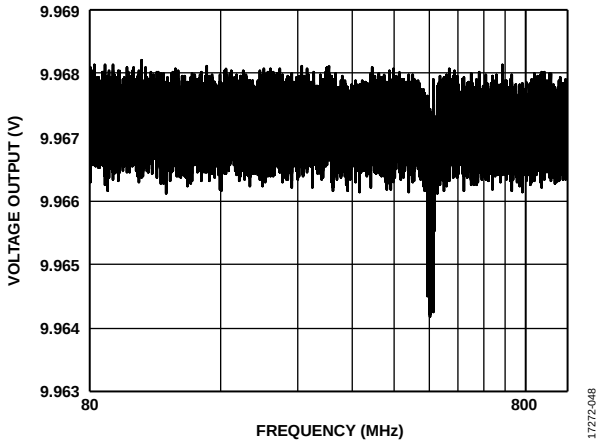

Figure 49. Voltage Output vs. Frequency Below 20 V/m, Horizontal Antenna

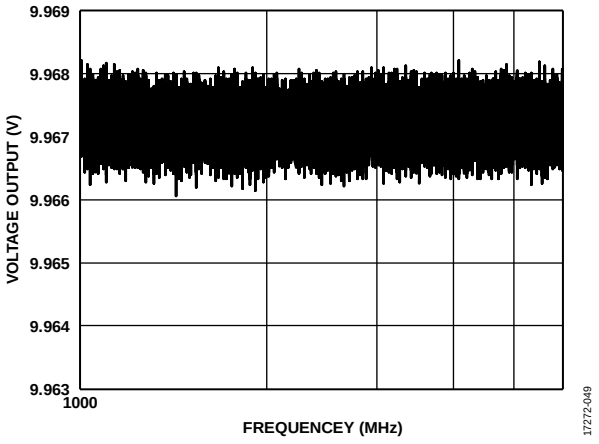

Figure 50. Voltage Output vs. Frequency Below 10 V/m, Horizontal Antenna

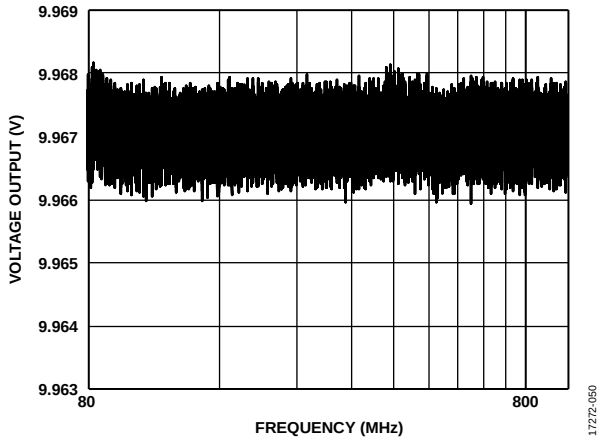

Figure 51. Voltage Output vs. Frequency Below 20 V/m, Vertical Antenna

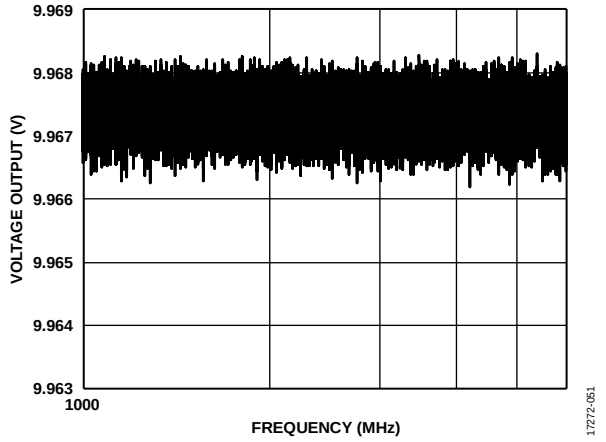

Figure 52. Voltage Output vs. Frequency Below 10 V/m, Vertical Antenna

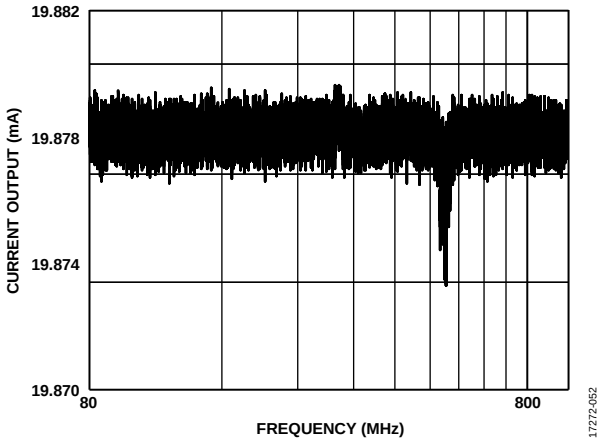

Figure 53. Current Output vs. Frequency Below 20 V/m, Horizontal Antenna

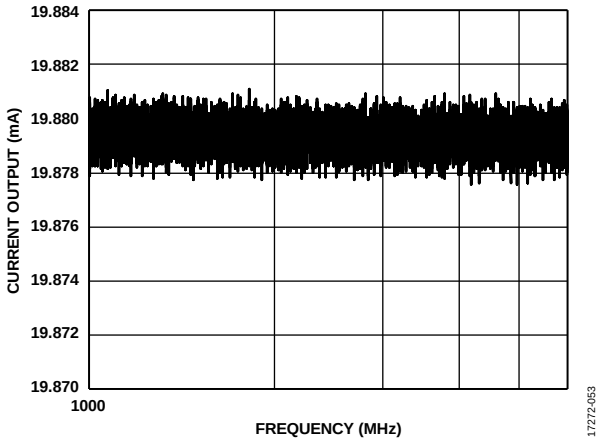

Figure 54. Current Output vs. Frequency Below 10 V/m, Horizontal Antenna

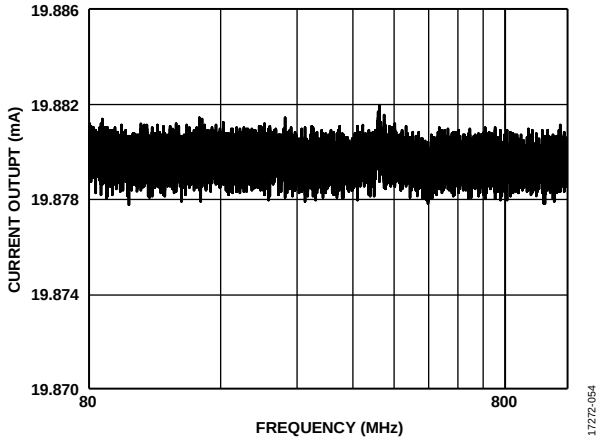

Figure 55. Current Output vs. Frequency Below 20 V/m, Vertical Antenna

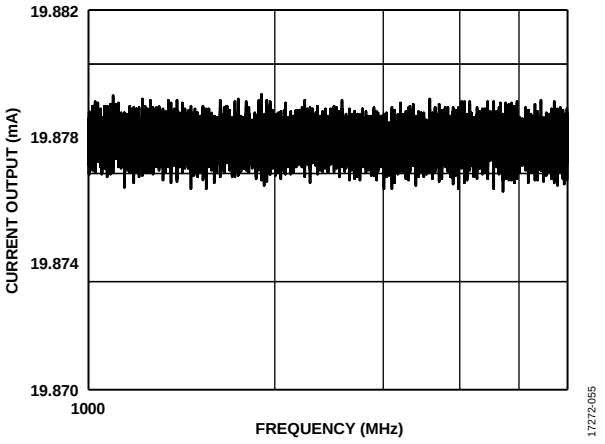

Figure 56. Current Output vs. Frequency Below 10 V/m, Vertical Antenna

RADIATED EMISSIONS

Per the CISPR 11 standard, the EUT is placed on top of a rotating table, 0.8 m above the ground, in a 10 m, semianechoic chamber. The table is rotated 360° to identify the position of the highest radiation. The EUT is set 10 m from the interference receiving antenna, which can be set to a horizontal or vertical polarization position. The antennas are mounted on top of a variable height antenna tower. The heights of the antennas vary from 1 m to 4 m above the ground to identify the maximum value of the field strength. The EUT is configured to its typical worst case where the antenna is tuned to a height from 1 m to 4 m and the table is turned from 0° to 360° to find the maximum reading. The typical worst case for the EUT means that the AD5758 is being refreshed at 1 kHz at its full-scale voltage or current output. The test receiver system is set to quasipeak detection mode. The EUT is powered by two 24 V dc battery packs. Any radiated emission from the auxiliary supply can be excluded.

For improved EMI performances, refer to the AN-2046 application note for more discussion about the AD5758 EMC test board with the ADP1031. The AD5758 EMC test board with the ADP1031 share the same blank PCB of this AD5758 board but is assembled with a partially different bill of materials variant. This variant implements the ADP1031 power and digital isolations. The AD5758 EMC test board with the ADP1031 passes CISPR 11 Class B limits with a margin greater than 9 dB.

Table 11. CISPR 11 Radiated Emissions at Critical Frequencies, V_{OUT} = 10 V

Frequency (MHz)	Result (dBµV)	Limit (dBµV)	Margin (dB)	Height (cm)	Degree (°)	Antenna Polarity	Remark
32.9100	23.16	40	−16.84	100	20	Vertical	Peak detection
82.3800	19.84	40	−20.16	200	155	Vertical	Peak detection
204.6000	22.42	40	−17.58	400	216	Vertical	Peak detection
642.0700	28.49	47	−18.51	300	0	Vertical	Peak detection
817.6400	30.31	47	−16.69	400	0	Vertical	Peak detection
928.2200	29.78	47	−17.22	300	112	Vertical	Peak detection
32.9100	26.94	40	−13.06	400	360	Horizontal	Peak detection
33.2600	23.03	40	−16.97	400	115	Horizontal	Quasi peak
100.8100	19.75	40	−20.25	200	68	Horizontal	Peak detection
204.5100	24.18	40	−15.82	300	66	Horizontal	Quasi peak
204.6000	25.98	40	−14.02	300	294	Horizontal	Peak detection
689.6000	30.45	47	−16.55	100	360	Horizontal	Peak detection
825.4000	29.66	47	−17.34	400	44	Horizontal	Peak detection
932.1000	30.08	47	−16.92	100	195	Horizontal	Peak detection

Table 12. CISPR 11 Radiated Emissions at Critical Frequencies, I_{OUT} = 20 mA

Frequency (MHz)	Result (dBµV)	Limit (dBµV)	Margin (dB)	Height (cm)	Degree (°)	Antenna Polarity	Remark
32.7300	21.80	40	−18.20	100	332	Vertical	Quasi peak
32.9100	25.32	40	−14.68	100	82	Vertical	Peak detection
205.5700	23.42	40	−16.58	400	222	Vertical	Peak detection
639.1600	28.16	47	−18.84	100	0	Vertical	Peak detection
732.2800	29.64	47	−17.36	300	360	Vertical	Peak detection
911.7300	29.59	47	−17.41	100	106	Vertical	Peak detection
977.6900	29.94	47	−17.06	400	0	Vertical	Peak detection
32.7650	24.90	40	−15.10	400	265	Horizontal	Quasi peak
32.9100	28.14	40	−11.86	400	21	Horizontal	Peak detection
205.5700	27.62	40	−12.38	400	298	Horizontal	Peak detection
205.7300	26.30	40	−13.70	400	214	Horizontal	Quasi peak
224.9700	23.66	40	−16.34	400	59	Horizontal	Peak detection
699.3000	30.96	47	−16.04	100	0	Horizontal	Peak detection
870.0200	30.22	47	−16.78	300	360	Horizontal	Peak detection
928.2200	30.16	47	−16.84	200	38	Horizontal	Peak detection

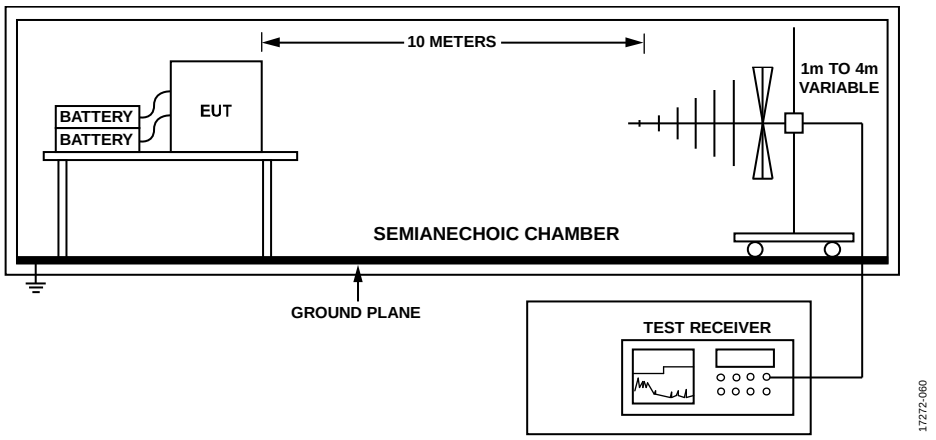

Figure 57. CISPR 11 Test Setup Configuration Diagram

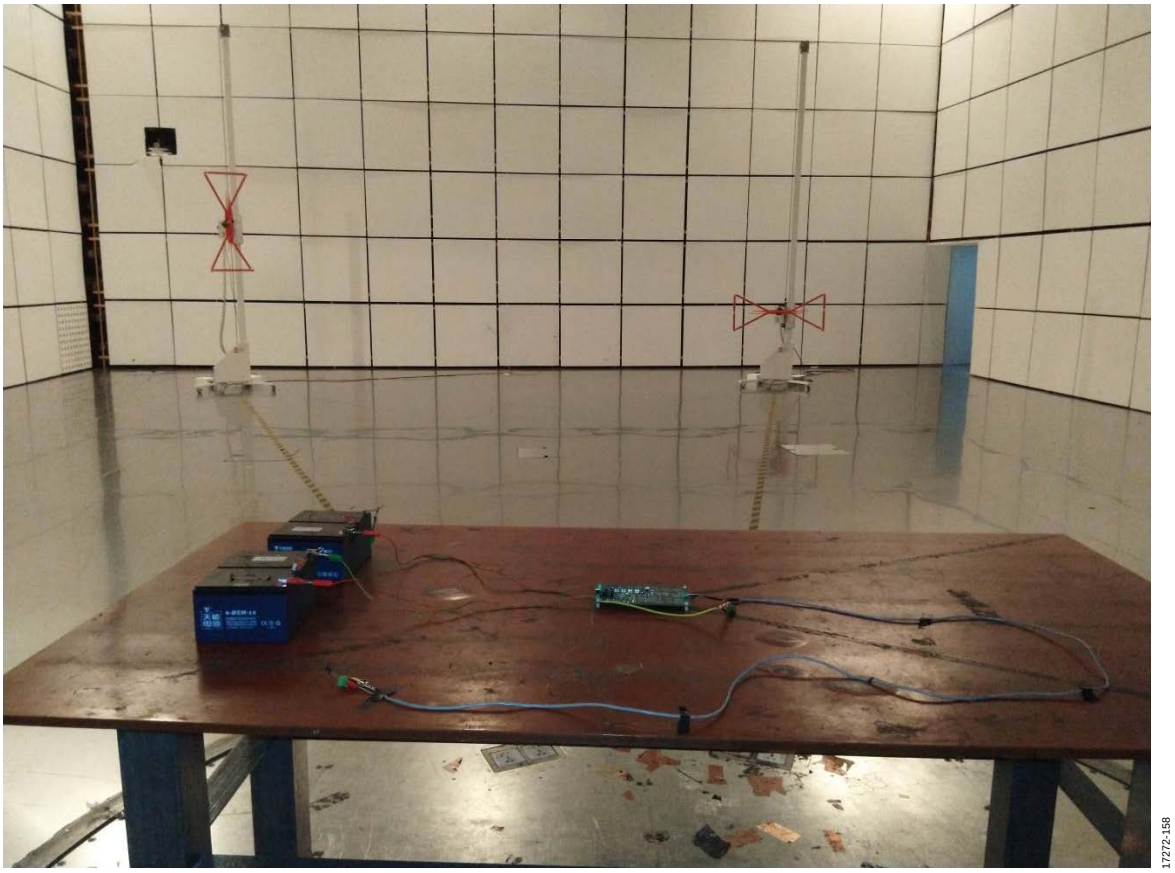

Figure 58. CISPR 11 Radiated Emission Test Setup Photograph

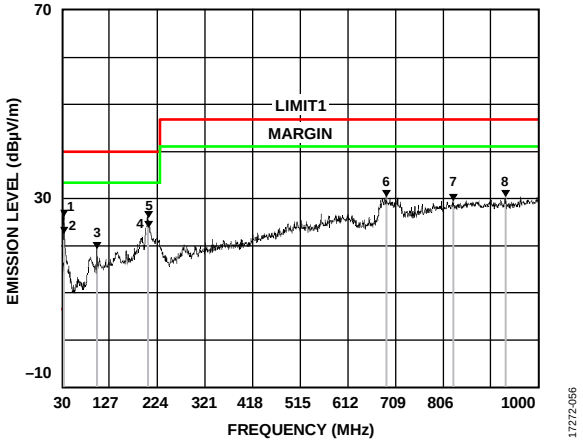

Figure 59. Emission Level vs. Frequency, Horizontal Antenna Polarization, V_{OUT} = 10 V

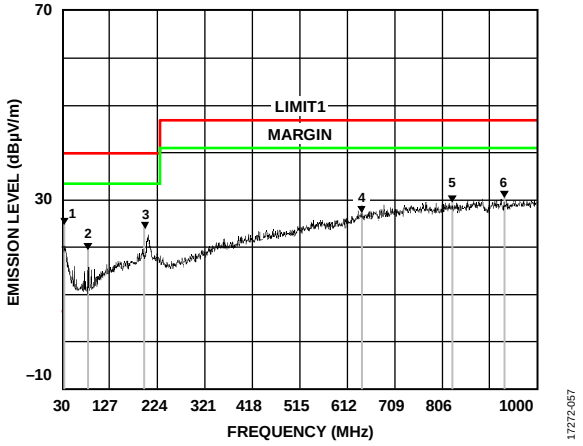

Figure 60. Emission Level vs. Frequency, Vertical Antenna Polarization, V_{OUT} = 10 V

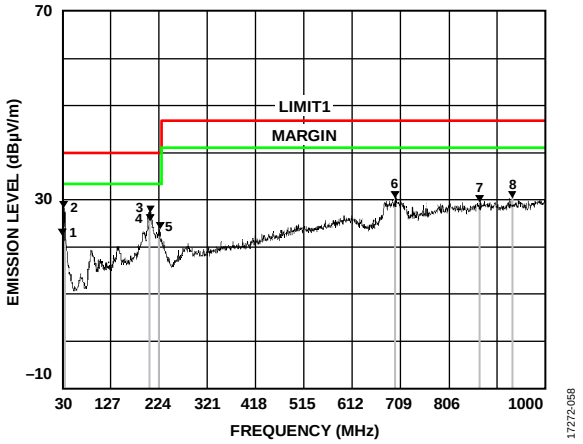

Figure 61. Emission Level vs. Frequency, Horizontal Antenna Polarization, I_{OUT} = 20 mA

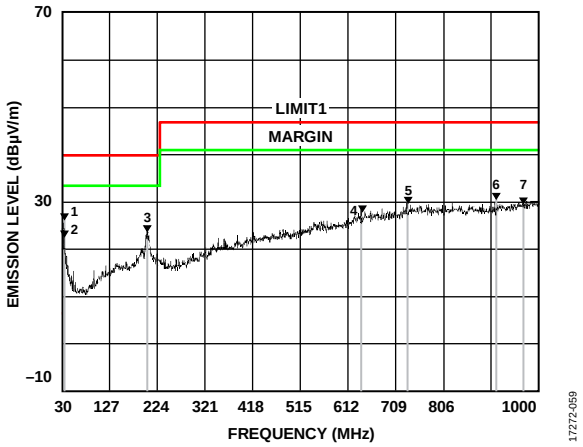

Figure 62. Emission Level vs. Frequency, Vertical Antenna Polarization, I_{OUT} = 20 mA

EMC BOARD SCHEMATICS AND ARTWORK

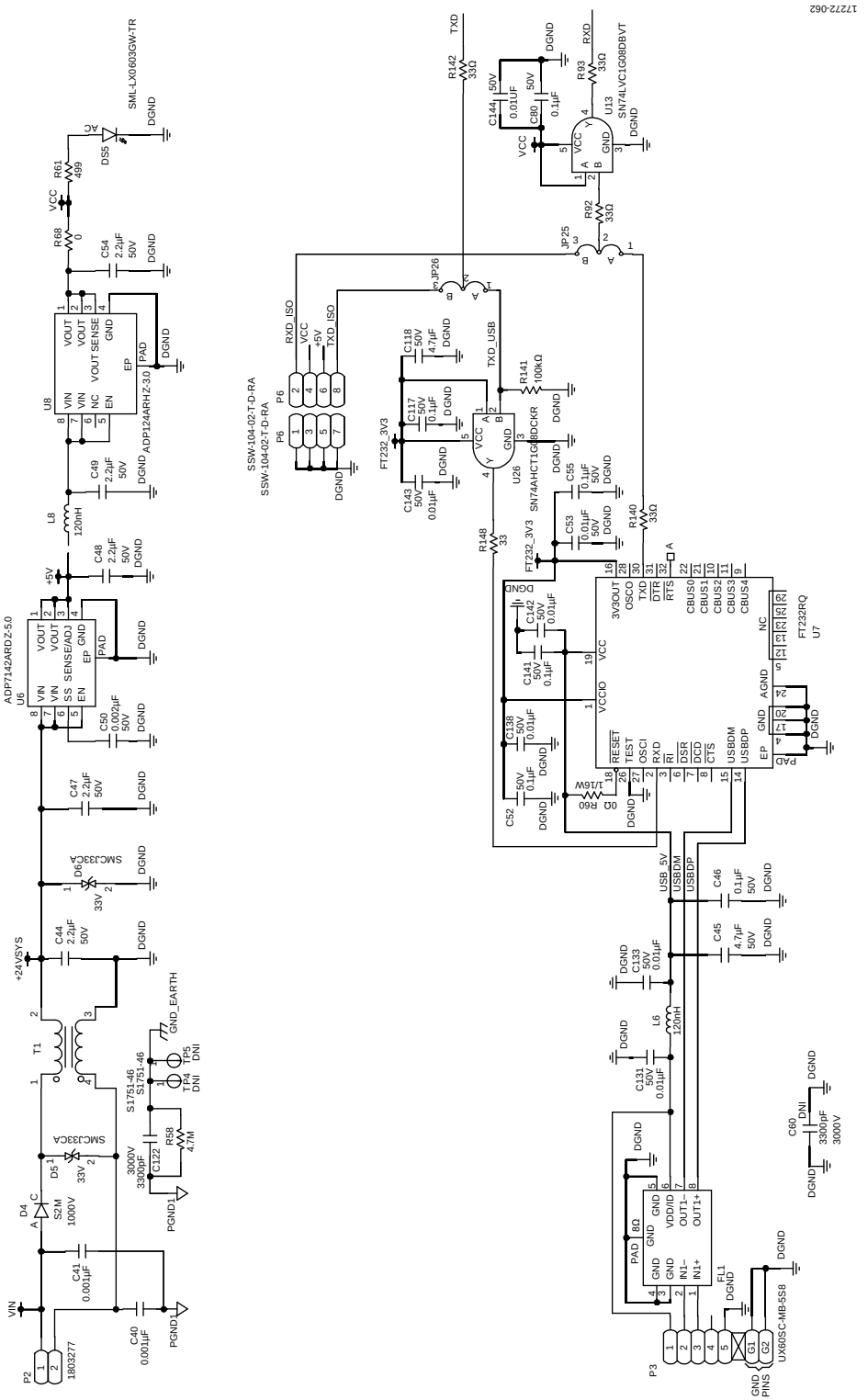

Figure 63. AD5758 EMC Test Board Schematics, System Power Supply and USB Communication Port

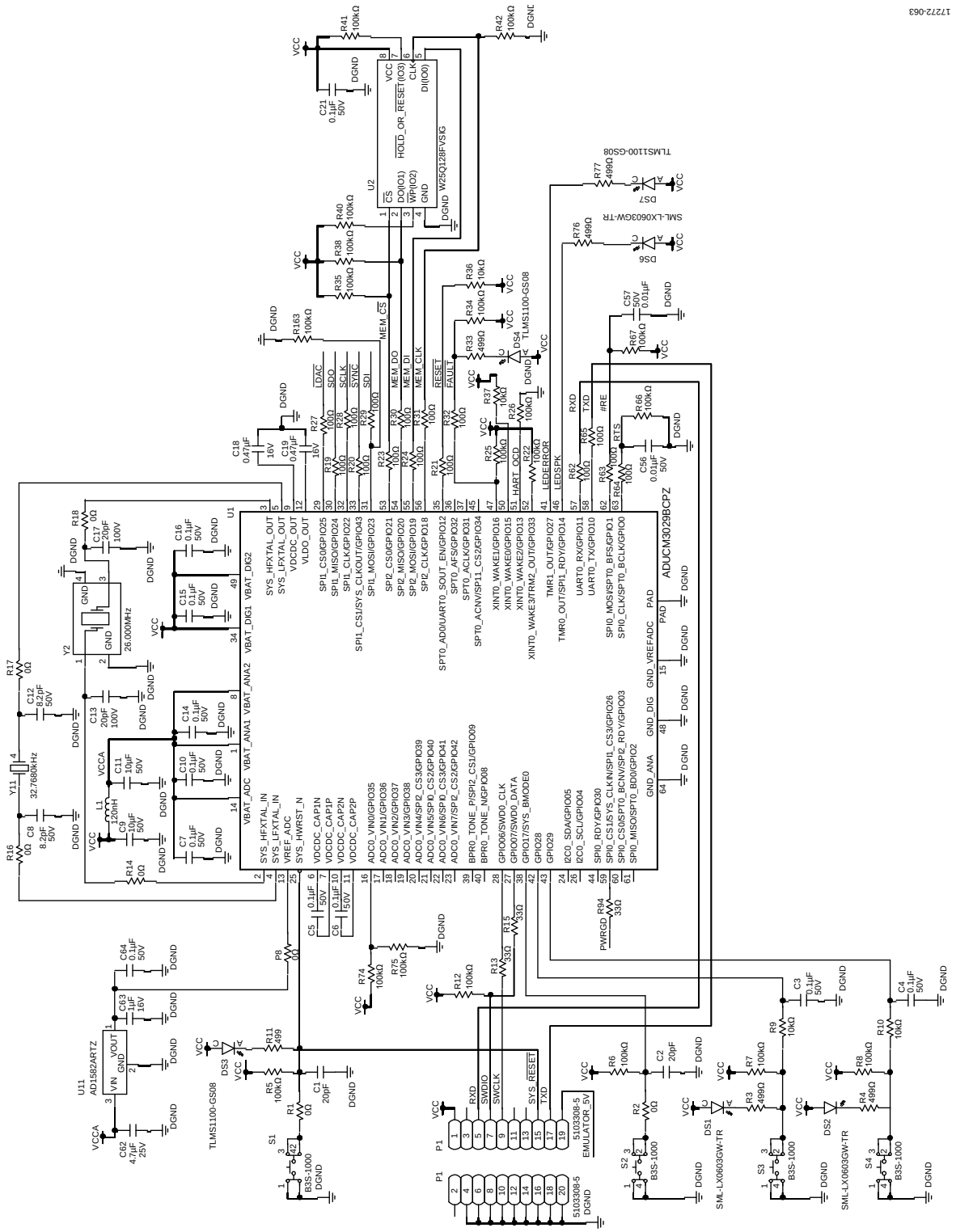

Figure 64. AD5758 EMC Test Board Schematics, MCU and Periphery Circuit

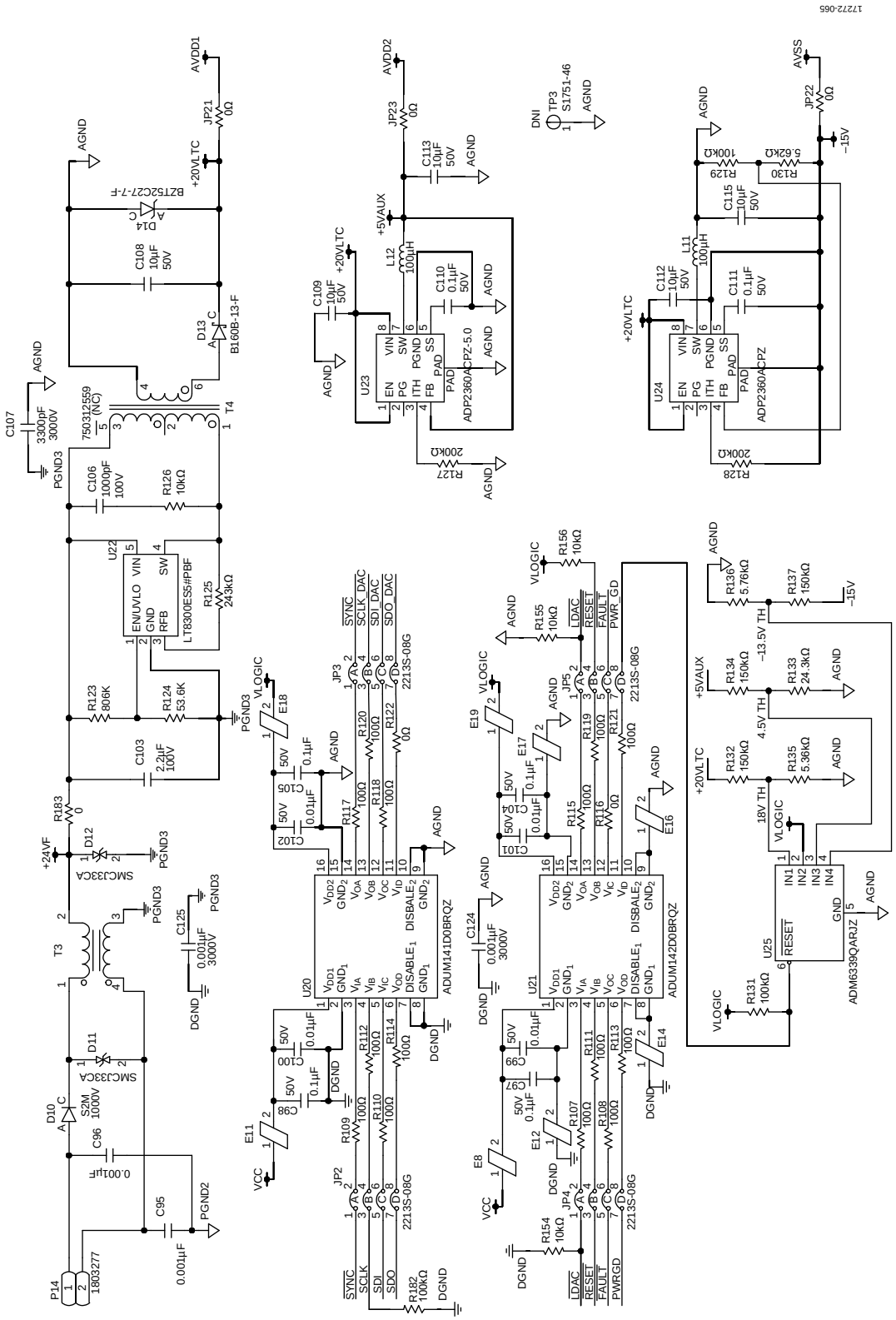

Figure 65. AD5758 EMC Test Board Schematics, Field Power Supply and Digital Isolation

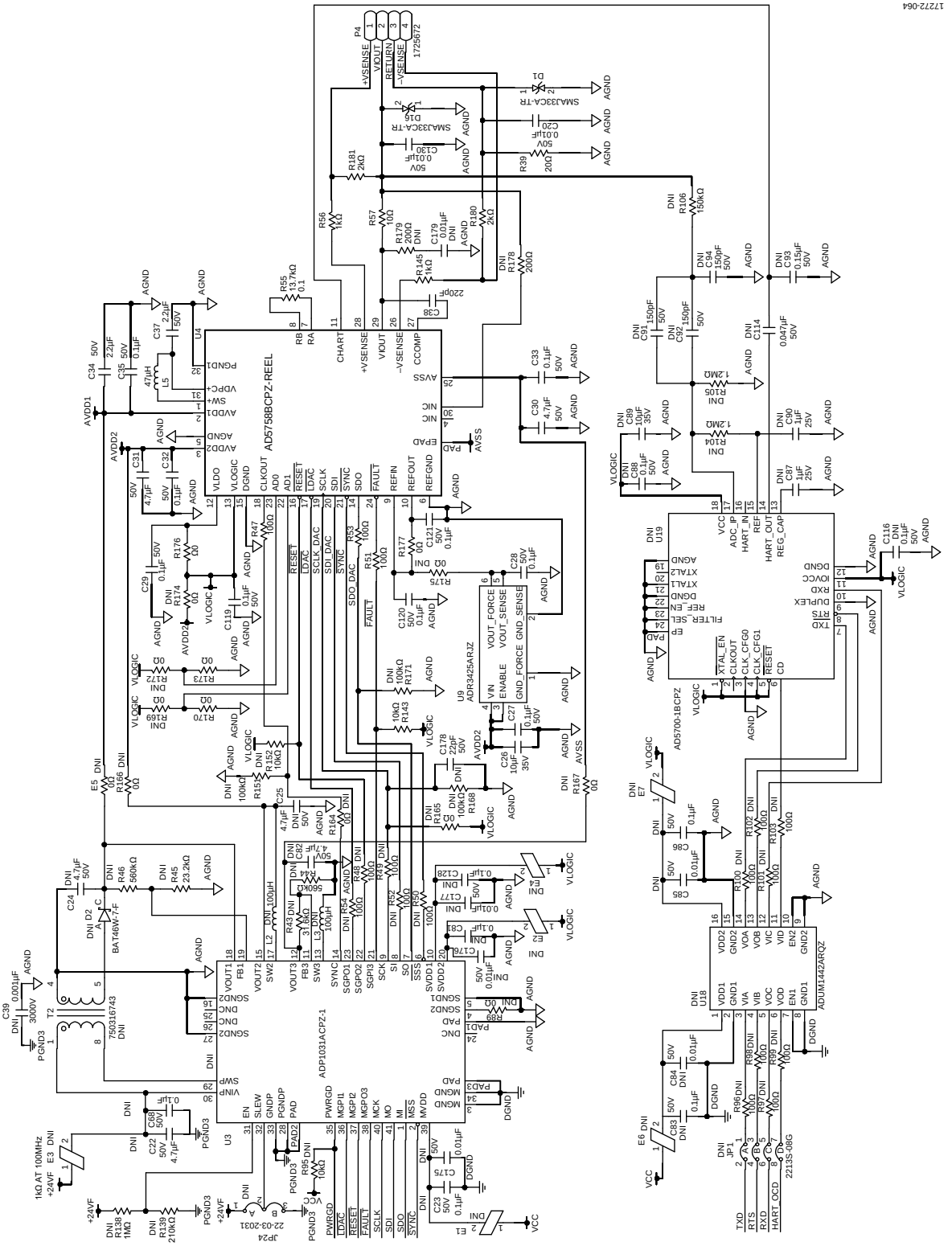

Figure 66. AD5758 EMC Test Board Schematics, AD5758 Periphery Circuit

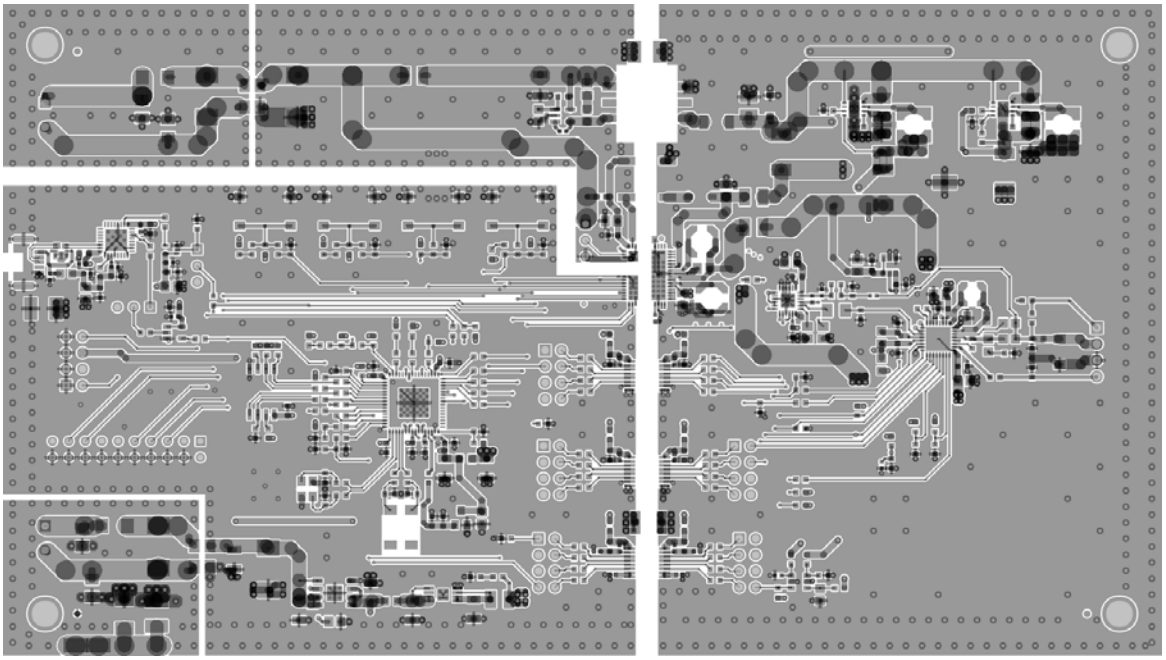

Figure 67. Layer 1, Top Side

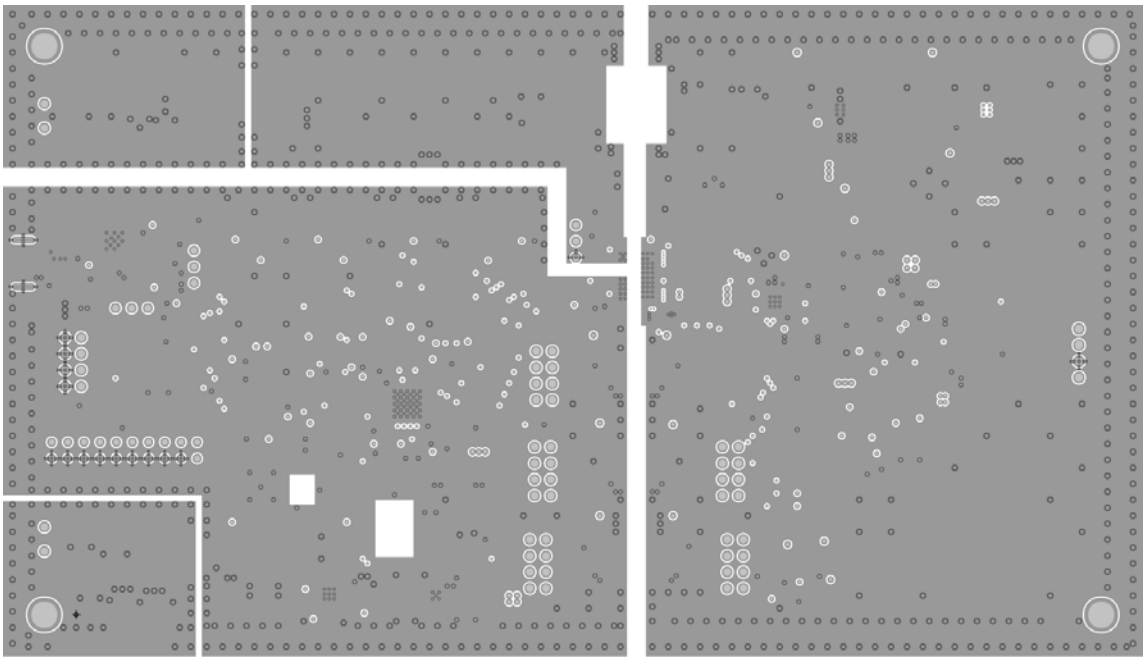

Figure 68. Layer 2, Inner Ground Plane

Figure 69. Layer 3, Inner Power Plane

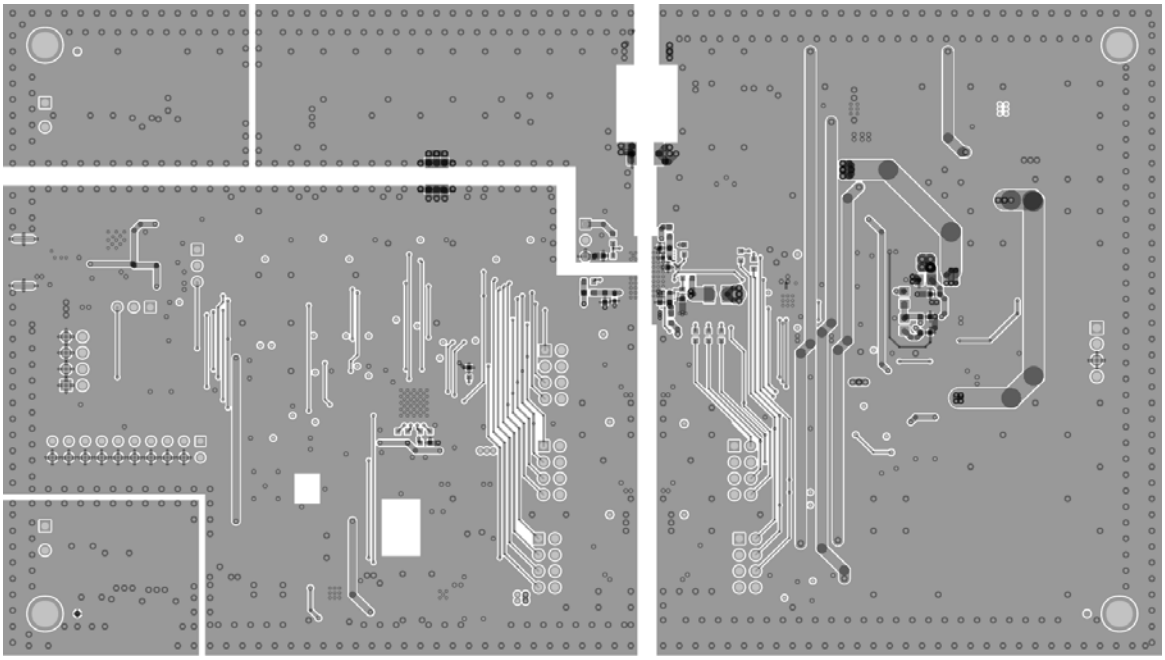

Figure 70. Layer 4, Bottom Side

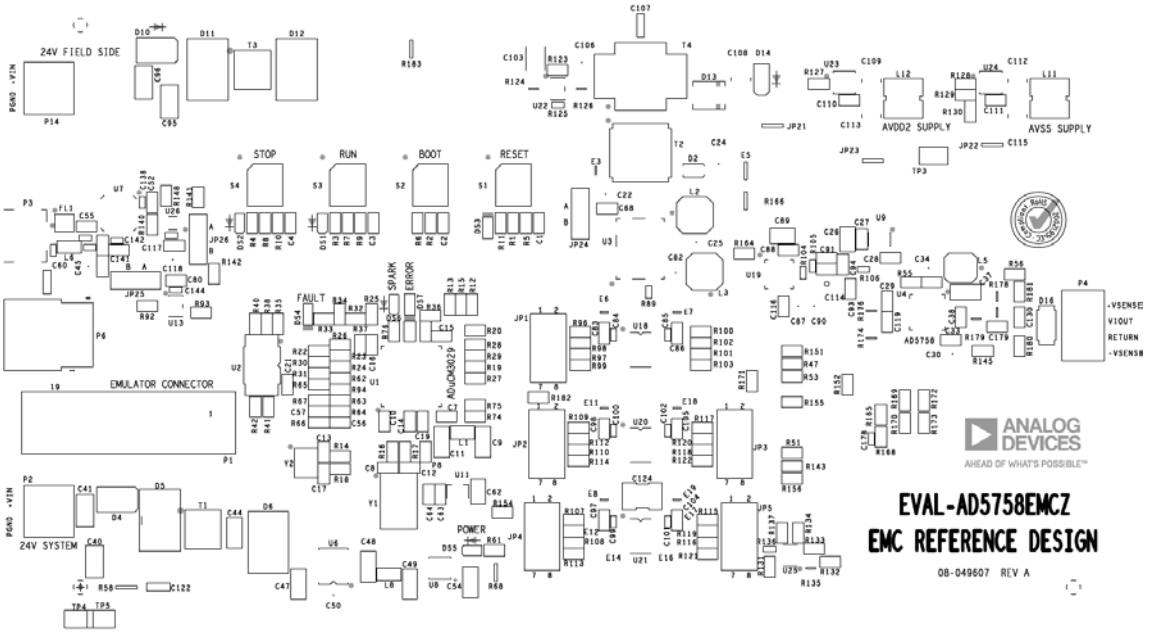

Figure 71. Silkscreen Top

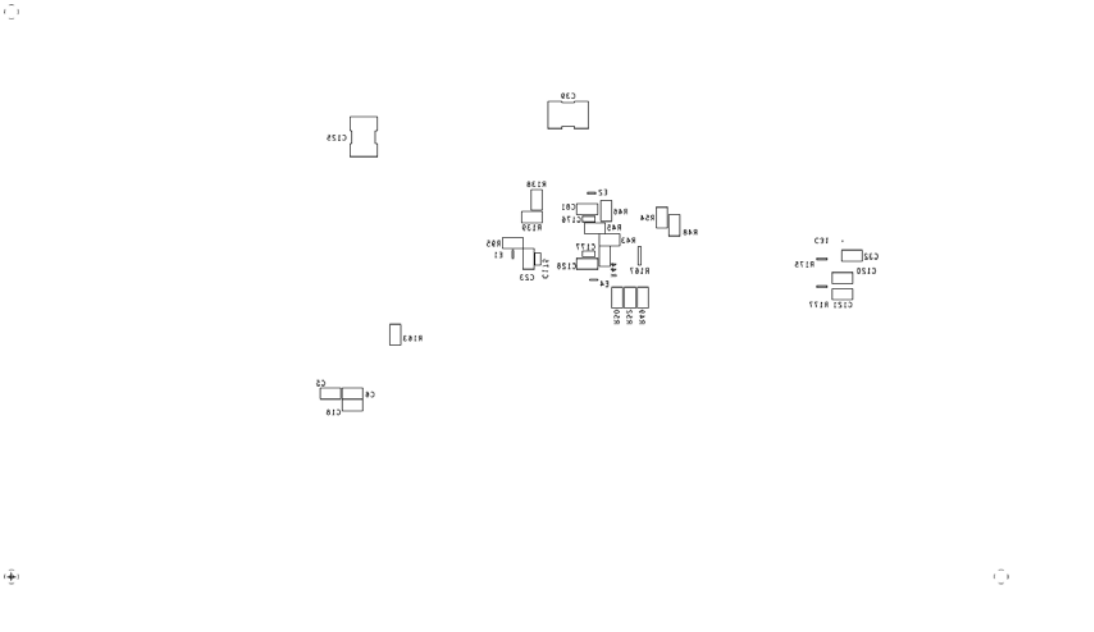

Figure 72. Silkscreen Bottom

ORDERING INFORMATION

BILL OF MATERIALS

Table 13.

Reference Designator	Part Description	Part Number	Manufacturer
C1, C2, C13, C17	Capacitors, ceramic, C0G (NP0), general-purpose, 20 pF	GRM1885C1H200JA01D	Murata
C3 to C7, C10, C14 to C16, C21, C27 to C29, C32, C33, C35, C46, C52, C55, C64, C80, C97, C98, C104, C105, C117, C119, C120, C121, C141	Capacitors, ceramic, X7R, 0603, 0.1 µF	06035C104KAT2A	AVX
C99 to C102	Capacitors, ceramic, X7R, general-purpose, 0.01 µF	GRM155R71E103KA01D	Murata
C103	Capacitor, ceramic, X7R, 2.2 µF	C1210C225K1RACTU	Kemet
C106	Capacitor, ceramic, X7R, chip, 1000 pF	08051C102KAT2A	AVX
C107, C122	Multilayer ceramic capacitors (MLCCs) for high voltage, X7R, 3300 pF	HV1812Y332KXHATHV	Vishay
C108, C109, C112, C113, C115	Capacitors, ceramic, X7R, general-purpose, 10 µF	GRM32ER71H106KA12L	Murata
C9, C11	Capacitors, ceramic, X5R, general-purpose, 10 µF	GRM31CR61H106KA12L	Murata
C110, C111	Capacitors, ceramic, X7R, general-purpose, 0.1 µF	GRM188R71H104KA93D	Murata
C30, C31, C45, C118	MLCCs, X5R, 4.7 µF	C2012X5R1H475K125AB	TDK
C8, C12	Capacitors, ceramic, 8.2 pF	06035A8R2CAT2A	AVX
C124, C125	Capacitors, ceramic, X7R, high voltage, 0.001 µF	C1812C102KHRACTU	Kemet
C130	Capacitor, ceramic, X7R, soft termination, 0.01 µF	C1608X7R1H103K080AE	TDK
C53, C131, C133, C138, C142 to C144	Capacitors, ceramic, X7R, 0.01 µF	GCM155R71H103KA55D	Murata
C18, C19	Capacitors, ceramic, X7R, 0.47 µF	C1608X7R1H474MT	TDK
C26	MLCC, X5R, 10 µF	C2012X5R1V106K085AC	TDK
C34	Capacitor, ceramic, X7R, 2.2 µF	UMK212BB7225KG-T	Taiyo Yuden
C37, C44, C47 to C49, C54	Capacitors, ceramic, X7R, general-purpose, 2.2 µF	GRM31CR71H225KA88L	Murata
C38	Capacitor, ceramic, NP0, 220 pF	CC0603JRNPO9BN221	Yageo
C40, C41, C95, C96	Capacitors, ceramic, NP0, 0.001 µF	12065A102JAT2A	AVX
C50	Capacitor, ceramic, C0G (NP0), general-purpose, 0.002 µF	GRM2165C1H202JA01D	Murata
C56, C57	Capacitors, ceramic, X7R, general-purpose, 0.01 µF	GCG188R71H103KA01D	Murata
C62	Capacitor, ceramic, X5R, general-purpose, 4.7 µF	GRM21BR61E475KA12L	Murata
C63	Capacitor, ceramic, X7R, 1 µF	0603YC105KAT2A	AVX
D4, D10	Diodes, general-purpose, rectifier	S2M	ON Semiconductor
D5, D6, D11, D12, D16	Diodes, TVS, bidirectional	SMCJ33CA-TR	ST Microelectronics
D13	Diode, Schottky	B160B-13-F	Diodes Incorporated
D14	Diode, Zener, commercial grade	BZT52C27-7-F	Diodes Incorporated
DS1, DS2, DS5, DS6	Light emitting diodes (LEDs), surface-mount device (SMD), 0603, green	SML-LX0603GW-TR	Lumex
DS3, DS4, DS7	LEDs, SMD, 0603, red	TLMS1100-GS08	Vishay
E8, E11, E18, E19	Inductors, ferrite bead, 1 kΩ, 100 MHz	BLM18HK102SN1D	Murata
E12, E14, E16, E17	Inductors, ferrite bead, 2.2 Ω, maximum dc resistance, 0.2 A, 1.8 kΩ, 100 MHz	BLM15HD182SN1D	Murata
FL1	Filter, EMI, common-mode, 30 dB, 0.1 A, 8 Ω	EMI2121MTTAG	ON Semiconductor
JP2 to JP5	Connectors, PCB, header, jumper, 4 × M000385	2213S-08G	Multicomp
JP21 to JP23	Resistors, thick film, chip, 2512, 0 Ω	CRCW25120000Z0EG	Vishay
JP25, JP26	Connectors, PCB, header jumper, 1 × M000385	22-03-2031	Molex
L1, L6, L8	Ferrite beads, SMD, 120 Ω, 120 nH	LI0805H750R-10	Laird
L11, L12	Inductors, power choke, 100 µH	744043101	Wurth Elektronik
L5	Inductor, shielded power, 47 µH	LPS4018-473MRB	Coilcraft
P1	Connector, PCB, header, low profile	5103308-5	TE Connectivity LTD

Reference Designator	Part Description	Part Number	Manufacturer
P2, P14	Connectors, PCB, terminal block, two position, green	1727010	Phoenix Contact
P3	Connector, PCB, receptor, mini USB 2.0	UX60SC-MB-5S8	Hirose
P4	Connector, PCB, four-position terminal block, single-row, straight, 2.54 mm pitch, 3.5 mm tail length	1725672	Phoenix Contact
P8, R1, R2, R14, R16 to R18, R60, R116, R122, R170, R173	Resistors, film, SMD, 0603, 0 Ω	MC0603WG00000T5E-TC	Multicomp
R9, R10, R36, R37, R143, R154 to,R156	Resistors, thick film, chip, 0603, 10 kΩ	MC0100W0603110K	Multicomp
R19 to R21, R23, R24, R27 to R32, R47, R51, R53, R62 to R65, R107 to R115, R117 to R121	Resistors, precision, thick film, chip, 0603, 100 Ω	MC0.063W06031100R	Multicomp
R3, R4, R11, R33, R61, R76, R77	Resistors, precision, thick film, chip, 0603, 499 Ω	ERJ-3EKF4990V	Panasonic
R5 to, R8, R12, R22, R25, R26, R34, R35, R38, R40 to R42, R66, R67, R74, R75, R131, R141, R163, R182	Resistors, precision, thick film, chip, 100 kΩ	ERJ-3EKF1003V	Panasonic
R123	Resistor, film, SMD, 0603, 806 kΩ	9C06031A8063FKHFT	Yageo
R124	Resistor, chip, SMD, 0805, 53.6 kΩ	9C08052A5362FKHFT	Yageo
R125	Resistor, thick film, chip, 243 kΩ	RCW0402243KFKED	Vishay
R126	Resistor, thick film, chip, 10 kΩ	CRCW080510K0FKEAHP	Vishay
R127, R128	Resistors, thick film, chip, 200 kΩ	ERJ-3EKF2003V	Panasonic
R129	Resistor, thick film, chip, 100 kΩ	MC0.063W06031100K	Multicomp
R13, R15, R92 to R94, R140, R142, R148	Resistors, film, SMD, 0603, 33 Ω	MC0.063W0603133R	Multicomp
R130	Resistor, film SMD 0603, 5.62 kΩ	9C06031A5621FKHFT	Yageo
R132, R134, R137	Resistors, precision, thick film, chip, 0603, 150 kΩ	ERJ-3EKF1503V	Panasonic
R133	Resistor, precision, thick film, 0603, 24.3 kΩ	ERJ-3EKF2432V	Panasonic
R135	Resistor, antisurge/antipulse, high power, thick film, chip, 5.63 kΩ	ERJ-P06F5361V	Panasonic
R136	Resistor, precision, thick film, chip, 5.67 kΩ	ERJ-2RKF5761X	Panasonic
R56, R145	Resistors, thick film, chip, 1 kΩ	MC0063W060311K	Multicomp
R176, R177	Resistors, thin film, chip, 0 Ω	MC0.1W08050R	Multicomp
R180, R181	Resistors, thick film, chip, 2 kΩ	MC0.063W060312K	Multicomp
R68, R183	Resistors, high power, thick film, chip, 0 Ω	CRCW12100000Z0EAHP	Vishay
R55	Resistor, precision, thin film, 13.7 kΩ	RN73C1J13K7BTG	TE Connectivity
R57	Resistor, precision, thick film, chip, 10 Ω	ERJ-6ENF10R0V	Panasonic
R58	Resistor, thick film, high voltage, chip, 4.7 MΩ	CHV2010-JW-475ELF	Bourns
S1 to S4	Switches, surface mount, SMT	B3S1000	Omron
T1, T3	Common-mode chokes, DLW5BS series, 190 Ω, 5 A	DLW5BSN191SQ2L	Murata
T4	Flyback transformer	750312559	Wurth Elektronik
U1	IC, ultra low power, Arm Cortex-M3, MCU	ADuCM3029BCPZ	Analog Devices, Inc.
U11	IC, micropower, precision, series mode, voltage reference	AD1582ARTZ	Analog Devices
U13	IC, TTL, single, two input positive and gate	SN74LVC1G08DBVT	Texas Instruments
U2	IC, 3 V, 128 Mb, serial flash memory with dual/quad SPI and quick path interconnect (QPI)	W25Q128FVSIG	Winbond
U20	IC, 3 kV rms, quad digital isolators	ADuM141D0BRQZ	Analog Devices
U21	IC, 3.0 kV rms/3.75 kV rms, quad digital isolators	ADuM142D0BRQZ	Analog Devices
U22	IC, 100 V input voltage, micropower isolated, flyback controller with 150 V/0.26 A switch	LT8300ES5#PBF	Analog Devices
U23	IC, high efficiency buck regulator, 5 V voltage output	ADP2360ACPZ-5.0-R7	Analog Devices
U24	IC, high efficiency buck regulator	ADP2360ACPZ-R7	Analog Devices
U25	IC, quad, voltage microprocessor, supervisory circuit	ADM6339QARJZ-RL7	Analog Devices

Reference Designator	Part Description	Part Number	Manufacturer
U26	IC, TTL, single, two input, positive and gate	SN74AHCT1G08DCKR	Texas Instruments
U4	IC, single-channel, 16-bit, current/voltage output DAC, dynamic power control, HART connectivity	AD5758BCPZ-REEL	Analog Devices
U6	IC, low noise, CMOS, LDO regulator, 5 V voltage output	ADP7142ARDZ-5.0	Analog Devices
U7	IC, USB, serial universal asynchronous receiver/transmitter (UART)	FT232RQ	FTDI
U8	IC, low quiescent current, CMOS linear regulator, 3.0 V voltage output	ADP124ARHZ-3.0-R7	Analog Devices
U9	IC, micropower voltage reference, 2.5 V voltage output	ADR3425ARJZ-R7	Analog Devices
Y1	IC, crystal, SMD, 12.5 pF, 32.7680 kHz	MC-306-32.7680K-A0:ROHS	Seiko
Y2	IC, crystal, ultraminiature ceramic sealed, 10 pF, 26.000 MHz	ABM8G-26.000MHZ-B4Y-T	Abracon

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