LINEAR TECHNOLOGY

DESIGN NOTES

Hex Level Shift Shrinks Board Space – Design Note 20

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Although simple in concept, interfacing digital levels between different logic families usually requires many parts and appreciable board space. Other applications that require some form of level shifting of the output swing have solutions just as complicated. A logic to CMOS analog switch (Figure 1) is just one example where a level shift must occur. A new device, the LTC®1045, solves this and other level shift related problems conveniently. The LTC1045 is a hex level translator with a linear comparator on the front end. A latch and three-state output buffer are at the back. These features make it useful in other applications as a hex comparator or in interfacing to a data bus. Almost any input and output voltage requirements can be accommodated by simply setting the level of the appropriate power supply voltages.

The LTC1045 consists of six high speed comparators with output latches and three-state capability (see Figure 2). Each comparator's non-inverting input is brought out separately. The inverting inputs of comparators 1-4 are tied to V_{TRIP1} and 5-6 are tied to V_{TRIP2}. With these inputs the switching point of the comparators can be set anywhere within the common-mode range of V^- to (V^+ – 2V). There are four power supply pins on the LTC1045: V^+, V^-, V_{OH} and V_{OL}. V^+ and V^- power the comparator's front end, and V_{OH} and V_{OL} power the output drivers. Almost any combination of power supply voltages can be used. There are three restrictions: V_{OH} must be less than or equal to V^+; there must be a minimum differential voltage of 4.5V between V^+ and V^- and 3V between V_{OH} and V_{OL}. The maximum voltage between any two pins must not exceed the 18V absolute maximum.

The supply current is programmed with an external resistor. The R_{SET} resistor allows trade-offs between speed and power consumption. The propagation delay, with the I_{SET} pin at V^- and a single 5V supply, is typically 100ns with a total supply current of 4.5mA. The quiescent current can be brought down to 100µA (15 microamps per comparator) with an R_{SET} of 1M and a propagation delay of only 1.2µs. In addition, the I_{SET} pin completely shuts off power and latches the translator output voltages. The DISABLE input sets the six outputs to a high impedance state allowing the LTC1045 to be interfaced to a data bus.

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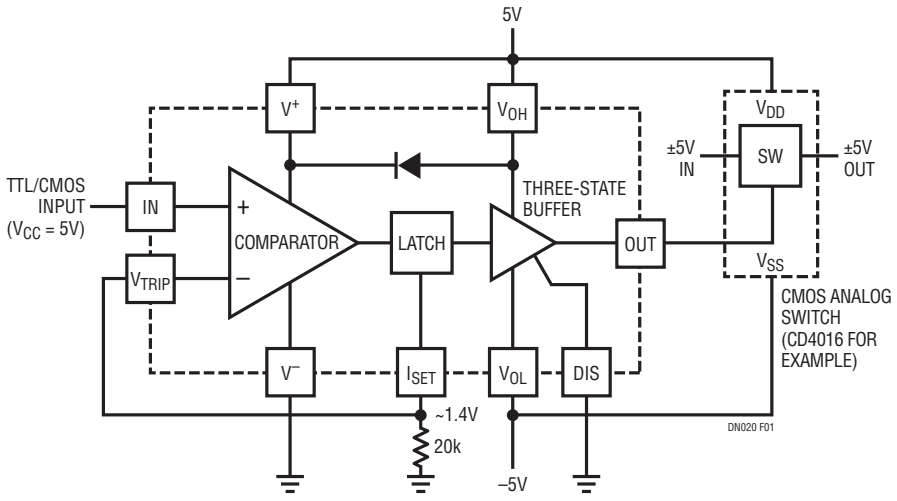

Figure 1. TTL/CMOS logic Levels to ±5V Analog Switch Driver

Figure 3 shows a simple way to build a battery powered RS232 receiver. The input voltage may be driven ±30V without adverse effects because the 100k resistor prevents device damage. With a 1M R_{SET} the hex RS232 line receiver draws only 100µA of quiescent current and has a propagation delay of 1.2µs. Only a single supply is needed for operation.

Board space can be saved by using the LTC1045 level translator as a hex comparator—even though both comparator inputs are not available. Figure 4 shows the LTC1045 used as a power supply monitor. The outputs of three power supplies are tied to the positive inputs through an appropriate resistive voltage divider. The divider ratio is set so that the voltage into the comparator equals the reference on the inverting input when the power supply voltage is at a critical level.

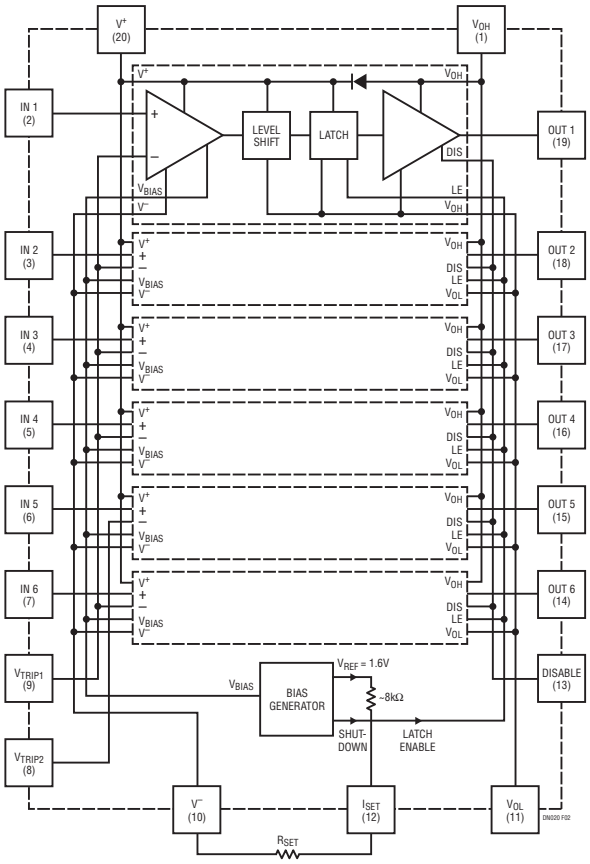

Figure 2. LTC1045 Block Diagram

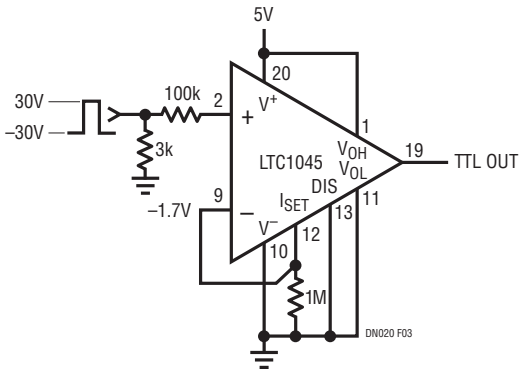

Figure 3. RS232 Receiver

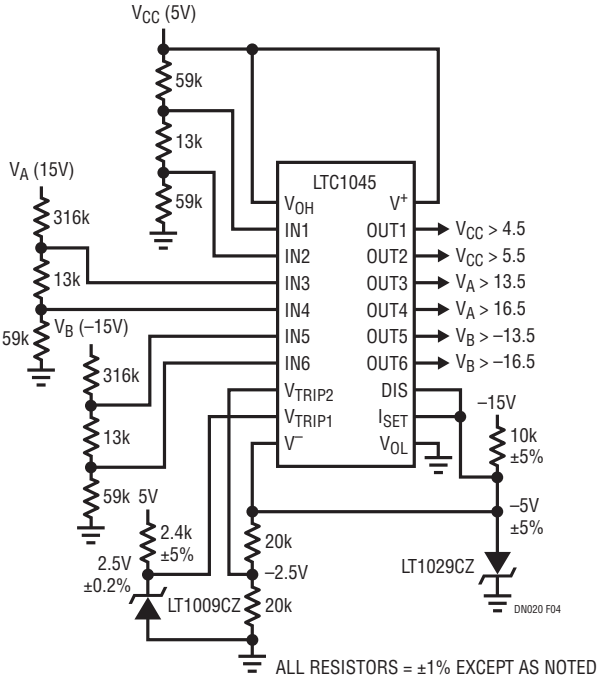

Figure 4. Power Supply Monitor

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