Composite Amplifiers

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Amplifier design, regardless of the technology utilized, is a study in compromise. Device limitations make it difficult for a particular amplifier to achieve optimal speed, drift, bias current, noise and power output specifications. As such, various amplifier families emphasizing one or more of these areas have evolved. Some amplifiers are very good attempts at doing everything well, but the best achievable performance figures are limited to dedicated designs.

Practical applications often require an amplifier that has extremely high performance in several areas. For example, high speed and DC precision are often needed. If a single device cannot simultaneously achieve the desired characteristics, a composite amplifier made up of two (or more) devices can be configured to do the job. Composite designs combine the best features of two or more amplifiers to achieve performance unobtainable in a single device. More subtly, composite designs permit circuit approaches which are normally impractical. This is particularly true of high speed stages which may be designed with little attention to DC biasing considerations if a separate stabilizing stage is employed.

Figure 1 shows a composite made up of an LT®1012 low drift device and an LT1022 high speed amplifier. The overall circuit is a unity-gain inverter, with the summing node located at the junction of three 10k resistors. The LT1012 monitors this summing node, compares it to ground and drives the LT1022's positive input, completing a DC stabilizing loop around the LT1022. The 10k-300pF time constant at the LT1012 limits its response to low frequency signals. The LT1022 handles high frequency inputs while the LT1012 stabilizes the DC operating point. The 4.7k-220Ω divider at the LT1022 prevents excessive input overdrive during start-up. This circuit combines the LT1012's 35µV offset and 1.5V/°C drift with the LT1022's 23V/µs slew rate and 300kHz full-power bandwidth. Bias current, dominated by the LT1012, is about 100pA.

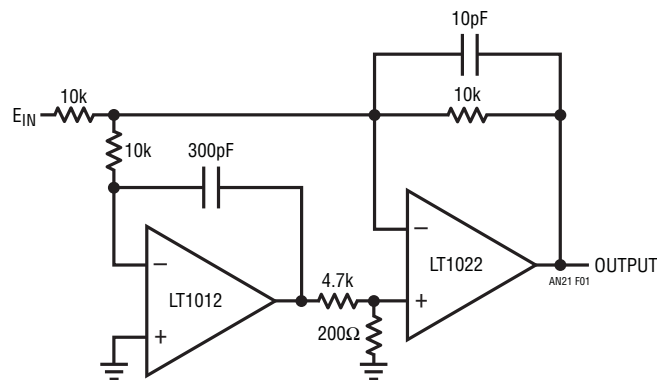**Figure 1. Basic DC-Stabilized Fast Amplifier**

Figure 2 is similar, but uses discrete FETs to more than triple the speed. Here A1's input stage is turned off by connecting its inputs to the negative rail. The differentially connected FETs bias the second state via A1's offset pins. This connection replaces A1's input stage, reducing bias current and increasing speed. FET mismatch would normally result in excessive offset and drift. A2 corrects this by monitoring the summing point (the junction of the two 4.7k resistors) and forcing Q2's gate to eliminate overall offset. The 10k-1000pF pair limits A2's response to low frequency, and the 1k divider chain prevents overdrive to Q2 on startup. The 1k-10pF damper at the summing node aids high frequency stability. Figure 3 shows pulse response. Trace A is the input and Trace B the output. Slew rate exceeds 100V/µs, with clean damping. Full-power bandwidth is about 1MHz, and the input bias current is in the 100pA range. DC offset and drift are similar to Figure 1.

Figure 4 shows a highly stable unity-gain buffer with good speed and high input impedance. Q1 and Q2 constitute a simple, high speed FET input buffer. Q1 functions as a source follower, with the Q2 current source load setting the drain-source channel current. The LT1010 buffer provides output drive capability for cables or whatever load is required. Normally, this open-loop configuration would be quite drifty because there is no DC feedback. The LTC®1052 contributes this function to stabilize the circuit. It does this by comparing the filtered circuit output to a similarly filtered version of the input signal. The amplified difference between these signals is used to set Q2's bias, and hence Q1's channel current. This forces Q1's V_{GS} to whatever voltage is required to match the circuit's input and output potentials. The 2000pF capacitor at A1 provides stable loop compensation. The RC network in A1's output prevents it from seeing high speed edges coupled through
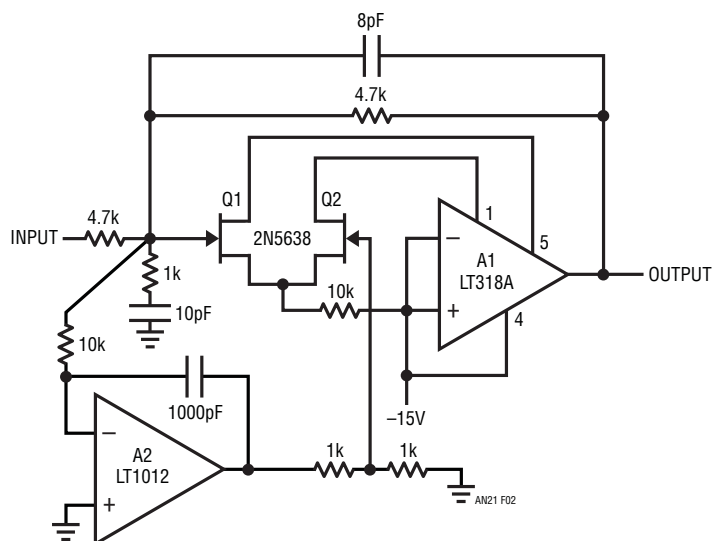

Figure 2. Fast DC-Stabilized FET Amplifier

HORIZONTAL = 100ns/DIV
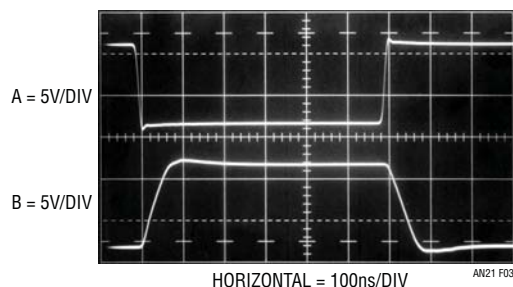
A = 5V/DIV

B = 5V/DIV

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Figure 3. Figure 2's Waveforms

Q2's collector-base junction. A2's output is also fed back to the shield around Q1's gate lead, bootstrapping the circuit's effective input capacitance down to less than 1pF.

The LT1010's 15MHz bandwidth and 100V/µs slew rate, combined with its 150mA output, are fast enough for most circuits. For very fast requirements, the alternate discrete component buffer shown will be useful. Although its output is current limited at 75mA, the GHz range transistors employed provide exceptionally wide bandwidth, fast slewing and very little delay. Figure 5 shows the LTC1052 stabilized buffer circuit's response using the discrete stage. Response is clean and quick, with delay inside 4ns. Slew exceeds 2000V/µs with full-power bandwidth approaching 50MHz. Note that rise time is limited by the pulse generator and not the circuit. For either stage, offset is set by the LTC1052 at 5µV, with gain about 0.95.
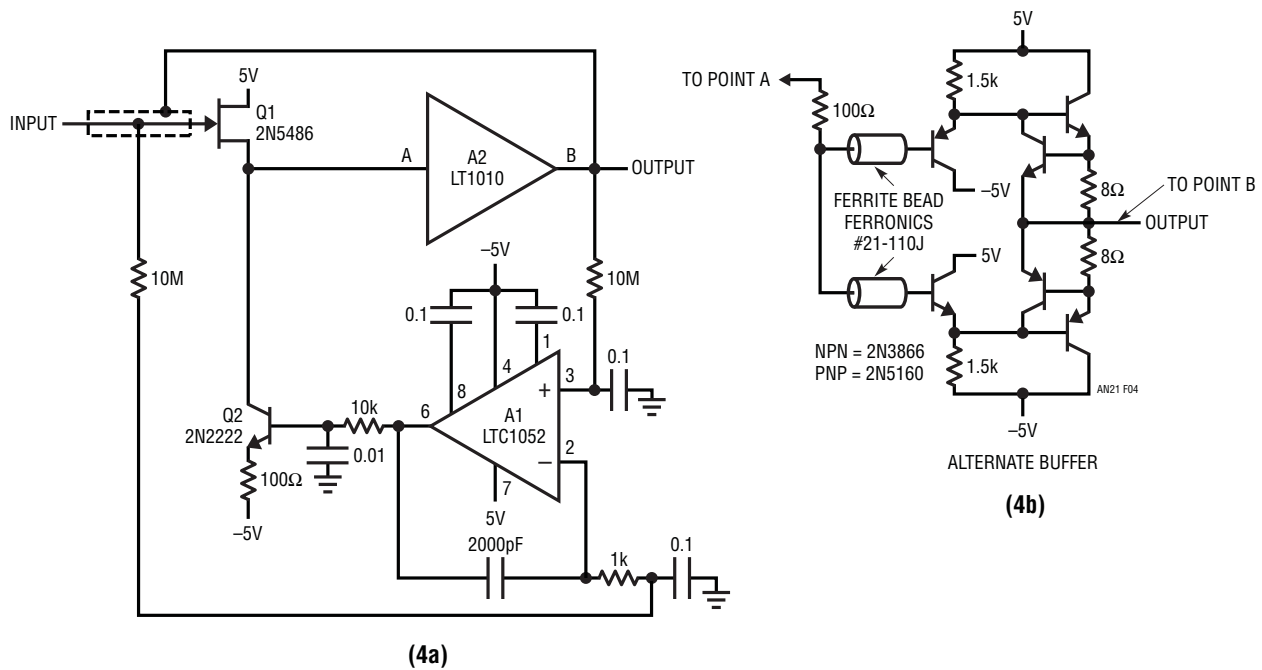

(4a)

(4b)

ALTERNATE BUFFER

Figure 4. Wideband FET Input Stabilized Buffer

A = 0.5V/DIV
B = 0.5V/DIV

HORIZONTAL = 10ns/DIV

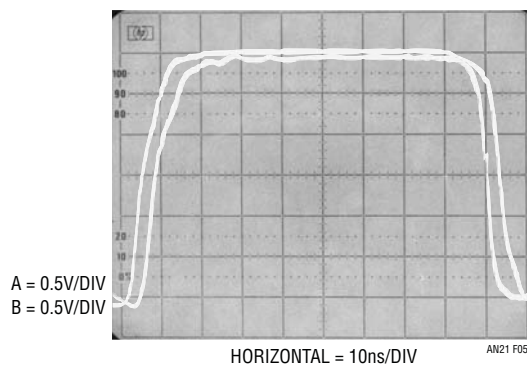**Figure 5. Figure 4's Waveforms**

A potential difficulty with Figure 4's circuit is that the gain is not quite unity. Figure 6 maintains high speed and low bias while achieving a true unity-gain transfer function.

This circuit is somewhat similar to Figure 4, except that the Q2-Q3 stage takes gain. A2 DC stabilizes the input-output path, and A1 provides drive capability. Feedback is to Q2's emitter from A1's output. The 1k adjustment allows the gain to be precisely set to unity. With the LT1010 output stage slew and full-power bandwidth ($1V_{P-P}$) are 100V/µs and 10MHz, respectively. –3dB bandwidth exceeds 35MHz. At

A = 10 (e.g., 1k adjustment set at 50Ω) full-power bandwidth stays at 10MHz while the –3dB point falls to 22MHz.

With the optional discrete stage, slew exceeds 1000V/µs and full-power bandwidth ($1V_{P-P}$) is 18MHz. –3dB bandwidth is 58MHz. At A = 10, full power is available to 10MHz, with the –3dB point at 36MHz.

Figures 7a and 7b show response with both output stages. The LT1010 is used in Figure 7a (Trace A = input, Trace B = output). Figure 7b uses the discrete stage and is slightly faster. Either stage provides more than adequate
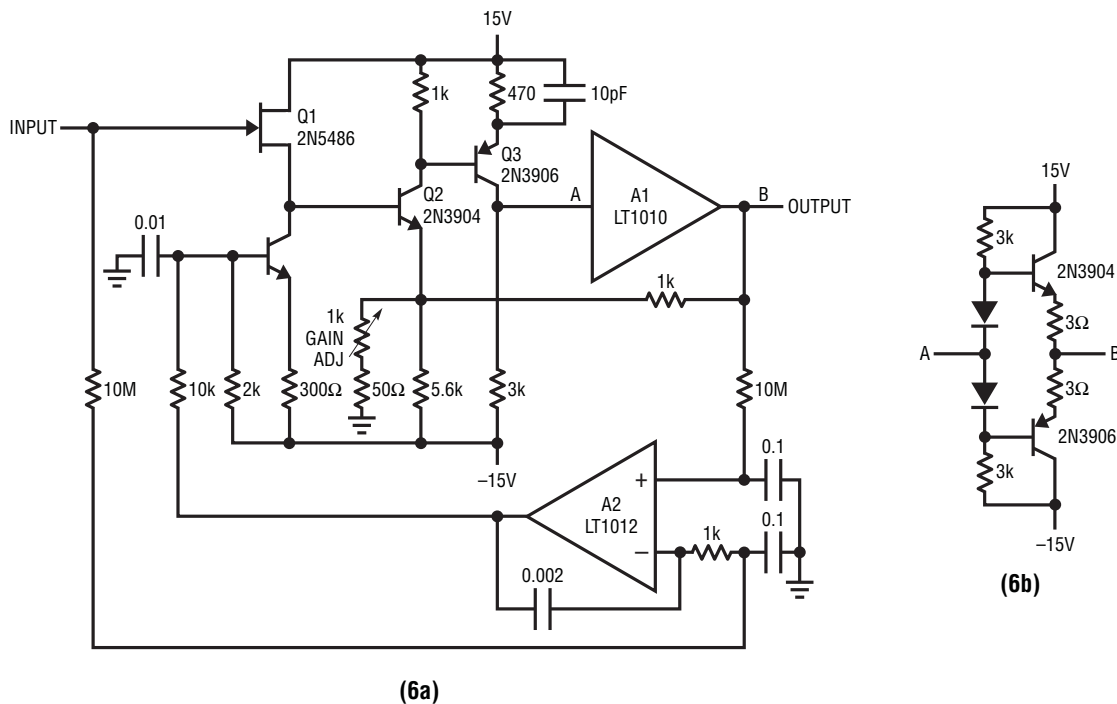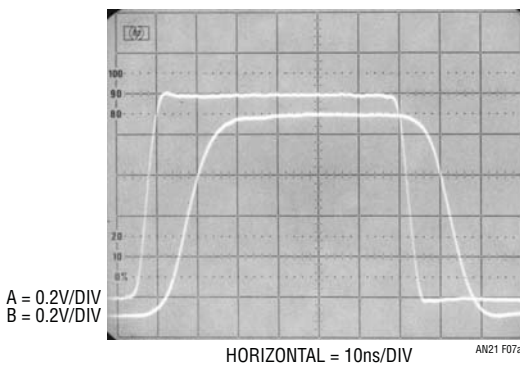

(6a)

(6b)

Figure 6. Gain Trimmable Wideband FET Amplifier

A = 0.2V/DIV
B = 0.2V/DIV

HORIZONTAL = 10ns/DIV   AN21 F07a

Figure 7a. Figure 6's Waveforms Using the LT1010

A = 0.2V/DIV
B = 0.2V/DIV

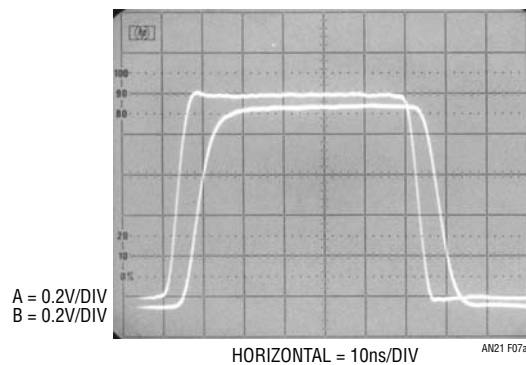HORIZONTAL = 10ns/DIV   AN21 F07a

Figure 7b. Figure 6's Waveforms Using Discrete Stage

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performance for driving video cable or data converters, and the LT1012 maintains DC stability under all conditions.

Figure 8 is another DC-stabilized fast amplifier which functions over a wide range of gains (typically 1-10). It combines the LT1010 and a fast discrete stage with an LT1008 based DC stabilizing loop. Q1 and Q2 form a differential stage which single-ends into the LT1010. The circuit delivers $1V_{P-P}$ into a typical 75Ω video load. At A = 2, the gain is within 0.5dB to 10MHz with the –3dB point occurring at 16MHz. At A = 10, the gain is flat (±0.5dB to 4MHz) with a –3dB point at 8MHz. The peaking adjustment should be optimized under loaded output conditions.

Normally, the Q1-Q2 pair would be quite drifty, but the LT1008 corrects for this. This correction stage is similar to the one in Figures 4 and 6, except that the feedback is taken from a divided down sample of the fast amplifier. The ratio of this divider should be set to the same value as the circuit's closed-loop gain. Frequency roll-off of this stage is set by the 1M-0.022µF filters in the LT1008's input lines. The 0.22µF capacitor at the amplifier eliminates oscillations. The DC loop servo controls drift by biasing the DC operating point of Q2's collector to force zero error between the LT1008's inputs.

This is a simple stage for fast applications where relatively low output swing is required. Its $1V_{P-P}$ output works nicely for video circuits. A possible problem is the relatively high bias current, typically 10µA. Additional swing is possible, but more circuitry is needed.
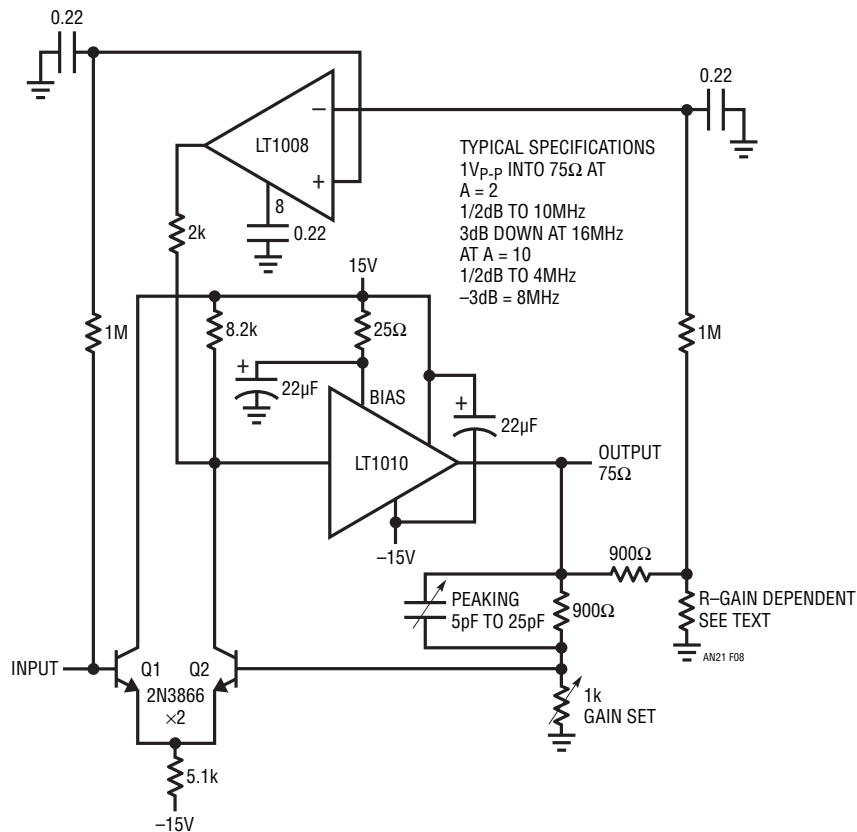

Figure 8. Fast, Stabilized Noninverting Amplifier

Figure 9's circuit addresses these issues. It trades speed for output swing and reduced bias current. As before, a separate loop maintains DC stability. This circuit is a good example of an approach made practical by composite techniques. Without the separate stabilizing loop, the DC imbalances in the signal path would preclude any level of operation.

In this arrangement a PNP level-shifting stage (Q4) has been added to Figure 8's circuit to increase available swing at the LT1010 output. This is obtained at the expense of available bandwidth and amplifier stability. The 33pF capacitor from Q4's collector to the circuits summing node (Q3's gate) affords stable loop compensation.

Figure 8's bias current errors are eliminated by Q3, a FET source follower. This device buffers the summing point from the relatively high bias current required by Q2. Normally, this configuration would cause volts of offset, due to Q3's gate-source voltage. Here, A1 closes a DC restoration loop, forcing Q1's base to whatever point is required to compensate for the offset. Thus, A1's operation not only provides low DC error but permits a simplistic approach to minimizing summing point bias current. Figure 10 shows operating waveforms for a 10V output. Trace A is the input, while Trace B is the output. Slew rate is about 100V/µs, with a full-power bandwidth of 1MHz. The LT1010 allows 100mA outputs and makes cable driving practical at these speeds.
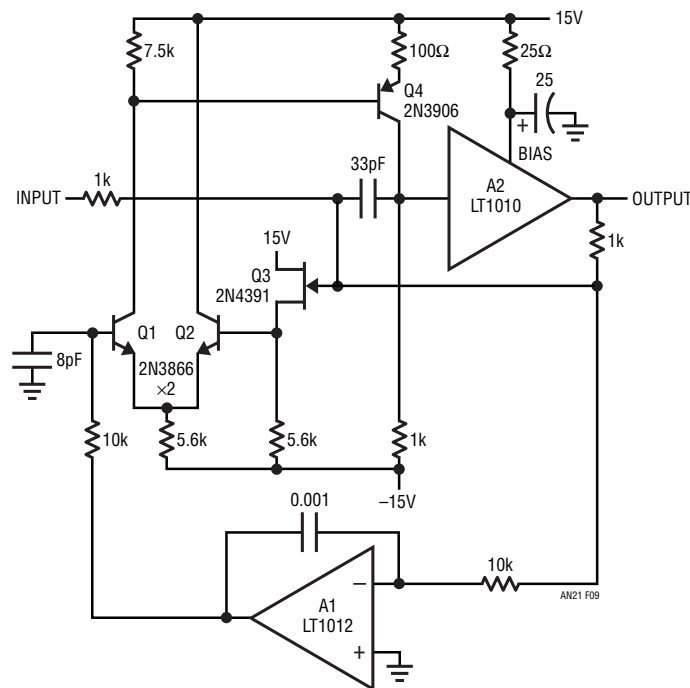
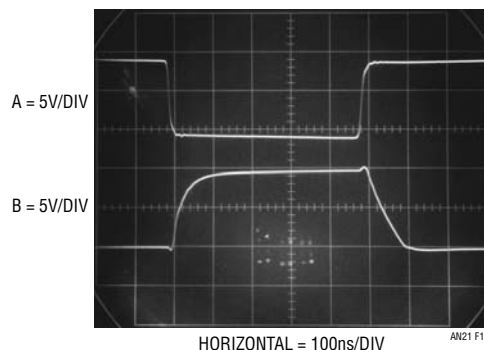**Figure 9. Fast, Stabilized Inverting Amplifier with Low Summing Point Bias Current**

Figure 10. Figure 9's Pulse Response

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Figure 11 shows another fast stage with wide output swing. The circuit is noninverting, and has higher input impedance than Figure 9. Additionally, it's operation is based on an arrangement commonly referred to as "current mode" feedback. This technique, well established in RF design and also employed in some monolithic instrumentation amplifiers, permits fixed bandwidth over a wide range of closed-loop gains. This contrasts with normal feedback schemes, where bandwidth degrades as closed-loop gain increases.

The overall amplifier is composed of two LT1010 buffers and a gain stage, Q1 and Q2. A3 acts as a DC restoration loop. The 33Ω resistors sense A1's operating current, biasing Q1 and Q2. These devices furnish complementary voltage gain to A2, which provides the circuit's output. Feedback is from A2's output to A1's output, which is a low impedance point.

A3's stabilizing loop compensates large offsets in the signal path, which are dominated by mismatch in Q1 and

Q2. Correction is implemented by controlling the current through Q3, which shunts Q2's base bias resistor. Adequate loop capture range is assured by deliberate skewing of Q1's operating point via the 330Ω unit. The 9k-1k feedback divider feeding A3 is selected to equal the gain ratio of the circuit, in this case 10.

The feedback scheme makes A1's output look like the negative input of the amplifier, with closed-loop gain set by the ratio of the 470Ω and 51Ω resistors. The outstanding feature of this connection is that bandwidth becomes relatively independent of closed-loop gain over a reasonable range. For this circuit, full-power bandwidth remains at 1MHz over gains of 1 to about 20. The loop is quite stable, and the 15pF value at A2's input provides good damping over a wide range of gains. The LT1010 buffers limit bandwidth in this circuit. Dramatic speed improvement is possible if they are replaced by discrete stages.
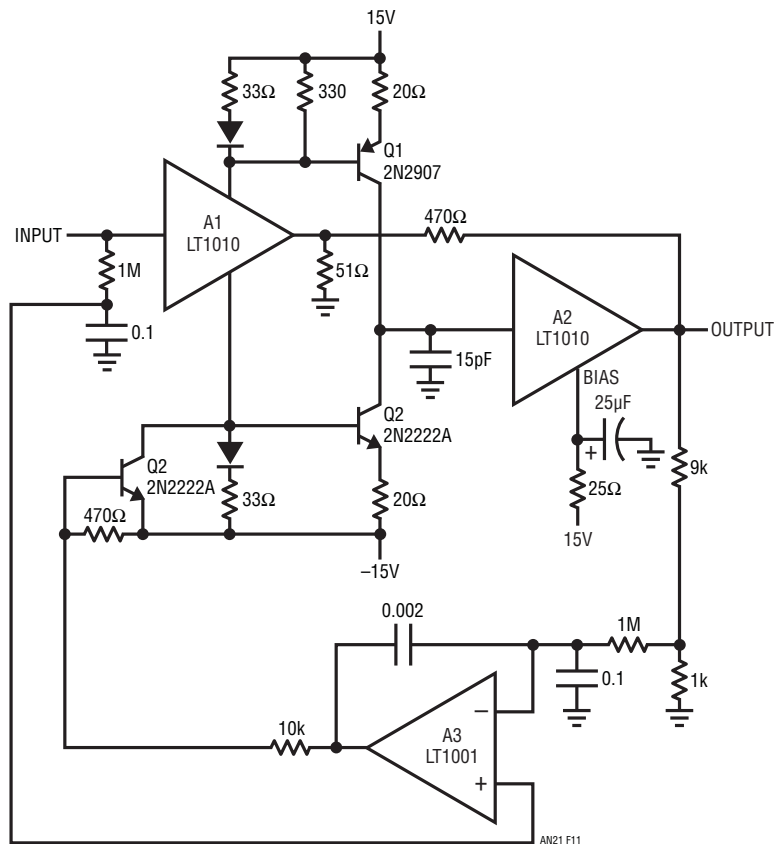

Figure 11. "Current Mode Feedback" Amplifier

Figure 12 substitutes discrete elements for Figure 11's LT1010s. Although this arrangement is substantially more complex, it provides an extraordinarily wideband amplifier. This composite design is composed of three amplifiers; the discrete wideband stage, a quiescent current control amp and an offset servo. Q1-Q4 replace Figure 11's A1, although complementary voltage gain is taken at the collectors Q3 and Q4. Q5 and Q6 provide additional
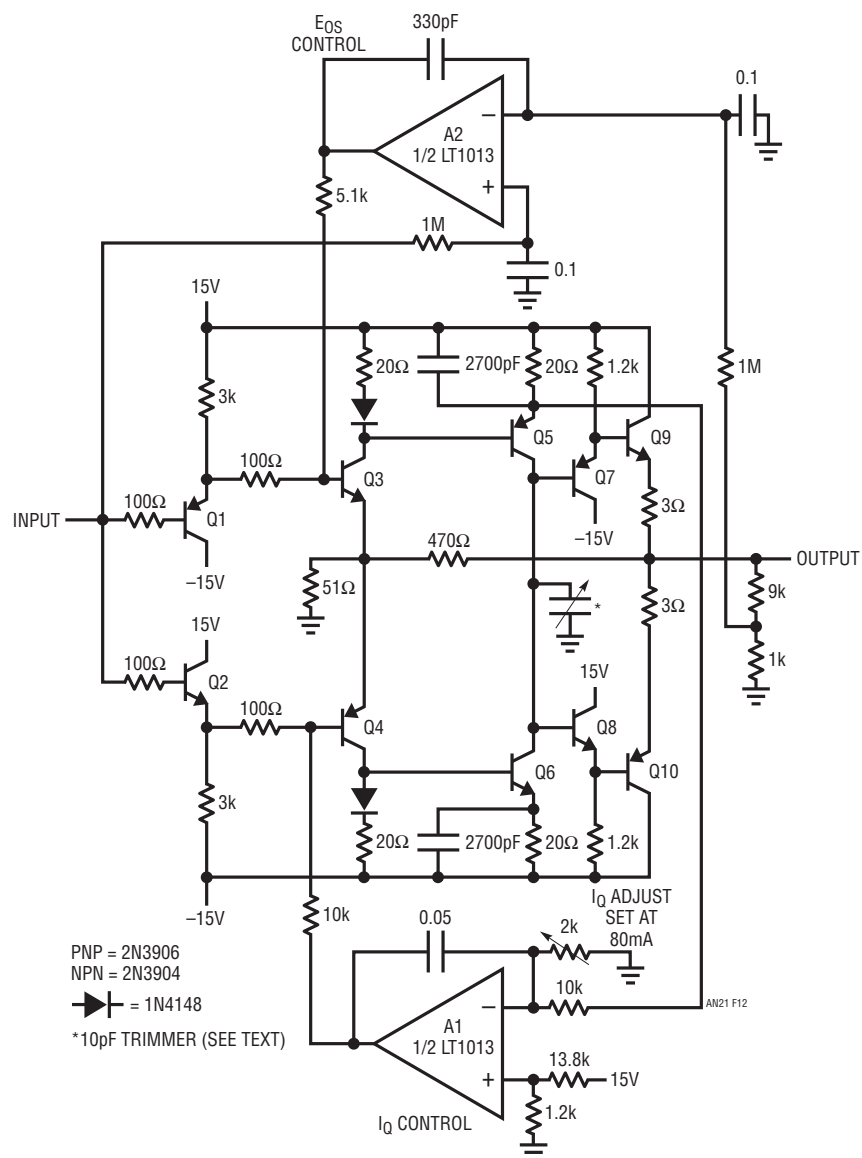

Figure 12. Stabilized, Ultra-Wideband "Current Mode Feedback" Amplifier (Son of Godzilla Amplifier)

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gain, similar to Q1 and Q2 in Figure 11. Q7-Q10 form the output buffer stage. The feedback scheme is identical to Figure 11's, with summing action at the Q3-Q4 emitter connection. To obtain maximum bandwidth, quiescent current is quite high. Without closed-loop control, the circuit will quickly go into thermal runaway and destroy itself. A1 provides the required servo control of quiescent current. It downs this by sampling a resistively divided version of the voltage across Q5's emitter resistor and comparing it to a power supply derived reference. A1's output biases Q4, completing a loop which forces fixed current through Q5. This action effectively controls overall quiescent current in the discrete stage. Simultaneously, A2 corrects for offset by forcing Q3's base to equalize the DC input and output values at the discrete stage. Because the closed-loop gain is set at 10 (470Ω and 51Ω ratio), A2 samples the output via the 10:1 divider. Both A1 and A2 have local roll-off, limiting their response to low frequency. Casual consideration of A1 and A2's operation might raise concern about interaction, but detailed analysis shows this is not so. The offset and quiescent current loops do not influence each others operation.

When this circuit is constructed using high frequency layout techniques and a ground plane, performance is quite impressive. For gains of 1 to 20, full-power bandwidth remains at 25MHz, with the −3dB point beyond 110MHz. Slew rate exceeds 3000V/μs. These figures can be improved upon by using RF transistors, although the types shown are inexpensive and readily available. Figure 13 shows pulse response for a ±12V output (Trace B) at a gain of 10 (input is Trace A). Delay is about 6ns, with rise time limited by the input pulse generator. Damping is optimized with the 10pF trimmer at the Q5-Q6 collector line. To use this circuit, adjust the I_Q level to 80mA *IMMEDIATELY* after turn on. Next, set A2's input resistor divider to a ratio appropriate to the closed-loop circuit gain. Finally, adjust the 10pF trimmer for best response. Note that, in the interests of speed, this circuit has no output protection.
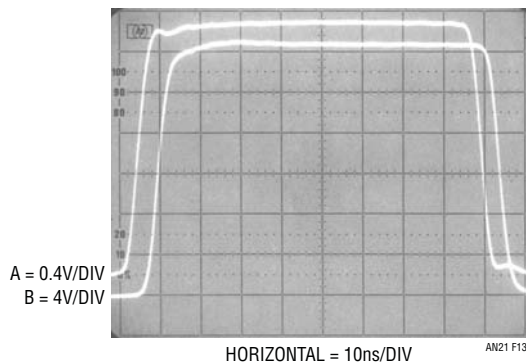

A = 0.4V/DIV
B = 4V/DIV

HORIZONTAL = 10ns/DIV   AN21 F13

Figure 13. Figure 12's Pulse Response (Measurement Limited by Pulse Generator)

Although speed and offset combinations are the most common area for composite techniques, other circuits are possible. Figure 14 shows a way to combine a low drift chopper-stabilized amplifier with an ultralow noise bipolar amplifier. The LTC1052 measures the DC error at the LT1028's input terminals and biases its offset pins to force offset to a few microvolts. The 1N758 Zeners allow the LTC1052 to function from ±15V rails. The offset pin biasing at the LT1028 is arranged so the LTC1052 will always

be able to find the servo point. The 0.01µF capacitor rolls off the LTC1052 at low frequency, and the LT1028 handles high frequency signals. The combined characteristics of these amplifiers yield the following performance:

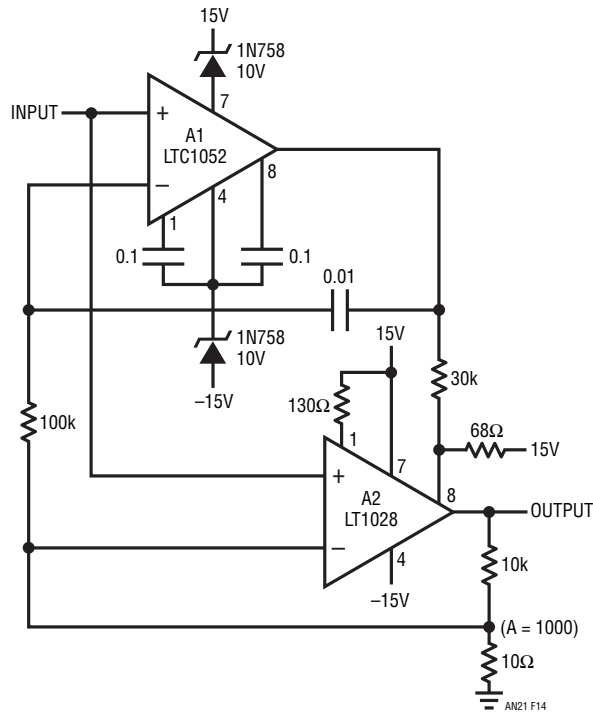|	
Offset Voltage	5µV Max
Offset Drift	50nV/°C Max
Noise	1.1nV $\sqrt{Hz}$ Max

Figure 14. DC-Stabilized, Low Noise Amplifier

Figure 15 plots noise amplitude over time in a 0.1Hz to 10Hz bandwidth.

Figure 16 uses multiple LT1028 low noise amplifiers in a statistical noise reduction technique. It is based on the fact that noise decreases by the $\sqrt{N}$ of the number of devices in parallel. For example, for nine paralleled amplifiers, noise would decrease by a factor of three, to about $0.33nV\sqrt{Hz}$ at 1kHz. A potential penalty of this connection is that the input current noise increases by $\sqrt{N}$ devices.
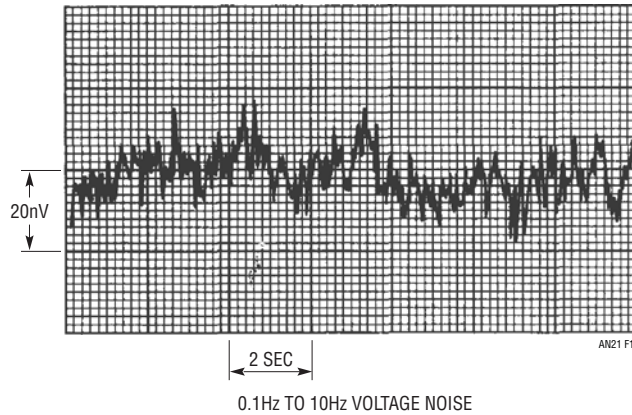

2 SEC

0.1Hz TO 10Hz VOLTAGE NOISE

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Figure 15. Figure 14's Noise vs Time

$$GAIN = N \times 200$$
$$OUTPUT\ NOISE = \sqrt{N} \times 200 \times 1.1nV/\sqrt{Hz}$$
$$INPUT\ NOISE = \frac{OUTPUT\ NOISE}{N \times 200} = \frac{1.1}{\sqrt{N}}\ nV/\sqrt{Hz}$$
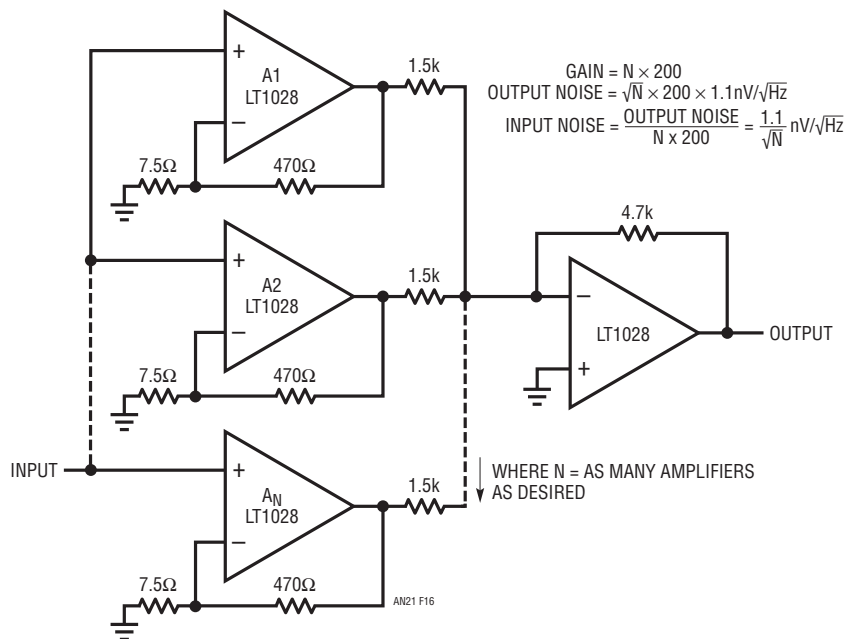
WHERE N = AS MANY AMPLIFIERS AS DESIRED

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Figure 16. Low Noise Amplifier Using Paralleled Amplifiers

A final circuit, Figure 17, uses a composite of paralleled LT1010 buffers to create a simple, high current stage. Parallel operation provides reduced output impedance, more drive capability and increased frequency response under load. Any number of LT1010s can be directly paralleled as long as the increased dissipation in individual units caused by mismatches of output resistance of offset voltage is taken into account.

When the inputs and outputs of two buffers are connected together, a current, ΔI_{OUT}, flows between the outputs:

$$\Delta I_{OUT} = \frac{V_{OS1} - V_{OS2}}{R_{OUT1} + R_{OUT2}}$$

where V_{OS} and R_{OUT} are the offset voltage and output resistance of the respective buffers.

Normally, the negative supply current of one unit will increase and the other decrease, with the positive supply current staying the same. The worst-case ($V_{IN} \to V^+$) increase in standby dissipation can be assumed to be $\Delta I_{OUT} V_T$, where V_T is the total supply voltage.

Offset voltage is specified worst-case over a range of supply voltages, input voltage and temperature. It would be unrealistic to use these worst-case numbers above because paralleled units are operating under identical conditions. The offset voltage specified for $V_S = \pm15V$, $V_{IN} = 0$ and $T_A = 25°C$ will suffice for a worst-case condition.

Output load current will be divided based on the output resistance of the individual buffers. Therefore, the available output current will not quite be doubled unless output resistances are matched. As for offset voltage above, the 25°C limits should be used for worst-case calculations.

Parallel operation is not thermally unstable. Should one unit get hotter than its mates, its share of the output and its standby dissipation will decrease.

As a practical matter, parallel connection needs only some increased attention to heat sinking. In some applications a few ohms equalization resistance in each output may be wise. Only the most demanding applications should require matching, and then just of output resistance at 25°C.
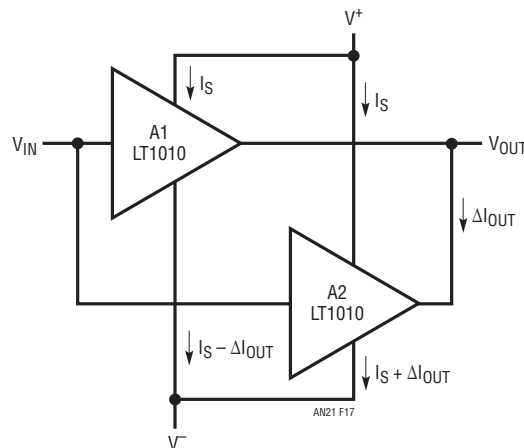

Figure 17. Paralleling Scheme for High Current Output