# Low Noise, Voltage-Boosted Varactor Driver

**OBSOLETE:**
**FOR INFORMATION PURPOSES ONLY**
Contact Linear Technology for Potential Replacement

## FEATURES

- **Generates 5V Varactor Drive from a 3V Supply**
- Wide Supply Voltage Range: 2.7V to 6V
- **Requires Only Three External Components**
- Micropower Operation: 400μA at 3V Supply
- Shutdown Mode Drops Supply Current Below 1μA
- **Low Output Noise: 15μ$V_{RMS}$**
- Amplifier Gain: 2.3
- Up to 500kHz Signal Bandwidth
- MS8 and SO-8 Packages
- Very Low Input Bias Current: 10nA Max
- Amplifier Offset Maintains Phase Detector in Linear Region

## APPLICATIONS

- 5V Varactor Drive from a Single Li-Ion Cell
- 5V Varactor Drive from Three NiCd/NiMH Cells
- Cellular Telephones
- Portable RF Equipment
- Radio Modems
- Wireless Data Transmission



## DESCRIPTION

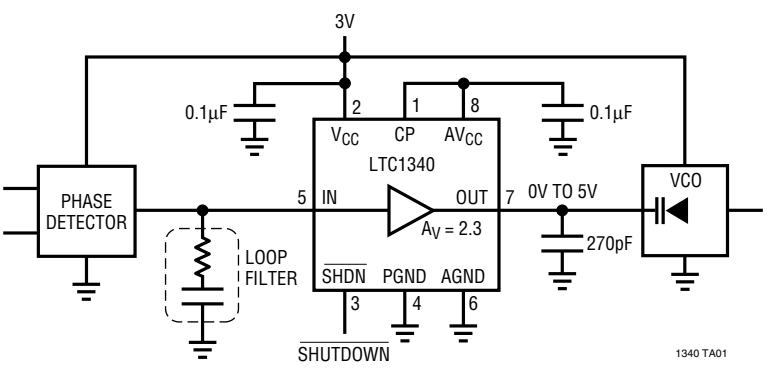
The LTC®1340 is a varactor diode driver designed to generate 5V varactor drive from a single 3V or higher voltage supply. It includes a low noise amplifier with an internal gain of 2.3 and a self-contained charge pump to generate output voltages above the input supply. The amplifier input stage includes a built-in offset voltage that allows the output voltage to swing to ground without requiring OV on the input. This feature maintains the phase detector within its linear range of operation. The LTC1340 requires only three external surface mount capacitors to implement a complete varactor driver module.

The LTC1340 features output referred noise of 15μ$V_{RMS}$, minimizing frequency deviation in PLL frequency synthesizer systems. Supply current is 400μA typically with a 3V supply, and drops to 1μA in shutdown, maximizing operating life in battery-powered systems. Amplifier bandwidth is user-adjustable from 10kHz up to 500kHz and the output typically sinks or sources 20μA, allowing fast output signal changes with a typical varactor load. The amplifier input features rail-to-rail input common mode range, allowing it to interface with the output of virtually any phase detector circuit.

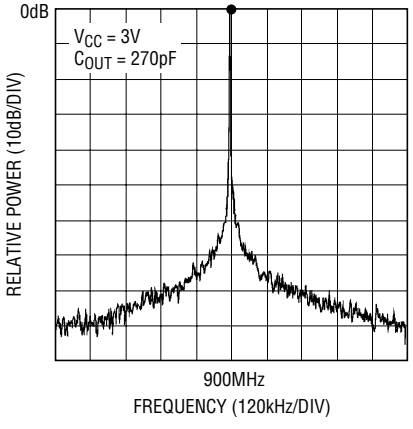
The LTC1340 is available in MS8 and SO-8 packages.

## TYPICAL APPLICATION

**Low Voltage Frequency Synthesizer**




**Spectral Plot of VCO Output Driven by LTC1340**
**Resolution Bandwidth = 300Hz**

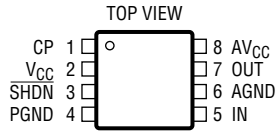


## ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V_{CC}$) ..... 7V
Input Voltage ($AV_{CC}$) ..... 14V
Input Voltage ($\overline{SHDN}$, IN) ..... –0.3V to $V_{CC}$ + 0.3V
Output Voltage (CP, OUT) ..... –0.3V to $AV_{CC}$ + 0.3V
Output Short-Circuit Duration ..... Indefinite

Commercial Temperature Range ..... 0°C to 70°C
Extended Commercial Operating
Temperature Range (Note 1) ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

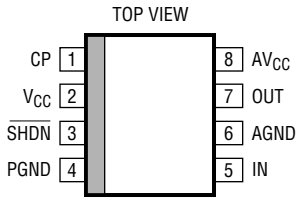
## PACKAGE/ORDER INFORMATION




MS8 PACKAGE
8-LEAD PLASTIC MSOP

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 200°C/W

| ORDER PART NUMBER |
|---|
| LTC1340CMS8 |
| MS8 PART MARKING |
| LTBM |




S8 PACKAGE
8-LEAD PLASTIC SO

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 130°C/W

| ORDER PART NUMBER |
|---|
| LTC1340CS8 |
| S8 PART MARKING |
| 1340 |

Consult factory for Industrial and Military grade parts.

## ELECTRICAL CHARACTERISTICS

**$T_A$ = 25°C, unless otherwise noted. (Note 1)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Input Supply Voltage | | ● | 2.7 | | 6 | V |
| $I_{CC}$ | Supply Current | $I_{OUT}$ = 0, 2.7V ≤ $V_{CC}$ ≤ 6V<br>Shutdown, 2.7V ≤ $V_{CC}$ ≤ 6V | ●<br>● | | 500<br>1 | 900<br>10 | µA<br>µA |
| $V_{OL}$ | Low Output Voltage Swing | $V_{CC}$ = 2.7V, 6V, $\lvert I_{OUT}\rvert$ = 0µA<br>$V_{CC}$ = 2.7V, 6V, $\lvert I_{OUT}\rvert$ = 14µA | ●<br>● | | | 0.25<br>0.6 | V<br>V |
| $V_{OH}$ | High Output Voltage Swing | $V_{CC}$ = 2.7V, $\lvert I_{OUT}\rvert$ = 0µA<br>$V_{CC}$ = 6V, $\lvert I_{OUT}\rvert$ = 0µA<br>$V_{CC}$ = 2.7V, $\lvert I_{OUT}\rvert$ = 14µA<br>$V_{CC}$ = 6V, $\lvert I_{OUT}\rvert$ = 14µA | ●<br>●<br>●<br>● | 4.6<br>10.5<br>4.25<br>9.75 | | | V<br>V<br>V<br>V |
| $I_{OUT}$ | Output Sink/Source Current | 0.6V ≤ $V_{OUT}$ ≤ 4.25V, $V_{CC}$ = 2.7V<br>0.6V ≤ $V_{OUT}$ ≤ 9.75V, $V_{CC}$ = 6V | ●<br>● | ±14<br>±14 | ±20<br>±20 | ±35<br>±35 | µA<br>µA |
| $t_{OUT}$ | Output Transition Time | $C_{OUT}$ = 1nF, $\Delta V_{OUT}$ = ±4V | ● | | 200 | 285 | µs |
| $V_{IN}$ | Input Voltage Range | | ● | 0 | | $V_{CC}$ | V |
| $I_B$ | Input Bias Current | 0.1V ≤ $V_{IN}$ ≤ $V_{CC}$ | <br>● | | ±0.01 | ±1<br>±10 | nA<br>nA |
| $V_{OS}$ | Input Offset Voltage | | ● | 0.15 | 0.35 | 0.60 | V |
| $A_V$ | Amplifier Gain | $V_{IN}$ = 1V, $AV_{CC}$ = 5V | ● | 2.1 | 2.3 | 2.5 | V/V |
| $g_m$ | Amplifier Transconductance | $V_{OUT}$ = 2.5V, $AV_{CC}$ = 5V<br>$V_{OUT}$ = 2.5V, $AV_{CC}$ = 5V | <br>● | 1200<br>800 | 1800 | 2300<br>3200 | µmho<br>µmho |
| $R_{OUT}$ | Output Impedance | $V_{OUT}$ = 1/2$AV_{CC}$ | | | 1 | | MΩ |
| $e_n$ | Output Noise Voltage | 1kHz to 100kHz, $C_{OUT}$ = 1nF | | | 15 | 25 | $\mu V_{RMS}$ |
| BW | –3dB Signal Bandwidth | $C_{OUT}$ = 1nF | | | 125 | | kHz |
| PSRR | Power Supply Rejection Ratio | $AV_{CC}$ = 4V to 6V, $C_{OUT}$ = 1nF | ● | 60 | 90 | | dB |
| $I_{\overline{SHDN}}$ | Shutdown Logic Input Current | 0.1V ≤ $V_{\overline{SHDN}}$ ≤ $V_{CC}$ | | | ±0.01 | ±1 | µA |

## ELECTRICAL CHARACTERISTICS

**$T_A$ = 25°C, unless otherwise noted. (Note 1)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $t_{START}$ | Charge Pump Start-Up Time | $C_{CP}$ = 0.1µF, $V_{CC}$ = 2.7V, $I_{OUT}$ = 0 | ● | | 1.2 | 5 | ms |
| $V_{RIPPLE}$ | Charge Pump Output Ripple at $C_P$ | $C_{CP}$ = $C_{VCC}$ = 0.1µF, $V_{CC}$ = 2.7V, $I_{OUT}$ = 0 (Note 2) | | | 200 | | $\mu V_{P-P}$ |
| $f_{CP}$ | Charge Pump Frequency | (Note 3) | ● | 2.5 | 4 | | MHz |

The ● denotes specifications which apply over the specified temperature range.

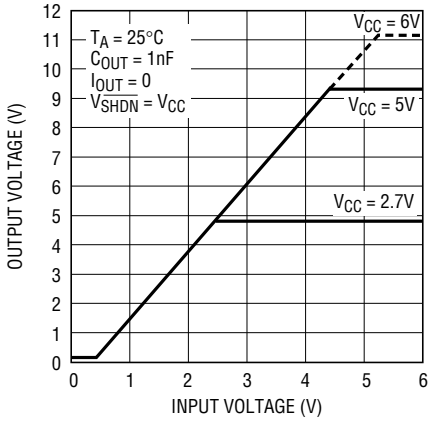
**Note 1:** C grade device specifications are guaranteed over the 0°C to 70°C temperature range. In addition, C grade device specifications are assured over the –40°C to 85°C temperature range by design or correlation, but are not production tested.

**Note 2:** The charge pump output ripple is not tested but is correlated with a PCB ground plane and high quality, low ESR, low ESL metalized polyester 0.1µF capacitors.

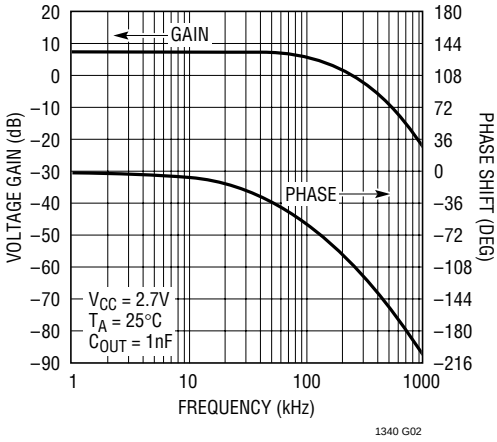
**Note 3:** The internal oscillator typically runs at 2MHz, but the charge pump refreshes the output on both phases of the clock, resulting in an effective 4MHz operating frequency.

## TYPICAL PERFORMANCE CHARACTERISTICS

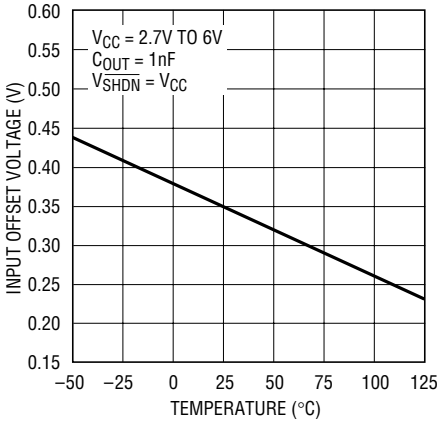
**DC Transfer Curve**



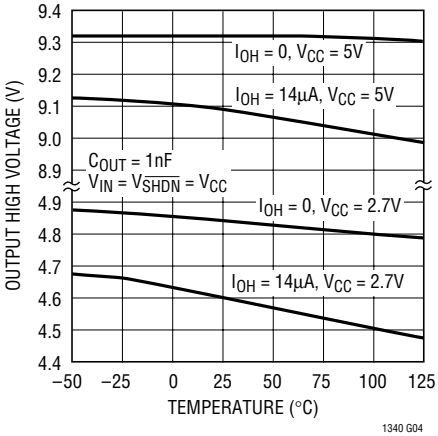

**Gain and Phase Shift vs Frequency**



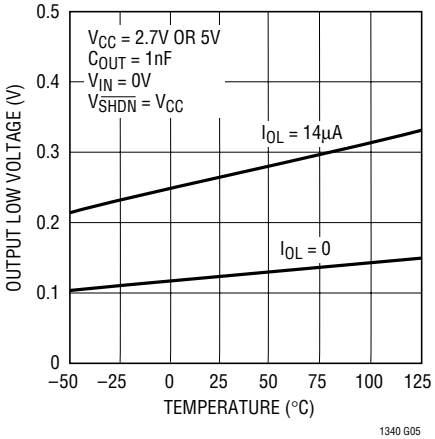

**Input Offset Voltage vs Temperature**



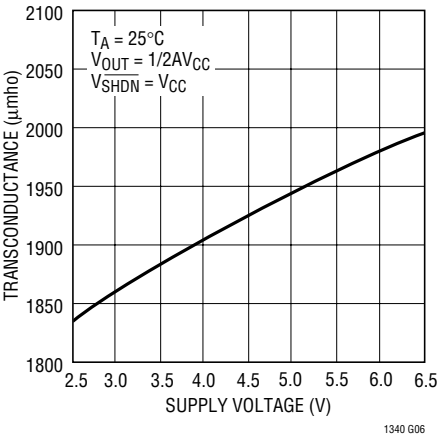

**Output High Voltage vs Temperature**




**Output Low Voltage vs Temperature**

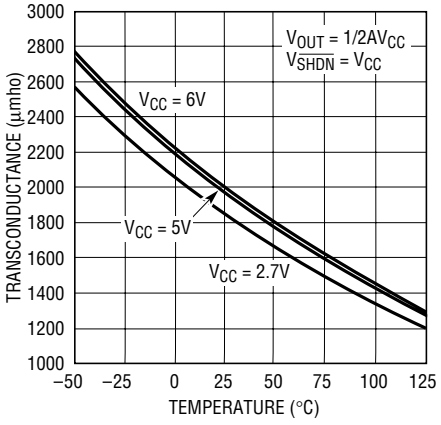



**Transconductance vs Supply Voltage**

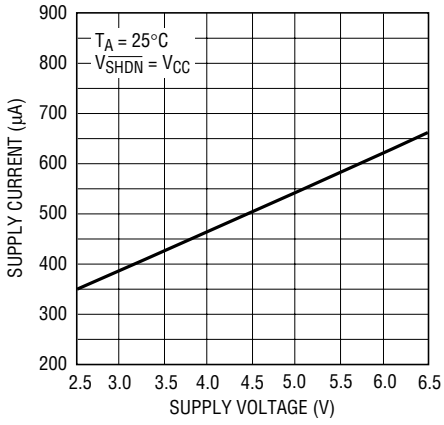


# TYPICAL PERFORMANCE CHARACTERISTICS

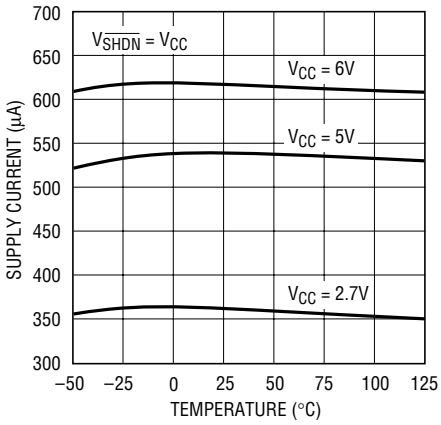
### Transconductance vs Temperature



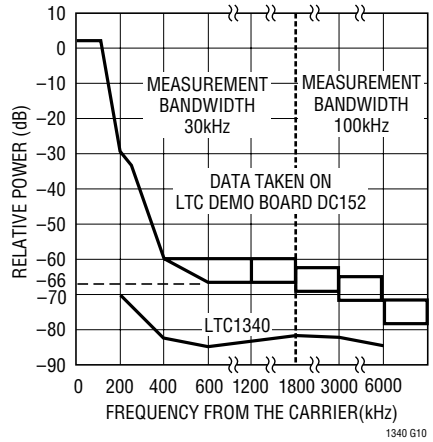

### Supply Current vs Supply Voltage



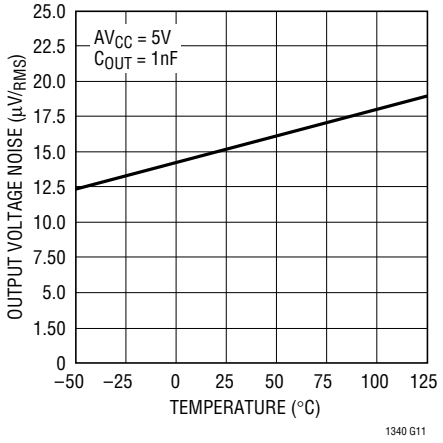

### Supply Current vs Temperature



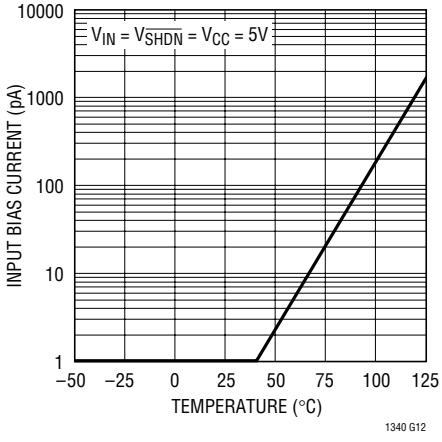

### GSM 900 MS Spectrum Due to Modulation



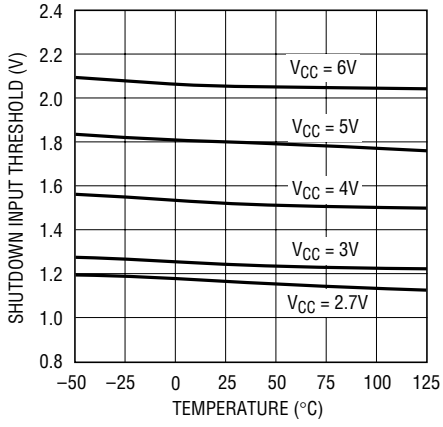

### Output Voltage Noise vs Temperature



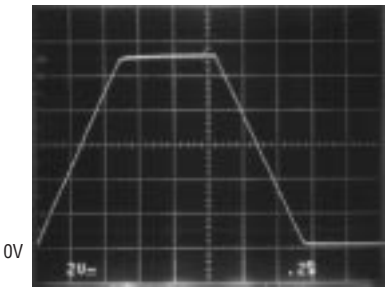

### Input Bias Current vs Temperature



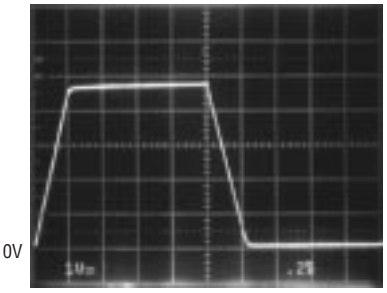

### Shutdown Input Threshold vs Temperature




### Rail-to-Rail Step Response at $V_{CC}$ = 6V

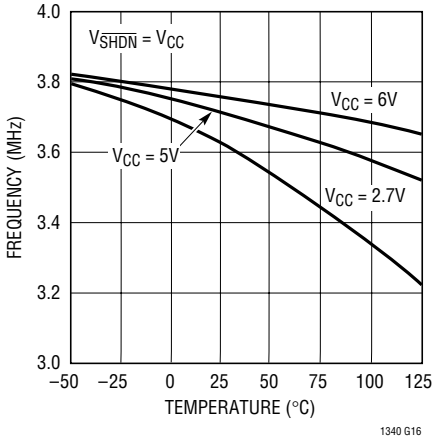



### Rail-to-Rail Step Response at $V_{CC}$ = 2.7V

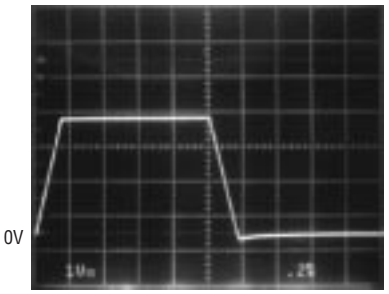


## TYPICAL PERFORMANCE CHARACTERISTICS

**Charge Pump Frequency vs Temperature**

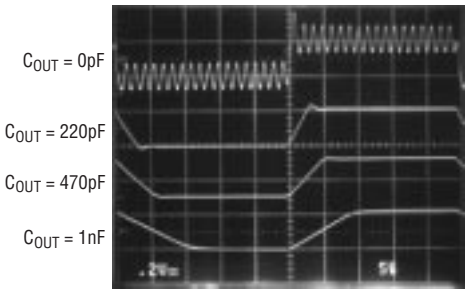



**Large-Signal Response**




$V_{IN}$ = 0.5V TO 2V
$V_{CC}$ = 2.7V
$C_{OUT}$ = 1nF

**Small-Signal Response**




## PIN FUNCTIONS

**CP (Pin 1):** Charge Pump Output. This is the output of the internal charge pump. The voltage at CP is nominally twice the $V_{CC}$ input voltage. Connect CP to an external 0.1µF filter capacitor and $AV_{CC}$.

**$V_{CC}$ (Pin 2):** Supply Input. This is the input supply to the charge pump. $V_{CC}$ can range from 2.7V to 6V and requires a 0.1µF bypass capacitor to PGND.

**$\overline{SHDN}$ (Pin 3)** Shutdown. If $\overline{SHDN}$ is high (>$V_{CC}$ – 0.5V), the LTC1340 operates normally. If $\overline{SHDN}$ is pulled low (<0.5V), the LTC1340 enters shutdown mode and the supply current drops to less than 1µA typically. In shutdown, the charge pump output voltage collapses and the OUT pin enters a high impedance state. If $\overline{SHDN}$ returns high, the charge pump output requires 1.2ms typically to resume full voltage.

**PGND (Pin 4):** Power Ground. This is the charge pump ground. Connect PGND to the system power supply return.

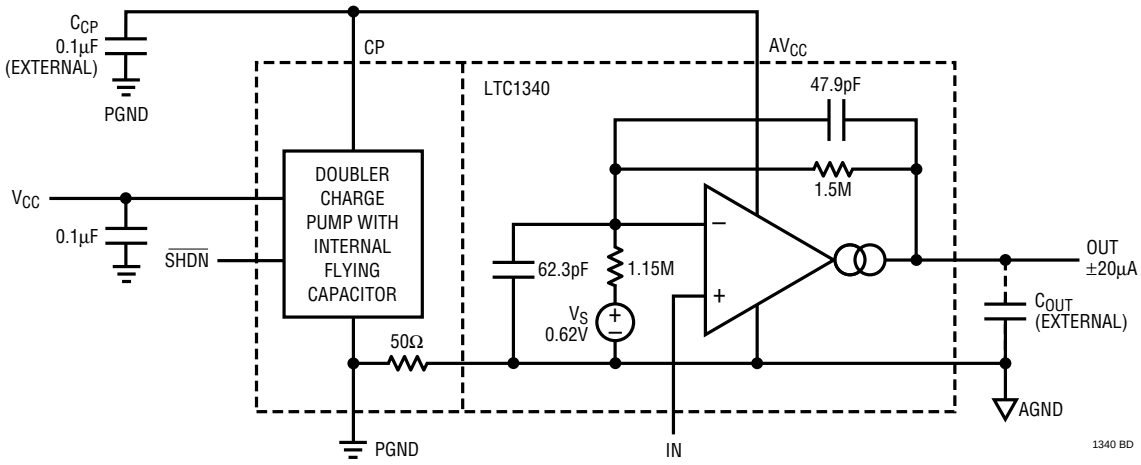
**IN (Pin 5):** Signal Input. The internal amplifier amplifies the signal input at this pin typically by 2.3 to the OUT pin. IN accepts signals from GND to $V_{CC}$ without phase reversal or unusual behavior, allowing a direct connection to the output of virtually any phase detector or loop filter powered from $V_{CC}$.

**AGND (Pin 6):** Signal Ground. Connect AGND to the ground plane in close proximity to the VCO ground. There is an internal parasitic resistance of 50Ω between AGND and PGND.

**OUT (Pin 7):** Driver Output. OUT is the output of the internal $g_m$ amplifier and the internal feedback network. It swings from GND to $AV_{CC}$, and drives a varactor load directly. The OUT pin requires an external capacitor (≥ 220pF) to AGND to ensure stability. OUT typically sinks or sources 20µA.

**$AV_{CC}$ (Pin 8):** Amplifier Supply. LTC recommends a direct connection from $AV_{CC}$ to CP and also recommends a 0.1µF filter capacitor from CP to PGND.

## BLOCK DIAGRAM




## APPLICATIONS INFORMATION

### Overview

The LTC1340 is a monolithic IC that combines a charge pump and a low noise amplifier to provide a 0V to 5V swing to drive a varactor diode-based PLL system from a single 3V supply. Traditional PLL frequency synthesizers used in cellular phones and other portable RF systems use varactor diodes as the voltage variable element in the VCO. Typical varactor diodes require at least 4V of control voltage swing to obtain their full range of capacitance adjustment. Newer battery-powered systems, operating from low voltage power supplies, have trouble providing this bias voltage without an additional step-up circuit.

The LTC1340 design provides a 5V signal swing suitable for biasing such a varactor diode when powered from a 3V or higher voltage supply. The internal op amp and feedback network with built-in offset provide a gain of 2.3 so that a 0.35V to 2.5V swing at the noninverting input provides a 0V to 5V swing at the output. The onboard charge pump provides the boosted voltage necessary to drive the varactor and requires only a single 0.1µF output filter capacitor to complete the boost circuit. The amplifier requires one capacitor (typically 1nF) at its output to set amplifier noise bandwidth and to ensure amplifier stability. The performance characteristics of the LTC1340 are designed to meet the requirements of GSM and similar cellular phone transceivers without requiring additional circuitry. The LTC1340's high level of functional integration allows it to replace several power supply and regulator components in a typical PLL synthesizer. This results in significant space and complexity savings.

### Charge Pump

The LTC1340 features a self-contained doubling charge pump with internal flying capacitors. The charge pump refreshes the output on each phase of the internal 2MHz clock, giving an effective 4MHz switching frequency. An external 0.1µF capacitor at the CP pin acts as a charge reservoir and provides filtering to minimize clock feedthrough to the amplifier section. The CP pin can be connected directly to the amplifier power supply at $AV_{CC}$. In addition, it can be filtered with an RC or LC network prior to its connection to $AV_{CC}$. The LTC1340 minimizes interaction between the charge pump and the amplifier through careful internal shielding.

### Amplifier

The LTC1340 includes an internal $g_m$ amplifier with an on-chip feedback network to amplify the input signal to the gained output level. The amplifier requires an external capacitor from its output to AGND to provide closed-loop stability, noise bandwidth limiting and to further reduce charge pump feedthrough. The –3dB signal bandwidth of the amplifier is given by the following equation:

$$BW_{-3dB} = g_m/(2\pi)(C_{OUT})(A_V)$$

## APPLICATIONS INFORMATION

Amplifier transconductance is typically 1800μmho. With a 1nF external capacitor at the amplifier output, the bandwidth is 125kHz. The amplifier transconductance varies with temperature and process. The minimum recommended $C_{OUT}$ is 220pF with a typical bandwidth of 566kHz.

The slew rate of the amplifier is:

$$SR = I_{OUT}/C_{OUT}$$

The amplifier typically sinks or sources 20μA, allowing it to slew a 1nF output capacitance at 20V/ms, or 5V in 250μs.

The on-chip amplifier feedback network is set for a DC gain of 2.3 with an input offset of 0.35V as shown in the typical curves. The amplifier allows a rail-to-rail input swing with a 3V supply and provides a 5V swing at the output. The output swings to within millivolts of the $AV_{CC}$ voltage and to about 100mV above AGND. The input stage of the amplifier is powered from $AV_{CC}$ and accepts full GND to $V_{CC}$ rail-to-rail input signals without exceeding the input common mode range. The output noise of the amplifier is typically $15\mu V_{RMS}$ at frequencies between 1kHz and 100kHz.

There are two feedthrough signals at the amplifier OUT pin from the charge pump, the main component at 4MHz and the second harmonic signal at 8MHz. The 4MHz feedthrough is typically below 50μV with $C_{OUT}$ equal to 1nF and $C_{CP}$ equal to 0.1μF. The feedthrough signal decreases in amplitude when larger $C_{OUT}$ is used. Most systems should require no additional filtering. Additional filtering to reduce feedthrough noise is possible by inserting a resistor or a ferrite bead between OUT and $C_{OUT}$.

### Hookup

The two sections of the LTC1340 are carefully shielded from each other inside the chip, but care must also be taken in the external hookup to minimize noise at the amplifier output. The two halves of the chip should only meet electrically where the CP and $AV_{CC}$ pins connect together and at the common point of AGND and PGND. Separate PGND and AGND as much as possible. AGND is the amplifier ground. Connect it to a ground plane and as close to the VCO ground as possible. Bypass $V_{CC}$ and CP to PGND with a 0.1μF capacitor. Select high quality, low ESR and low ESL surface mount ceramic capacitors for both the CP and the VCC bypass capacitors. Poor grade capacitors will result in unacceptable ripple amplitude or ringing characteristics. Connect both terminals of the bypass capacitors as close to the chip as possible to minimize charge pump output ripple amplitude and ground currents in the rest of the system. Keep IN and OUT away from $V_{CC}$, CP and $AV_{CC}$ as much as possible. Crosstalk from $V_{CC}$, CP and $AV_{CC}$ PCB traces to IN and OUT PCB traces can be minimized by routing AGND PCB traces as shield as shown in Figures 1 and 2. Connect the 1nF output capacitor close to the varactor diode and return it to the AGND plane. The $\overline{SHDN}$ and IN pins, should not be allowed to go below PGND potential as the ESD diode forms an NPN and bleeds the charge pump output.

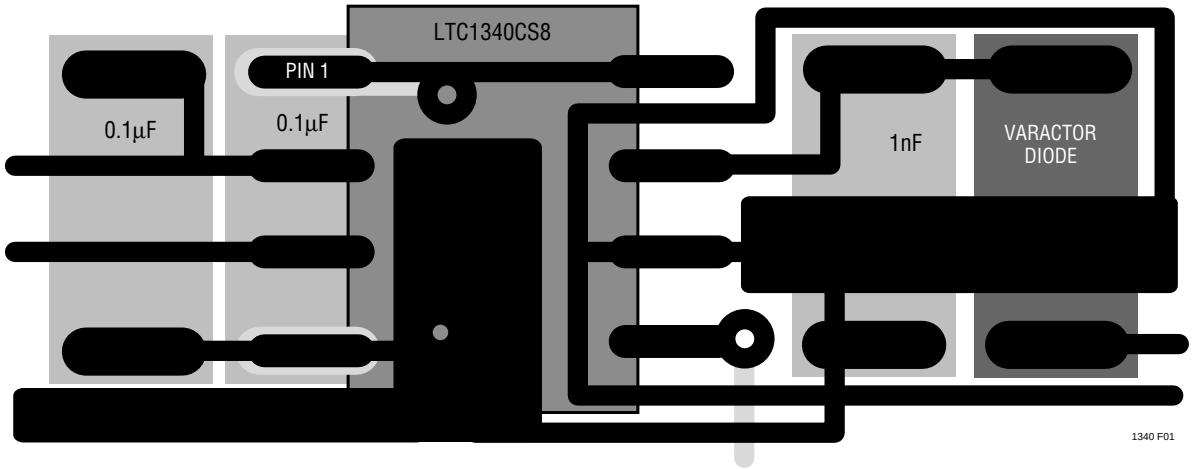



**Figure 1. Suggested Surface Mount PCB Layout for LTC1340CS8**

## APPLICATIONS INFORMATION

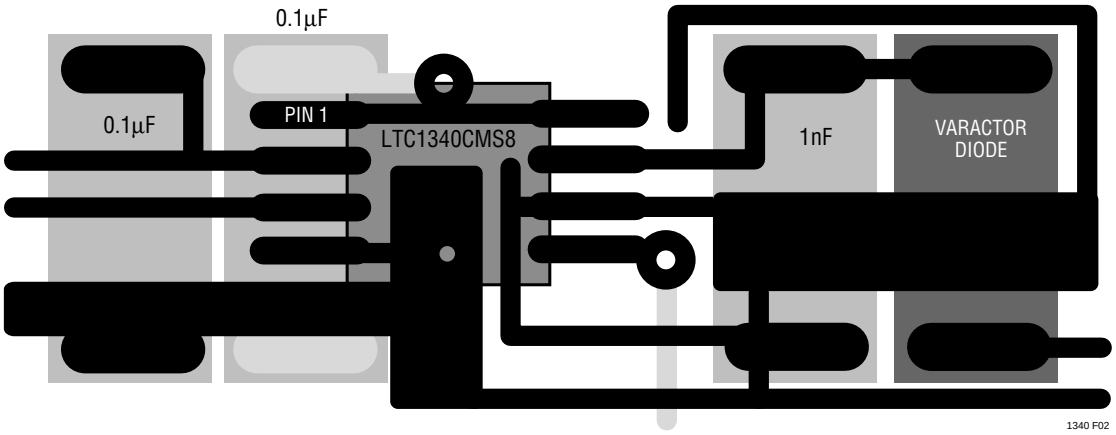
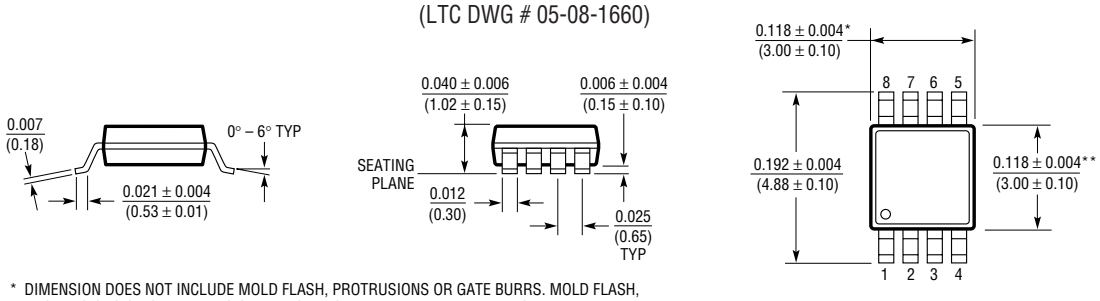



**Figure 2. Suggested Surface Mount PCB Layout for LTC1340CMS8**

## PACKAGE DESCRIPTION

**Dimensions in inches (millimeters) unless otherwise noted.**

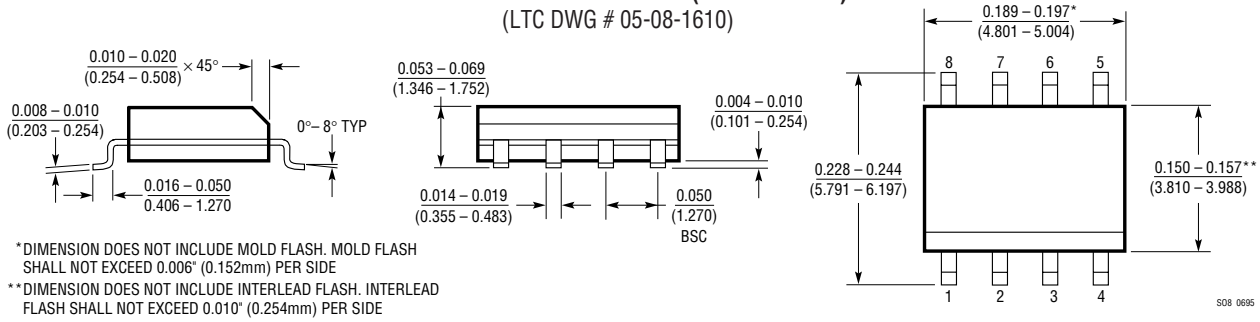
**MS8 Package**
**8-Lead Plastic MSOP**
(LTC DWG # 05-08-1660)




* DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

** DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**S8 Package**
**8-Lead Plastic Small Outline (Narrow 0.150)**
(LTC DWG # 05-08-1610)




*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTC1261, LTC1429, LTC1550, LTC1551 | GaAs FET Bias Generators | Regulated negative voltage generator from a single positive supply |



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