LTC1430 High Power Step-Down Switching Regulator Controller

DESCRIPTION

Introduction

Demo Board DC201 is a synchronous buck regulator designed to provide a low voltage, very high current output for logic devices and high speed ASICs from a 5V input voltage. The heart of the design is the 8-pin LTC®1430CS8 synchronous buck regulator controller. There are two independent synchronous buck regulators operated 180° out of phase with one another, each capable of 15A of output current. The two regulators are forced to share the load current equally. This scheme trades a small amount of additional control-circuit complexity for radical reductions in the volume, and hence cost, of the energy-storage

elements required. Advantages of this approach include very low input and output ripple voltages, higher ripple frequency and extremely fast transient response. The maximum height above the board is less than 6mm and the circuit uses surface mount components exclusively. Continuous load currents of more than 30A and intermittent operation to more than 40A are possible.

The demo board uses tantalum input and output capacitors for the smallest possible board footprint. Both buck inductors are small, low cost, surface mount devices.

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PERFORMANCE SUMMARY $T_A = 25°C$, $V_{IN} = 5V$, S/S pin open, unless otherwise specified.

| PARAMETER		CONDITIONS	VALUE
Input Voltages	Main Power		5V ±5%
	Gate Supply		12V ±10%
Output Voltage			2.5V Nominal
Output Accuracy		Zero Load	±0.5% Typ, ±2% Max
Output Current			30A Continuous, 40A Intermittent
Output Ripple		I_O = 30A, 20MHz Bandwidth	<30mV Peak-Peak
Load Regulation		I_O = 0 to 30A	<20mV
Transient Response		I_O from 10A to 20A, 10μs Rise Time	<60mV Peak
Efficiency		I_O = 20A, V_O = 2.5V	>88% (See Figures 1a, 1b)

TYPICAL PERFORMANCE CHARACTERISTICS AND BOARD PHOTO
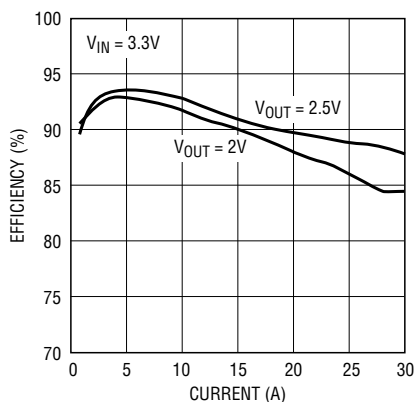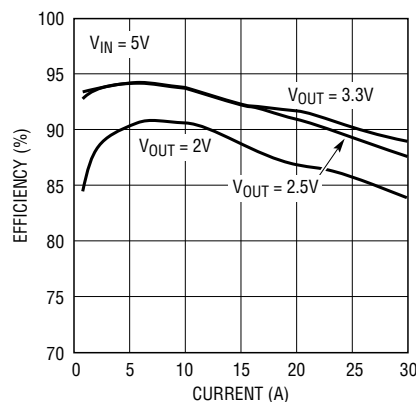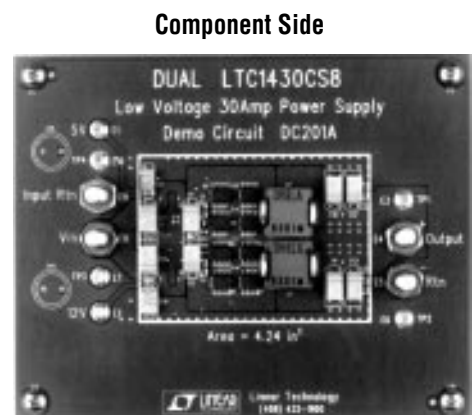

Figure 1a. Efficiency, V_{IN} = 3.3V

Figure 1b. Efficiency, V_{IN} = 5V

Component Side

PACKAGE A ID SCHEMATIC DIAGRAMS
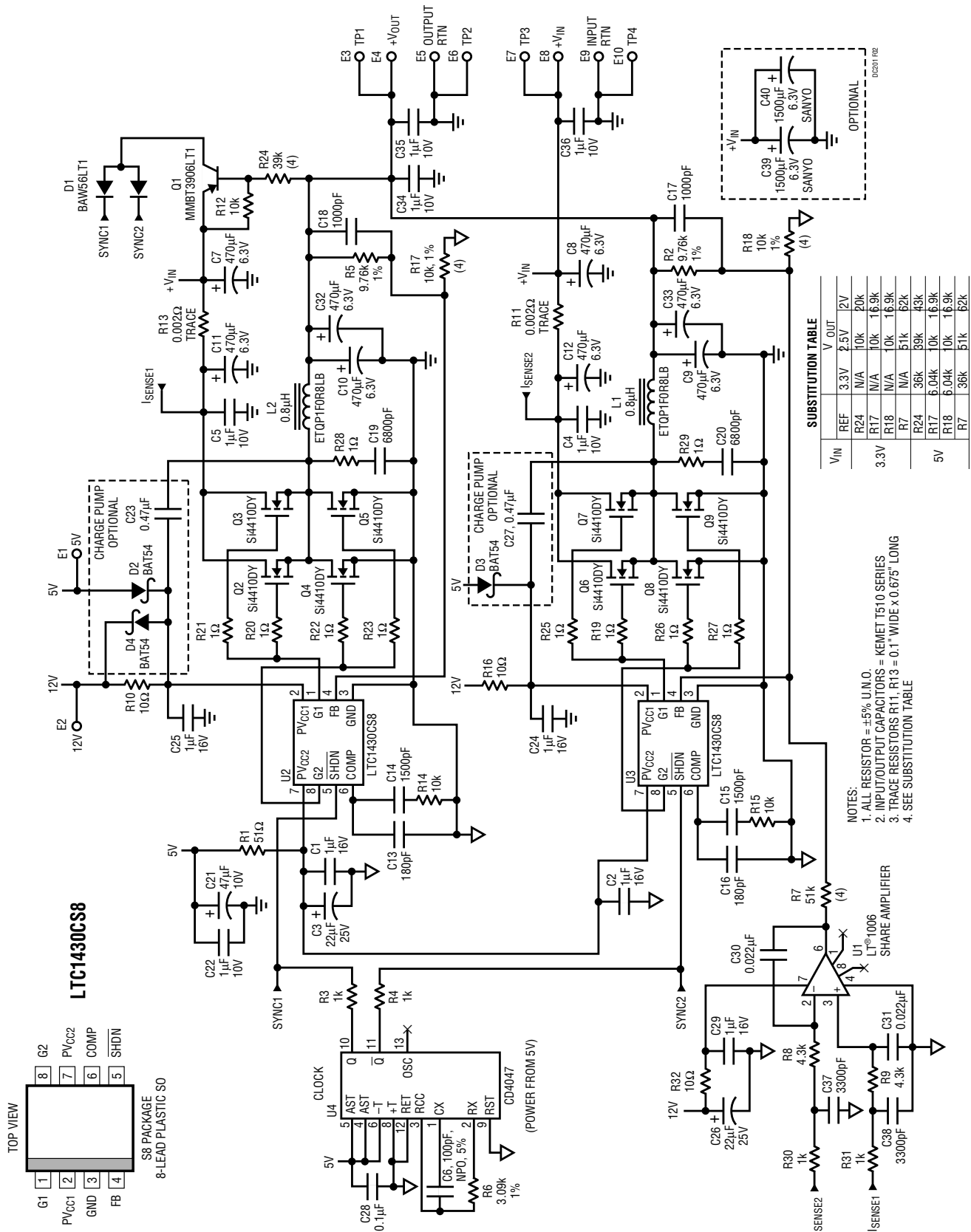
Figure 2. 2-Phase Synchronous Buck Regulator Schematic

SUBSTITUTION TABLE

V_IN	REF	2V	2.5V	3.3V	V_OUT
					2V
	R24	20k	16.9k		
	R17	10k	16.9k		
	R18	10k	16.9k		
	R7	51k	62k		
3.3V	R24	36k	43k		
	R17	10k	16.9k		
	R18	6.04k	10k		
	R7	36k	51k		

NOTES:
1. ALL RESISTOR = ±5% U.N.O.
2. INPUT/OUTPUT CAPACITORS = KEMET T510 SERIES
3. TRACE RESISTORS R11, R13 = 0.1" WIDE x 0.675" LONG
4. SEE SUBSTITUTION TABLE

LTC1430CS8

TOP VIEW

S8 PACKAGE
8-LEAD PLASTIC SO

PARTS LIST

REFERENCE DESIGNATOR	QUANTITY	PART NUMBER	DESCRIPTION	VENDOR	TELEPHONE
C1, C2, C24, C25, C29	5	0805YG105ZAT	1μF 16V Y5V Chip Capacitor	AVX	(803) 946-0362
C3, C26	2	TPSD226M025R0200	22μF 25V 20% Tantalum Capacitor	AVX	(207) 282-5111
C4, C5, C22, C34, C35, C36	6	0805ZC105KAT	1μF 10V 10% X7R Chip Capacitor	AVX	(803) 946-0362
C6	1	06035A101KAT	100pF 50V 10% NPO Chip Capacitor	AVX	(803) 946-0362
C7 to C12, C32, C33	8	T510X477K006/006	470μF 6V 10% Tantalum Capacitor	Kemet	(408) 986-0424
C13, C16	2	06035A181JAT	180pF 50V 5% NPO Chip Capacitor	AVX	(803) 946-0362
C14, C15	2	06035C152KAT	1500pF 50V 20% X7R Chip Capacitor	AVX	(803) 946-0362
C17, C18	2	06035A102FAT	1000pF 50V 1% NPO Chip Capacitor	AVX	(803) 946-0362
C19, C20	2	06035C682KAT	6800pF 50V 20% X7R Chip Capacitor	AVX	(803) 946-0362
C21	1	TAC476M010R	47μF 10V 20% Tantalum Capacitor	AVX	(207) 282-5111
C23, C27	2	0805ZC474MAT	0.47μF Chip Capacitor (Optional)	AVX	(803) 946-0362
C28	1	0603YC104KAT2A	0.1μF 16V 10% X7R Chip Capacitor	AVX	(803) 946-0362
C30, C31	2	0603YC223MAT	0.022μF 16V 20% X7R Chip Capacitor	AVX	(803) 946-0362
C37, C38	2	0603YC332MAT	3300pF 16V 20% X7R Chip Capacitor	AVX	(803) 946-0362
C39, C40	2	6MV1500GX	1500μF 6.3V Al Capacitor (Optional)	Sanyo	(619) 661-6835
D1	1	BAW56LT1	Dual Switching Diode	Motorola	(602) 244-3576
D2 to D4	3	BAT54	Schottky Diode (Optional)	Philips	(401) 767-4427
E1 to E3, E6, E7, E10	6	2501-2	Testpoint Turret	Mill-Max	(516) 922-6000
L1, L2	2	ETQP1F0R8LB	0.8μH Inductor	Panasonic	(201) 348-7522
Q1	1	MMBT3906LT1	General Purpose Transistor	Motorola	(602) 244-3576
Q2 to Q9	8	Si4410DY	N-Channel MOSFET	Siliconix	(800) 544-5565
R1	1	CR16-510J	51Ω 1/8W 5% Chip Resistor	TAD	(800) 508-1521
R2, R5	2	CR16-9761FM	9.76k 1/8W 1% Chip Resistor	TAD	(800) 508-1521
R3, R4	2	CR16-102J	1k 1/8W 5% Chip Resistor	TAD	(800) 508-1521
R6	1	CR16-3091FM	3.09k 1/8W 1% Chip Resistor	TAD	(800) 508-1521
R7	1	CR16-513J	51k 1/8W 5% Chip Resistor	TAD	(800) 508-1521
R8, R9	2	CR16-432J	4.3k 1/8W 5% Chip Resistor	TAD	(800) 508-1521
R10, R16, R32	3	CR16-100J	10Ω 1/8W 5% Chip Resistor	TAD	(800) 508-1521
R11, R13	2		Trace Resistor (These are Not Components)		
R12, R14, R15	3	CR16-103J	10k 1/8W 5% Chip Resistor	TAD	(800) 508-1521
R17, R18	2	CR16-1002FM	10k 1/8W 1% Chip Resistor	TAD	(800) 508-1521
R19 to R23, R25 to R29	10	CR16-1R0J	1Ω 1/8W 5% Chip Resistor	TAD	(800) 508-1521
U1	1	LT1006CS8	IC	LTC	(408) 432-1900
U2, U3	2	LTC1430CS8	IC	LTC	(408) 432-1900
U4	1	CD4047BCM	IC	Fairchild	(207) 775-4502

DESCRIPTION

The MOSFET power switches are SO-8, surface mount types. Parts are placed on both sides of the 4-layer PCB. Power devices are confined to the top side, whereas the control circuitry is all on the bottom of the board. As much board area as possible has been left as unetched copper area to maximize heat transfer ability. With the circuit at a room ambient temperature of 23°C in still air, the FET drain pins only rise to 90°C at 30A out. Much lower temperatures are obtained with several hundred linear feet per minute of airflow.

The Advantages of 2-Phase Design; Why It Works

By incorporating two regulators that are phased opposite to one another, both the input ripple currents and the output ripple currents tend to cancel. (See the waveforms in Figures 3 and 4 for a detailed look at this phenomenon.)This permits running much higher ripple currents in the output inductors than would be tolerable in a single-channel design. The overall output ripple current in a 2-phase design is approximately one-half of a single channel's ripple current, allowing the inductor value of each channel to be one-half of what a single-channel

system would require for equal output ripple. Since energy storage varies as the square of inductor current and directly as the inductance, each inductor stores only one-eighth the energy of a single-inductor design. Since there are two inductors, total energy storage, and therefore inductor volume, is one-fourth that of a single-phase system.

Similar analysis can be done for the input capacitor requirements. In fact, a 2-phase regulator will actually require less input capacitance than a single-channel design at one-half the load current. The photo in Figure 4 shows how the ripple currents tend to cancel one another.

Another significant advantage of the 2-phase topology is radically improved transient response. During a load transient, each of the two channels reaches its maximum (or minimum) duty cycle. The two channels' ripple currents now end up reinforcing one another rather than canceling. The result is a very high di/dt, and hence, very fast transient recoveries. Once steady-state conditions return, the ripple currents begin to cancel again, providing very low output ripple voltage.
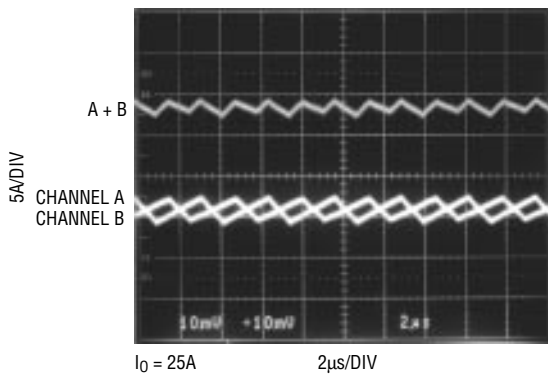

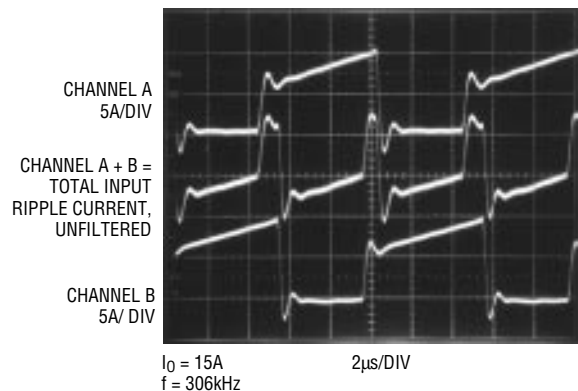**Figure 3. Ripple Cancellation—Output**

Figure 4. Ripple Cancellation—Input

QUICK START GUIDE

The circuit is very simple as far as the basic input and output connections are concerned. However, due to the very high current nature of this design, care must be exercised or unreliable results will be obtained. The first consideration is wire gauge for input and output power connections. The load current of 30A will require at least three strands of 18 AWG wire or equivalent for the power and ground connections. Use the #10 ring lugs provided and solder the power leads into the lugs prior to installing the lugs to the demo board. Be sure to tighten the #10 brass nuts securely. Under no circumstances should clip leads be used for the power connections. They will pose a fire hazard. The input current will be somewhat less than the output current and two strands of #18 AWG will be adequate if they are fairly short (less than one foot). If longer leads are used, a larger wire size should be used for both input and output connections.

The lab supply used for the input source must be capable of supplying at least 20A. If the supply has remote sense capability, it is strongly recommended that this feature be used. Solder the sense leads to the input voltage test points on the demo board (E7 and E10). If the main input power source has an unusually high output impedance or the input power cables need to be excessively long, it is recommended that capacitors C39 and C40 be installed. Any low impedance electrolytic capacitors may be used in these locations. Their purpose is to provide some additional input bypassing and ensure that the input supply's source impedance is sufficiently low. Since all switching power supplies offer a negative impedance to their input supplies, they are capable of oscillating if the input supply's source impedance is too high. This is especially true for very high current designs such as this one.

Another lab supply should be used for the 12V gate supply. A 5V supply is also required for the control circuitry. If the main input is 5V, it can also be used for the low power 5V input by making a connection between the $+V_{IN}$ terminal, E8, and E1. If a lower main supply voltage is used, provide a separate 5V input to E1. The low level 5V and 12V supplies need only be rated for about 500mA.

Be sure to verify that all lab supplies are set up for the correct output voltages prior to connecting them to the demo board. Even a momentary overvoltage on any of the inputs can prove destructive.

Connect the output leads to a suitable load. If you use an electronic load box, be sure it is capable of high current operation at very low voltage. Many older electronic loads use Darlington transistors for load elements and will only work correctly above 3V or so. Newer load box designs tend to use power MOSFETs for load elements and can operate correctly down to around 1.5V. An alternative is to use power resistors in series/parallel combination to obtain the desired load. Pay careful attention to power ratings and cooling airflow. At the power levels involved with this circuit, serious burns are possible if loads are not cooled adequately.

Attach voltmeters to the input and output test points. If you wish to directly measure input and output currents, be sure to use high current shunts rather than using the current scale on a DVM. Most DVMs are only good to 10A or 12A. 50A shunts are an excellent choice.

When all connections are complete, turn on all of the input supplies. Verify that the output voltage is correct. The board is shipped from the factory configured for a 5V input and a 2.5V output unless specifically requested otherwise. See the section on board modification if different input or output voltages are desired.

Test Setup
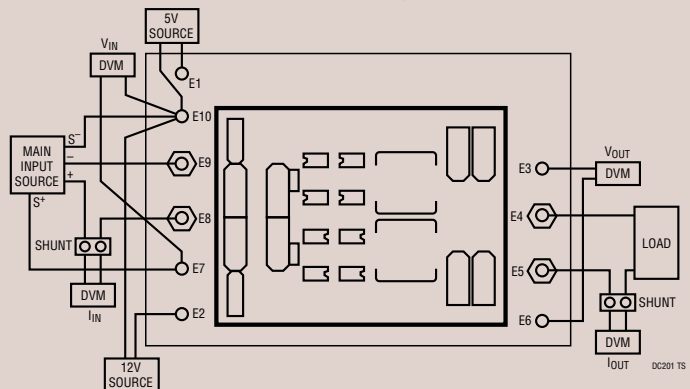
OPERATION

The basic circuit building block is a conventional synchronous buck regulator. The LTC1430 controller uses voltage mode control, and therefore does not require any load current information for pulse-by-pulse control of the power path. In a voltage mode control architecture, the output of the error amplifier (COMP pin) is compared to a ramp waveform generated by an on-chip oscillator (200kHz for the LTC1430). The higher the error voltage, the larger the high side switch on-time. The comparator output controls the complimentary MOSFET drivers, G1 and G2, which, in turn, control the power FETs. The output of this chopper is then filtered by the LC output filter. The DC output voltage is compared to an internal 1.265V reference and the resulting error voltage is amplified by the error amplifier. Frequency compensation is connected between the COMP pin and ground to stabilize the loop.

The two channels are clocked by oscillator U4, the CD4047. This chip is a low cost, CMOS multivibrator with a built-in divide-by-two flip-flop. The oscillator runs at twice the desired clock frequency. Sync signals are derived from the Q and $\overline{Q}$ outputs. The LTC1430s will free run at 200kHz. By driving their shutdown pins at 300kHz, they are synchronized to the higher clock frequency. Since the sync signals are derived from the clock's divide-by-two outputs, they are inherently 180° out of phase and at the desired clock frequency. Q1, D1 and the two resistors connected to Q1's base are used to disable the synchronization at turn-on. Failure to do this can result in the circuit failing to start (this is related to the LTC1430's start-up behavior, not the antiphase topology). As long as the input-output differential voltage is large enough to turn on Q1, the sync is disabled and both LTC1430s will free run at 200kHz. Once the output rises over approximately 1.5V, the regulators are allowed to lock to the clock.

One challenge with a voltage mode, 2-phase design is to force current sharing between channels. Unlike current mode control, which offers inherent current sharing, voltage mode control virtually ensures that one channel will try to hog a large percentage of the load current. The simplest solution to this is to sample the two currents and force one to match the other in a master/slave configuration. The upper regulator in Figure 2 determines the output voltage, while the lower regulator is forced to match the upper regulator's current. Current is sensed at the inputs to the regulators rather than at the outputs. As a result, sense-resistor power dissipation is lower by the duty factor than would result from directly sensing output currents (for equal sense voltages). It also reduces load regulation errors in the output voltage. The sense elements are a pair of trace resistors in series with the input current path. (See Linear Technology Application Note 69, Appendix "A" for details on trace resistor design.)

Op amp U1 compares the voltage across both sense resistors and adds or subtracts a small current into U3's feedback divider, forcing the two regulators' input currents to be equal. The two trace resistors are intentionally chosen to have a very low value, thereby minimizing power losses. In order to ensure reasonably accurate current sharing, the share amplifier must therefore have a very low input offset voltage. V_{OS} is typically 80μV for the LT1006S8 used in this design, ensuring very accurate current sharing.

There are three problems associated with this current-sharing approach that must be dealt with. The first is that the sense resistors should be well matched. This is accomplished by using trace resistors that are laid out symmetrically. Since they are formed of the same material and processed identically, they will inherently match very well. Note that the absolute value of these resistors is not important; only the ratiometric match is of concern. The trace-resistor matching will probably prove better than would be expected from a pair of 1% discrete resistors and they cost nothing to produce.

The second issue is related to the choice of reference point for the two current sense voltages. In order to avoid the need to use a true differential amplifier to measure input current, the circuit is configured so that the input sides of the sense resistors must be at exactly the same potential. The layout must be configured in a manner that forces this condition to be met or the current sharing accuracy will prove disappointing. With 0.002Ω sense resistors, a seemingly small layout error will produce a rather large current mismatch between channels.

The last issue is related to current sense noise. The current wave shape at the input to a buck regulator is trapezoidal.

OPERATION

Therefore, the sense amplifier must integrate the two current measurements in order to compare the average input currents. The 2-stage RC filter on the sense amplifier cleans up the signal enough for the share circuit to operate correctly. High speed is not required in the current sense loop. In normal, balanced operation, any offsets in the slave regulator are cancelled out by the share amplifier. If a sudden load change should occur, both regulators will respond immediately and in the right direction. If there are any gain differences in the two loops, a small correction must be made in the current share error voltage. This can occur over a relatively long time period with no adverse effects. As such, the share amplifier's bandwidth is only on the order of a few hundred Hertz, helping to ensure good noise immunity.

Measured Performance

Figures 1a and 1b show the measured efficiency of the board over a load current range of 1A to 30A. Figures 5 and 6 are the output voltage transient response to a 10A load step. Note that the vast majority of the step-response amplitude is due to the output capacitors' ESR. The four output capacitors are specified at 0.03Ω each for a total of approximately 0.007Ω. For a 10A step, therefore, the initial droop will be: (0.007Ω)(10A) = 70mV. The output voltage returns to its nominal value in approximately 10μs, as can be seen in Figure 6. Note that the slight amount of ringing during the recovery is due to lead inductance of the load. Output ripple voltage (Figure 7) is approximately 20mV$_{P-P}$ at full load current. The inductors used on this design have a tendency to increase in inductance at light

load. Hence, at load currents below 4A or 5A, the ripple current, and therefore the output ripple voltage, are somewhat lower than at full load. When measuring the inductor ripple current, don't confuse this with early saturation.

Board Modifications

The demo board is designed to permit operation without a 12V external supply. By installing charge pump capacitors on the board and eliminating several other components, the board can produce its own supply of approximately 10V. This will power the high-side FET gates as well as the LT1006 op amp. If 5V-only operation is desired, install C23 and C27 and remove R10, R16, C24 and C25. The demo board is shipped with diodes D2, D3 and D4 installed. They are not required if a 12V supply is available and are only provided to make converting to 5V-only operation easier for the user. When implementing a design that has a 12V supply available, these diodes should be eliminated.

It is also possible to derive the main power from 3.3V rather than 5V. In this case, connect the V$_{IN}$ terminal to a 3.3V source. A 5V supply is still needed for the control circuitry, but the power requirements are very low. The 12V supply is optional, as discussed above. Obviously, only output voltages below 3.3V will now be available. Due to the LTC1430's maximum duty factor limitations, 2.5V is the highest output voltage obtainable with a 3.3V input. The substitution table on the bottom of the schematic shows the correct resistor values to use for various combinations of input and output voltages.
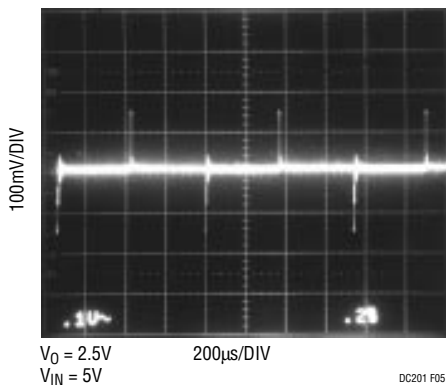

V$_O$ = 2.5V   200μs/DIV
V$_{IN}$ = 5V   DC201 F05
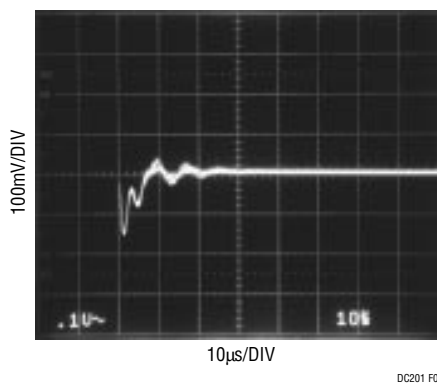
Figure 5. Transient Response 10A Load Step

10μs/DIV
DC201 F06

Figure 6. Transient Response 10A Load Step (100ns Rise Time)

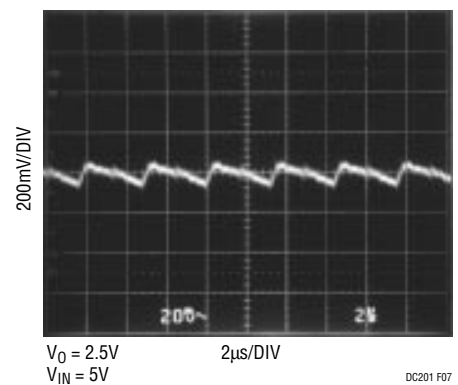V$_O$ = 2.5V   2μs/DIV
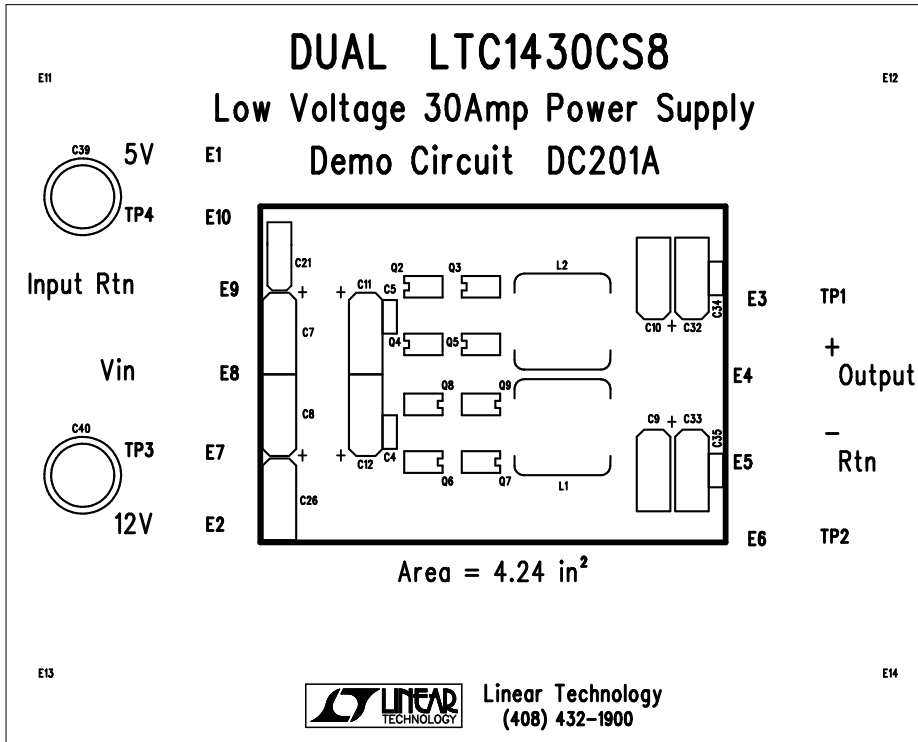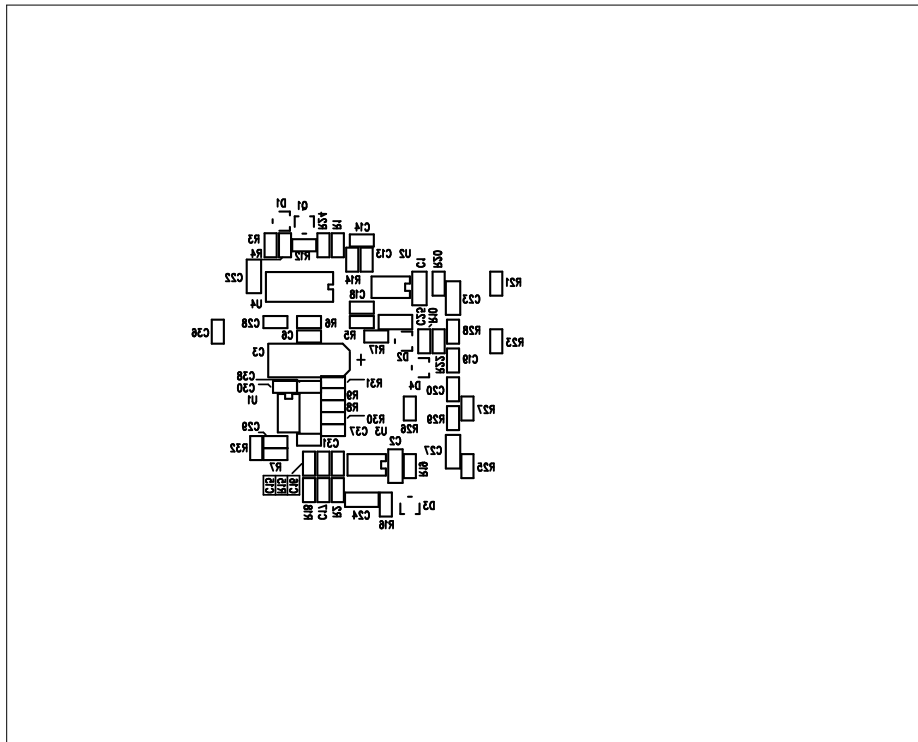V$_{IN}$ = 5V   DC201 F07

Figure 7. Output Ripple 30A Load
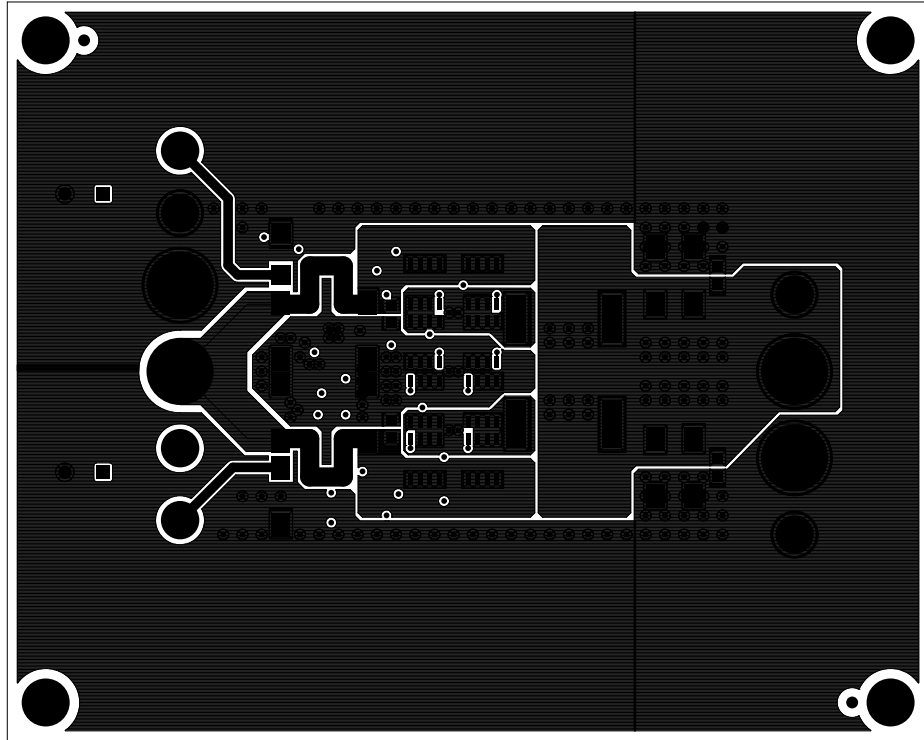
PCB LAYOUT AND FILM

Silkscreen Top

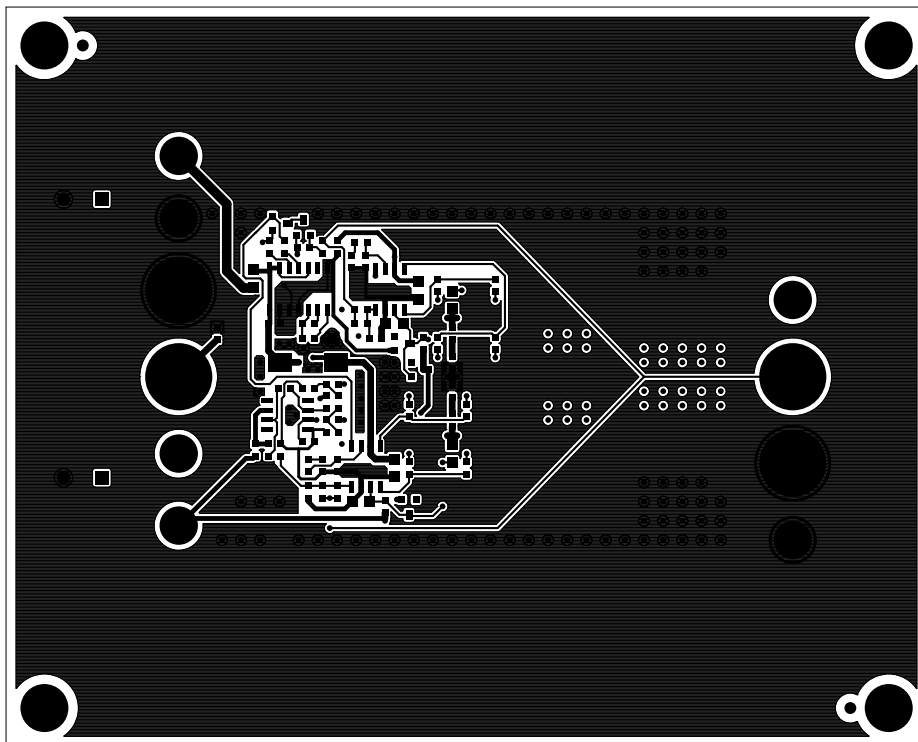DC201 SST

Silkscreen Bottom
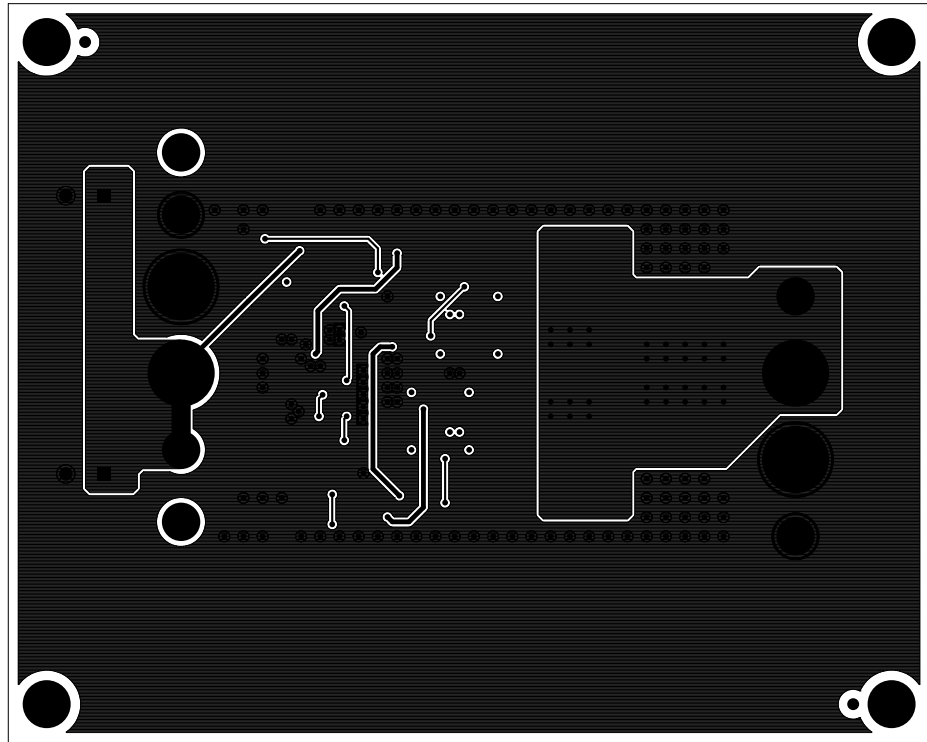
DC201 SSB

PCB LAYOUT AND FILM

DC201 CMP

Component Side

DC201 SS

Solder Side

PCB LAYOUT AND FILM

DC201 IL1

Inner Layer 1

DC201 IL2
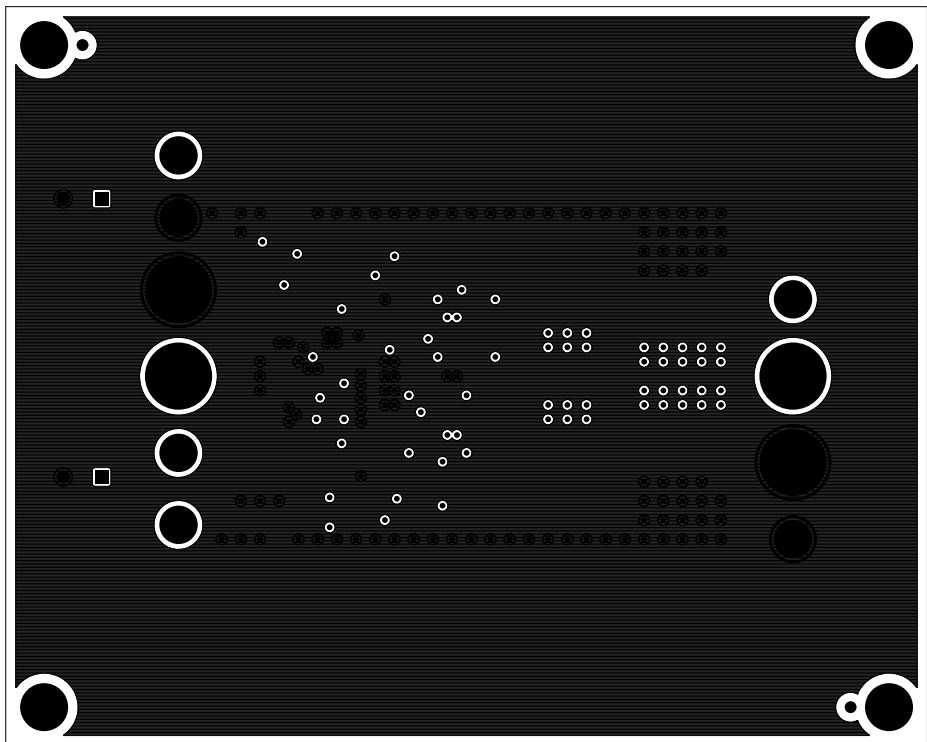
Inner Layer 2

PCB LAYOUT AND FILM
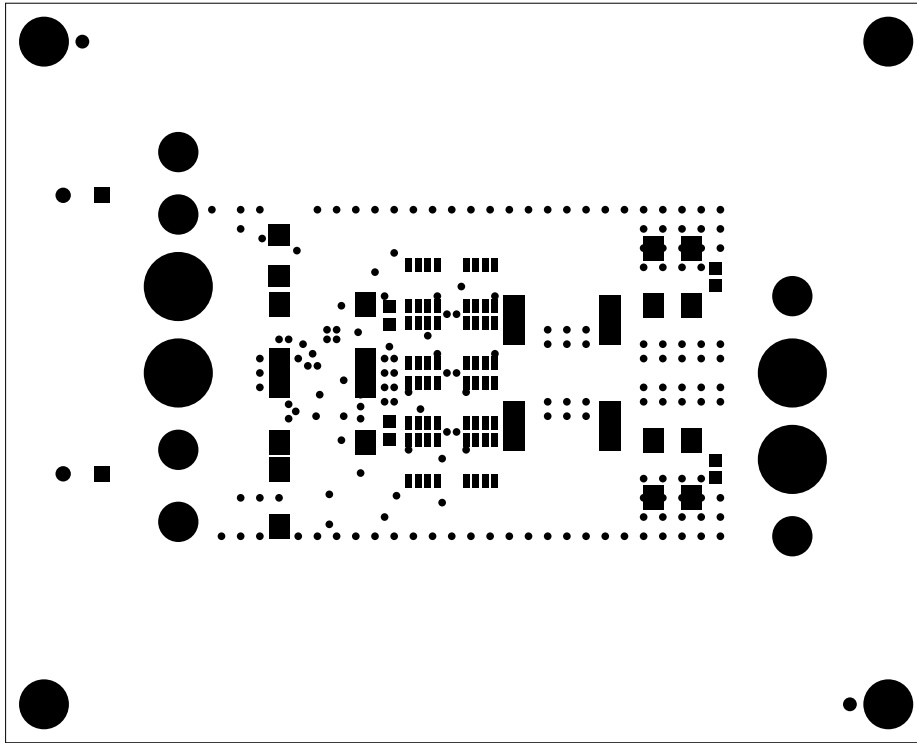
Solder Mask Top

DC201 SMT
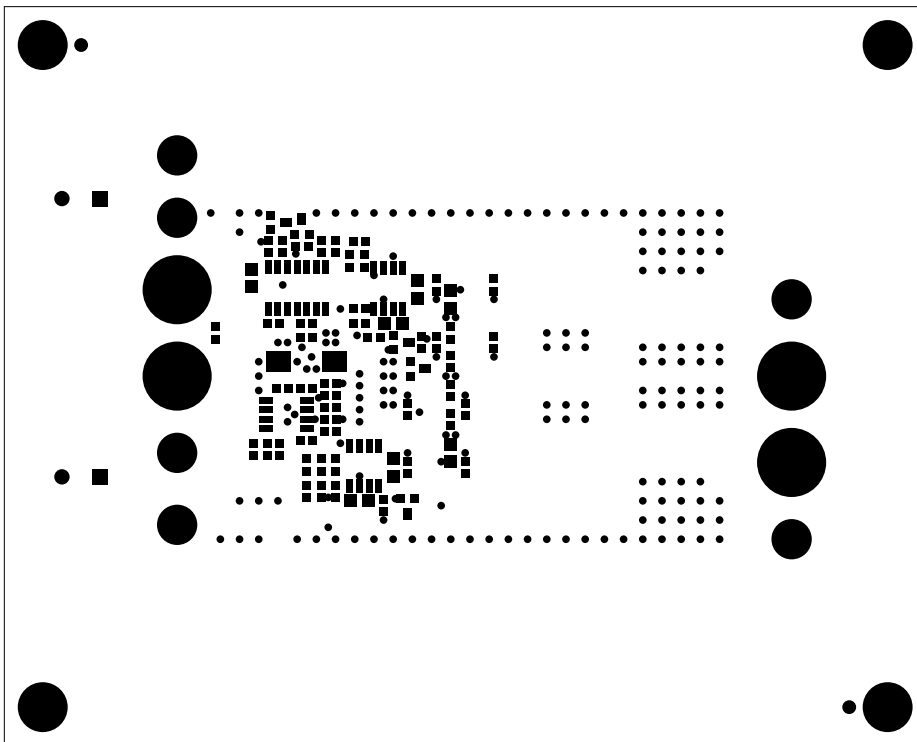
Solder Mask Bottom

DC201 SMB

11

PC FAB DRAWING

3.850

4.800

0.200

0.200

DC201 SMT
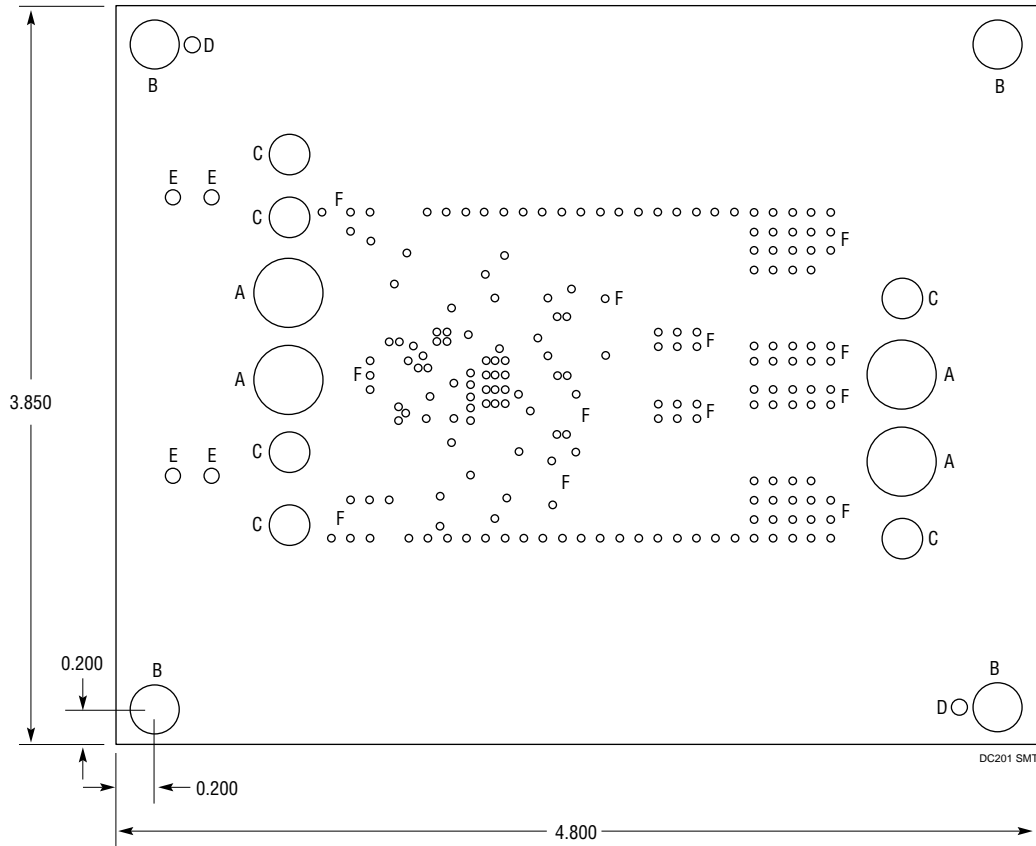
Hole Chart

SYMBOL	DIAMETER	NUMBER OF HOLES	TOLERANCE	PLATED
A	0.187	4	+0.003 −0.000	YES
B	0.130	4	+0.003 −0.000	YES
C	0.095	6	+0.003 −0.000	YES
D	0.072	2	+0.003 −0.000	NO
E	0.027	4	+0.003 −0.000	YES
F	0.015	183	+0.003 −0.000	YES
	TOTAL HOLES	203		

NOTES: UNLESS OTHERWISE SPECIFIED
1. MATERIAL: FR4 OR EQUIVALENT EPOXY, 2 OZ COPPER CLAD THICKNESS 0.062 ± 0.006 TOTAL OF FOUR LAYERS
2. FINISH: ALL PLATED HOLES 0.001 MIN, 0.0015 MAX. COPPER PLATE ELECTRODEPOSITED TIN-LEAD COMPOSITION BEFORE REFLOW, SOLDER MASK OVER BARE COPPER (SMOBC)
3. SOLDERMASK: BOTH SIDES USING SR1020 OR EQUIVALENT
4. SILKSCREEN: USING WHITE NONCONDUCTIVE EPOXY INK
5. ALL DIMENSIONS ARE IN INCHES

Layer Construction

COMP SIDE
INNER 1
INNER 2
SOLDER SIDE

DC201 LC

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