

TUV Telecom Services, Inc.

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TEST REPORT NO.

CTR2/091301/99

Date: September 20, 1999

Total Number of Pages: 32

Equipment: **LTC1544/LTC1546**

Client: **Linear Technology Corporation**

Address: **1630 McCarthy Blvd.**

Milpitas, CA 95035

USA

European Harmonised Standard: **CTR 2**

Authorised Signature:

September 20, 1999 David A. Freemore

Lead Engineer

Date

Name

Title

A handwritten signature in black ink, appearing to read "D. A. Freemore".

Signature

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7 PHOTOGRAPHS

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1 IDENTIFICATION SUMMARY

1.1 Test Laboratory

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UKAS accredited testing laboratory, no. 1845

1.2 Limits and Reservations

This test report satisfies European Standard EN 45001 (1989), ISO Guide 25, NIST Handbook 150 and NAMAS accreditation standard M10. The test results in this test report apply only to the particular System under Test (SUT) and component Implementations under Test (IUTs) declared in this test report.

1.3 Client Information

Name : Linear Technology Corporation
Street : 1630 McCarthy Blvd.
City : Milpitas, CA 95035
Country : USA
Phone : +1 (408) 954-8400
Fax : +1 (408) 434-0507

Contact Person : Dan Eddleman
Phone : +1 (408) 954-8400
Fax : +1 (408) 434-0507

1.4 Product

Supplier's name : Linear Technology Corporation
Street : 1630 McCarthy Blvd.
City : Milpitas, CA 95035
Country : USA
Phone : +1 (408) 954-8400
Fax : +1 (408) 434-0507

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1.4.1 System under Test (SUT)

SUT Hardware Configuration for testing (PC, Bus System, Clock etc.)	Linear Technology LTC1544/LTC1546 mounted on Multi-Protocol Transceiver Demo Circuit DC196A
Operating System	--
Version No.	--
Miscellaneous	--

1.4.2 Description of Product

(As provided by the client)

The LTC1544/LTC1546 chipset will support X.21, V.35, V.24, and V.36 interfaces.



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1.4.3 15-pin DTE/DCE interface ISO 4903
 (CCITT Recommendation X.21V.10/V.11 interface)

Name	LTC1544/LTC1546		
Version/Model	--		
Serial No.	--		
minimum speed (bit/s)	--		
maximum speed (bit/s)	8 Mbit/s		
Interface board	LTC1544/LTC1546 Multi-Protocol Transceiver Demo Circuit DC196A		
Chip set	V.11 Transmitter: LTC1544/LTC1546	Receiver: LTC1544/LTC1546	
Cable (name, P/N)	--		
Cable Length	--	shielded	unshielded

Supported Circuits

supported
 (X) V.11
 () V.10

- T(A) (X)
- C(A) (X)
- R(A) (X)
- I(A) (X)
- S(A) (X)
- B(A) (X)
- G (X)
- T(B) (X)
- C(B) (X)
- R(B) (X)
- I(B) (X)
- S(B) (X)
- B(B) (X)



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1.4.4 25-pin DTE/DCE interface ISO 2110
 (CCITT Recommendation V.24/V.28 (RS232) interface)

Name	LTC1544/LTC1546		
Version/Model	--		
Serial No.	--		
minimum speed (bit/s)	--		
maximum speed (bit/s)	19.2 kbit/s		
Interface board	LTC1544/LTC1546 Multi-Protocol Transceiver Demo Circuit DC196A		
Chip set	V.28 Transmitter: LTC1544/LTC1546	V.28 Receivers: LTC1544/LTC1546	
Cable (name, P/N)	--		
Cable Length	--	shielded	unshielded

Supported Circuits

<u>CCITT circuit</u>	<u>supported</u>
102	(X)
103	(X)
104	(X)
105	(X)
106	(X)
107	(X)
108	(X)
109	(X)
114	(X)
115	(X)
140	()
141	(X)
142	()

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1.4.5 34-pin DTE/DCE interface ISO 2593 (CCITT Recommendation V.35 interface)

Name	LTC1544/LTC1546		
Version/Model	--		
Serial No.	--		
minimum speed (bit/s)	--		
maximum speed (bit/s)	640 kbit/s		
Interface board	LTC1544/LTC1546 Multi-Protocol Transceiver Demo Circuit DC196A		
Chip set	V.35 Transmitter: LTC1546 V.11 Transmitter: -- V.28 Transmitter: LTC1544	V.35 Receivers: LTC1546 V.11 Receivers: -- V.28 Receivers: LTC1544	
Cable (name, P/N)	--		
Cable Length	--	shielded	unshielded

Supported Circuits

<u>CCITT circuit</u>	<u>Electrical characteristics</u>		<u>supported</u>
102a			()
102			(X)
103	V.35 (X)	V.11 ()	(X)
104	V.35 (X)	V.11 ()	(X)
105	V.28 (X)	V.10 ()	(X)
106	V.28 (X)	V.10 ()	(X)
107	V.28 (X)	V.10 ()	(X)
108	V.28 (X)	V.10 ()	(X)
109	V.28 (X)	V.10 ()	(X)
114	V.35 (X)	V.11 ()	(X)
115	V.35 (X)	V.11 ()	(X)
140	V.28 ()	V.10 ()	()
141	V.28 (X)	V.10 ()	(X)
142	V.28 ()	V.10 ()	()

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1.4.6 37-pin DTE/DCE interface ISO 4902
 (CCITT Recommendation V.36 interface)

Name	LTC1544/LTC1546		
Version/Model	--		
Serial No.	--		
minimum speed (bit/s)	--		
maximum speed (bit/s)	8 Mbit/s		
Interface board	LTC1544/LTC1546 Multi-Protocol Transceiver Demo Circuit DC196A		
Chip set	V.11 Transmitter: LTC1544/LTC1546 V.10 Transmitter: LTC1544	V.11 Receivers: LTC1544/LTC1546 V.10 Receivers: --	
Cable (name, P/N)	--		
Cable Length	--	shielded	unshielded

Supported Circuits

<u>CCITT circuit</u>	<u>Electrical characteristics</u>		<u>supported</u>
102			()
102a			()
102b			()
103	V.11 (X)	V.10 ()	(X)
104	V.11 (X)	V.10 ()	(X)
105	V.11 (X)	V.10 ()	(X)
106	V.11 (X)	V.10 ()	(X)
107	V.11 (X)	V.10 ()	(X)
108	V.11 (X)	V.10 ()	(X)
109	V.11 (X)	V.10 ()	(X)
114	V.11 (X)	V.10 ()	(X)
115	V.11 (X)	V.10 ()	(X)
140	V.10 ()		()
141	V.10 (X)		(X)
142	V.10 ()		()

1.5 Nature of Conformance Testing

The purpose of Conformance Testing is to increase the probability that different implementations can interwork. However, the complexity of OSI protocols makes exhaustive testing impractical on both technical and economic grounds. Furthermore, there is no guarantee that an IUT which has passed all the relevant tests conforms to a specification. Neither is there any guarantee that such an IUT will interwork with other real open systems. Rather, the passing of the tests gives confidence that the IUT has the stated capabilities and that its behaviour conforms consistently in representative instances of communication.

2 Test Conditions

2.1 Environmental Conditions

Temperature	: In the range of 15°C to 35°C	<input checked="" type="checkbox"/> Yes	<input type="checkbox"/> No
Relative humidity	: In the range of 5% to 75%	<input checked="" type="checkbox"/> Yes	<input type="checkbox"/> No

2.2 Power Supply Limitations

All tests were carried out within +/- 5% of the normal operating voltage of 120 V.

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3 System Report Summary

3.1 Test Report Summary

Protocol Standard: TBR 2 (01.97)
Protocol Conformance Test Report: See Section 6
Abstract Test Suite (ATS) Standard: TBR 2 (01.97)
Abstract Test Method: *Remote Single Layer Embedded (RSE)*

Real Test system:

Executable Test Suite (ETS) Identification:

	Serial-No.
Schnittstellen-Messbox VX	V0009
Digital Multimeter HP 34401A	3146A25410
Digital Multimeter HP 34401A	3146A34621
Power Supply HP6235A	2450A08776
Oscilloscope HP 54520A	3415A00472
Frequency Generator HP 33120A	US34014718
Protocol Tester HP Idacom PT 300	02-0127
Capacitance/Resistance Decade RCS-500	A0010

Conformance Status:

Static Conformance Errors : No
Dynamic Conformance Errors : No

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4 Observations

Date: September 13, 1999

Note 1: The SUT was an evaluation board, the measurements were taken at the board test points.

5 Summary of Compliance

Date: September 13, 1999

The test results in this test report apply only to the particular System under Test (SUT) and component Implementations under Test (IUTs) declared in this test report.

The SUT/IUT has not been shown by the conformance assessment to be non-conforming to the specified protocol standard. The test campaign did not reveal errors in the SUT/IUT.
Exclusion: the SUT/IUT did not provide means of connection, see note 1.



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6 Protocol Conformance Test Report


6.1 Protocol Conformance Test Report Layer 1

6.1.1 Dates

Receipt of SUT/IUT: August 31, 1999
Date of Test: September 13, 1999

6.1.2 Operator

David A. Freemore



(Signature)

6.1.3 Test System

Schnittstellen-Messbox VX
Digital Multimeter HP 34401A
Power Supply HP6235A
Oscilloscope HP 54520A
Frequency Generator HP 33120A
Protocol Tester HP Idacom PT 300
Capacitance/Resistance Decade RCS-500

6.1.4 Test Environment

Temperature : In the range of 15°C to 35°C Yes No
Relative humidity : In the range of 5% to 75% Yes No

All tests are carried out within +/- 5% of the normal operating voltage of 120V.

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6.2 Test Results

6.2.1 15-pin DTE/DCE interface ISO 4903

(CCITT Recommendation X.21/V.10/V.11 interface)

Test Case	Requirement	Result	Verdict	Comment
7.2.5.1	6.2.5.1	ISO 4903 (15-pole)	NA	
7.2.5.2	6.2.5.2	Table A.24 and A.25	NA	

CCITT V.11 Interchange Circuits

A - C terminated with 3.9 Kohm

Binary State 1

Circuit T

Test Case	Description	Limits	Result	Verdict	Comment
7.4.1.1	A - B	$V_o \leq 12.0V$	-4.87 V	pass	
	A - C	$V_{oa} \leq 12.0V$	-4.93 V	pass	
	B - C	$V_{ob} \leq 12.0V$	-0.06 V	pass	

Circuit C

Test Case	Description	Limits	Result	Verdict	Comment
7.4.1.1	A - B	$V_o \leq 12.0V$	-4.87 V	pass	
	A - C	$V_{oa} \leq 12.0V$	-4.93 V	pass	
	B - C	$V_{ob} \leq 12.0V$	-0.06 V	pass	

Circuit T

Binary State 2

Test Case	Description	Limits	Result	Verdict	Comment
7.4.1.1	A - B	$V_o \leq 12.0V$	4.87 V	pass	
	A - C	$V_{oa} \leq 12.0V$	-0.06 V	pass	
	B - C	$V_{ob} \leq 12.0V$	-4.93 V	pass	

Circuit C

Test Case	Description	Limits	Result	Verdict	Comment
7.4.1.1	A - B	$V_o \leq 12.0V$	4.87 V	pass	
	A - C	$V_{oa} \leq 12.0V$	-0.06 V	pass	
	B - C	$V_{ob} \leq 12.0V$	-4.93 V	pass	

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A - B terminated with 2 x 50 Ohm

Binary State 1

Circuit T

Test Case	Description	Limits	Result	Verdict	Comment
7.4.1.2	A - B	$V_t \geq 2.0V$	-2.75 V	pass	
	R1/R2 - C	$V_{os} \leq 3.0V$	1.29 V	pass	

Circuit C

Test Case	Description	Limits	Result	Verdict	Comment
7.4.1.2	A - B	$V_t \geq 2.0V$	-2.93 V	pass	
	R1/R2 - C	$V_{os} \leq 3.0V$	1.32 V	pass	

Binary State 2

Circuit T

Test Case	Description	Limits	Result	Verdict	Comment
7.4.1.2	A - B	$V_t \geq 2.0V$	2.81 V	pass	
	R1/R2 - C	$V_{os} \leq 3.0V$	1.22 V	pass	

Circuit C

Test Case	Description	Limits	Result	Verdict	Comment
7.4.1.2	A - B	$V_t \geq 2.0V$	3.00 V	pass	
	R1/R2 - C	$V_{os} \leq 3.0V$	1.22V	pass	



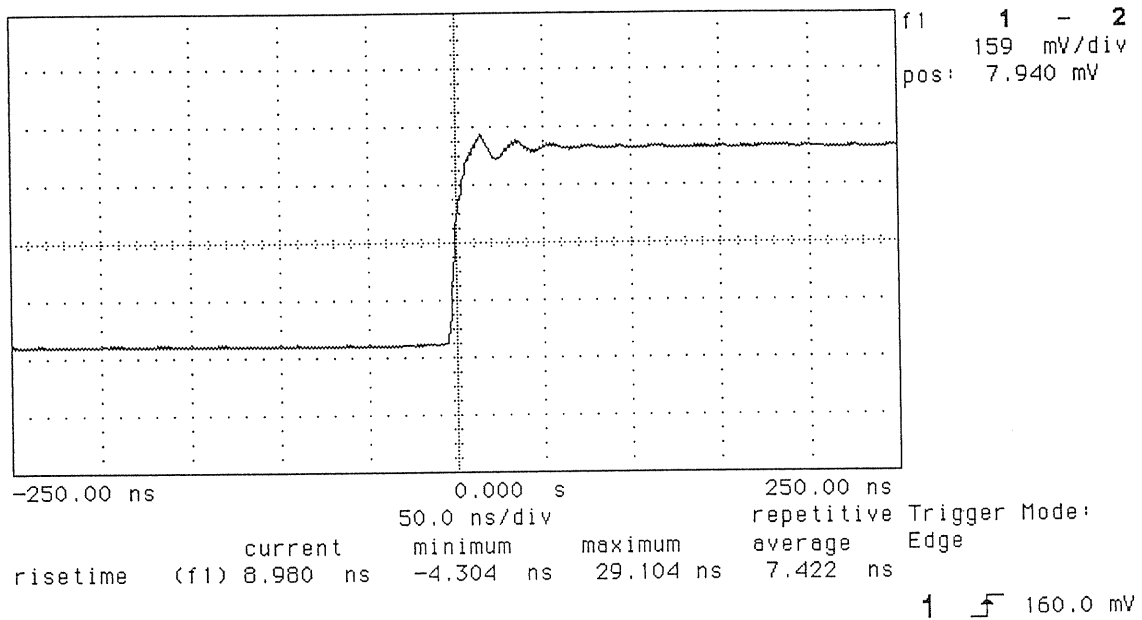
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Generator Output Risetime

Circuit T

Test Case	Description	Limits	Result	Verdict	Comment
7.4.1.3	A - B	$t \leq 0.3 \text{ tb}$	7.4 ns pos 8.2 ns neg	pass	

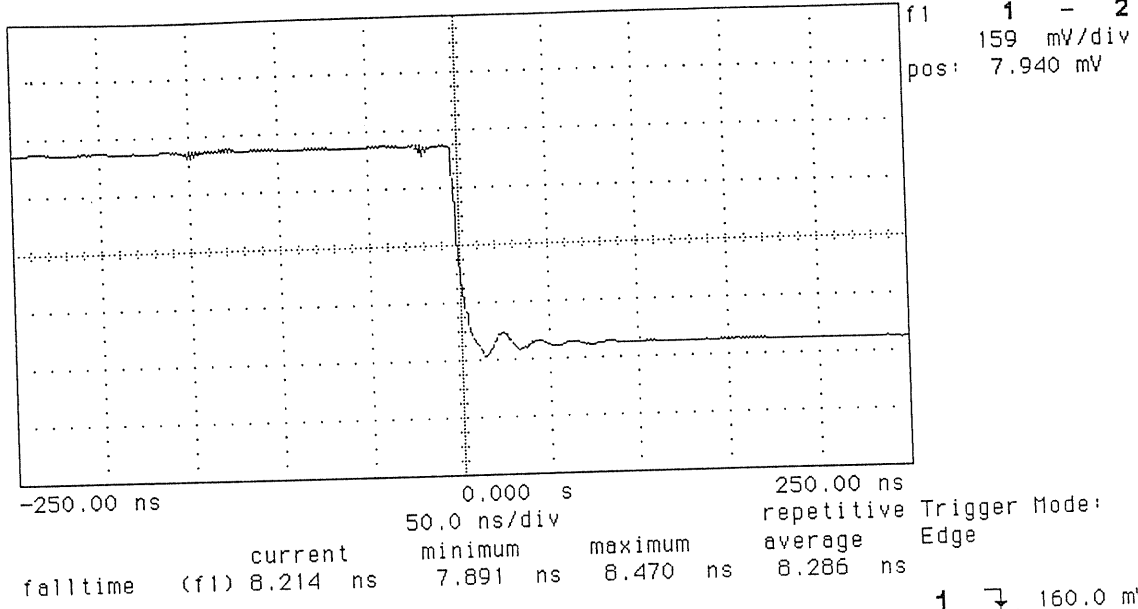
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6.2.2 25-pin DTE/DCE interface ISO 2110

(CCITT Recommendation V.24/V.28 (RS232) interface)

Test Case	Requirement	Result	Verdict	Comment
7.2.1.1	6.2.1.1	ISO 2110 (25-pole)	NA	
7.2.1.2	6.2.1.2	Table A.1 and A.2	NA	

CCITT V.28 Interchange Circuits

A - C unterminated

Test Case	Circuit	Limits	Result	Verdict	Comment
7.5.1.1	103	$V \leq 25.0V$	9.35 V	pass	
	105	$V \leq 25.0V$	9.35 V	pass	
	108	$V \leq 25.0V$	9.35 V	pass	
	141	$V \leq 25.0V$	8.99 V	pass	

Binary State 1

A - C terminated with 3 KOhm

Test Case	Circuit	Limits	Result	Verdict	Comment
7.5.1.2	103	$V \geq 3.0V$	8.46 V	pass	
	105	$V \geq 3.0V$	8.53 V	pass	
	108	$V \geq 3.0V$	8.53 V	pass	
	141	$V \geq 3.0V$	8.28 V	pass	

Binary State 2

Test Case	Circuit	Limits	Result	Verdict	Comment
7.5.1.2	103	$V \geq 3.0V$	-8.66 V	pass	
	105	$V \geq 3.0V$	-8.89 V	pass	
	108	$V \geq 3.0V$	-8.89 V	pass	
	141	$V \geq 3.0V$	-8.75 V	pass	

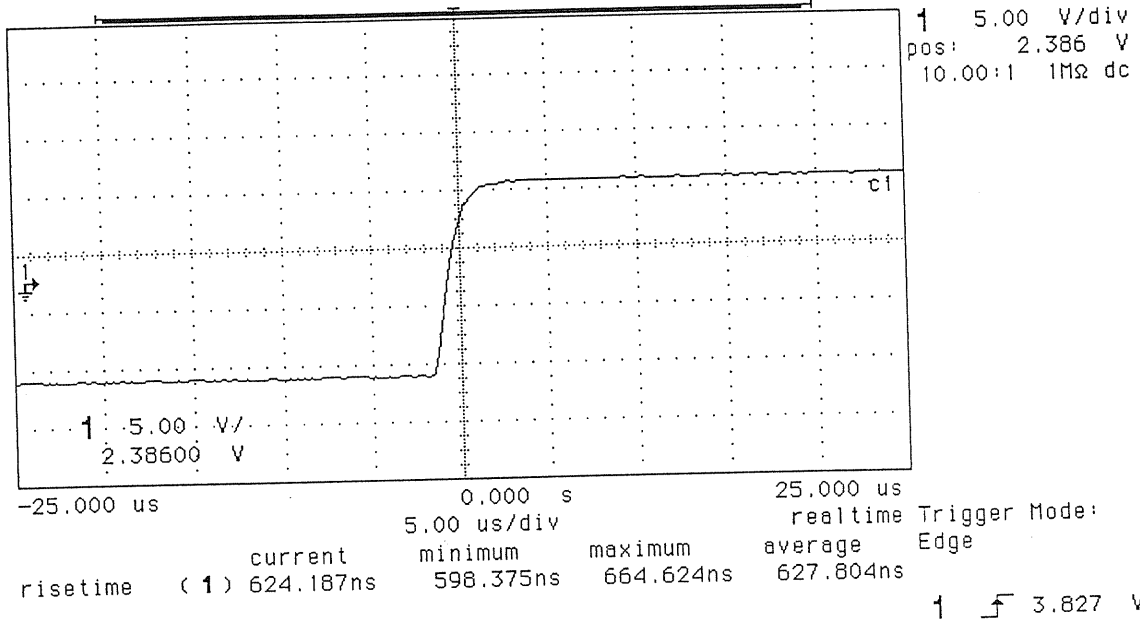


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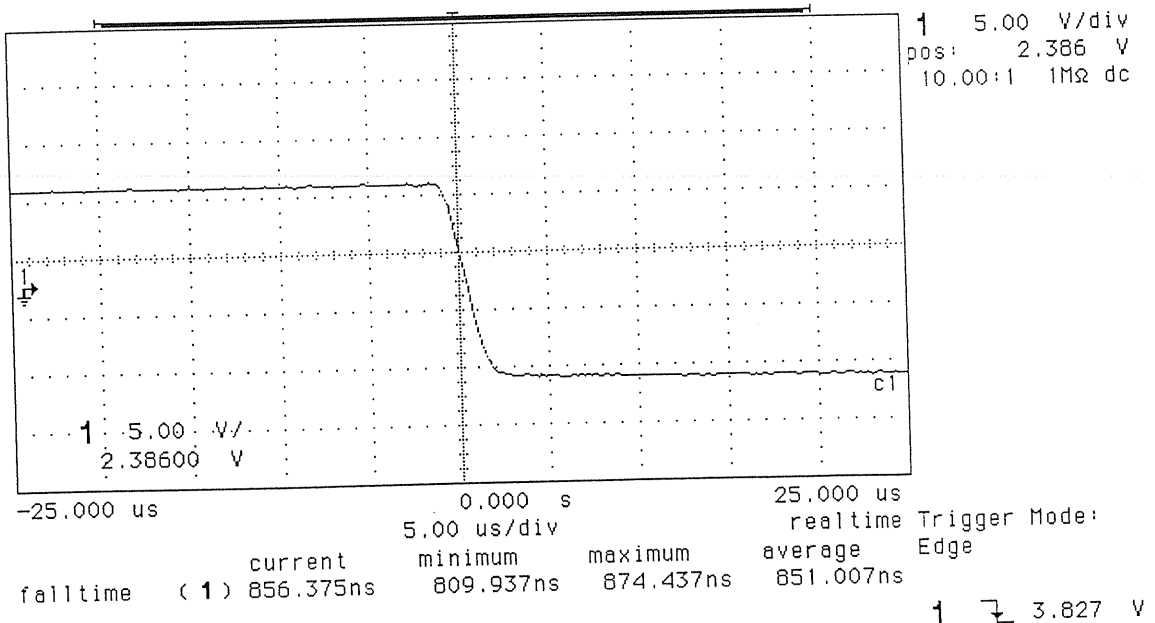
Generator Output Risetime

Test Case	Circuit	Limits	Result	Verdict	Comment
7.5.1.3	103	$t \leq 0.03 \text{ tb}$	627 ns pos	pass	
		$t \leq 0.03 \text{ tb}$	851 ns neg	pass	

hp stopped



hp stopped



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Receiver Shunt Capacitance

Test Case	Circuit	Limits	Result $t_3 = 3.5 \mu s$	Verdict	Comment
7.5.2.1	106	t_1 and $t_2 \leq t_3$	$t_1 = 49$ ns $t_2 = 46$ ns	pass	
	107	t_1 and $t_2 \leq t_3$	$t_1 = 47$ ns $t_2 = 46$ ns	pass	
	109	t_1 and $t_2 \leq t_3$	$t_1 = 75$ ns $t_2 = 52$ ns	pass	
	104	t_1 and $t_2 \leq t_3$	$t_1 = 75$ ns $t_2 = 65$ ns	pass	
	114	t_1 and $t_2 \leq t_3$	$t_1 = 100$ ns $t_2 = 67$ ns	pass	
	115	t_1 and $t_2 \leq t_3$	$t_1 = 72$ ns $t_2 = 64$ ns	pass	

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6.2.3 34-pin DTE/DCE interface ISO 2593 (CCITT Recommendation V.35 interface)

Test Case	Requirement	Result	Verdict	Comment
7.2.4.1	6.2.4.1	ISO 2593 (34-pole)	NA	
7.2.4.2	6.2.4.2	Table A.17 and A.18	NA	

CCITT V.35 Interchange Circuits

A - C terminated with 3.9 KOhm

Circuit 103

Binary State 1

Test Case	Description	Limits	Result	Verdict	Comment
7.6.1.1	A - B	$V_o \leq 1.2 \text{ V}$	0.98 V	pass	
	A - C	$V_{oa} \leq 1.2 \text{ V}$	0.54 V	pass	
	B - C	$V_{ob} \leq 1.2 \text{ V}$	-0.44 V	pass	

Binary State 2

Test Case	Description	Limits	Result	Verdict	Comment
7.6.1.1	A - B	$V_o \leq 1.2 \text{ V}$	-0.98 V	pass	
	A - C	$V_{oa} \leq 1.2 \text{ V}$	-0.51 V	pass	
	B - C	$V_{ob} \leq 1.2 \text{ V}$	0.47 V	pass	

A - C terminated with 2 x 50 Ohm

Circuit 103

Binary State 1

Test Case	Description	Limits	Result	Verdict	Comment
7.6.1.2	A - B	$0.44\text{V} \leq V_t \leq 0.66\text{V}$	0.52 V	pass	
	R1/R2 - C	$V_{os} \leq 0.6 \text{ V}$	0.008 V	pass	

Binary State 2

Test Case	Description	Limits	Result	Verdict	Comment
7.6.1.2	A - B	$0.44\text{V} \leq V_t \leq 0.66\text{V}$	-0.52 V	pass	
	R1/R2 - C	$V_{os} \leq 0.6 \text{ V}$	-0.002 V	pass	

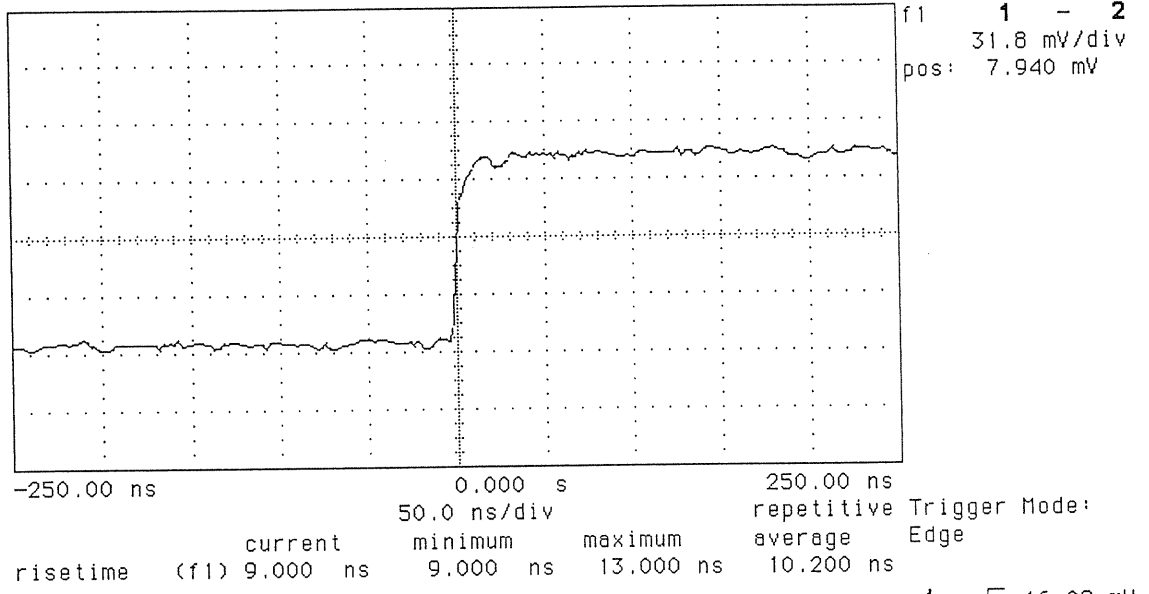


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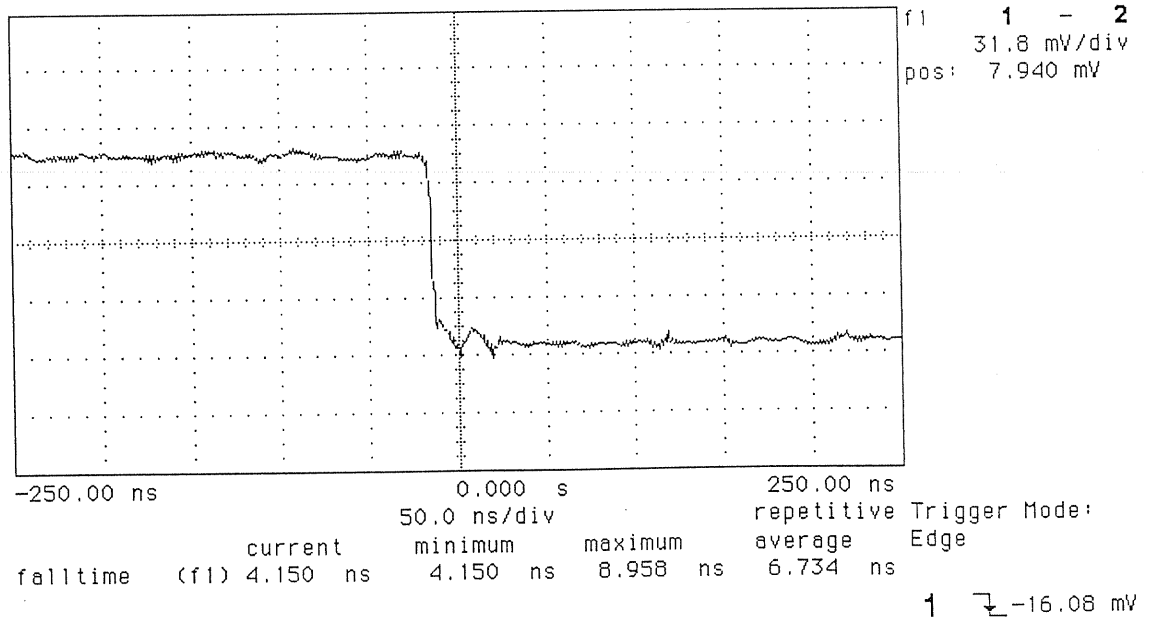
Generator Output Risetime

Test Case	Circuit	Limits	Result	Verdict	Comment
7.6.1.3	103	$t \leq 0.1$ tb	10.2 ns pos 6.7 ns neg	pass	

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CCITT V.28 Interchange Circuits

A - C unterminated

Test Case	Circuit	Limits	Result	Verdict	Comment
7.5.1.1	105	$V \leq 25.0V$	8.6 V	pass	
	108	$V \leq 25.0V$	8.6 V	pass	
	141	$V \leq 25.0V$	-7.6 V	pass	

Binary State 1

A - C terminated with 3 KOhm

Test Case	Circuit	Limits	Result	Verdict	Comment
7.5.1.2	105	$V \geq 3.0V$	7.8 V	pass	
	108	$V \geq 3.0V$	7.8 V	pass	
	141	$V \geq 3.0V$	-7.1 V	pass	

Binary State 2

Test Case	Circuit	Limits	Result	Verdict	Comment
7.5.1.2	105	$V \geq 3.0V$	-7.3 V	pass	
	108	$V \geq 3.0V$	-7.3 V	pass	
	141	$V \geq 3.0V$	7.5 V	pass	

Receiver Shunt Capacitance

Test Case	Circuit	Limits	Result $t_3 = 3.5 \mu s$	Verdict	Comment
7.5.2.1	106	$t_1 \text{ and } t_2 \leq t_3$	$t_1 = 85 \text{ ns}$ $t_2 = 80 \text{ ns}$	pass	
	107	$t_1 \text{ and } t_2 \leq t_3$	$t_1 = 47 \text{ ns}$ $t_2 = 45 \text{ ns}$	pass	
	109	$t_1 \text{ and } t_2 \leq t_3$	$t_1 = 90 \text{ ns}$ $t_2 = 48 \text{ ns}$	pass	

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6.2.4 37-pin DTE/DCE interface ISO 4902

(CCITT Recommendation V.36 interface)

Test Case	Requirement	Result	Verdict	Comment
7.2.3.1	6.2.3.1	ISO 4902 (37-pole)	NA	
7.2.3.2	6.2.3.2	Table A.13 and A.14	NA	

CCITT V.10 Interchange Circuits

Binary State 1

A - C terminated with 3.9 KOhm

Test Case	Circuit	Limits	Result	Verdict	Comment
7.3.1.1	141	$V \leq 12.0V$	-5.56 V	pass	

A - C terminated with 450 Ohm

Test Case	Circuit	Limits	Result	Verdict	Comment
7.3.1.2	141	$V_o \geq 2.0V$	-5.18 V	pass	

Binary State 2

A - C terminated with 3.9 KOhm

Test Case	Circuit	Limits	Result	Verdict	Comment
7.3.1.1	141	$V \leq 12.0V$	4.87 V	pass	

A - C terminated with 450 Ohm

Test Case	Circuit	Limits	Result	Verdict	Comment
7.3.1.2	141	$V_o \geq 2.0V$	4.50 V	pass	

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CCITT V.11 Interchange Circuits

A - C terminated with 3.9 Kohm
Binary State 1

Circuit 103

Test Case	Description	Limits	Result	Verdict	Comment
7.4.1.1	A - B	$V_o \leq 12.0V$	-4.82 V	pass	
	A - C	$V_{oa} \leq 12.0V$	-4.93 V	pass	
	B - C	$V_{ob} \leq 12.0V$	-0.06 V	pass	

Circuit 105

Test Case	Description	Limits	Result	Verdict	Comment
7.4.1.1	A - B	$V_o \leq 12.0V$	-4.87 V	pass	
	A - C	$V_{oa} \leq 12.0V$	-4.93 V	pass	
	B - C	$V_{ob} \leq 12.0V$	-0.06 V	pass	

Circuit 108

Test Case	Description	Limits	Result	Verdict	Comment
7.4.1.1	A - B	$V_o \leq 12.0V$	-4.87 V	pass	
	A - C	$V_{oa} \leq 12.0V$	-4.93 V	pass	
	B - C	$V_{ob} \leq 12.0V$	-0.06 V	pass	

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Binary State 2

Circuit 103

Test Case	Description	Limits	Result	Verdict	Comment
7.4.1.1	A - B	$V_o \leq 12.0V$	4.87 V	pass	
	A - C	$V_{oa} \leq 12.0V$	-0.06 V	pass	
	B - C	$V_{ob} \leq 12.0V$	-4.93 V	pass	

Circuit 105

Test Case	Description	Limits	Result	Verdict	Comment
7.4.1.1	A - B	$V_o \leq 12.0V$	4.87 V	pass	
	A - C	$V_{oa} \leq 12.0V$	-0.06 V	pass	
	B - C	$V_{ob} \leq 12.0V$	-4.93 V	pass	

Circuit 108

Test Case	Description	Limits	Result	Verdict	Comment
7.4.1.1	A - B	$V_o \leq 12.0V$	4.87 V	pass	
	A - C	$V_{oa} \leq 12.0V$	-0.06 V	pass	
	B - C	$V_{ob} \leq 12.0V$	-4.93 V	pass	



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A - B terminated with 2 x 50 Ohm

Binary State 1

Circuit 103

Test Case	Description	Limits	Result	Verdict	Comment
7.4.1.2	A - B	$V_t \geq 2.0V$	-2.81 V	pass	
	R1/R2 - C	$V_{os} \leq 3.0V$	1.32 V	pass	

Circuit 105

Test Case	Description	Limits	Result	Verdict	Comment
7.4.1.2	A - B	$V_t \geq 2.0V$	-3.00 V	pass	
	R1/R2 - C	$V_{os} \leq 3.0V$	1.38 V	pass	

Circuit 108

Test Case	Description	Limits	Result	Verdict	Comment
7.4.1.2	A - B	$V_t \geq 2.0V$	-3.00 V	pass	
	R1/R2 - C	$V_{os} \leq 3.0V$	1.35 V	pass	

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**Binary State 2**

Circuit 103

Test Case	Description	Limits	Result	Verdict	Comment
7.4.1.2	A - B	$V_t \geq 2.0V$	2.81 V	pass	
	R1/R2 - C	$V_{os} \leq 3.0V$	-0.97 V	pass	

Circuit 105

Test Case	Description	Limits	Result	Verdict	Comment
7.4.1.2	A - B	$V_t \geq 2.0V$	3.00 V	pass	
	R1/R2 - C	$V_{os} \leq 3.0V$	-1.28 V	pass	

Circuit 108

Test Case	Description	Limits	Result	Verdict	Comment
7.4.1.2	A - B	$V_t \geq 2.0V$	3.00 V	pass	
	R1/R2 - C	$V_{os} \leq 3.0V$	-1.25 V	pass	



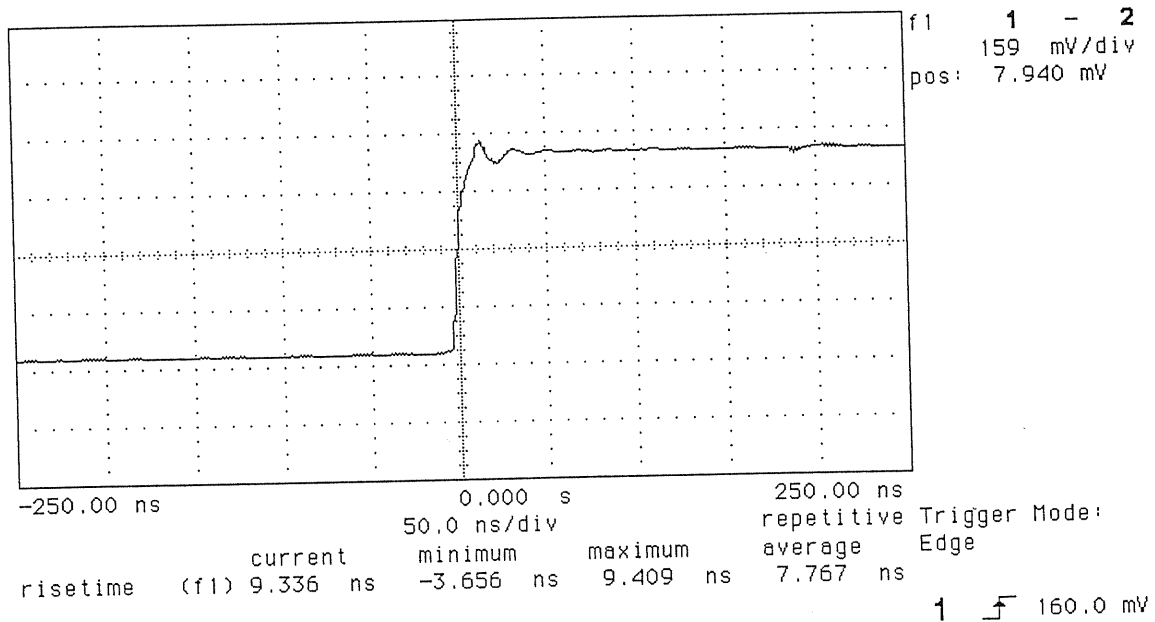
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Generator Output Risetime

Circuit 103

Test Case	Description	Limits	Result	Verdict	Comment
7.4.1.3	A - B	$t \leq 0.3 \text{ tb}$	7.7 ns pos 7.9 ns neg	pass	

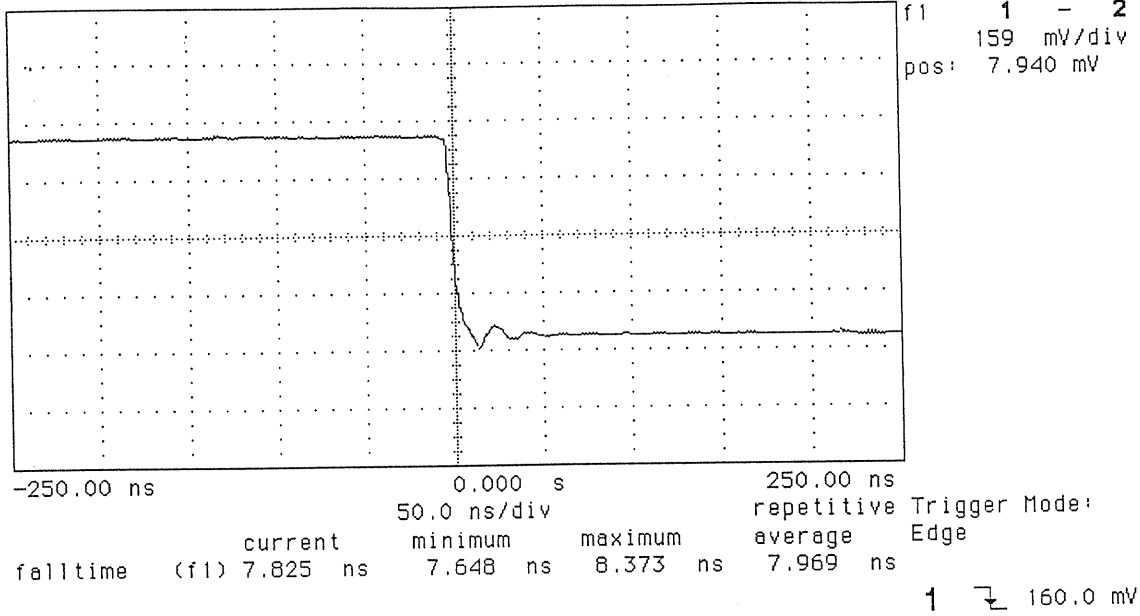
hp stopped



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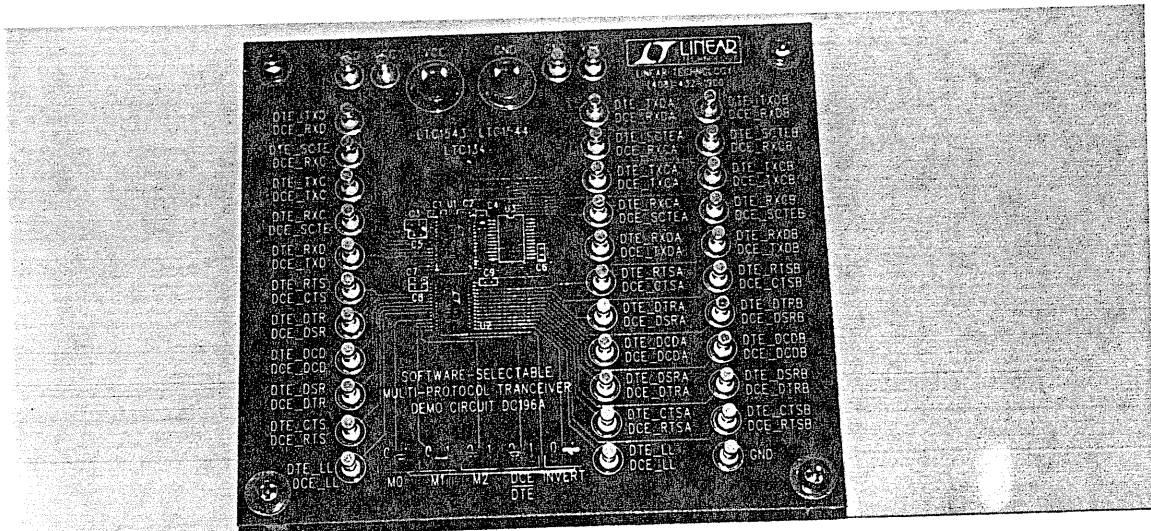


hp stopped

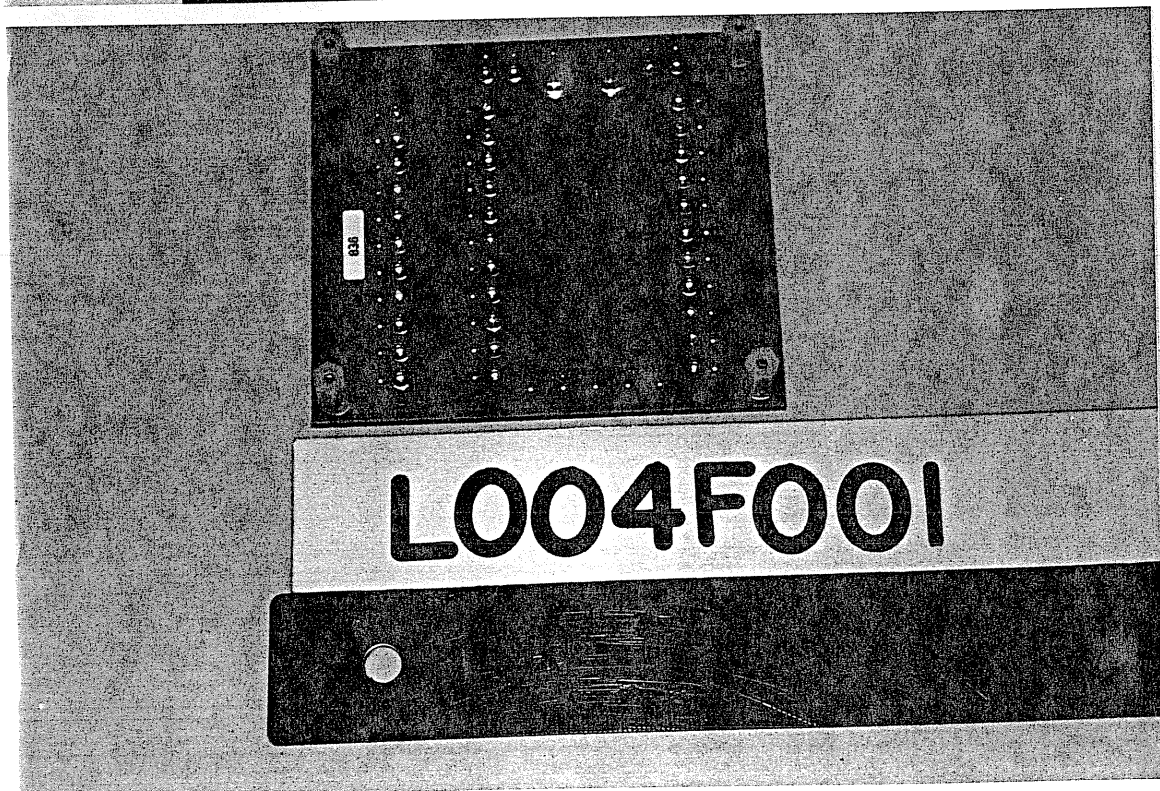


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7 Photographs



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