

REVISIONS

REV	APPR	DATE

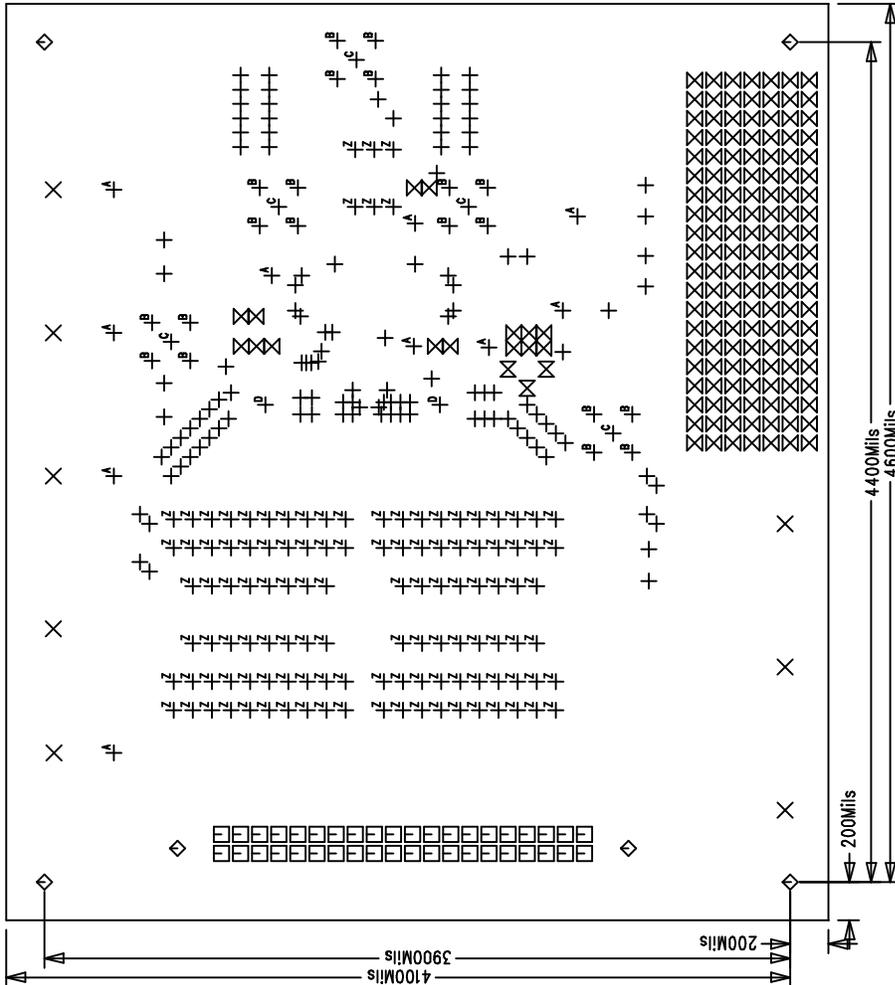
NOTES: Unless Otherwise Specified

1. FINISHED MATERIAL: FR-4, 4-layers, 62-mil thickness.
2. All via holes (8-mil hole size) should be plated-solid.
3. Plate thru holes 1.4-mils min. wall thickness.
All hole sizes given as after plating, +/- 3-mils.
4. SILKSCREEN: White non-conductive epoxy ink, top only.
5. PROCESS: Solder Mask Over Bare Copper (SMOBC).
6. SOLDER MASK: Glossy green LPI, both sides, smd features.
7. DO NOT MODIFY silkscreen, such as adding company logo.
8. CONTROLLED IMPEDANCE on outer dielectric layers.
Target impedance: 50-Ohms, 8-mil trace, 1GHz.
Expected dielectric thickness approx. 5-mils (er=4.6).
9. Layer order and copper thickness:



SIZE	QTY	SYM	PLTD
8	120	+	PLTD
203	8	X	PLTD
37	40	□	PLTD
125	6	◇	PLTD
35	155	⊗	PLTD
25	3	⊗	PLTD
40	10	A	PLTD
67	20	B	PLTD
62	5	C	PLTD
125	2	D	NPLTD
52	118	Z	PLTD

Linear Technology Corp.
LTC1668
Demo Board 245A
Component Side



1630 McCarthy Blvd.
Milpitas, CA 95035
PH: (408)432-1900

TITLE: LTC1668 High-Speed Current Output
DAC Evaluation Board

SIZE: NONE
REV: A
Demo Board 245A

DES-0281
SHT 1 of 1

APPROVALS

	INIT	DATE
DRAWN		
CHECK		
DESIGN	Rmb	
ENGR	AG	

SCALE = NONE