DESCRIPTION

Demonstration circuit 295B is a VRM for Geyserville CPUs. It has two 550kHz synchronous buck converters to power the CPU core and I/O and an LDO for clock. It features the LTC1705. The switchers use MOSFET $R_{DS\ (ON)}$ for current limit. This improves efficiency and eliminates cost and size of discrete sense resistors. The switchers run out of phase to minimize input capacitance requirements. The core output is programmed by a 5-bit VID code compatible with many Intel P3 type processors. The demo board can be evaluated using the VRM interface board DC296A.

Design files for this circuit board are available. Call the LTC factory.

Table 1. Performance Summary

PARAMETER	CONDITION	VALUE
Minimum Input Voltage		4.75V
Maximum Input Voltage		5.5V
V_{CORE}	V_{IN} = 4.75V to 5.5V, I_{CORE} = 0A to 15A	0.9V-2.0V Mobile VID ±1.5%
$V_{I/O}$	V_{IN} = 4.75V to 5.57V, $I_{I/O}$ = 0A to 2A	1.5V ±2%
V_{CLK}	V_{IN} = 4.75V to 5.57V, Iclk=0-150mA	2.5V ±2%
Typical V_{CORE} Output Ripple	V_{IN} = 5V, I_{CORE} = 15A	$10mV_{P-P}$
Typical $V_{I/O}$ Output Ripple	V_{IN} = 3.3V, I_{OUT2} = 2A	$12mV_{P-P}$
Nominal Switching Frequency		550kHz

QUICK START PROCEDURE

Demonstration circuit 295B is easy to set up to evaluate the performance of the LTC1705. It is evaluated using DC296A VRM interface board. Refer to Figure 1 for correct board orientation and proper measurement equipment setup, and follow the procedure below:

NOTE: When measuring the input or output voltage ripple, care must be taken to avoid a long ground lead on the oscilloscope probe. Measure the input or output voltage ripple by touching the probe tip directly across the Vin or Vout and GND terminals.

1. Set VID jumpers (JP1) on DC296A to the following positions corresponding to 1.5V Vcore.

   VID4, VID3, VID2, VID1, VID0=0,1,0,1,0.

   (0=shorted jumper, 1=open)

2. With power off, connect the input power supply to Vin and GND making sure voltage is not set greater than 6V. Set all loads to zero.
3. Turn on the power at the input. Set Vin=5V
4. Check for the proper output voltages. Vcore = 1.478V to 1.522V, Vclk = 2.450V to 2.550V and VIO=1.470V to 1.530V.

   If there is no output, temporarily disconnect the load to make sure that the load is not set too high.
5. Once the proper output voltages are established, adjust the loads within the operating range and observe the output voltage regulation, ripple voltage, efficiency, and other parameters.

6. Note: For precise load regulation and load transient response measurements, measure Vcore at C11 on DC296.

7. For continuous full load testing of Vcore at 15A (more than 5 minutes) some airflow, about 200 LFM is recommended. Avoid applying more than 12A at Vcore continuously without airflow.

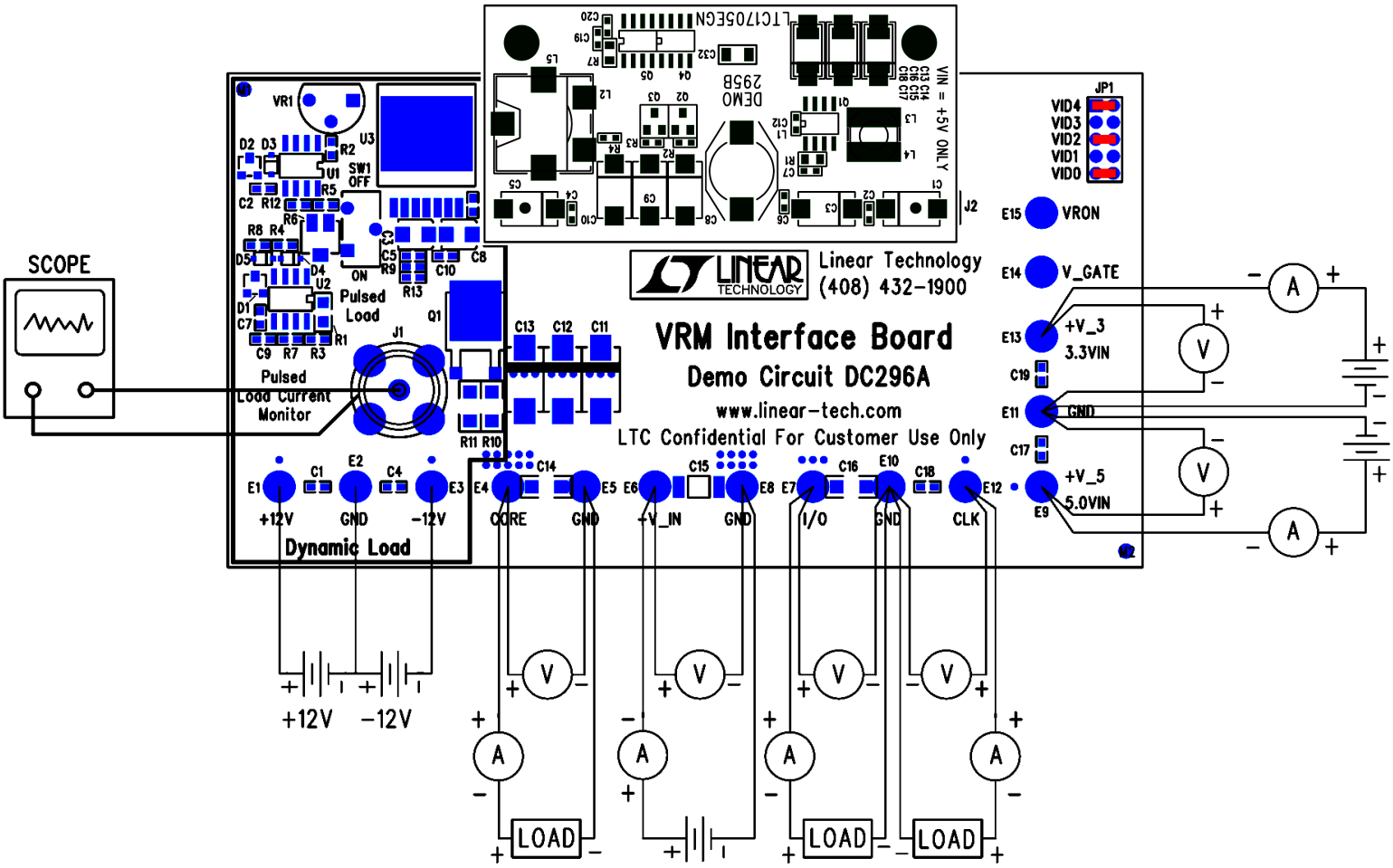


Figure 1. DC296A Hookup Diagram

Table 2. VID codes and corresponding core outputs

VID4	VID3	VID2	VID1	VID0	VCORE (VOLTS)
0	0	0	0	0	2.00
0	0	0	0	1	1.95
0	0	0	1	0	1.90
0	0	0	1	1	1.85
0	0	1	0	0	1.80
0	0	1	0	1	1.75
0	0	1	1	0	1.70
0	0	1	1	1	1.65
0	1	0	0	0	1.60
0	1	0	0	1	1.55
0	1	0	1	0	1.50
0	1	0	1	1	1.45
0	1	1	0	0	1.40
0	1	1	0	1	1.35
0	1	1	1	0	1.30
0	1	1	1	1	1.25
1	0	0	0	0	1.275
1	0	0	0	1	1.250
1	0	0	1	0	1.225
1	0	0	1	1	1.200
1	0	1	0	0	1.175
1	0	1	0	1	1.150
1	0	1	1	0	1.125
1	0	1	1	1	1.100
1	1	0	0	0	1.075
1	1	0	0	1	1.050
1	1	0	1	0	1.025
1	1	0	1	1	1.000
1	1	1	0	0	0.975
1	1	1	0	1	0.950
1	1	1	1	0	0.925
1	1	1	1	1	0.900

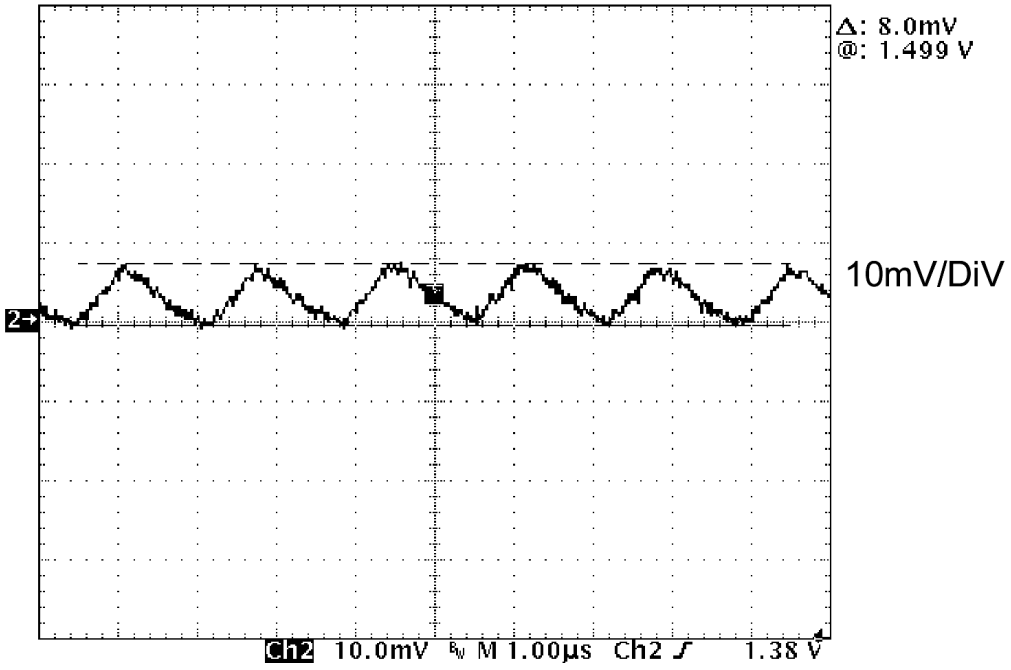


Figure 2. Core Output ripple at 1.5V, 15A

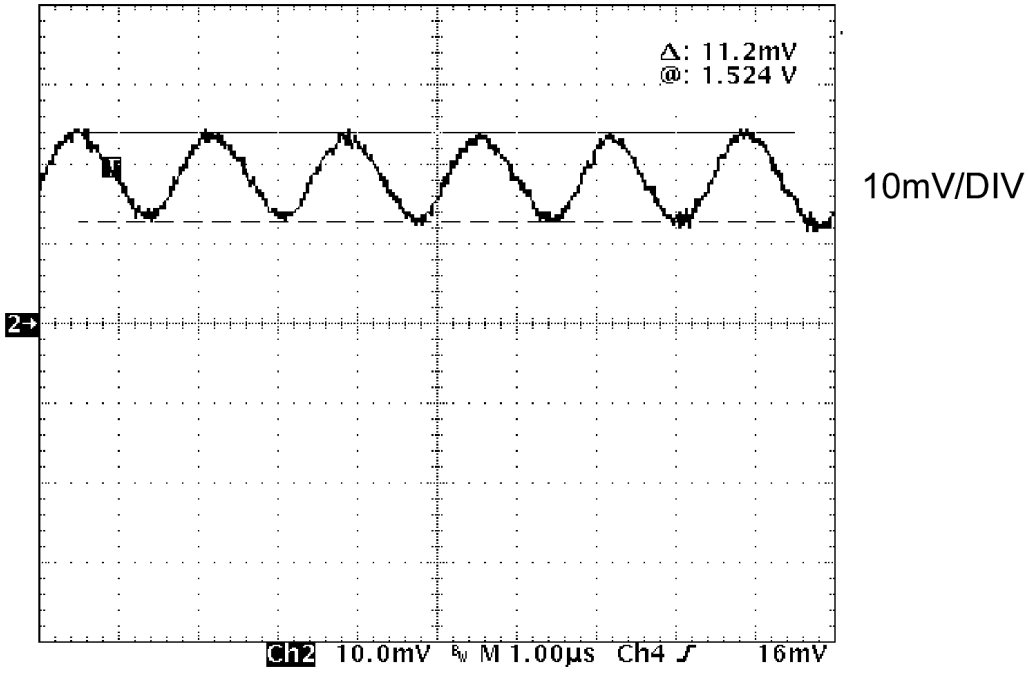


Figure 3. VI/O ripple at no load

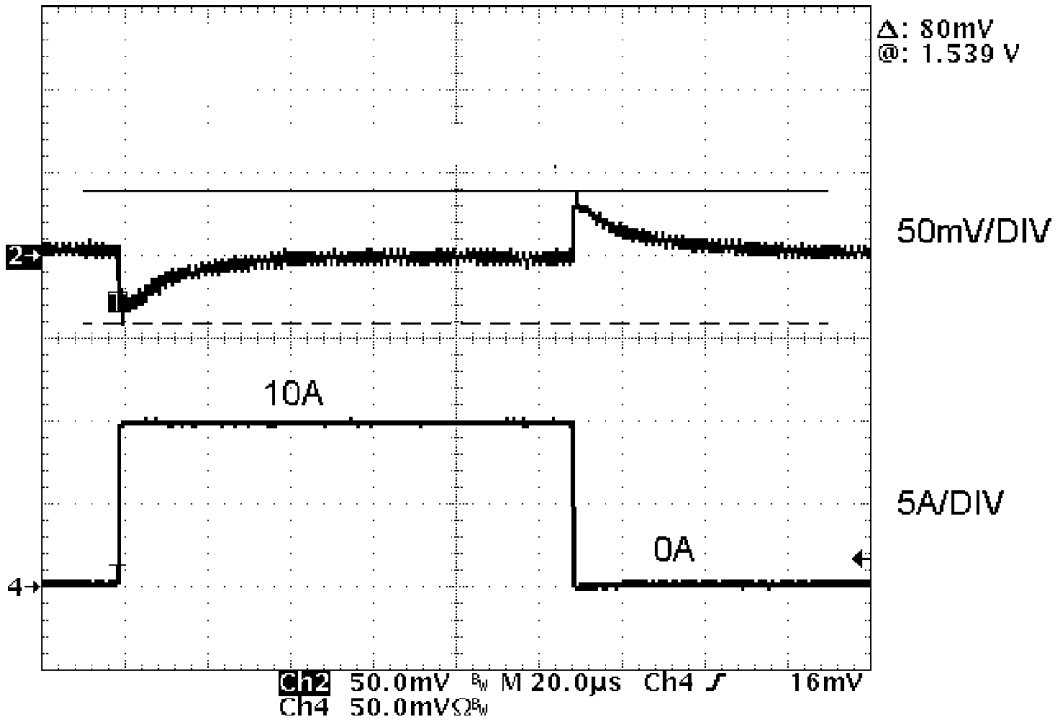
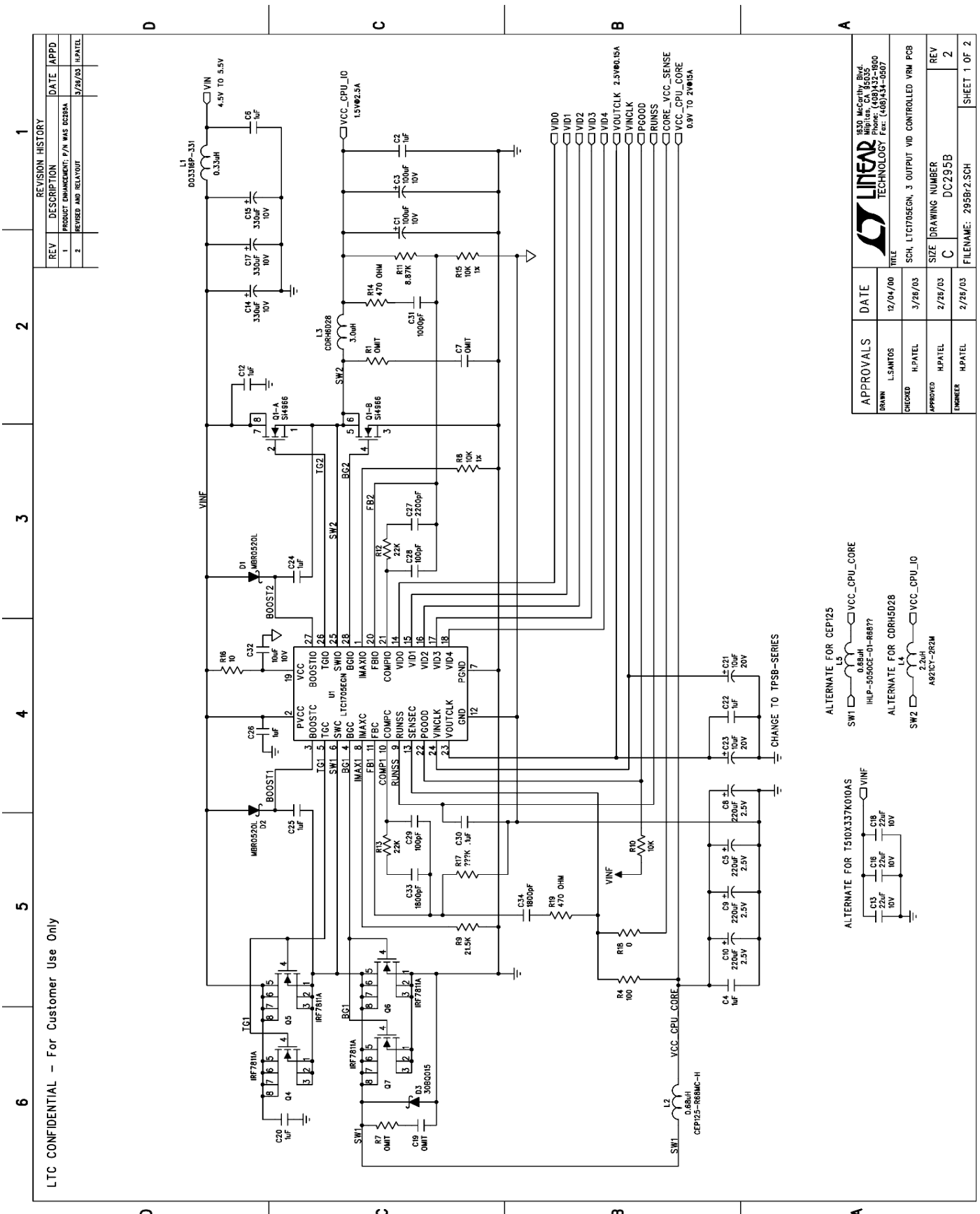
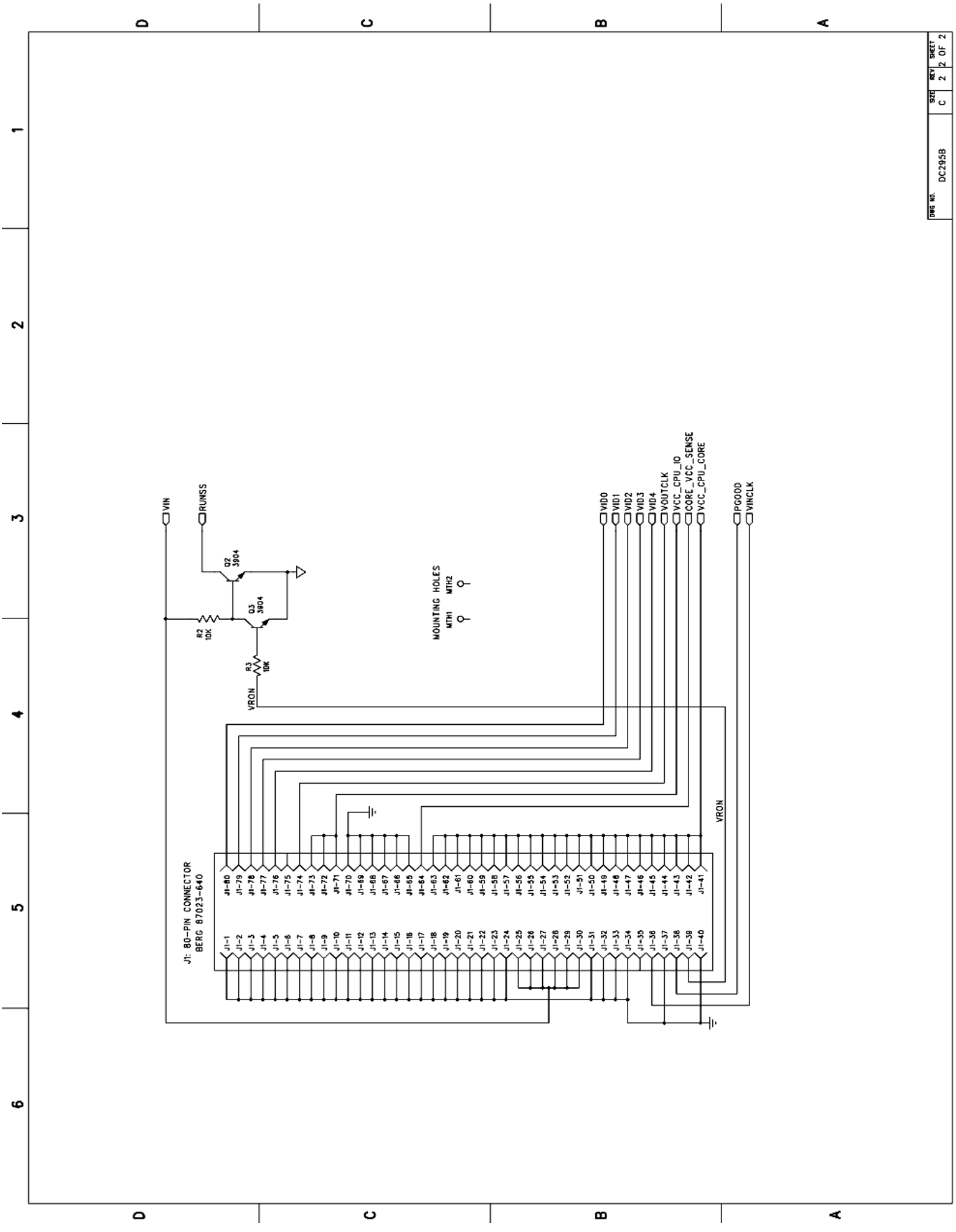


Figure 4. Load transient response of Vcore


REVISION HISTORY
REV | DESCRIPTION | DATE | APPD
1 | PRODUCT ENHANCEMENT: P/N WAS DC295A | | 3/26/03 | H.PATEL
2 | REVISED AND RELAYOUT
LTC CONFIDENTIAL – For Customer Use Only
APPROVALS | DATE
DRAWN L.SANTOS 12/04/00
CHECKED H.PATEL 3/26/03
APPROVED H.PATEL 2/26/03
ENGINEER H.PATEL 2/26/03
LINEAR TECHNOLOGY
1630 McCarthy Blvd.
Milpitas, CA 95035
Phone: (408)432-1900
Fax: (408)434-0507
TITLE: SCH, LTC1705EGN, 3 OUTPUT VID CONTROLLED VRM PCB
SIZE C | DRAWING NUMBER DC295B | REV 2
FILENAME: 295Br2.SCH | SHEET 1 OF 2
LTC1705EGN
ALTERNATE FOR CEP125
ALTERNATE FOR CDRH5D28
ALTERNATE FOR T510X337K010AS
CHANGE TO TPSB-SERIES
VIN 4.5V TO 5.5V
VCC_CPU_IO 1.5V@2.5A
VCC_CPU_CORE 0.9V TO 2V@15A
VOUTCLK 2.5V@0.15A
VID0
VID1
VID2
VID3
VID4
VINCLK
PGOOD
RUNSS
CORE_VCC_SENSE


VIN
RUNSS
Q2
3904
Q3
3904
R2
10K
R3
10K
VRON
MOUNTING HOLES
MTH1
MTH2
VID0
VID1
VID2
VID3
VID4
VOUTCLK
VCC_CPU_IO
CORE_VCC_SENSE
VCC_CPU_CORE
PGOOD
VINCLK
J1: 80-PIN CONNECTOR
BERG 87023-640
DWG NO. DC295B
SIZE C
REV 2
SHEET 2 OF 2