Active Voltage Positioning Reduces Output Capacitors

by Robert Sheehan

INTRODUCTION

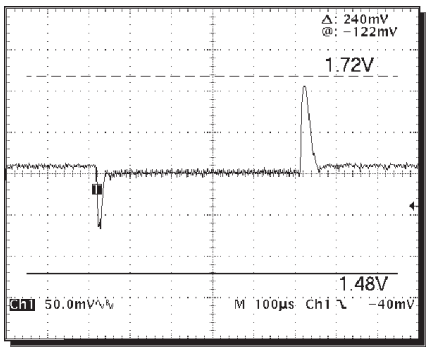
Power supply performance, especially transient response, is key to meeting today's demands for low voltage, high current microprocessor power. In an effort to minimize the voltage deviation during a load step, a technique that has recently been coined "active voltage positioning" is generating substantial interest and gaining popularity in the portable computer market. The benefits include lower peak-to-peak output voltage deviation for a given load step, without having to increase the output filter capacitance. Alternatively, the output filter capacitance can be reduced while maintaining the same peak-to-peak transient response.

BASIC PRINCIPLE

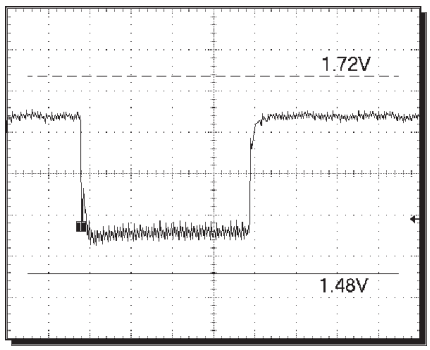
The term "active voltage positioning" (AVP) refers to setting the power supply output voltage at a point that is dependent on the load current. At minimum load, the output voltage is set to a slightly higher than nominal level. At full load, the output voltage is set to a slightly lower than nominal level. Effectively, the DC load regulation is degraded, but the load transient voltage deviation will be significantly improved. This is not a new idea, and it has been observed and described in many articles. What is new is the application of this principle to solve the problem of transient response for microprocessor power. Let's look at some numbers to see how this works.

Assume a nominal 1.5V output capable of delivering 15A to the load, with a ±6% (±90mV) transient window. For the first case, consider a classic converter with perfect DC regulation. Use a 10A load step with a slew rate of 100A/µs. The initial voltage spike will be determined solely by the output capacitor's equivalent series resistance (ESR) and inductance (ESL). A bank of eight 470µF, 30mΩ, 3nH tantalum capacitors will have an ESR = 3.75mΩ and ESL = 375pH. The initial voltage droop will be (3.75mΩ • 10A) + (375pH • 100A/µs) = 75mV. This leaves a 1% margin for set point accuracy. The voltage excursion will be seen in both directions, for the full load to minimum load transient and for the minimum load to full load transient. The resulting deviation is 2 • 75mV = 150mV peak-to-peak (Figure 2a).

Now look at the same transient using active voltage positioning. At the minimum load, purposefully set the output 3% (45mV) high. At full load, the output voltage will be set 3% low. During the minimum load to full load transient, the output voltage starts 45mV high, drops 75mV initially, and then settles to 45mV below nominal. For the full load to minimum load transient, the output voltage starts 45mV low, rises 75mV to 35mV above nominal, and settles to 45mV above nominal. The resulting deviation is now only 2 • 45mV = 90mV peak-to-peak (Figure 2b). Now reduce the number of output capacitors from eight to six. The ESR = 5mΩ and ESL = 500pH. The



(1a) Without AVP – 4 Output Capacitors



(1b) With AVP – 3 Output Capacitors

Figure 1. Transient Response with Load Step from 0A to 12A

transient voltage step is now (5mΩ • 10A) + (500pH • 100A/μs) = 100mV. With the 45mV offset, the resultant change is ±55mV around center, or 110mV peak-to-peak (Figure 2c). The initial specification has been easily met with a 25% reduction in output capacitors.

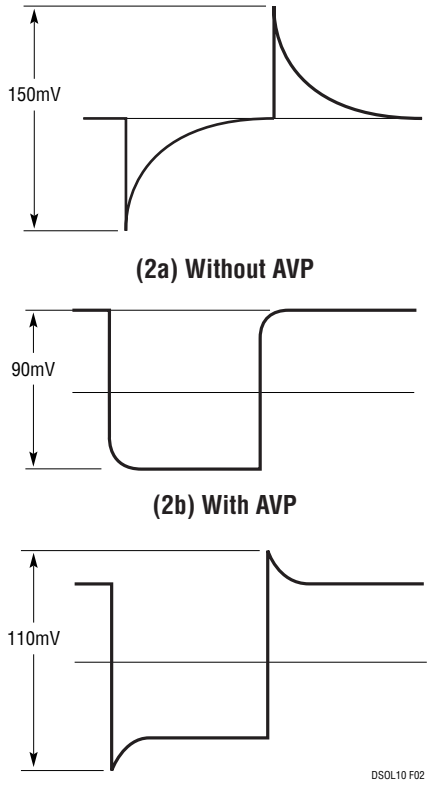


Figure 2. Transient Response Comparison

An added benefit of voltage positioning is an incremental reduction in CPU power dissipation. With the output voltage set to 1.50V at 15A, the load power is 22.5W. By decreasing the output voltage to 1.47V, the load current is 14.7A and the load power is now 21.6W. The net saving is 0.9W.

BASIC IMPLEMENTATION

In order to implement voltage positioning, a method for sensing the load current is required. This must then be converted to a voltage, and used to move the output voltage in the correct direction. Figure 3 shows a simplified buck regulator in the normal configuration. R1 and R2 are used to set the output voltage, and near perfect DC load regulation is achieved. The simplest way to cause the output voltage to drop with load current is to add some resistance to the output, or use resistance that is already there. This is shown in Figure 4. Using a current sense resistor will cause V_{OUT} to drop by R_S times the load current. R1 and R2 can be adjusted to center the nominal output voltage on the required amount of deviation. For many current mode controllers, a current sense resistor is already used. Note that the wiring resistance R_W will cause additional drop at the load. Figure 5 shows the same buck

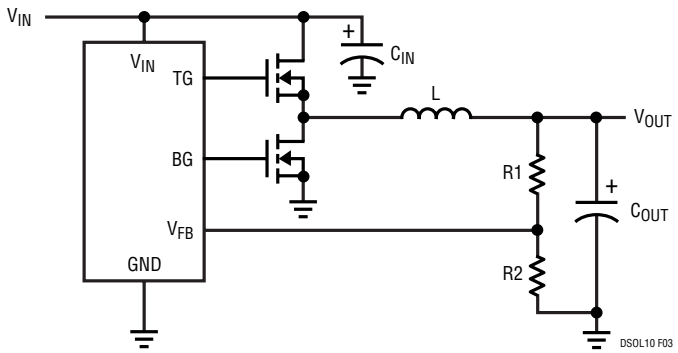


Figure 3. Simplified Buck Regulator

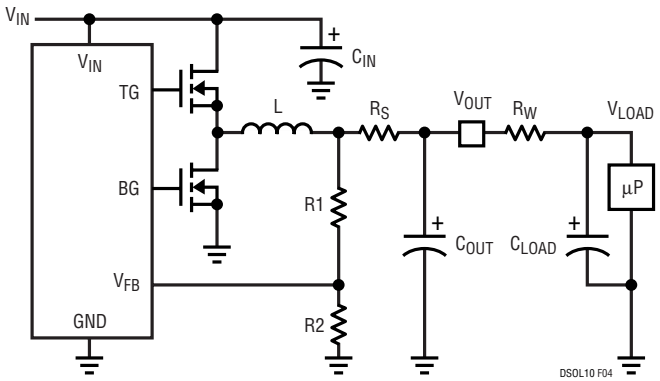


Figure 4. Simplified Buck Regulator with Current Sense Resistor and Wiring Resistance

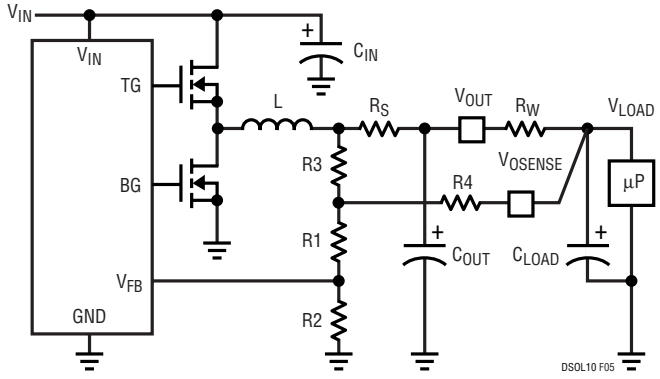


Figure 5. Simplified Buck Regulator with Remote Sense

regulator, this time with remote sense. If the voltage drop at the load is too great, R3 and R4 can be scaled to select the right amount of voltage positioning.

IC SPECIFIC IMPLEMENTATIONS

Current Mode Control Example – LTC®1736

Figure 6 shows the basic power stage and feedback compensation circuit for the LTC1736. The corresponding transient response with 20V input and 1.6V output is shown in Figure 1a. In order to implement voltage positioning, we will control the error amplifier gain at the I_{TH} pin. The internal amplifier is a transconductance type, the gain being set by $g_m \bullet R_O$, where g_m is the transconductance in mmhos, and R_O is the output impedance in kohms. The voltage at the I_{TH} pin is proportional to the load current, where 0.48V = min load, 1.2V = half load, and 2V = full load in this application. R_O = 600kΩ and g_m = 1.3mmho. By setting a voltage divider to 1.2V from the 5V $INTV_{CC}$, the gain can be limited without effecting the nominal DC set point at half load. The Thevenin equivalent resistance is seen to be in parallel with the amplifiers R_O. Using the values shown in Figure 7, the effective R_O will be 600k||91k||27k = 20.12kΩ. The voltage deviation at the amplifier input $\Delta V_{FB} = \Delta V_{ITH}/(g_m \bullet R_{Oeff})$. ΔV_{FB} = (2.0V-0.48V)/(1.3mmho • 20.12kΩ) = 58mV, which is ±29mV from the nominal half load set point.

Care should be taken to keep the amplifier input from being pulled more than ±30mV from its nominal value, or nonlinear behavior may result. The DC reference voltage at V_{FB}

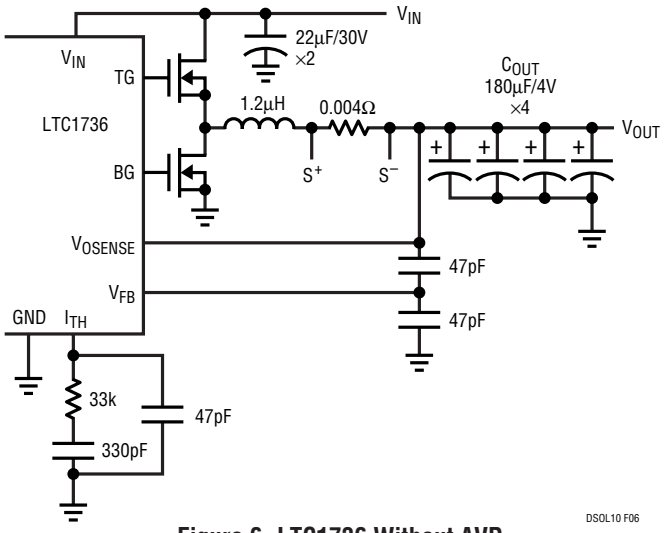


Figure 6. LTC1736 Without AVP

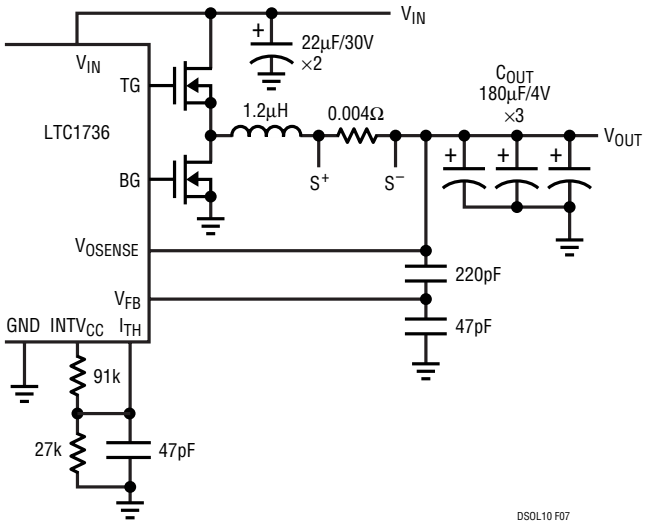


Figure 7. LTC1736 with AVP

is 0.8V and V_{OUT} is set for 1.6V, so $\Delta V_{OUT} = 2 \bullet \Delta V_{FB}$ = 116mV. The peak-to-peak ripple voltage will add to this. The resulting transient response is shown in Figure 1b. The transient performance has been improved, while using fewer output capacitors.

The optimal amount of AVP offset is equal to ΔI • ESR. Figure 1b exhibits this condition. In instances where the static regulation does not allow this much offset, the result will look like Figure 12.

Voltage Mode Control Example – LTC1703.

Voltage mode control presents some interesting challenges for active voltage positioning, since there is no information on the load current available within the feedback loop. Figure 8 shows the basic feedback path for the LTC1703, with transient response in Figure 9. The simplest way to position the output is to add R_{AVP}, as shown in Figure 10. This works well, but adds additional power dissipation ($I_{OUT}^2 \bullet R_{AVP}$) and lowers efficiency. A more efficient solution is presented in Figure 11. The inductor resistance is sensed and integrated by the 150Ω

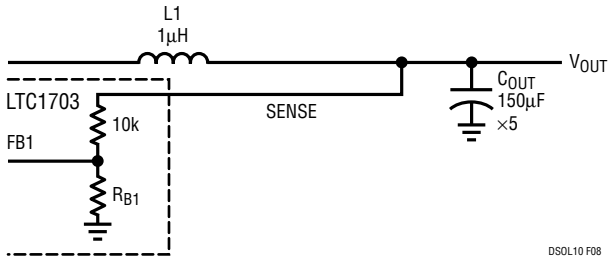


Figure 8. LTC1703 Without AVP

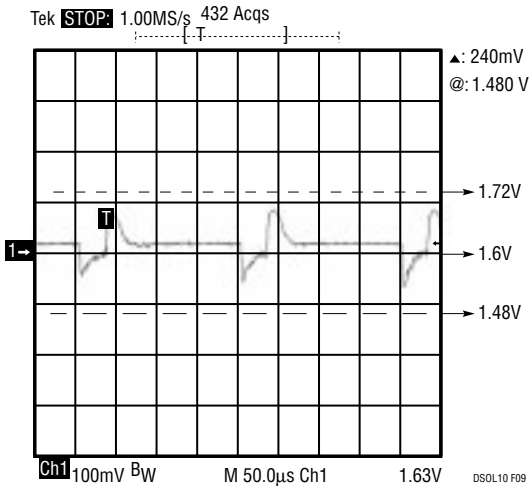


Figure 9. LTC1703 Transient Response Without AVP – 5 Output Capacitors with Load Step from 0A to 14A

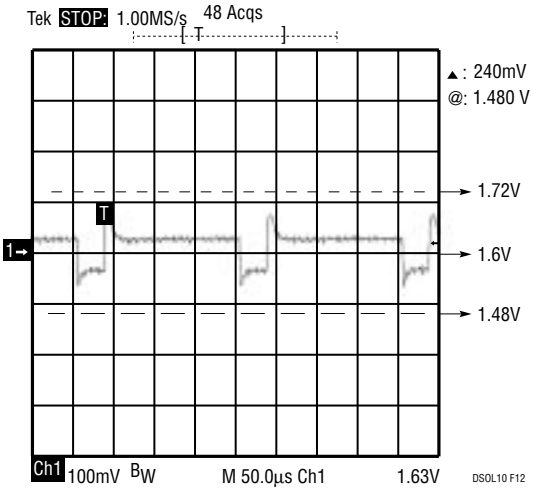


Figure 12. LTC1703 Transient Response with AVP – 4 Output Capacitors with Load Step from 0A to 14A

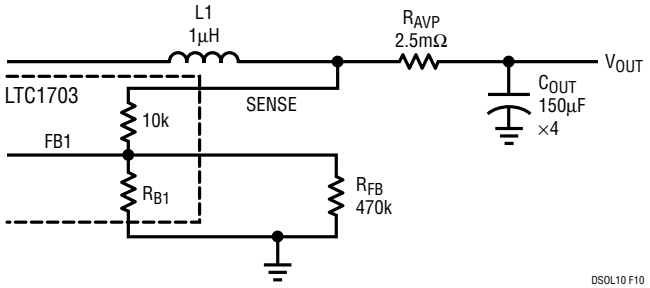


Figure 10. LTC1703 AVP Circuit I

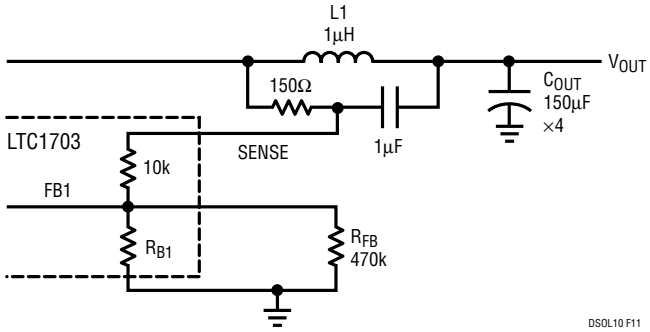


Figure 11. LTC1703 AVP Circuit II

resistor and 1µF capacitor. This technique is most suited to lower voltage inputs, as the dissipation in the resistor can become significant at higher input voltages. The time constant of the RC integrator should be relatively low, as this will effect the systems ability to respond to step load changes. The results are shown in Figure 12, again with an improvement in transient performance and reduction in output capacitance.

MOSFET $R_{DS(ON)}$ Sensing

This technique uses the on resistance of the MOSFET switches to provide the current information for active voltage positioning. Integrated into an IC, this can be used with either voltage mode or current mode methods. However, the variability of $R_{DS(ON)}$ is tremendous. It may vary more than ±20% from part to part and ±50% with temperature. If you design for the worst-case situation, the amount of voltage positioning at nominal conditions can make this method almost useless.

CONTRIBUTING AUTHORS

1 Craig Varga, Basis Implementation, Current Mode and Voltage Mode Control, $R_{DS(ON)}$ Sensing.

2 Wei Chen, LTC1736 Circuit and Performance.

3 Ajmal Godil, LTC1703 Circuit and Performance.

REFERENCES

1 Robert Sheehan, "Simple Technique Improves Transient Dynamics," EDN, June 12, 1999.

2 Ron Lenk, "Summing-Mode Control," PCIM, May, 1999.

3 Lloyd Dixon, "Switching Power Supply Control Loop Design," Unitrode SEM-800 Topic 7, October, 1991.

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408)432-1900 • FAX: (408) 434-0507 • www.linear-tech.com
dsol10 LT/TP 1199 2K REV A • PRINTED IN USA