DESIGN NOTES

12-Bit ADC with Sequencer Simplifies Multiple-Input Applications – Design Note 274

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The LTC®1851 is a new 12-bit, 1.25Msps ADC with an 8-channel input multiplexer, a programmable gain sample-and-hold and an internal reference. This Design Note describes a novel feature of the LTC1851: a programmable sequencer that can automatically control the input mux and sample-and-hold.

New ADC Automatically Converts Multiple Inputs with Different Spans at Different Rates

Let's imagine a hypothetical application with the following inputs: input A has a range of 0V to 4.096V and needs to be sampled at 400ksps, input B needs 400ksps with a range of 0V to 2.048V, input C has a range of ±2.048V around 2.5V and needs 200ksps, input D needs 100ksps with a range of ±1.024V and is truly differential with a common mode of 2V and input E needs 100ksps with a range of 1V to 3.048V. There are both single-ended and differential, unipolar and bipolar inputs, two different spans and different required sampling rates.

The solution is the LTC1851 sequencer, which allows the user to program a repeating pattern of up to 16 independent mux addresses and configurations and allocates the bandwidth of the LTC1851 as needed. The LTC1851 can easily be programmed to read all five of these inputs continuously and automatically.

Table 1 shows a twelve-step sequence sampling input A every third conversion, input B every third conversion, input C every sixth conversion, and inputs D and E once every 12 conversions. This will result in effective sampling rates of 1.25Msps • 4/12 = 416.67ksps for inputs A and B, 208.33ksps for input C and 104.167ksps for inputs D and E. The LTC1851 handles the channel selection and input configuration and will cycle through these twelve steps automatically as conversions are performed.

Writing and Reading the Sequencer

To write to the sequencer, $\overline{RD}$ must be high and M0 taken low (see Figure 2). The falling edge of $\overline{WR}$ enables the configuration control inputs (DIFF, A2, A1, A0, $\overline{UNI}$/BIP and PGA) and the rising edge latches the data and advances to the next location. Subsequent $\overline{WR}$ low pulses will write up to 16 locations. After the last desired location is written, M0 should be taken high.

To confirm the integrity of the programmed sequence, the user can read the contents of the Sequencer. $\overline{WR}$ must be high and M0 taken low (see Figure 3). An $\overline{RD}$ low pulse will output the first sequencer location on the 7 status word output pins (S6 to S0). The rising edge

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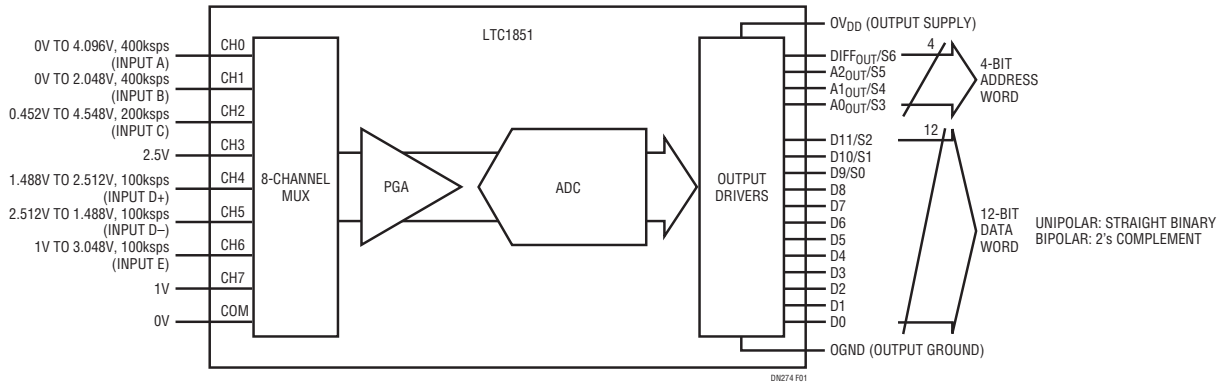
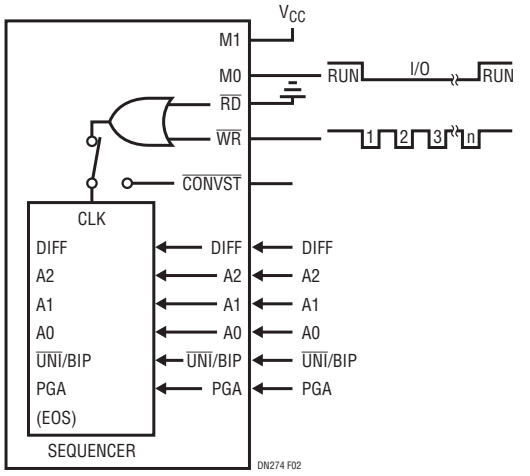


Figure 1. Simplified Block Diagram with Input Connections

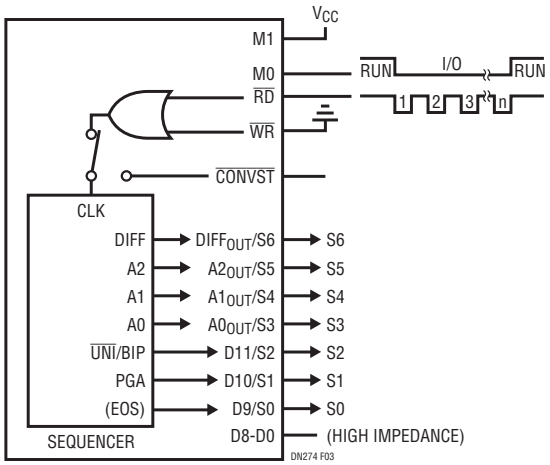
Table1. Twelve Step Sequence Provides Effective Sampling Rate of 416ksps for Inputs A and B, 208ksps for Input C and 104ksps for Inputs D and E

STEP	INPUT	+INPUT PIN	–INPUT PIN	INPUT RANGE (V)	MEMORY LOCATION	DIFF	A2	A1	A0	$\overline{UNI}$/BIP	PGA
1	A	CH0	COM	0 TO 4.096	0000	0	0	0	0	0	1
2	B	CH1	COM	0 TO 2.048	0001	0	0	0	1	0	0
3	C	CH2	CH3	±2.048	0010	1	0	1	0	1	1
4	A	CH0	COM	0 TO 4.096	0011	0	0	0	0	0	1
5	B	CH1	COM	0 TO 2.048	0100	0	0	0	1	0	0
6	D	CH4	CH5	±1.024	0101	1	1	0	0	1	0
7	A	CH0	COM	0 TO 4.096	0110	0	0	0	0	0	1
8	B	CH1	COM	0 TO 2.048	0111	0	0	0	1	0	0
9	C	CH2	CH3	±2.048	1000	1	0	1	0	1	1
10	A	CH0	COM	0 TO 4.096	1001	0	0	0	0	0	1
11	B	CH1	COM	0 TO 2.048	1010	0	0	0	1	0	0
12	E	CH6	CH7	1 TO 3.048	1011	1	1	1	0	0	1



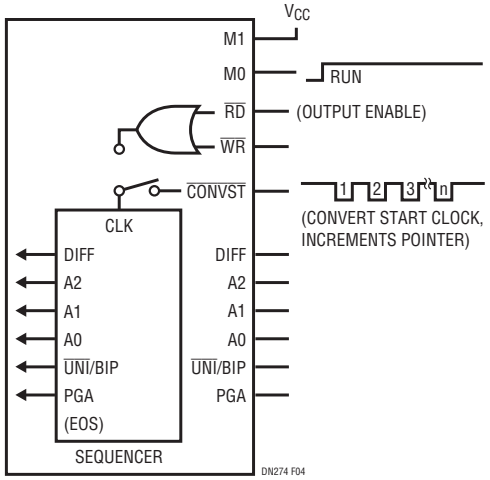
RISING EDGE OF $\overline{WR}$ LATCHES DATA INTO SEQUENCER AND INCREMENTS POINTER

Figure 2. Writing the Sequencer



FALLING EDGE OF $\overline{RD}$ ENABLES DATA OUTPUTS, RISING EDGE DISABLES OUTPUTS AND INCREMENTS POINTER

Figure 3. Reading the Sequencer



ANY EDGE OF M1 OR M0 RESETS THE SEQUENCER POINTER

Figure 4. Running the Sequencer

of $\overline{RD}$ will return the output pins to a high impedance state and advance to the next location. Subsequent $\overline{RD}$ low pulses will read through all 16 locations. The last location in the sequence will be indicated by a logic 1 on the S0 pin.

Running the Sequencer

The M0 pin must be returned high, which will reset the pointer to location 0000 (see Figure 4). The LTC1851 will begin acquiring the input signal using the configuration stored in that location. The falling edge of $\overline{CONVST}$ will sample the inputs and begin a conversion. After the conversion, the LTC1851 will begin acquiring the next input using the configuration stored in location 0001 and the 12-bit data output word (D11 to D0), along with the 4-bit mux address ($DIFF_{OUT}$, $A2_{OUT}$, $A1_{OUT}$, $A0_{OUT}$), will be available on the data output pins. (The 12-bit output word will automatically switch format for unipolar and bipolar inputs.) When the last programmed location is reached, the sequencer will start over at location 0000. The program stored in the sequencer memory is retained as long as power is continuously applied to the part.

Conclusion

The LTC1851 greatly simplifies the task of continuously converting multiple inputs. It can be programmed to handle a wide variety of inputs and automate channel selection and input configuration. For more information see the November 2001 issue of *Linear Technology* magazine or the LTC1851 data sheet.

Data Sheet Download

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