Uncompromised Clocking Solution for 16-Bit 2.5Gsps High Performance DAC

Design Note 555

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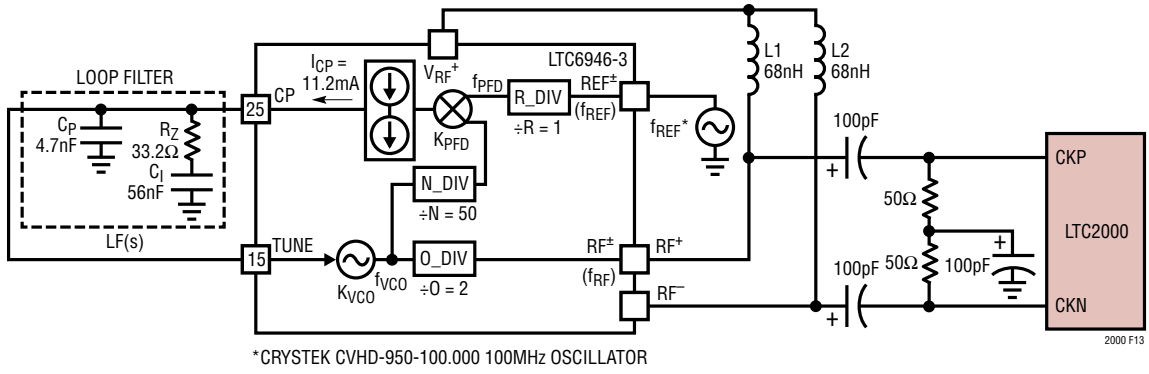
Introduction

The LTC®2000 16-bit 2.5Gsps DAC offers excellent AC performance. For many DAC applications, phase noise, noise spectral density (NSD), and spurious free dynamic range (SFDR) are critical to maximize the number of possible channels in a band without eroding the signal to noise ratio (SNR) in the band of interest. High speed DACs require a clean sample clock to achieve the best possible noise and spurious performance. Using the ultralow noise and spurious LTC6946 PLL synthesizer as a clock source for the LTC2000 maximizes system performance (Figure 1).

16-Bit High Speed DAC

The high spectral purity and low noise of the LTC2000 make it an excellent signal generator. Figure 2 highlights the excellent additive phase noise performance of the LTC2000 of –165dBc/Hz at 1MHz offset and –147dBc/Hz at 10kHz offset with a 65MHz output. For output frequencies up to 100MHz, the LTC2000 has NSD better than –166dBm/Hz and SFDR better than 76dB. For higher output frequencies up to 1GHz, the SFDR is more than 68dB and the NSD remains below –155dBm/Hz. Producing these results requires a clock with good noise, high spectral purity and excellent jitter performance.



*CRYSTEK CVHD-950-100.000 100MHz OSCILLATOR

Figure 1. LTC6946 Driving the LTC2000

Frequency Synthesizer as a Clock Source

The LTC6946 is an integer-N frequency synthesizer with integrated VCO that can produce signals from 370MHz up to 6.39GHz. It features excellent phase noise performance and very low spurious content, making it ideal to clock the LTC2000 at 2.5GHz. It can drive the LTC2000 directly without filtering to produce a spectrally pure low noise output.

The LTC2000 divides the clock frequency (f_{CLK}) down to an output frequency (f_{OUT}). This frequency division causes the phase noise of the clock to appear at the DAC output, attenuated by a factor of 20 • log(f_{CLK}/f_{OUT}). The total phase noise at the DAC output will be a combination of the additive phase noise of the LTC2000 (Figure 2) and the attenuated phase noise of the LTC6946.

Wideband phase noise or jitter on the sample clock must be minimized to avoid degrading the NSD of the DAC output, and the low spurious content of the LTC6946 output is critical to maintain high SFDR at the output of the LTC2000.

The lower the phase noise, the closer signals generated by the LTC2000 can be spaced. This allows more information to be transmitted in a given bandwidth. With a lower phase noise floor, the total SNR of the system increases, which improves the integrity of the signal produced by the LTC2000.

Results

The single-sideband phase noise of the LTC2000 clocked by the LTC6946 is shown in Figure 3. The LTC6946 works well with the LTC2000, producing a clean clock that maximizes the DAC's performance. The combination of the LTC2000 and the LTC6946 offer phase noise and spurious performance comparable to the best signal generators. For more information visit www.linear.com.

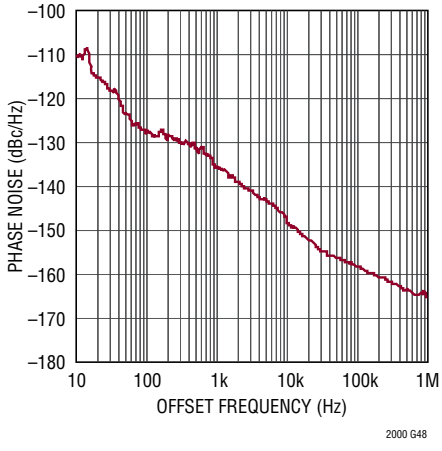


Figure 2. Additive Phase Noise of the LTC2000, f_{OUT} = 65MHz, f_{DAC} = 2.5GHz

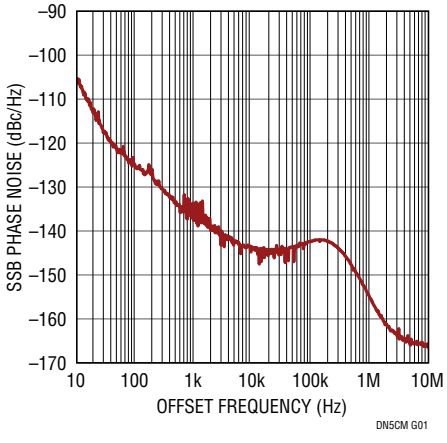


Figure 3. Phase Noise of the LTC2000 Output at 80MHz Clocked by the LTC6946-3

Data Sheet Download

www.linear.com/LTC2000

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